



NAME: AYESHA TASSAWER

SAP_ID:55430

LAB 8: COMPUTER ARCHITECTURE

SUBMITTED TO : Ma'am Ayesha

CLASS WORK

The screenshot shows a simulator interface with three main panels. The left panel displays the state of registers: AC (16 bits, 0001), AR (12 bits, 001), DR (16 bits, 0002), S (1 bit, 1), I (1 bit, 0), IR (16 bits, E001), PC (12 bits, 008), and S (1 bit, 1). The middle panel shows assembly code for a program titled 'subtracta X'. The code includes instructions like START, INP, STA NUM, INC, CMA, TNC, ADD NUM, OUT, and HLT, along with a data declaration 'NUM: .data 1 0'. The right panel shows a memory dump for the 'MAIN' segment, with addresses from 000 to 010 and corresponding hex values. Below the panels, a text area shows the execution log, indicating that the program executed normally and halted due to the HALT-BIT.

EXECUTING...
Enter Inputs, the first of which must be an Integer: 2
Enter Inputs, the first of which must be an Integer: 1
Output: 1
EXECUTION HALTED NORMALLY due to the setting of the bit(s): {HALT-BIT}

LAB TASK1

The screenshot shows a simulator interface similar to the one above. The left panel shows registers: AC (16 bits, 0004), AR (12 bits, 001), DR (16 bits, 0006), S (1 bit, 1), I (1 bit, 0), IR (16 bits, E001), PC (12 bits, 000), and S (1 bit, 1). The middle panel shows assembly code for a program titled '*subtracta X'. The code includes instructions like START, INP, STA NUM, INC, CMA, TNC, ADD NUM, OUT, and HLT, along with a data declaration 'NUM: .data 1 0'. The right panel shows a memory dump for the 'MAIN' segment, with addresses from 000 to 010 and corresponding hex values. Below the panels, a text area shows the execution log, indicating that the program executed normally and halted due to the HALT-BIT.

EXECUTING...
Enter Inputs, the first of which must be an Integer: 10
Enter Inputs, the first of which must be an Integer: 4
Enter Inputs, the first of which must be an Integer: 2
Output: 4
EXECUTION HALTED NORMALLY due to the setting of the bit(s): {HALT-BIT}

LAB TASK2

Registers

Name	Width	Data
AC	16	0002
AR	12	001
DR	16	0004
E	1	1
I	1	0
IR	16	E001
PC	12	006
S	1	1

subtracta X

```
1 START:
2 ADD NUM2
3 CMA
4 INC
5 ADD NUM1
6
7 OUT
8 HLT
9
10 NUM1: .data 1 6
11 NUM2: .data 1 2
12 RESULT: .data 1 0
13
```

MAIN

Addr	Data
000	2007
001	E200
002	E020
003	2006
004	F400
005	E001
006	0004
007	0002
008	0000
009	0000
00A	0000
00B	0000
00C	0000
00D	0000
00E	0000
00F	0000
010	0000

EXECUTING...
Output: 2
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]

LAB TASK3

Registers

Name	Width	Data
AC	16	0004
AR	12	001
DR	16	0006
E	1	1
I	1	0
IR	16	E001
PC	12	007
S	1	1

subtracta X

```
1 START:
2 ADD NUM2
3 CMA
4 INC
5 ADD NUM1
6 STA RESULT
7 OUT
8 HLT
9
10 NUM1: .data 1 6
11 NUM2: .data 1 2
12 RESULT: .data 1 0
13
```

MAIN

Addr	Data
000	2008
001	E200
002	E020
003	2007
004	6009
005	F400
006	E001
007	0006
008	0002
009	0004
00A	0000
00B	0000
00C	0000
00D	0000
00E	0000
00F	0000
010	0000

EXECUTING...
Output: 4
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]