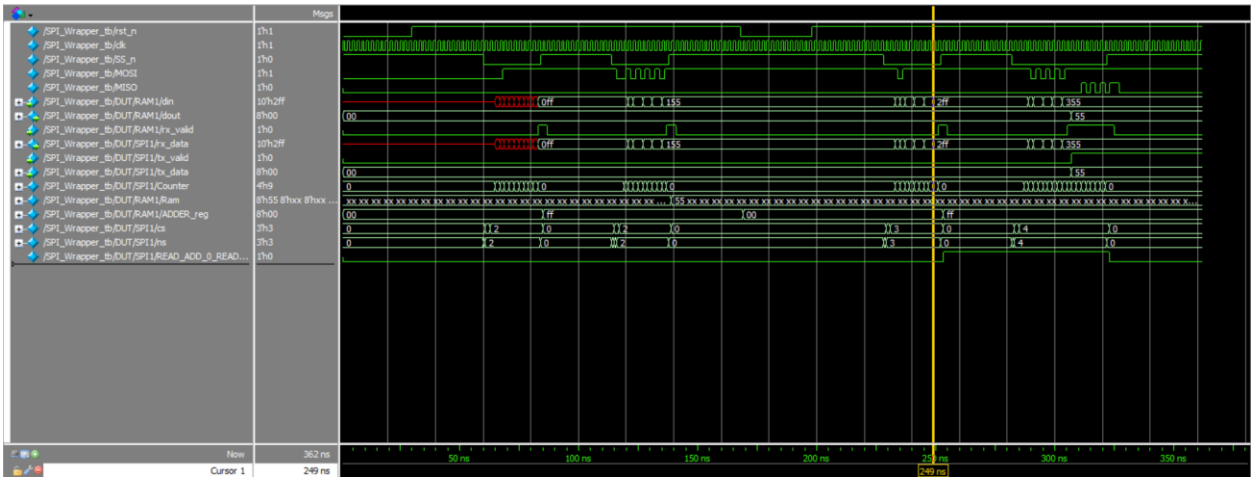
SPI PROJECT

Ayman Mostafa Sayed Hassan	Karim Ayman Refaat	Youssef hesham Abdelfatah Mohamed

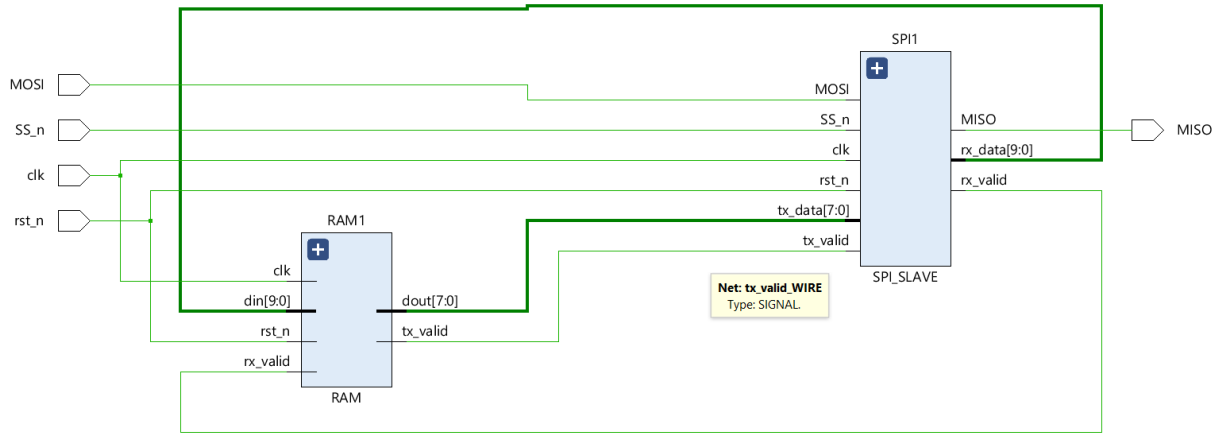
1-WaveForm



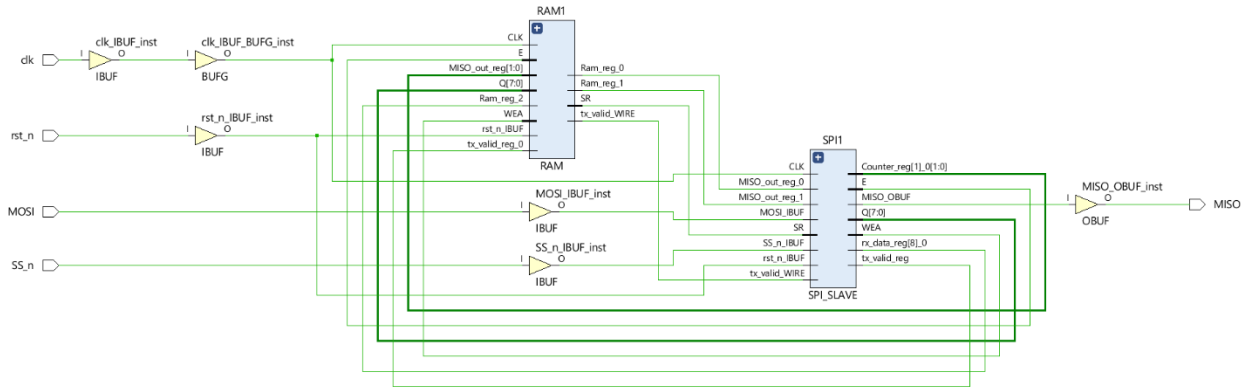
2-Synthesis snippets for each encoding

- One Hot

Elaborated Schematic



Synthesized Schematic



Encoding Used

```
-------------------------------------------------------------------------------------------------
                   State |                     New Encoding |                Previous Encoding
-------------------------------------------------------------------------------------------------
                    IDLE |                            00001 |                             000
                 CHK_CMD |                            00010 |                             001
                   WRITE |                            00100 |                             010
                READ_ADD |                            01000 |                             011
               READ_DATA |                            10000 |                             100
-------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_SLAVE'
```

Timing

Setup

Worst Negative Slack (WNS):	5.898 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	72

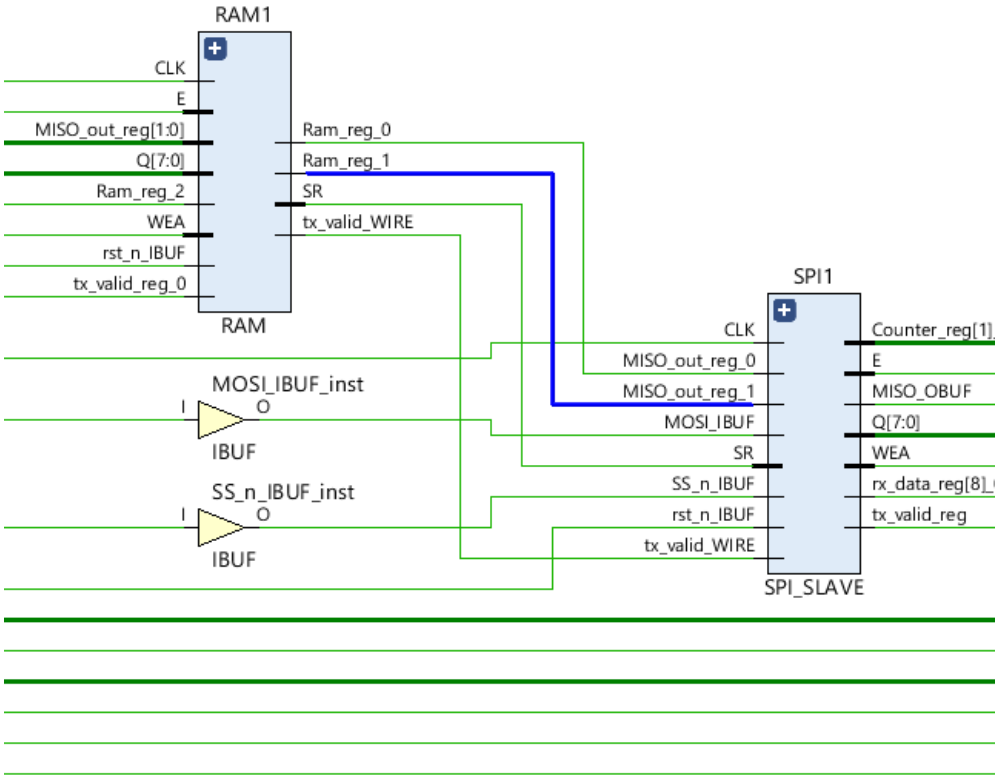
Hold

Worst Hold Slack (WHS):	0.149 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	72

Pulse Width

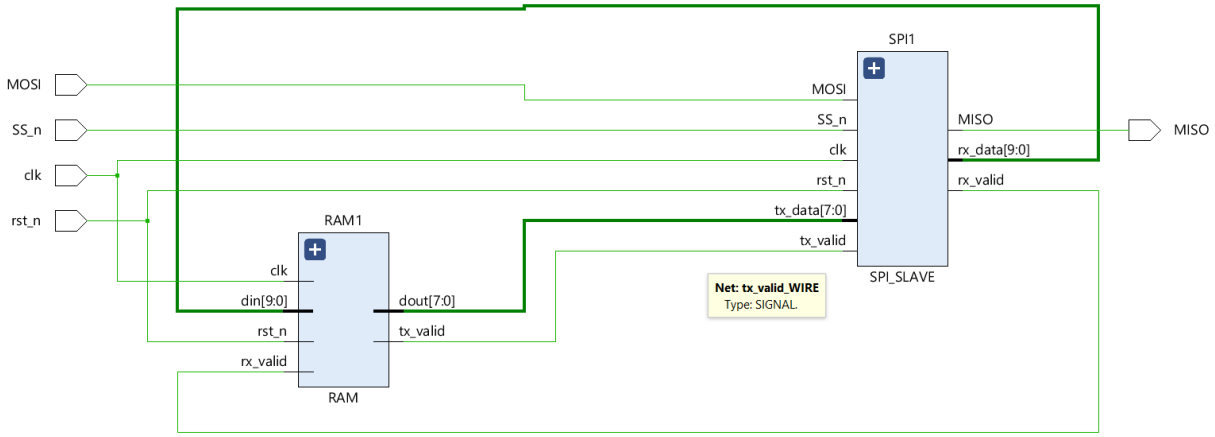
Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	36

Name	Slack ^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	5.898	2	1	RAM1/Ram_...CLKBWRCLK	SPI1/MISO_out_reg/D	3.951	2.702	1.249	10.000
Path 2	6.931	2	10	SPI1/FSM_one...cs_reg[3]/C	SPI1/rx_data_reg[0]/CE	2.687	0.875	1.812	10.000
Path 3	6.931	2	10	SPI1/FSM_one...cs_reg[3]/C	SPI1/rx_data_reg[1]/CE	2.687	0.875	1.812	10.000
Path 4	6.931	2	10	SPI1/FSM_one...cs_reg[3]/C	SPI1/rx_data_reg[2]/CE	2.687	0.875	1.812	10.000
Path 5	6.931	2	10	SPI1/FSM_one...cs_reg[3]/C	SPI1/rx_data_reg[3]/CE	2.687	0.875	1.812	10.000

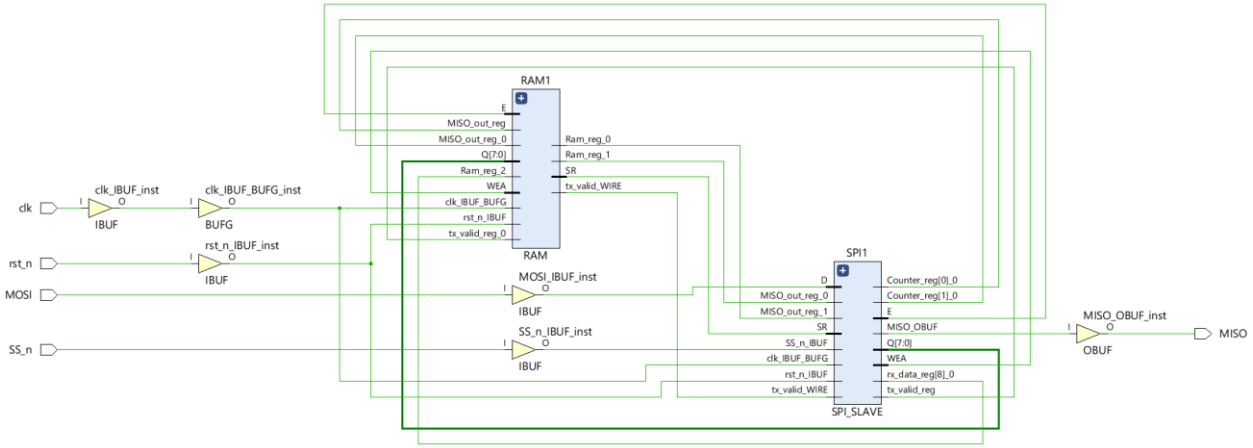


- Gray

Elaborated Schematic



Synthesized Schematic



Encoding Used

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_ADD	010	011
READ_DATA	111	100

```
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_SLAVE'
```

Timing

Setup

Worst Negative Slack (WNS):	5.445 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	74

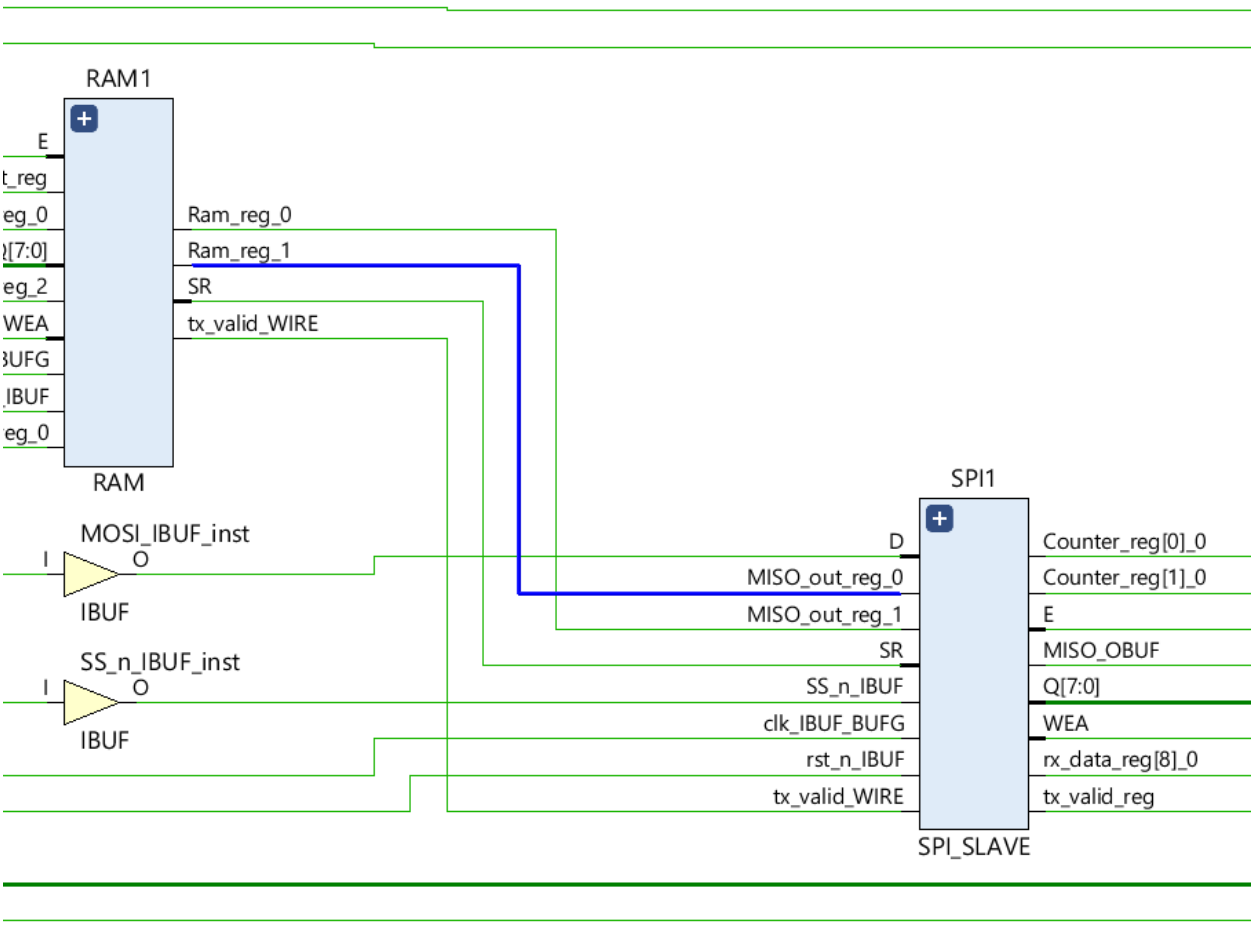
Hold

Worst Hold Slack (WHS):	0.139 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	74

Pulse Width

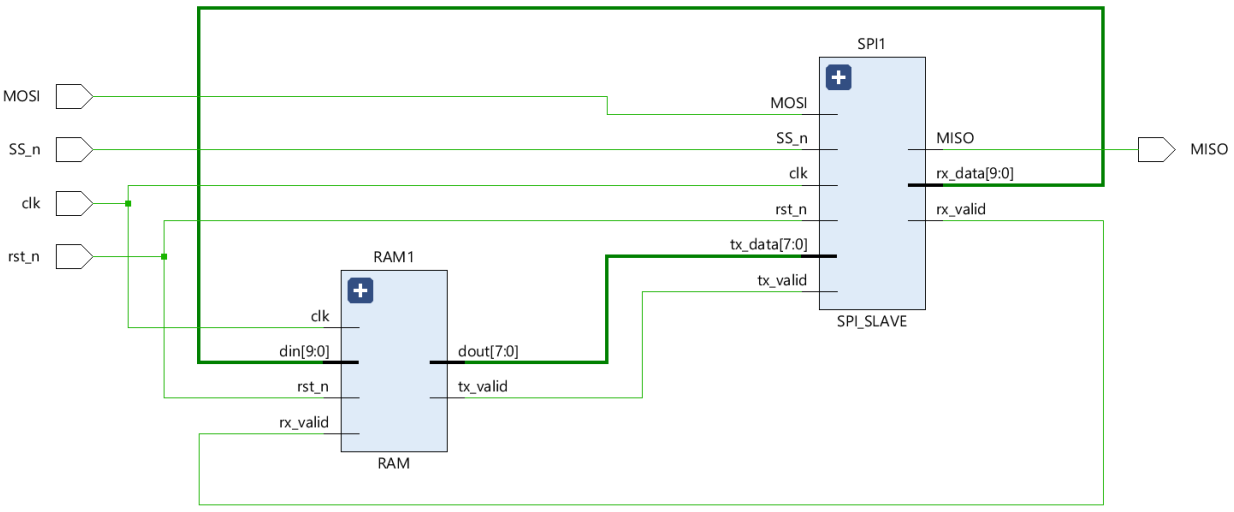
Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	34

Name	Slack ^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	5.445	2	1	RAM1/Ram_...CLKBWRCLK	SPI1/MISO_out_reg/D	4.404	2.702	1.702	10.000	sys_clk_pin
Path 2	6.662	3	19	SPI1/Counter_reg[0]/C	SPI1/READ_A..._out_reg/D	3.187	1.025	2.162	10.000	sys_clk_pin
Path 3	6.952	2	16	SPI1/Counter_reg[2]/C	SPI1/Counter_reg[0]/CE	2.666	0.901	1.765	10.000	sys_clk_pin
Path 4	6.952	2	16	SPI1/Counter_reg[2]/C	SPI1/Counter_reg[1]/CE	2.666	0.901	1.765	10.000	sys_clk_pin
Path 5	6.952	2	16	SPI1/Counter_reg[2]/C	SPI1/Counter_reg[2]/CE	2.666	0.901	1.765	10.000	sys_clk_pin

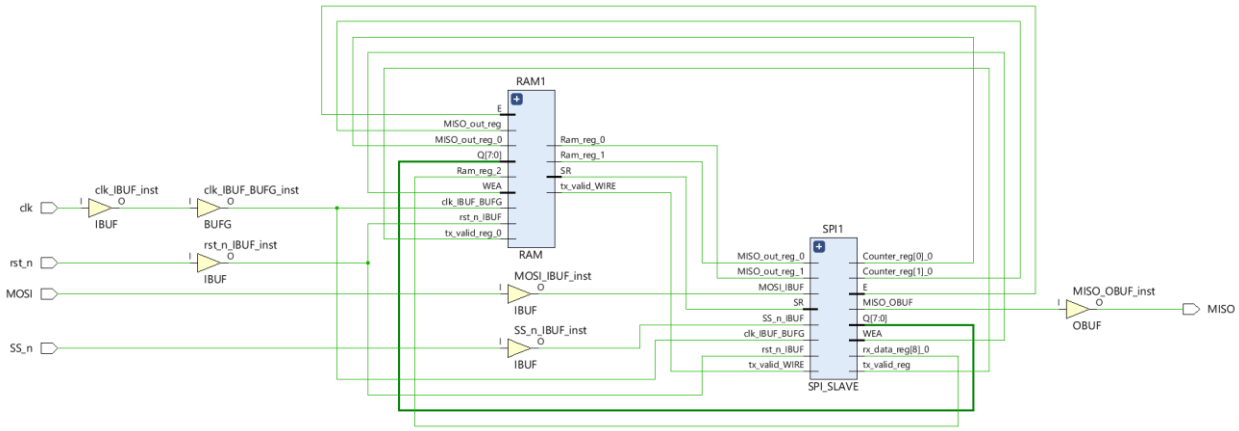


- Sequential

Elaborated Schematic



Synthesized Schematic



Encoding Used

```
INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_SLAVE'
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                              000
                 CHK_CMD |                              001 |                              001
                   WRITE |                              010 |                              010
                READ_ADD |                              011 |                              011
               READ_DATA |                              100 |                              100
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_SLAVE'
---------------------------------------------------------------------------------
```

Timing

Setup

Worst Negative Slack (WNS):	5.445 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	74

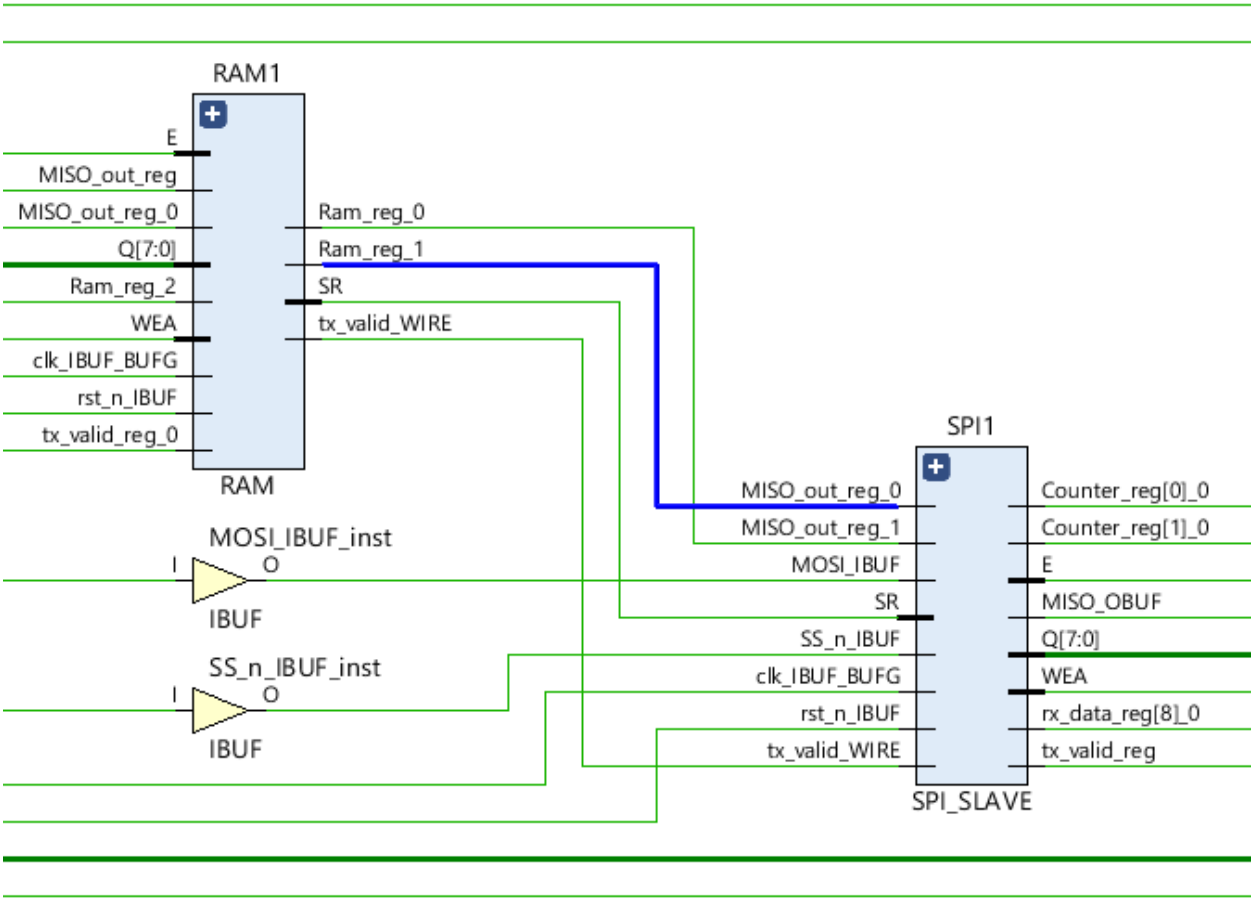
Hold

Worst Hold Slack (WHS):	0.155 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	74

Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	34

Name	Slack ^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	5.445	2	1	RAM1/Ram_...CLKBWRCLK	SPI1/MISO_out_reg/D	4.404	2.702	1.702	10.000	sys_clk_pin
Path 2	6.680	3	16	SPI1/Counter_reg[2]/C	SPI1/READ_A..._out_reg/D	3.169	0.999	2.170	10.000	sys_clk_pin
Path 3	6.961	2	13	SPI1/FSM_seq...cs_reg[1]/C	SPI1/rx_data_reg[0]/CE	2.657	0.901	1.756	10.000	sys_clk_pin
Path 4	6.961	2	13	SPI1/FSM_seq...cs_reg[1]/C	SPI1/rx_data_reg[1]/CE	2.657	0.901	1.756	10.000	sys_clk_pin

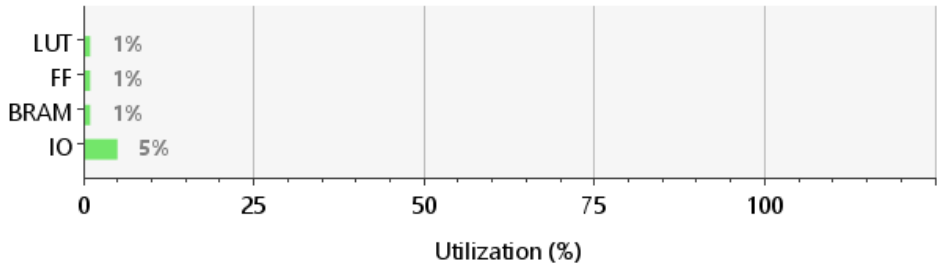

RAM1
E
MISO_out_reg
MISO_out_reg_0
Q[7:0]
Ram_reg_2
WEA
clk_IBUF_BUFG
rst_n_IBUF
tx_valid_reg_0
RAM
Ram_reg_0
Ram_reg_1
SR
tx_valid_WIRE
MOSI_IBUF_inst
I
O
IBUF
SS_n_IBUF_inst
I
O
IBUF
SPI1
MISO_out_reg_0
MISO_out_reg_1
MOSI_IBUF
SR
SS_n_IBUF
clk_IBUF_BUFG
rst_n_IBUF
tx_valid_WIRE
SPI_SLAVE
Counter_reg[0]_0
Counter_reg[1]_0
E
MISO_OBUF
Q[7:0]
WEA
rx_data_reg[8]_0
tx_valid_reg

3-Implementation

- One Hot

Utilization Report

Resource	Utilization	Available	Utilization %
LUT	34	20800	0.16
FF	33	41600	0.08
BRAM	0.50	50	1.00
IO	5	106	4.72



Timing

Setup

Worst Negative Slack (WNS):	5.668 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	73

Hold

Worst Hold Slack (WHS):	0.100 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	73

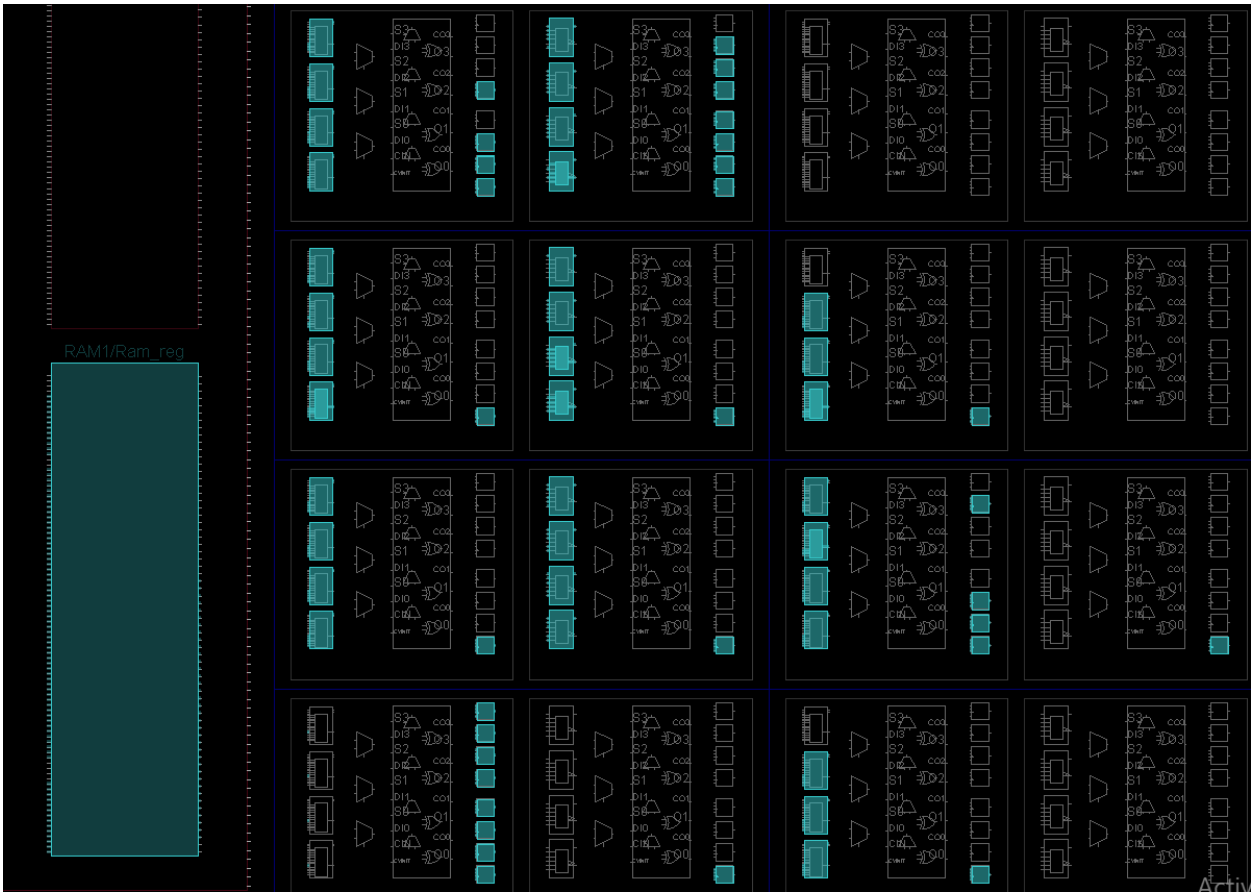
Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	36

Path 1	5.668	2	1	RAM1/Ram_...CLKBWRCLK	SPI1/MISO_out_reg/D	4.306	2.702	1.604	10.000	sys_clk_pin
Path 2	6.403	2	10	SPI1/FSM_one...cs_reg[2]/C	SPI1/rx_data_reg[4]/CE	3.332	1.078	2.254	10.000	sys_clk_pin
Path 3	6.464	2	10	SPI1/FSM_one...cs_reg[2]/C	SPI1/rx_data_reg[8]/CE	3.258	1.078	2.180	10.000	sys_clk_pin
Path 4	6.519	2	10	SPI1/FSM_one...cs_reg[2]/C	SPI1/rx_data_reg[2]/CE	3.239	1.078	2.161	10.000	sys_clk_pin
Path 5	6.601	2	10	SPI1/FSM_one...cs_reg[2]/C	SPI1/rx_data_reg[5]/CE	3.170	1.078	2.092	10.000	sys_clk_pin

Device

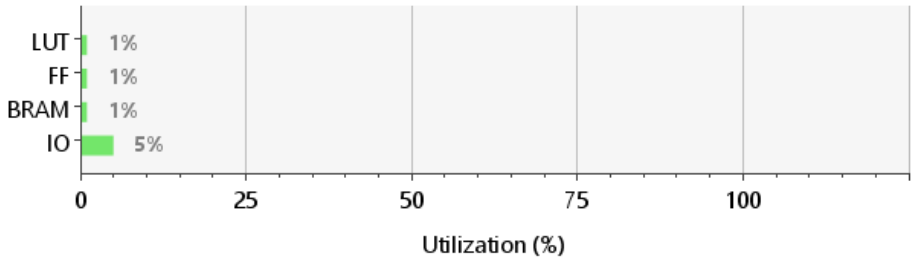
We used a synchronous reset so that vivado could implement it as ram block



- Gray

Utilization Report

Resource	Utilization	Available	Utilization %
LUT	33	20800	0.16
FF	31	41600	0.07
BRAM	0.50	50	1.00
IO	5	106	4.72



Timing

Setup

Worst Negative Slack (WNS):	5.577 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	75

Hold

Worst Hold Slack (WHS):	0.044 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	75

Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	34

Name	Slack ^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Des
Path 1	5.577	2	1	RAM1/Ram_...CLKBWRCLK	SPI1/MISO_out_reg/D	4.349	2.702	1.647	10.000	sys_clk_pin	sys_
Path 2	6.422	3	16	SPI1/Counter_reg[2]/C	SPI1/Counter_reg[0]/D	3.296	1.047	2.249	10.000	sys_clk_pin	sys_
Path 3	6.428	3	16	SPI1/Counter_reg[2]/C	SPI1/Counter_reg[3]/D	3.285	1.049	2.236	10.000	sys_clk_pin	sys_
Path 4	6.487	1	12	SPI1/FSM_gray_cs_reg[1]/C	SPI1/Counter_reg[0]/R	2.928	0.773	2.155	10.000	sys_clk_pin	sys_

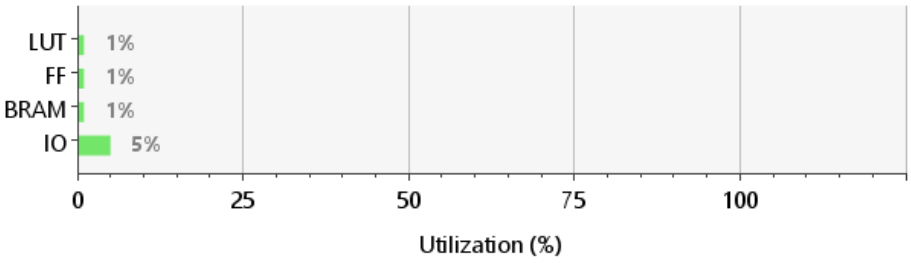
Device

We used a synchronous reset so that vivado could implement it as ram block

- Sequential

Utilization Report

Resource	Utilization	Available	Utilization %
LUT	34	20800	0.16
FF	31	41600	0.07
BRAM	0.50	50	1.00
IO	5	106	4.72



Timing

Setup

Worst Negative Slack (WNS):	5.814 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	75

Hold

Worst Hold Slack (WHS):	0.044 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	75

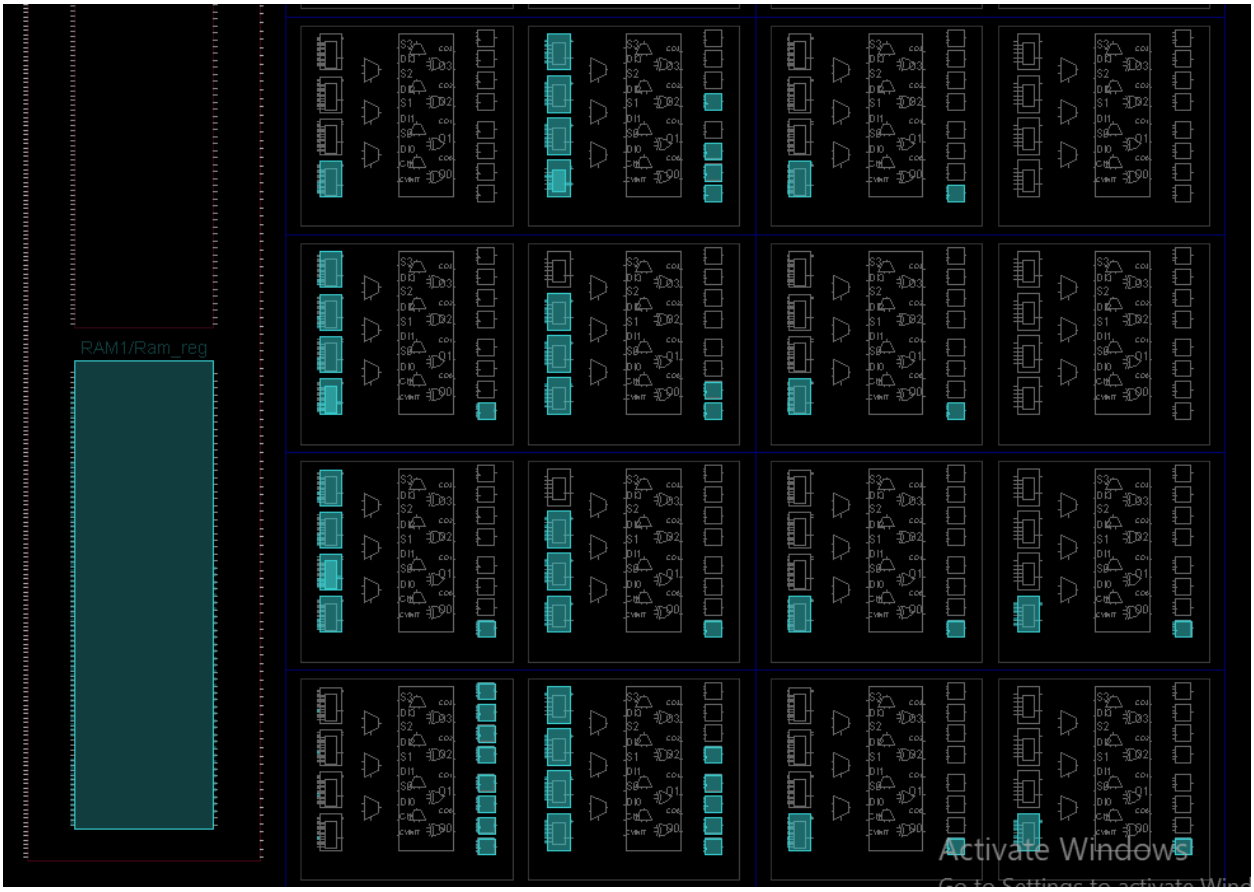
Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	34

Name	Slack ^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	De
Path 1	5.814	2	1	RAM1/Ram_...CLKBWRCLK	SPI1/MISO_out_reg/D	4.160	2.702	1.458	10.000	sys_clk_pin	sys
Path 2	6.002	3	16	SPI1/Counter_reg[2]/C	SPI1/rx_valid_reg/D	3.967	1.202	2.765	10.000	sys_clk_pin	sys
Path 3	6.187	2	16	SPI1/Counter_reg[2]/C	SPI1/Counter_reg[0]/CE	3.573	1.078	2.495	10.000	sys_clk_pin	sys
Path 4	6.187	2	16	SPI1/Counter_reg[2]/C	SPI1/Counter_reg[1]/CE	3.573	1.078	2.495	10.000	sys_clk_pin	sys
Path 5	6.187	2	16	SPI1/Counter_reg[2]/C	SPI1/Counter_reg[2]/CE	3.573	1.078	2.495	10.000	sys_clk_pin	sys

Device

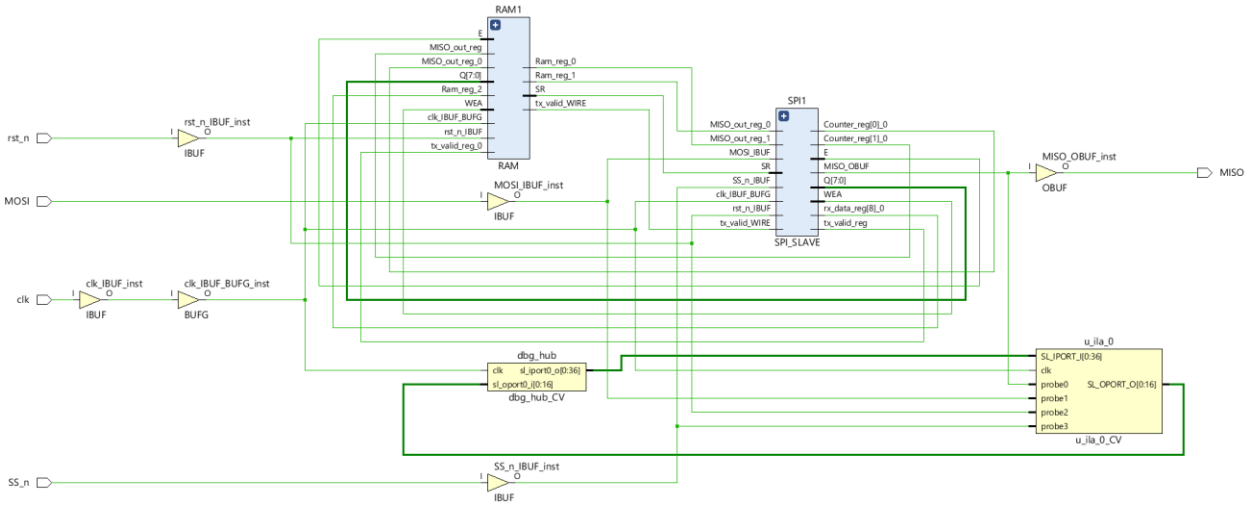
We used a synchronous reset so that vivado could implement it as ram block



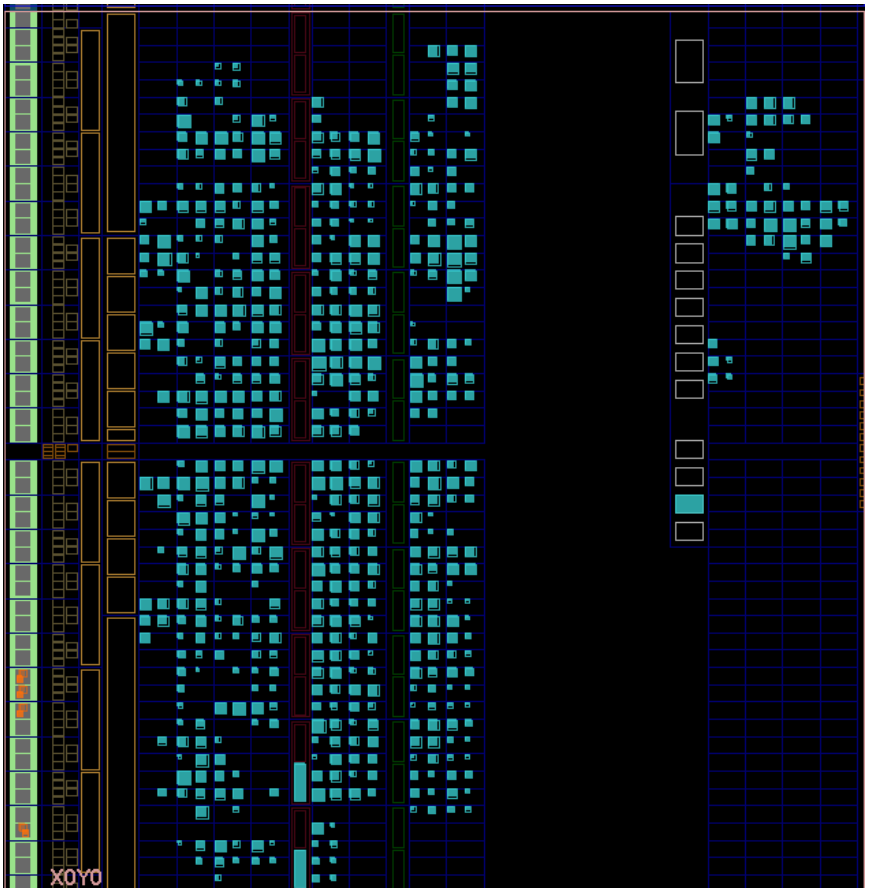
We saw that sequential encoding has the best Timing

After Debuging

Synthesized schematic



Implemented Device



4- Snippet of the “Messages” tab showing no critical warnings or errors