VERILOG ASSIGNMENT

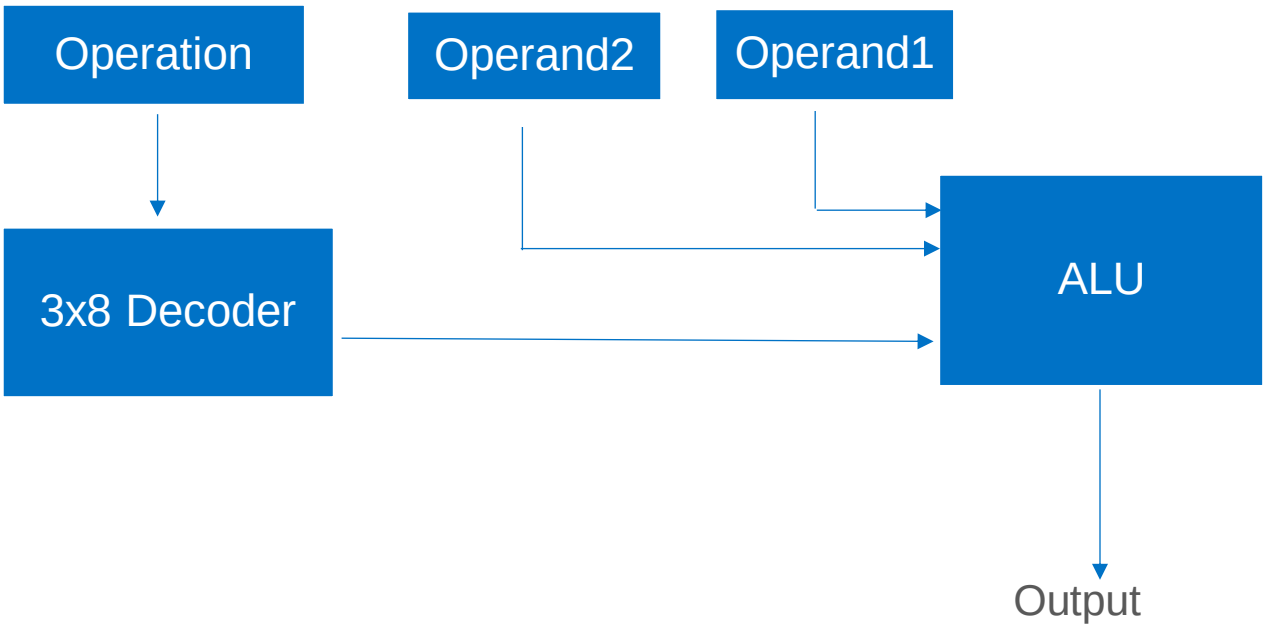
PROBLEM STATEMENT

To create a simple CPU using Verilog that performs the following instructions on 8-bit

- Add
- Subtract
- Increment
- Decrement
- AND
- OR
- NOT

APPROACH

The CPU Unit takes a 19-bit instruction as input. This instruction is split into a 3-bit operation, and two 8-bit operands. The 3-bit operation is passed into a decoder which gives an 8-bit control bus as output. The ALU takes the control bus and operands as input, and performs the operations on them and gives the required output.



FILES USED:-

FullAdder.v – Contains two modules : HalfAdder and FullAdder

- HalfAdder takes two one-bit inputs(A, B) , and outputs the sum and carry bits generated by them. Sum is the XOR of the two inputs and carry is the AND of the two inputs.
- FullAdder takes three one-bit inputs(A,B and Ci), and outputs the sum and carry bits generated by them. It uses two HalfAdder modules.

ADD_SUB.v – Contain two modules : ADD and SUB

- ADD takes two 8-bit buses and outputs the sum of the two. It uses 8 FullAdder modules to compute the result. It uses Ripple Carry Addition principle.
- SUB takes two 8-bit buses and outputs the difference(A-B). The result is obtained by adding A to the 2's complement of B using the ADD module. 2's complement is obtained by taking NOT of B and incrementing.

AND_OR_NOT.v – Contains three modules : AND, OR and NOT.

- AND takes two 8-bit buses and outputs the logic AND of the two.
- OR takes two 8-bit buses and outputs the logic OR of the two.
- NOT takes one 8-bit bus and outputs the logic NOT.

INC_DEC.v – Contains two modules : INC and DEC.

- INC takes an 8-bit bus and outputs the number obtained by incrementing it.
- DEC takes an 8-bit bus and outputs the number obtained by decrementing it.

CPU.v – Central Processing Unit.

- Takes a 19-bit instruction as input. Seperates the instruction to a 3-bit operation, and two 8-bit operands.
- Implements a 3x8 decoder taking the operation as input and an 8-bit control bus as output.
- Sends the operands and control bus to the ALU.
- Output of the ALU is the result.

ALU.v – Arithmetic and logic unit.

- Takes the two 8-bit operands and an 8-bit control bus as inputs and outputs an 8-bit result.
- Uses the seven modules and stores their outputs.
- Takes AND of the the seven modules with the corresponding control bus signal.
- Finally it takes OR of all the seven to give the final output.

SNAPSHOT OF GTKWAVE OUTPUT