NATIONAL POLYTECHNIC INSTITUTE SUPERIOR SCHOOL OF COMPUTER SCIENCES

Analog Electronics.

Practice 9: Analog-To-Digital Converter.

Hernandez Martinez Carlos David. Cruz Medina Isaac Abraham. Herrera Albavera Luis Enrique.

Group: 2cv3.

November 28, 2017

Contents

1	Objective:	2
2	Introduction: 2.1 Ladder-Network Conversion:	3 4
3	Development: 3.1 Analog-To-Digital Converter:	5 5
4	Simulations: 4.1 Analog-To-Digital Converter:	7 7
5	Theoretical Analysis: 5.1 Analog-To-Digital Converter:	9 9
6	Questionnaire:	11
7	Conclusion:	12
8	Bibliographic References:	13

1 Objective:

- The student will understand the functionality of the analog-to-digital converters.
- The student will difference the different techniques that the converters implement.
- \bullet The student will interpreted the results of the constructed circuits.

2 Introduction:

A popular method for converting an analog voltage into a digital value is the dual-slope method. Figure 1.0 (a) shows a block diagram of the basic dual-slope converter. The analog voltage to be converted is applied through an electronic switch to an integrator or ramp-generator circuit (essentially a constant current charging a capacitor to produce a linear ramp voltage). The digital output is obtained from a counter operated during both positive and negative slope intervals of the integrator. The method of conversion proceeds as follows. For a fixed time interval (usually the full count range of the counter), the analog voltage connected to the integrator raises the voltage at the comparator input to some positive level. Figure 1.0 (b) shows that at the end of the fixed time interval the voltage from the integrator is greater for the larger input voltage. At the end of the fixed count interval, the count is set to zero and the electronic switch connects the integrator to a reference or fixed input voltage.

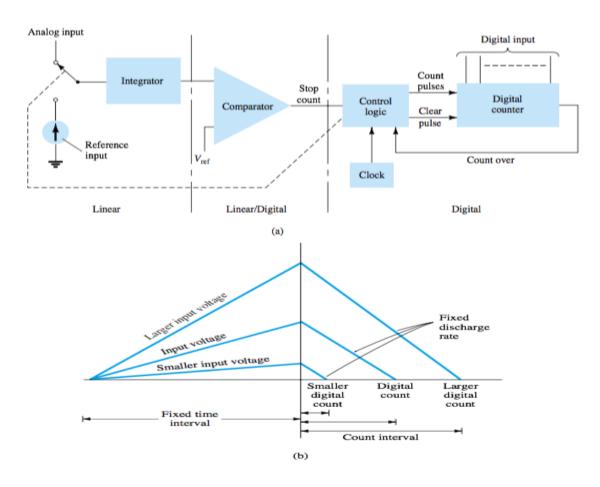


Figure 1.0: Analog-to-digital conversion using dual-slope method: (a) logic diagram; (b) waveform

The integrator output (or capacitor input) then decreases at a fixed rate. The counter advances during this time, while the integrators output decreases at a fixed rate until it drops below the comparator reference voltage, at which time the control logic receives a signal (the comparator output) to stop the count. The digital value stored in the counter is then the digital output of the converter. Using the same clock and integrator to perform the conversion during positive and negative slope intervals tends to compensate for clock frequency drift and integrator accuracy limitations. Setting the reference input value and clock rate can scale the counter output as desired. The counter can be a binary, BCD, or other form of digital counter, if desired.

2.1 Ladder-Network Conversion:

Another popular method of analog-to-digital conversion uses a ladder network along with counter and comparator circuits (see Figure 1.1). A digital counter advances from a zero count while a ladder network driven by the counter outputs a stair- case voltage, as shown in Figure 1.1 (b) which increases one voltage increment for each count step. A comparator circuit, receiving both staircase voltage and analog input voltage, provides a signal to stop the count when the staircase voltage rises above the input voltage. The counter value at that time is the digital output. The amount of voltage change stepped by the staircase signal depends on the number of count bits used. A 12-stage counter operating a 12-stage ladder network using a reference voltage of 10 V would step each count by a voltage of:

$$\frac{V_{ref}}{2^{12}} = \frac{10 \ V}{4096} = 2.4 \ mV.$$

This would result in a conversion resolution of 2.4 mV. The clock rate of the counter would affect the time required to carry out a conversion. A clock rate of 1 MHz operating a 12-stage counter would need a maximum conversion time of:

$$(4096)(1\mu s) = 4096\mu s \approx 4.1 \ ms.$$

The minimum number of conversions that could be carried out each second would then be:

Number of Conversions =
$$\frac{1}{4.1 \text{ ms}} \cong 244 \frac{conversions}{second}$$
.

Since on the average, with some conversions requiring little count time and others near maximum count time, a conversion time of $\frac{4.1\,ms}{2}=2.05\,ms$ would be needed, and the average number of conversions would be $2\cdot 244=488\,\frac{conversions}{second}$ A slower clock rate would result in fewer conversions per second. A converter using fewer count stages (and less conversion resolution) would carry out more conversions per second. The conversion accuracy depends on the accuracy of the comparator.

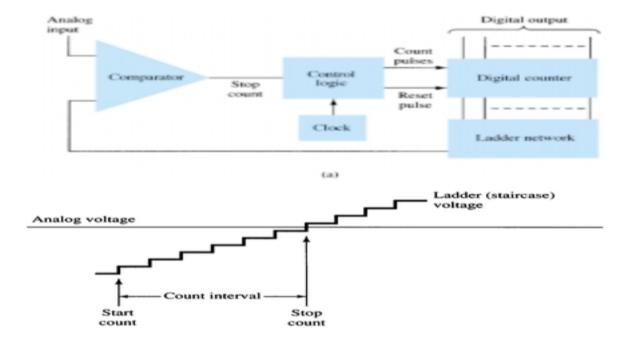


Figure 1.1: Analog-to-digital conversion using ladder network: (a) logic diagram; (b) waveform.

3 Development:

Using a **ADC0804** we are going to construct the circuit presented in Figure 3.0, the **LM35** must be connected like in Figure 3.1.

3.1 Analog-To-Digital Converter:

Once the Circuit of Figure 3.0 were assembled, we connected the **LM35** to the terminal 6 of the **ADC0804**, then, with the help of a lighter we variate the temperature of the sensor, this provided different voltage levels.

Observation: Both devices (ADC0804 and LM35) must be connected to a 5 $V_{\rm cc}$ source.

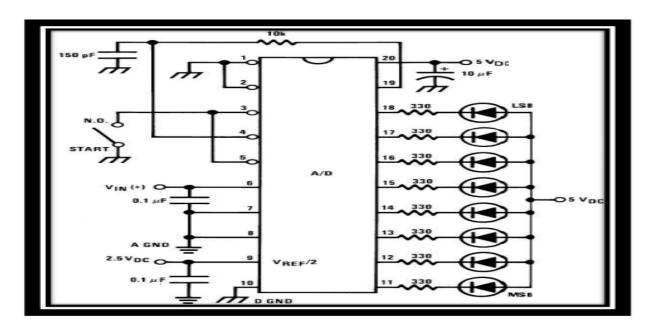


Figure 3.0: Analog-to-digital converter circuit.

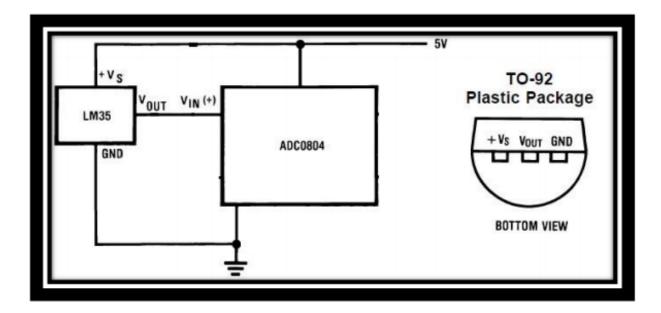


Figure 3.1: LM35 diagram.

Table 1 provide in its first column the voltage of the sensor, in its third column it's represented the binary-combination (the terminal 18 of the **ADC0804** it's the least-significant bit and the terminal 11 it's the most-significant bit) that the **ADC** provided on its output and the second column it's the temperature of the sensor. This are the final results of the practice that later will be compared with the *Theoretical* and *Simulated* results.

Sensor Voltage	Temperature	Binary Combination
0.42 V	42°	0010 1011
0.39 V	39°	0010 1000
0.36 V	36°	0010 0101
0.35 V	35°	0010 0100
0.33 V	33°	0010 0010
0.31 V	31°	0010 0000
0.29 V	29°	0001 1110
0.27 V	27°	0001 1100

Table 1: Practice results.

4 Simulations:

For each circuit that we have analyze in the section 3, we simulate each one of them, and we proceeded to make a comparative table with all the simulated, theoretical and development results.

4.1 Analog-To-Digital Converter:

The circuit presented in Figures 4.0 and 4.1 it's the same that we have analyzed in section's 3 Figure 3.0.

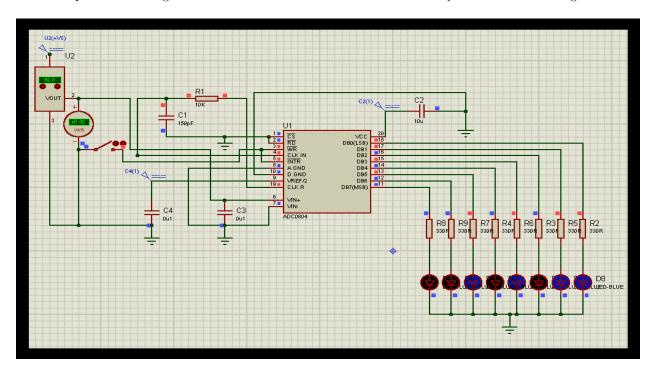


Figure 4.0: Analog-to-digital converter simulated circuit with a Sensor-Voltage $V_a = 0.42 \text{ V}$.

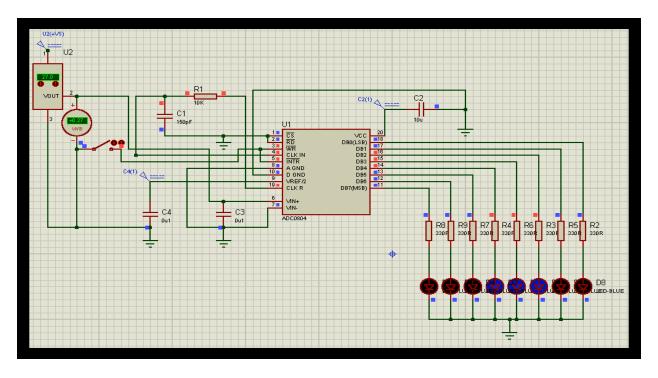


Figure 4.1: Analog-to-digital converter simulated circuit with a Sensor-Voltage $V_a=0.27~{\rm V}.$

Same as section 3, we capture the results in Table 2 according to the development's Table's 1 column **sensor voltage** to see if the simulated values are similar. Figure 4.0 represents the higher input voltage measured and Figure 4.1 the lowest input voltage. As we can see the simulated values are exactly the same as the development ones.

Sensor Voltage	Temperature	Binary Combination
0.42 V	42°	0010 1011
0.39 V	39°	0010 1000
0.36 V	36°	0010 0101
0.35 V	35°	0010 0100
0.33 V	33°	0010 0010
0.31 V	31°	0010 0000
0.29 V	29°	0001 1110
0.27 V	27°	0001 1100

Table 2: Simulated results.

5 Theoretical Analysis:

For the circuit that we have analyzed in the section 3, we make a theoretical analysis of it and we proceeded to make a comparative table with all the theoretical, simulated and the development results in section 6.

5.1 Analog-To-Digital Converter:

According to the counter that the **ADC0804** has, if the analog-voltage (V_a) it's higher than the digital-voltage (V_b) then the counter will have an *positive-edge* and the binary-output will increase in one unit, the process will stop until the following condition it's accomplish: $V_b \geq V_a$.

So, we will use a $V_{ref}=2.5$ V which the V_b will increase $\frac{2.5}{2^8}\cong 9.79x10^{-3}$ per iteration.

• For the first iteration:

When the binary-output it's equals to "0000 0000" $V_b = 0$ V then, the V_a which it's equals to 2.5 V it's higher, so the counter will increase in 1 unit.

• For the second iteration:

When the binary-output it's equals to "0000 0001" $V_b = \frac{2.5}{2^8} \cong 9.79x10^{-3} \text{ V}$ then, the V_a which it's equals to 2.5 V it's higher, so the counter will increase in 1 unit.

• For the third iteration:

When the binary-output it's equals to "0000 0010" $V_b = 0.019$ V then, the V_a which it's equals to 2.5 V it's higher, so the counter will increase in 1 unit.

• For the fourth iteration:

When the binary-output it's equals to "0000 0011" $V_b = 0.029$ V then, the V_a which it's equals to 2.5 V it's higher, so the counter will increase in 1 unit.

If we repeat this process consecutively we will have results showed in Table 3.

Iteration	V_b	Binary Combination
1	0 V	0000 0000
2	$9.79x10^{-3} \text{ V}$	0000 0001
3	0.019 V	0000 0010
4	0.029 V	0000 0011
5	0.039 V	0000 0100
6	0.048 V	0000 0101
7	0.058 V	0000 0110
8	0.068 V	0000 0111
9	0.078 V	0000 1000

Iteration	V_b	Binary Combination
10	0.087 V	0000 1001
11	0.097 V	0000 1010
12	0.10 V	0000 1011
13	0.11 V	0000 1100
14	0.12 V	0000 1101
15	0.13 V	0000 1110
16	0.14 V	0000 1111
17	0.15 V	0001 0000
18	0.16 V	0001 0001
19	0.17 V	0001 0010
20	0.18 V	0001 0011
21	0.19 V	0001 0100
22	0.20 V	0001 0101
23	0.21 V	0001 0110
24	0.22 V	0001 0111
25	0.23 V	0001 1000
26	0.24 V	0001 1001
27	0.25 V	0001 1010
28	0.26 V	0001 1011
29	0.27 V	0001 1100
30	0.28 V	0001 1101
31	0.29 V	0001 1110
32	0.30 V	0001 1111
33	0.31 V	0010 0000
34	0.32 V	0010 0001
35	0.33 V	0010 0010
36	0.34 V	0010 0011
37	0.35 V	0010 0100
38	0.36 V	0010 0101
39	0.37 V	0010 0110
40	0.38 V	0010 0111
41	0.39 V	0010 1000
42	0.40 V	0010 1001
43	0.41 V	0010 1010
44	0.42 V	0010 1011

Table 3: Theoretical results.

Finally, if we search for the development's sensor-voltages we can visualize that the binary-combination generated it's exactly the same.

6 Questionnaire:

• What does the LSB and the MSB?

The MSB refers to the most-significant bit and the LSB refers to the least-significant bit.

• What are the most suitable circuits to place the reference voltage at the ADC?

Any type of indicator that is needed in a circuit practical applications aeither temperature sensors, signaling devices, photo-resistors, or any device that delivers a value differing as they will modify their input values.

• Name 5 different techniques of analog to digital conversion:

- 1. ADCs.
- 2. Basic-steps converter.
- 3. Staircase ramp.
- 4. Successive approximations.
- 5. Dual-slop converter.

• What is the difference between ADC0801 and ADC0804?

The ADC0804 use successive approximations and the ADC0801 use staircase ramp technique.

• Which of the two ADC used in practice is the fastest and why?

The fastest is the successive approximations because use a *Johnson's Counter*, this allows to the ADC to find the binary-combination in the same times that output bits that the ADC has, for example if the ADC has 8 bits, then the counter will find the value in 8 cycles, others ADC like the *staircase ramp* find the most higher value in 2^n iterations.

7 Conclusion:

The ADC are one of the most powerful devices with a lot of applications in the industry, as well we can find that they implement different techniques which the most faster it's the *Successive approximations*, as well it's very interesting to see that a device can convert an analog-voltage to a binary-combination.

8 Bibliographic References:

 $[\ 1\]$ BOYLESTAD, Robert L. "Electronic Devices and Circuit Theory". Edit. Prentice Hall. 2009.