CENG311
Programming Assignment 3 - Report

300201051

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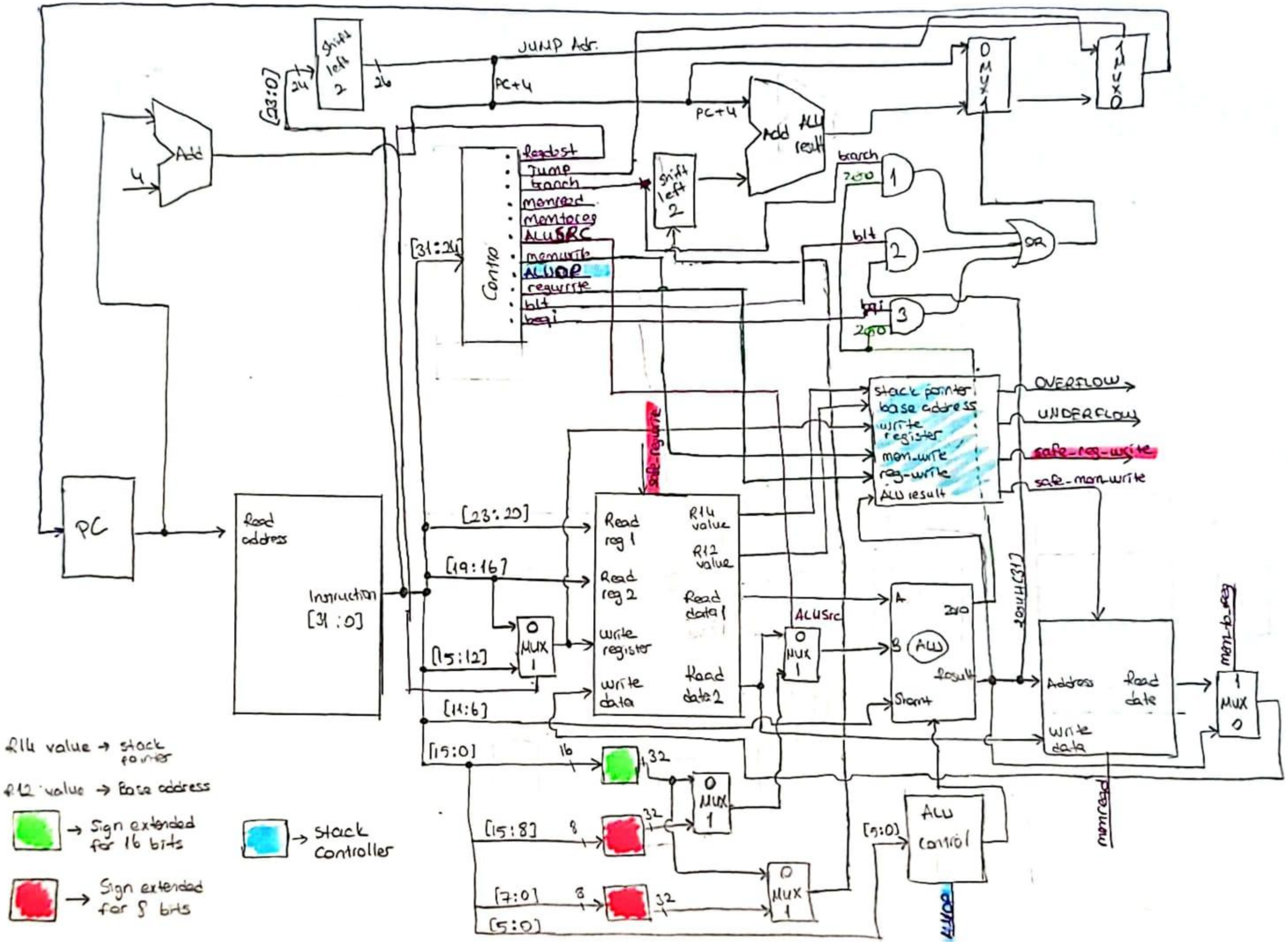
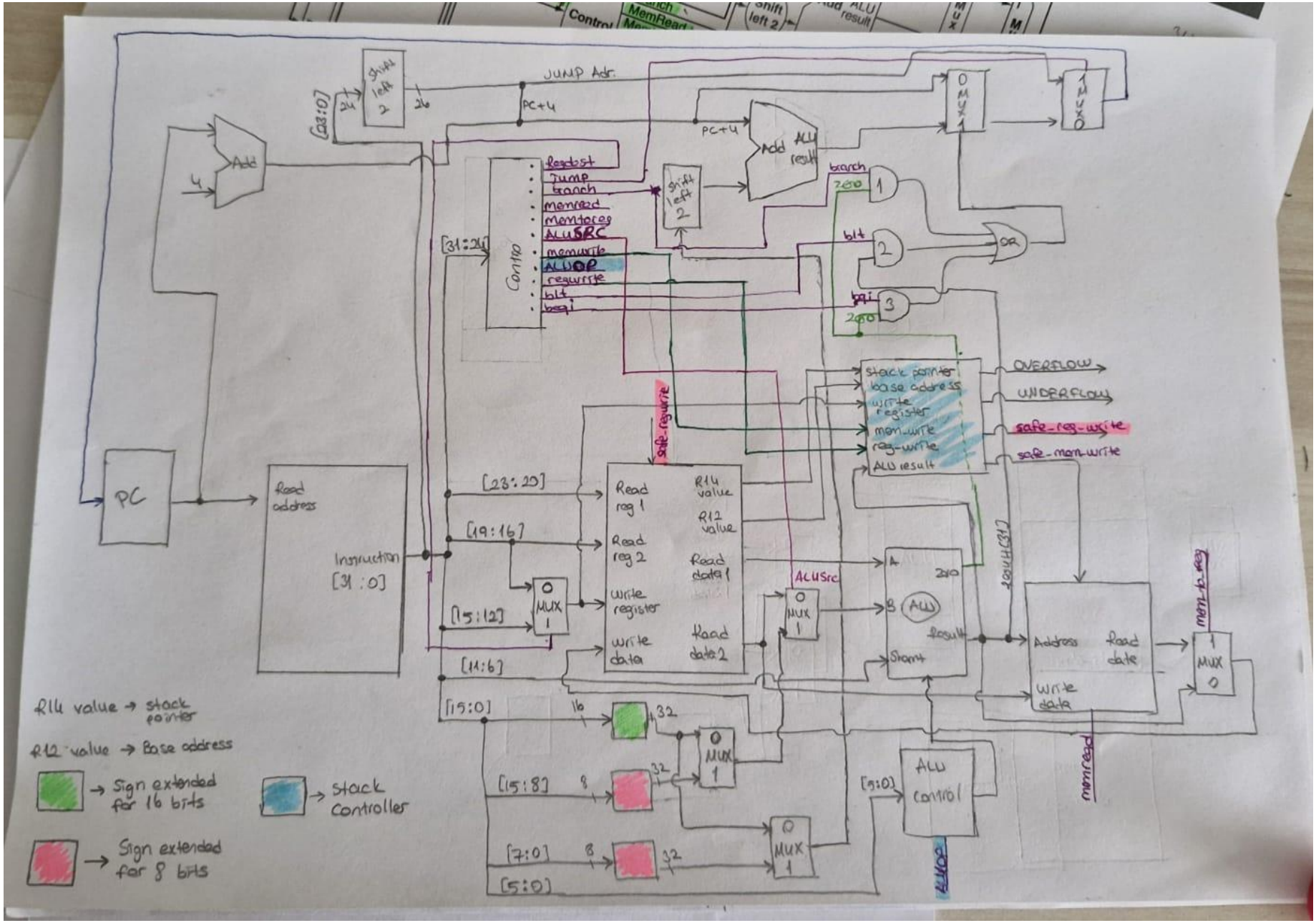
Instruction Set Architecture (ISA)

Opcode (Decimal)	Opcode (Binary)	Function Field (Decimal)	Function Field (Binary)	Instruction
51	00110011	1	000001	sll (R-type)
51	00110011	2	000010	$move$ (R-type)
51	00110011	3	000011	$nand$ (R-type)
51	00110011	4	000100	or (R-type)
51	00110011	5	000101	add (R-type)
52	00110100	X	xxxxxx	lw (I-type)
53	00110101	X	xxxxxx	sw (I-type)
54	00110110	X	xxxxxx	beq (I-type)
55	00110111	X	xxxxxx	blt (I-type)
56	00111000	X	xxxxxx	$subi$ (I-type)
57	00111001	X	xxxxxx	$addi$ (I-type)
58	00111010	X	xxxxxx	$beqi$ (B-I-type)
59	00111011	x	xxxxxx	j (J-type)

Diagram

In the below, there are two format of diagram. One of them is scanned version and the other is original image.


JUMP Adr.
Shift left 2
[23:0]
24
26
PC+4
Add
4
PC
Read address
Instruction [31:0]
Control
RegDst
Jump
branch
memread
memtoreg
ALUSRC
memwrite
ALUOP
regwrite
blt
beqi
[31:26]
Shift left 2
Add ALU result
branch
zero
blt
beqi
OR
MUX
[23:20]
[19:16]
[15:12]
[11:6]
[15:0]
[15:8]
[7:0]
[5:0]
Read reg 1
Read reg 2
write register
write data
R14 value
R12 value
Read data 1
Read data 2
safe-regwrite
stack pointer
base address
write register
mem-write
reg-write
ALU result
OVERFLOW
UNDERFLOW
safe-reg-write
safe-mem-write
ALUSrc
A
B
ALU
zero
result
Start
ALU control
ALUOP
Address
Read data
write data
memread
mem-to-reg
16
32
8
R14 value → stack pointer
R12 value → Base address
→ Sign extended for 16 bits
→ Sign extended for 8 bits
→ Stack Controller


JUMP Adr.
PC+4
Add
4
shift left 2
[25:0]
Control
Regdest
Jump
branch
memread
memtoreg
ALUSRC
memwrite
ALUOP
regwrite
blt
beqi
[31:26]
branch
zero
blt
beqi
OR
PC
Read address
Instruction [31:0]
[23:20]
[19:16]
[15:12]
[11:6]
[15:0]
[15:8]
[7:0]
[5:0]
Read reg 1
Read reg 2
Write register
Write data
R14 value
R12 value
Read data 1
Read data 2
safe_regwrite
stack pointer
base address
write register
mem_write
reg_write
ALU result
OVERFLOW
UNDERFLOW
safe_reg_write
safe_mem_write
ALUSrc
A
B
ALU
result
Shamt
zero
Address
Read data
Write data
memtoreg
memread
ALU control
[5:0]
ALUOP
16
32
8
MUX
R14 value → stack pointer
R12 value → Base address
→ Sign extended for 16 bits
→ Sign extended for 8 bits
→ stack controller