Practical No. 11 : Completely Random Design (CRD)

Four different designs for a digital computer circuit are being studied to compare the amount of noise present. The following data have been obtained:

Circuit Design	Noise Observed				
1	19	20	19	30	08
2	80	61	73	56	80
3	45	26	25	35	50
4	95	46	83	78	97

Enter this data in Minitab and generate the following reports:

Questions :

a) Carry out one-way ANOVA to determine whether same amount of noise present for all four designs? Use $\alpha = 0.05$.
b) Which circuit design would you select for use? Low noise is best.

Solution :

Step 1 : Type your data into the data pane of a worksheet. Make sure you put your data into columns. Use column headers for “Noise level”, and “Circuit type”. Type the “Noise level” data into column C1 and “Circuit type” data into column C2.

Step 2 : To perform completely random design (CRD), under the drop-down menu “Stat”, choose “ANOVA” then “One-Way…”. A “One-Way Analysis of Variance” dialogue box will appear. In the drop-down menu, choose “Response data are in one column for all factor levels”. Set the “Response:” as “C1 Noise level” and “Factor:” as “C2 Circuit type” from the table on the left.

Step 3 : Click on the “Options…” option. A “One-Way Analysis of Variance: Options” dialogue box will appear. Check the “Assume equal variances” checkbox. Set the “Confidence level:” as 95 and “Type of confidence interval:” as “Two-sided”. Click “OK”.

Step 4 : Click on the “Comparisons…” option. A “One-Way Analysis of Variance: Comparisons” dialogue box will appear. Set the “Error rate for comparisons:” as 5. Under the “Comparison procedures assuming equal variances”, check the “Tukey” checkbox. Under the “Results”, check the “Interval plot for differences of means” and “Grouping information” checkboxes. Click “OK”.

Step 5 : Click on the “Graphs…” option. A “One-Way Analysis of Variance: Graphs” dialogue box will appear. Under the “Data plots”, check the “Interval plot” checkbox. Under “Residual plots”, check the “Four in one” radio box. Click “OK”. Click “OK” again.

Method :

Null hypothesis	All means are equal
Alternative hypothesis	Not all means are equal
Significance level	$\alpha = 0.05$

Equal variances were assumed for the analysis.

Factor Information :

Factor	Levels	Values
Circuit type	4	1, 2, 3, 4

Test of significance of factor level :

Analysis of Variance :

Source	DF	Adj SS	Adj MS	F-Value	P-Value
Circuit type	3	12102	4033.9	22.18	0.000
Error	16	2910	181.9		
Total	19	15012			

Conclusion :

Since p-value (0.000) is less than significance level (0.05), we strongly reject H0 in favor of H1 at 5% level of significance. Hence, there is a significant difference in the mean noise levels of circuit designs.

Model Summary :

S	R-sq	R-sq(adj)	R-sq(pred)
13.4870	80.61%	76.98%	69.71%

Interpretation :

The reliability of linear model for CRD is 76.98%. We are 76.98% confident in predicting noise level knowing the circuit type using linear model.

Means :

Circuit type	N	Mean	StDev	95% CI
1	5	19.20	7.79	(6.41, 31.99)
2	5	70.00	11.02	(57.21, 82.79)
3	5	36.20	11.17	(23.41, 48.99)
4	5	79.80	20.51	(67.01, 92.59)

Pooled StDev = 13.4870

Interpretation :

The table shows that circuit 1 has the lowest mean noise level (best design) and circuit 4 has the highest mean noise level (worst design).

Pairwise Comparison :

Grouping Information Using the Tukey Method and 95% Confidence :

Circuit type	N	Mean	Grouping	
4	5	79.80	A	
2	5	70.00	A	
3	5	36.20		B
1	5	19.20		B

Means that do not share a letter are significantly different.

Interpretation :

On performing pairwise comparison, we found 2 clusters or groups: Group A includes circuit design 2 and 4 (similar effects) and Group B includes circuit design 1 and 3 (similar effects).

Mean plot :

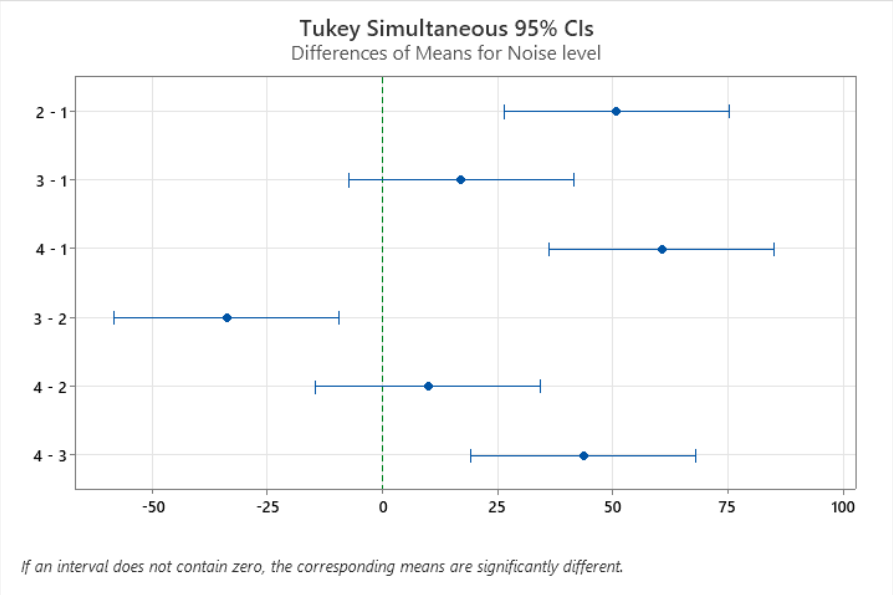

Fig 1 : Plot of differences of means for noise levels

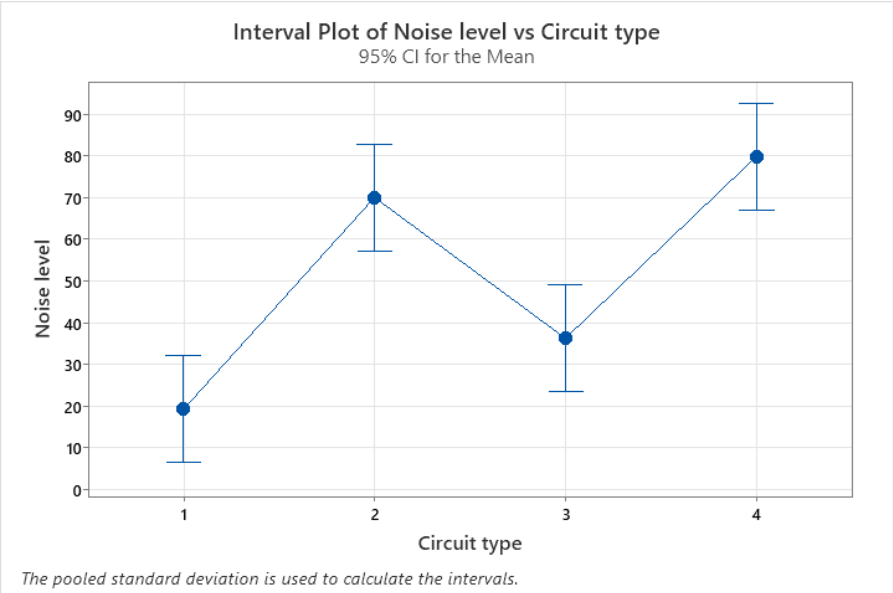

Fig 2 : Interval plot of noise level vs circuit type

Residual Analysis :

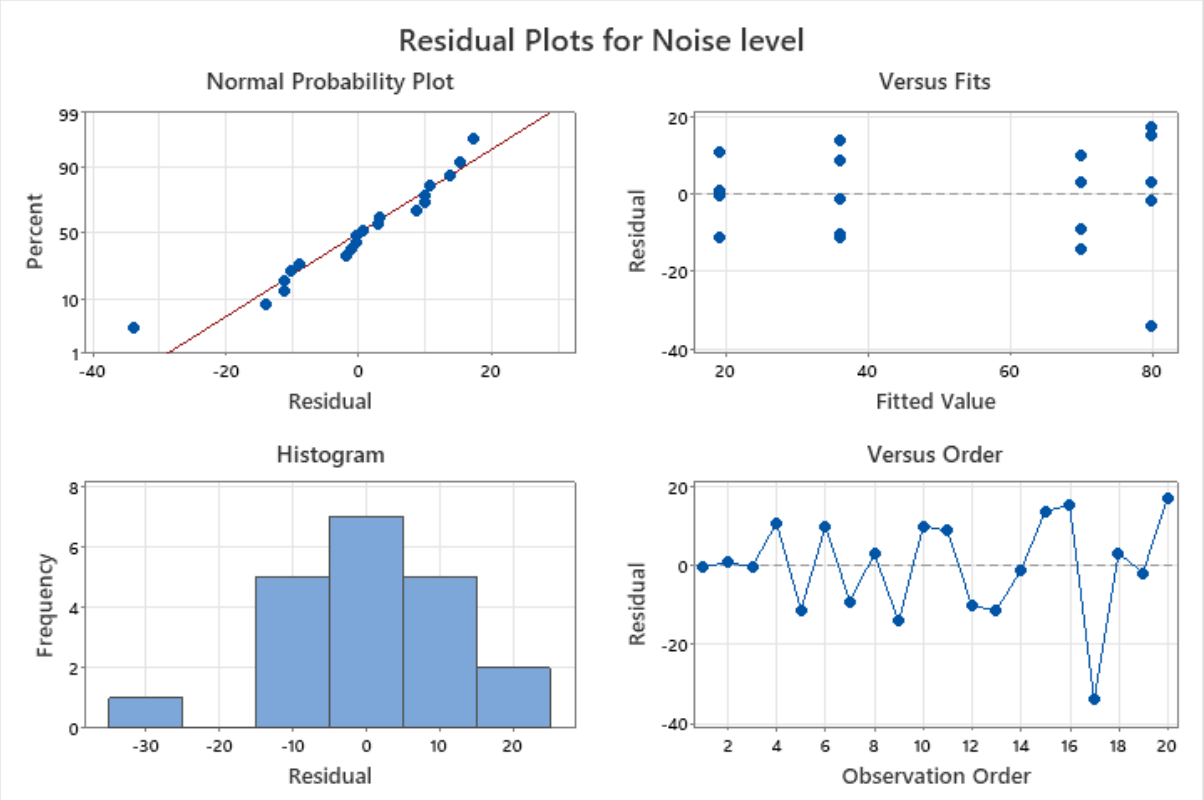

Fig 3 : Residual Analysis

(i) **Normality check of error distribution:** The histogram and normal probability plot shows that the error distribution is not satisfactorily normal i.e., it is left skewed. It may be due to the small sample size.

(ii) **Equal variance check:** The second graph shows that the distribution of dots about reference line e = 0 is almost same or equal, suggesting homoscedasticity. Hence, the assumption of equal variance across different levels of primary factor is satisfactorily met, however there is one potential extreme value in the graph.

(iii) **Linear relationship check:** The second graph also shows that the distribution of dots about the reference line e = 0 (below and above the line) has no obvious pattern (pattern is random), indicating linear model is valid for CRD.

(iv) **Independence of error check:** The fourth graph (graph of error vs observation order) shows that error distribution is in random pattern, indicating independence of errors. It means that positive and negative errors are in random order.

Worksheet :

↓	C1	C2	C3	C4	C5
	Noise level	Circuit type			
1	19	1			
2	20	1			
3	19	1			
4	30	1			
5	8	1			
6	80	2			
7	61	2			
8	73	2			
9	56	2			
10	80	2			
11	45	3			
12	26	3			
13	25	3			
14	35	3			
15	50	3			
16	95	4			
17	46	4			
18	83	4			
19	78	4			
20	97	4			
21					
22					