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Experiment no - 6

Aim :- To design and implement 2 bit magnitude using basic gates.

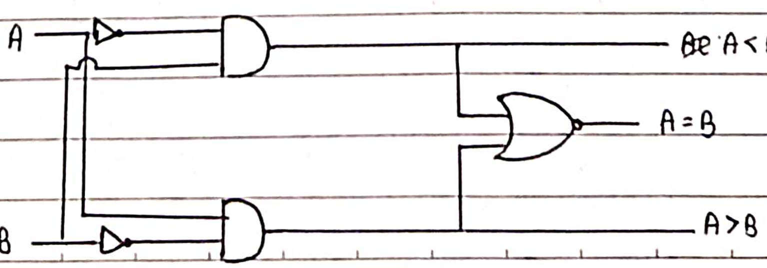
Apparatus :- 7C7408, 7C7480, 7C7432, 7C704

Theory :- A magnitude digital comparator is a combinational circuit that compares two ~~diagrams~~ digital or ~~bim~~ binary number. We logically design a circuit for which we will have two inputs one for A and the other B and have ~~their~~ three output terminals one for A > B one for A = B and one for A < B

1 bit magnitude comparator

A →	Comparator for 1 bit Numbers.	→ A > B
B →		→ A = B
		→ A < B

Input		Output		
A	B	$Y_{A=B}$	$Y_{A>B}$	$Y_{A<B}$
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0



(A<B) equation.

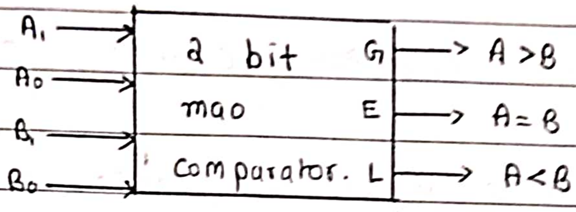
$\bar{A}B = A<B$

$\overline{\bar{A}B + A\bar{B}} = AB + \bar{A}\bar{B}$

$A > B = A\bar{B}$

* 2 bit magnitude comparator.

A magnitude comparator used to compare two binary numbers each of 2 bits is called a 2 bit magnitude comparator. It consists of 4 inputs and 3 outputs to generate less than equal to and greater than between two binary numbers.



A_1	A_0	B_1	B_0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Kmap.

A_1A_0 \ B_1B_0	00	01	11	10
00				
01	1			
11	1	1		1
10	1	1		

$A > B = A_0\overline{B_0}\,\overline{B_1} + A_1\overline{B_1} + A_1\overline{B_0}A_0$

A_1A_0 \ B_1B_0	00	01	11	10
00		1	1	1
01			1	1
11				
10			1	

$A < B = \overline{A_1}\,\overline{A_0}B_0 + \overline{A_0}B_0B_1 + \overline{A_1}B$

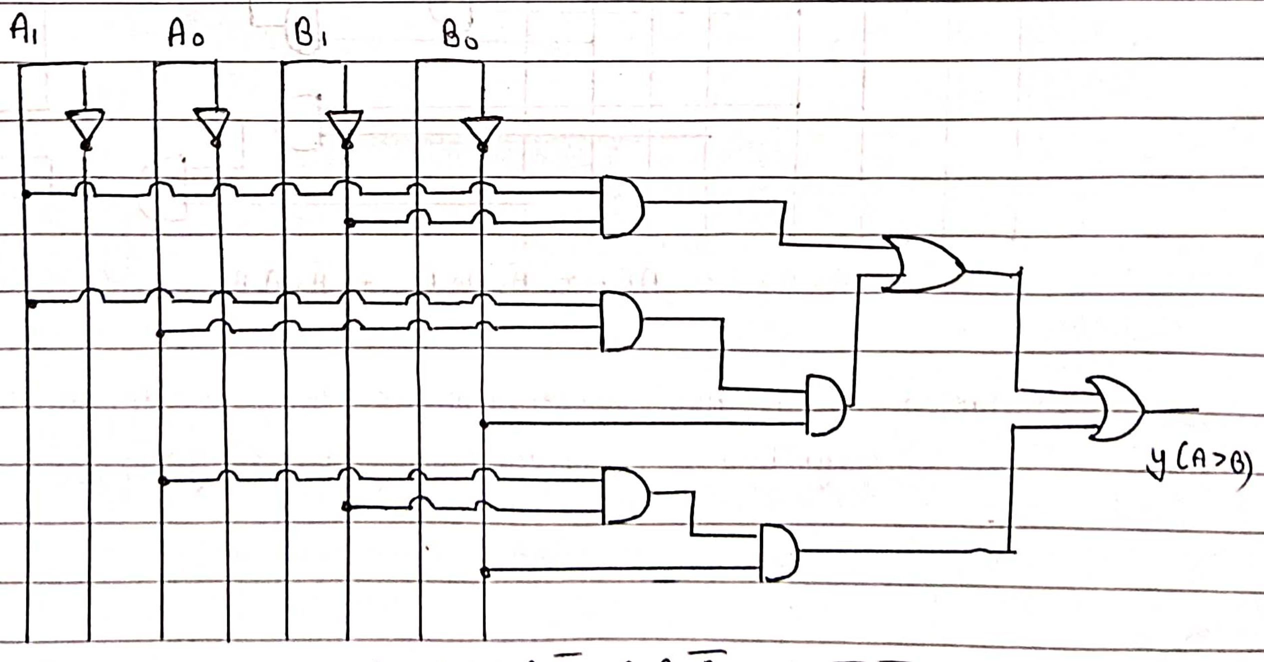
A_1A_0 \ B_1B_0	00	01	11	10
00	1			
01		1		
11			1	
10				1

$A = B \quad (A_0 \oplus B_0)(A_1 \oplus B_1)$

A_1A_0 \ B_1B_0	00	01	11	10
00				
01	1			
11	1	1		1
10	1			

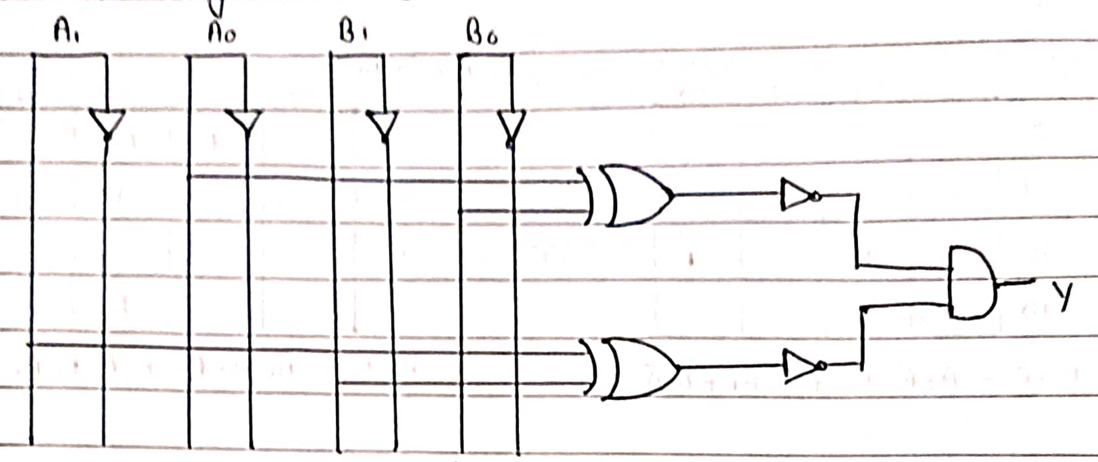
$A > B = A_0\overline{B_0}B_1 + AB_1 + A_1A_0\overline{B_0}$

$A > B$.



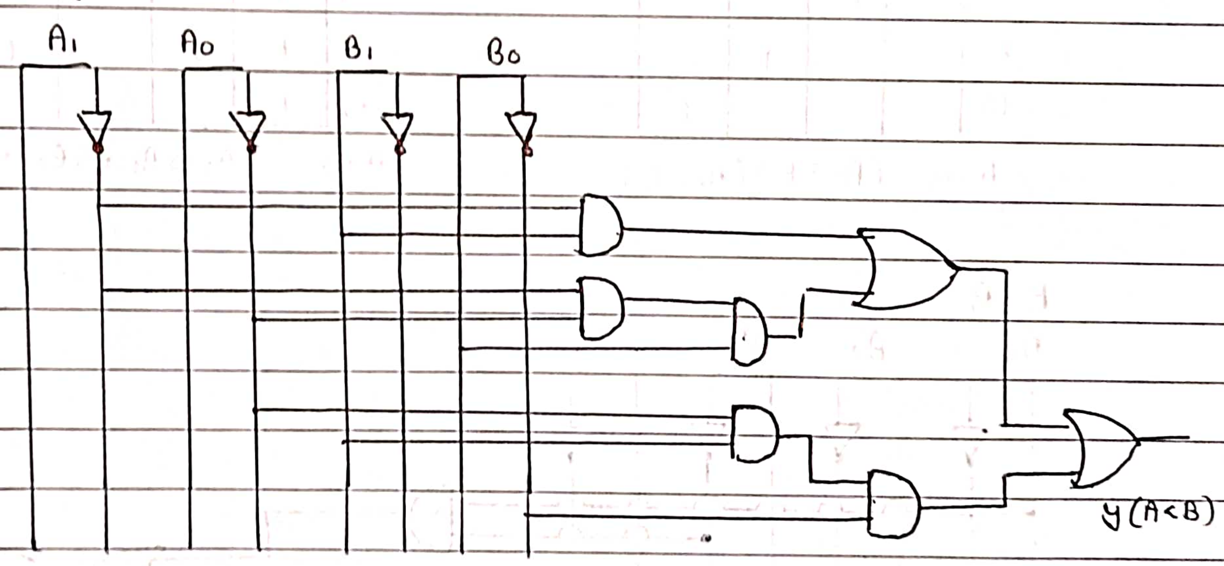
$y(A>B) = A_1\overline{B} + A_1A_0\overline{B_1} + A_0\overline{B_1}\,\overline{B_0}$

Circuit Diagram A = B.



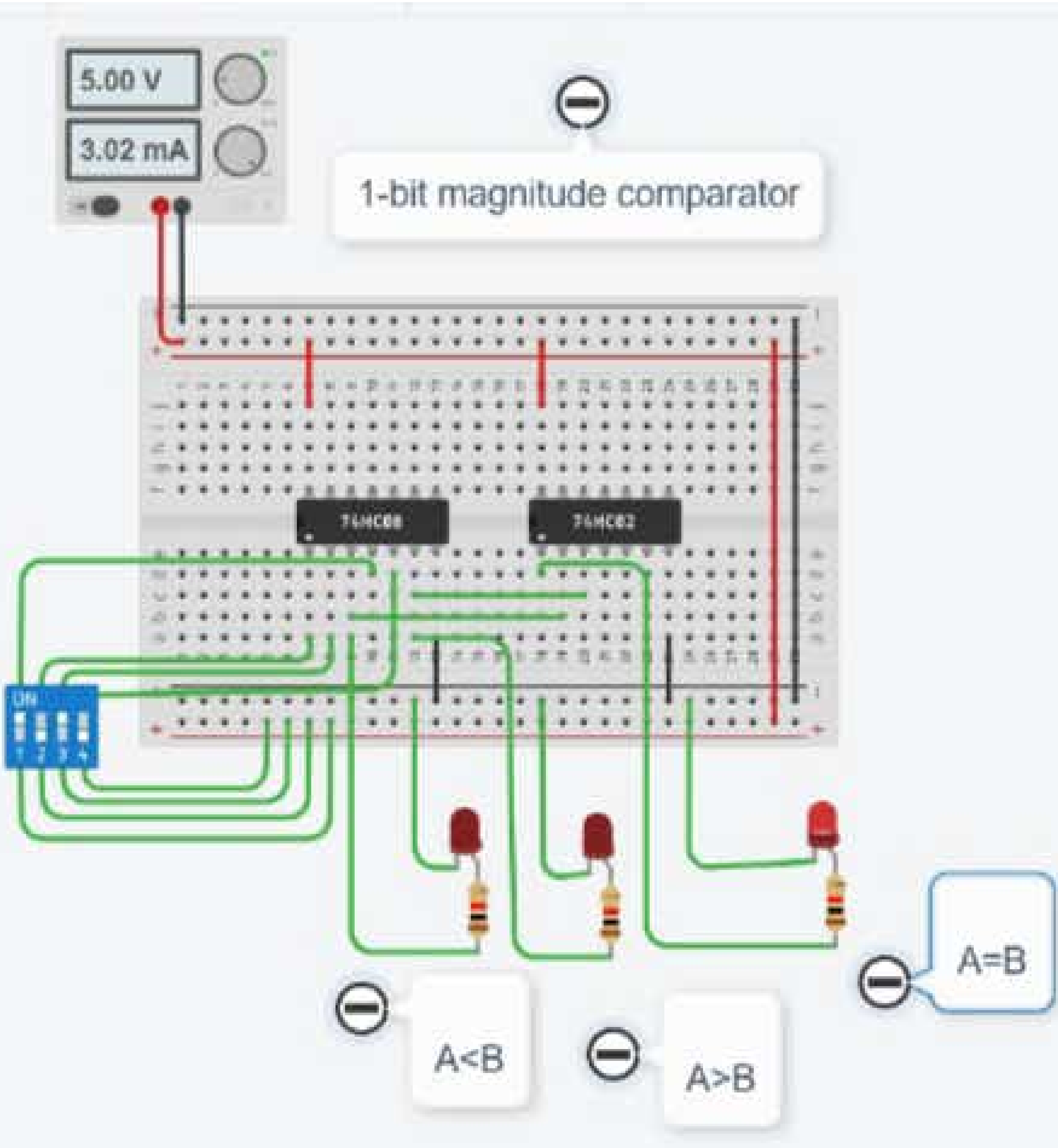
$$A = B = \overline{(A_0 \oplus B_0)}\,\overline{(A_1 \oplus B_1)}$$

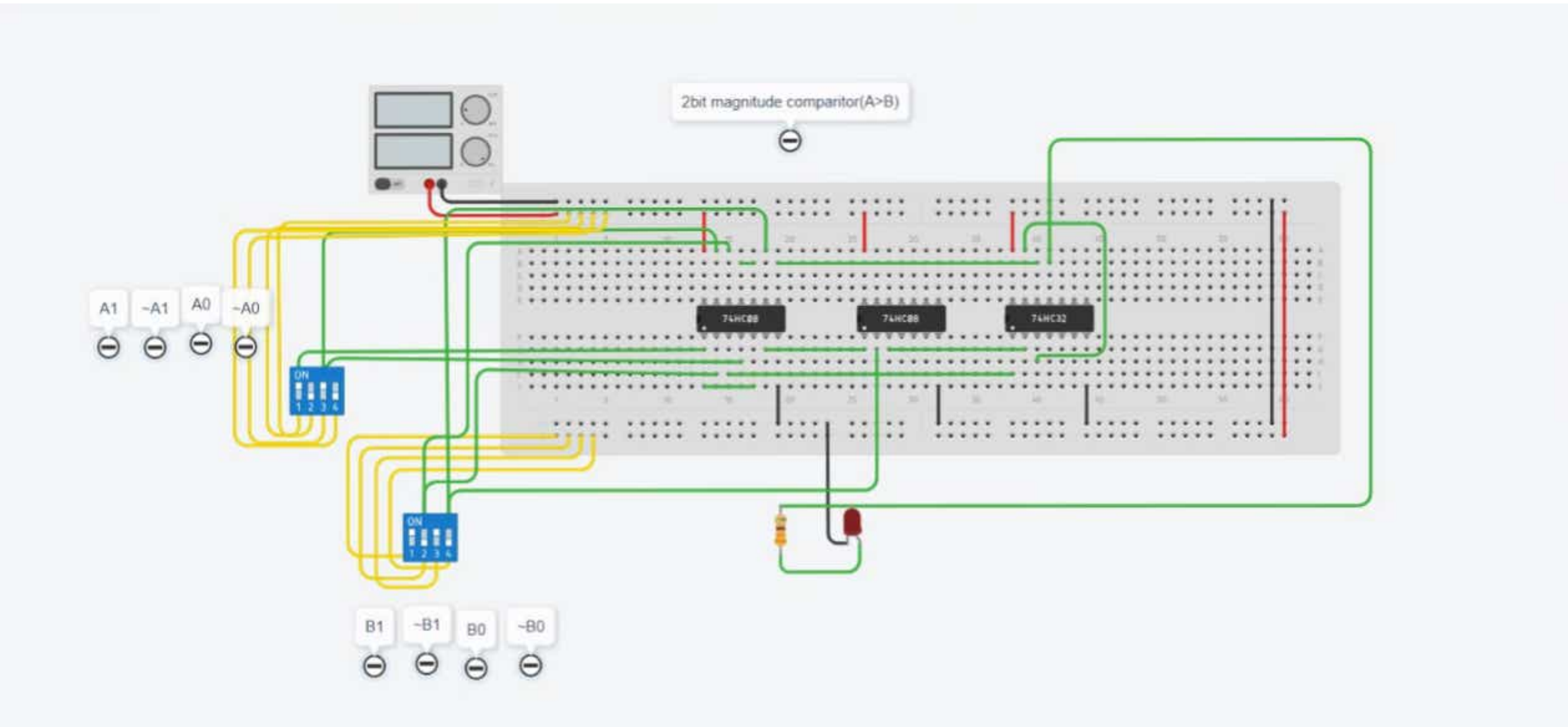
A<B

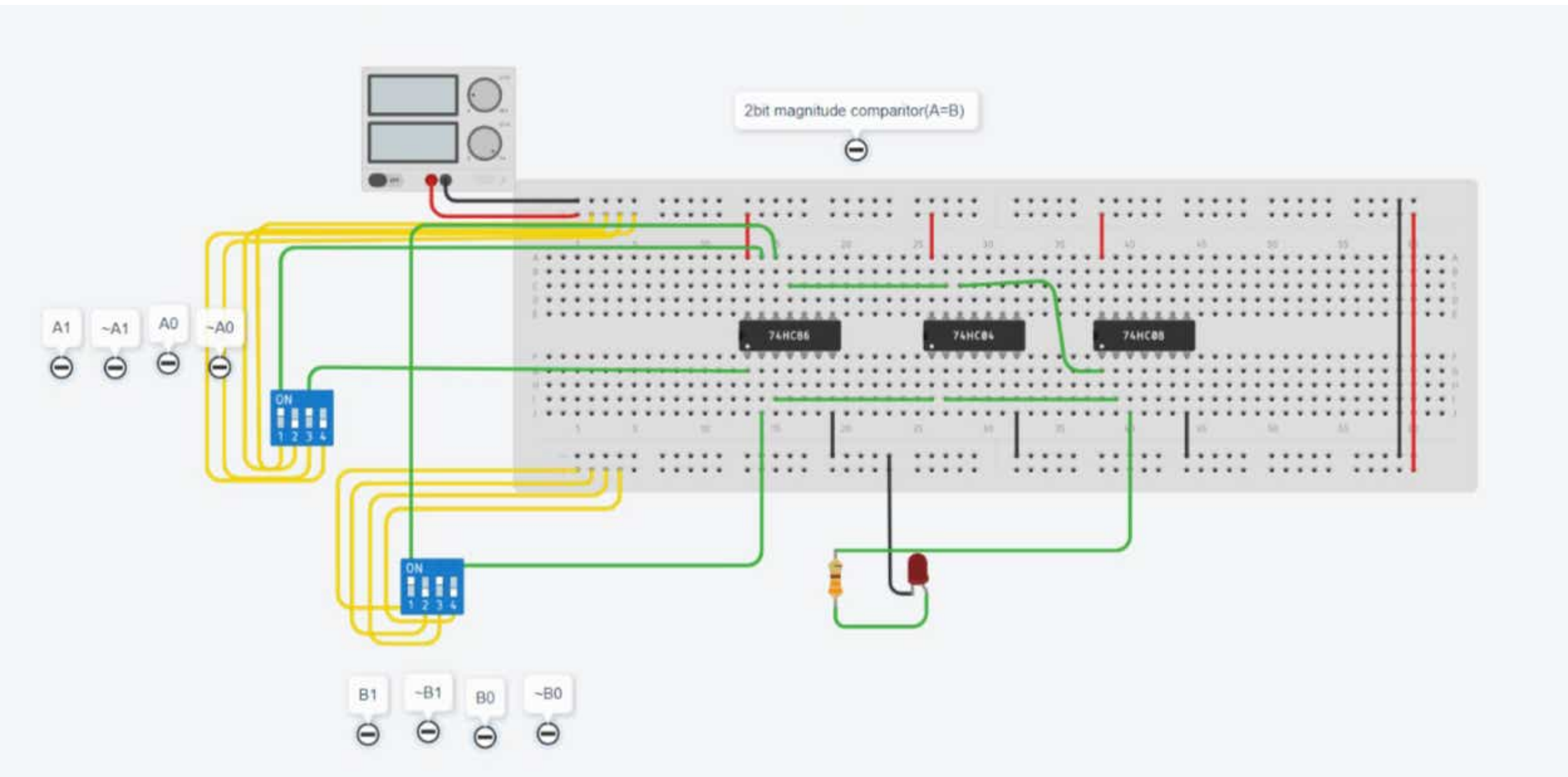


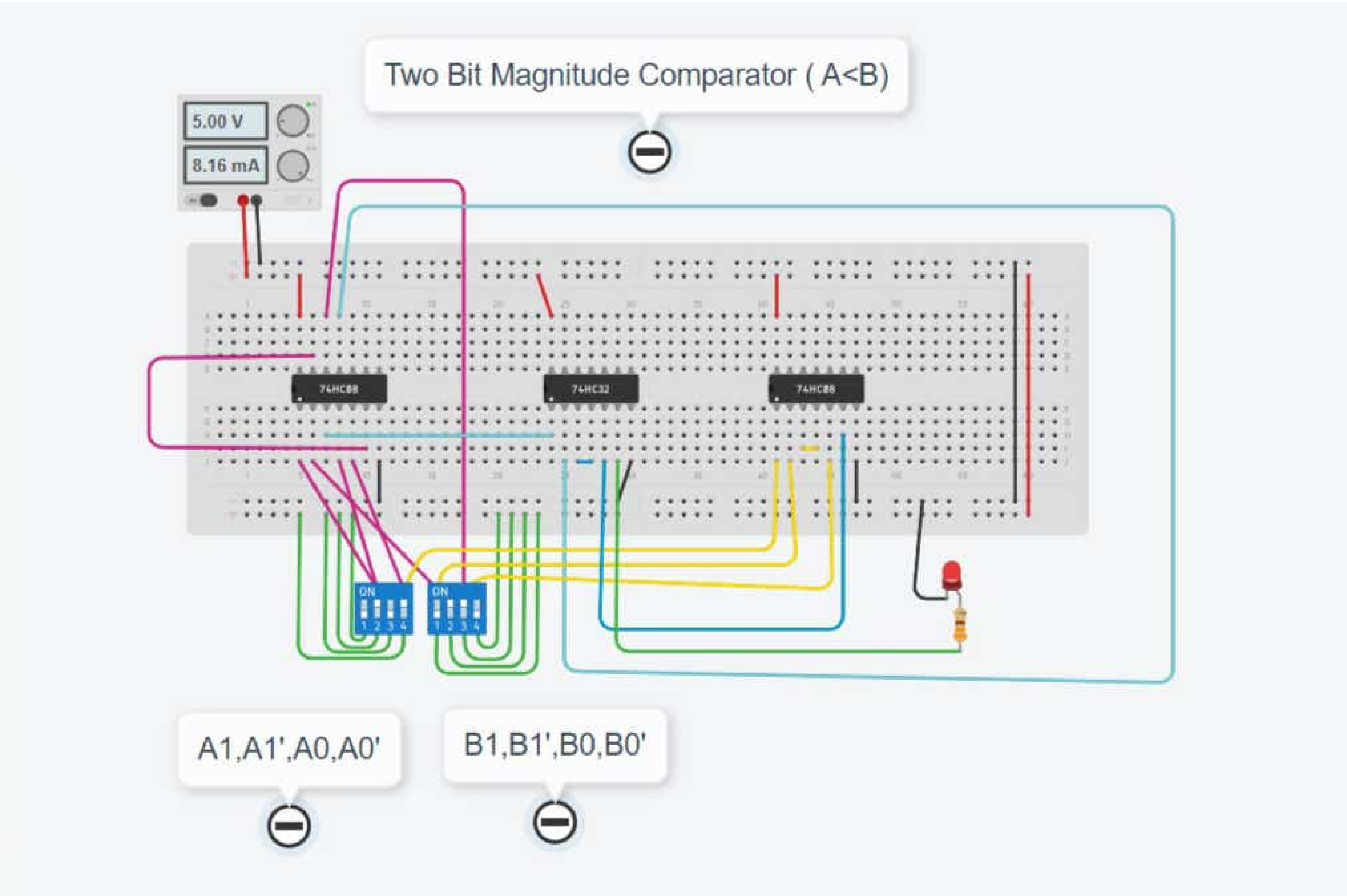
$$(A<B) = \bar{A}B_1 + \bar{A_1}\bar{A_0}B_0 + \bar{A_0}B_1B_0$$

Conclusion:- In this experiment we learn to design two bit magnitude comparator using basic gates.


5.00 V
3.02 mA
1-bit magnitude comparator
74HC08
74HC02
ON
A<B
A>B
A=B


2bit magnitude comparitor(A>B)
A1
~A1
A0
~A0
B1
~B1
B0
~B0
74HC08
74HC08
74HC32


2bit magnitude comparitor(A=B)
A1
~A1
A0
~A0
B1
~B1
B0
~B0
74HC86
74HC04
74HC08



Two Bit Magnitude Comparator (A<B)
5.00 V
8.16 mA
74HC08
74HC32
74HC08
A1,A1',A0,A0'
B1,B1',B0,B0'