Ayush Vinod Upadhyay

IO74 I-1

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_ {	LDCA - Experiment 4													
	Aim	<b>c</b> h	ecker.	TO OF	1			pari	hy	devex	ator	and p	arity_	
Control of the contro	Apparatus: Tinker CAD software													
	bit d	rity ata a	nd g	ator eneru	: I+ tes the	16 a	co tiriona	1 bit	\	iat is	s to b	that e tro bit.	accep	ts n-l
	Even - Parity generator Odd - Parity generator.										rator.			
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41.4.	K	- map	800	0 0		parit	J gen	erator		, ,	1	eir		
			0 0		0	0			•					

(Sundaram)

	K-map for 3-bit odd parity generator									
	P = A B B B C									
	1 0 1 0 1 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2									
	P = ABC + ABC + ABC									
	$= \overline{A}(\overline{B}C + B\overline{C}) + A(\overline{B}\overline{C} + BC)$									
1-11 -:	= A (BOC) r A (BOC)									
N	AL DE CARLO									
	The white P = KA & B & C tid Lorent Day 2 and persons the sub-									
	A									
+ 15-	Every Mande and Same									
	c									
	Even Parity Generator.									
1	A—————————————————————————————————————									
	8—17									
1 - 12	Odd- Parity Grenerator.									
Ü	@ Parity Checker.									
	It is a logic circuit that checks for possible errors in transmission									
	when it is used as an even parity checker, the number of input bit									
	must to always be even.									
	Even - parity checker.									
2	If any error occurs the received message consists of odd no. of I's.									
	The output of parity checker is denoted by PEC (parity error checker)									
<u>Sundaram</u>	FOR EDUCATIONAL USE									

3 bit even parity checker (OIP, PEO1)
3 bit odd parity checker (OIP, PEO2) Bo Ba B, PEO, PEO2 ) 1. 

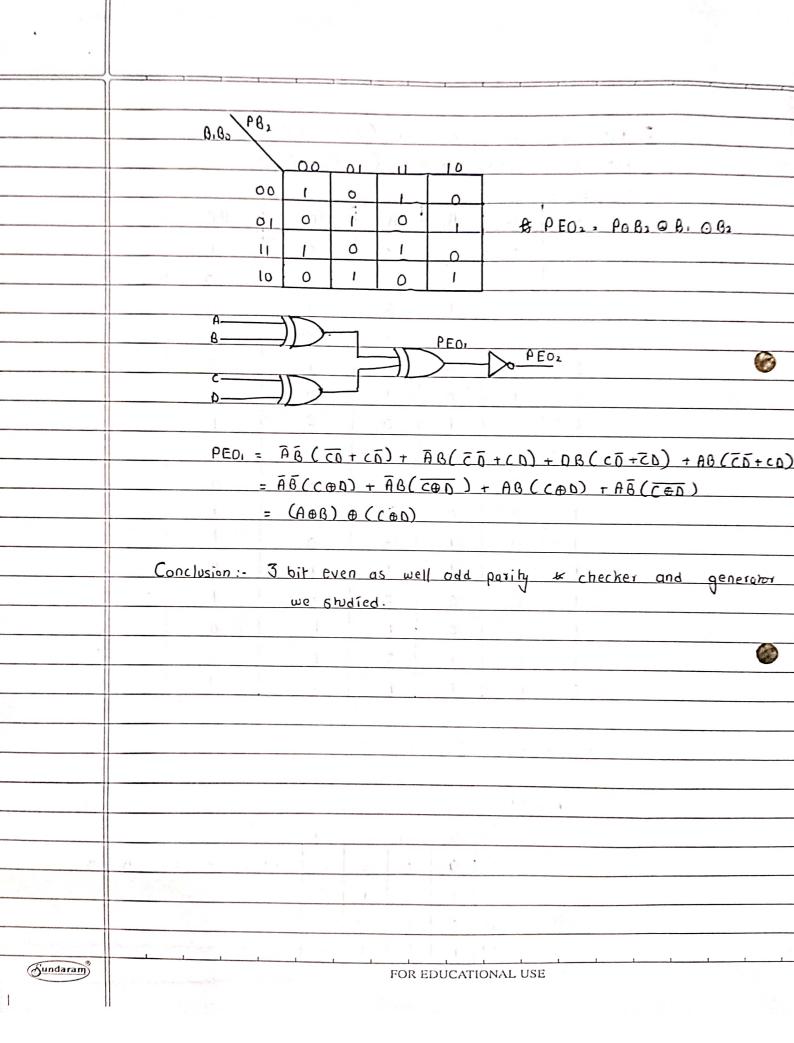
K-map for PEO, and PEO.

PB2 B. G. PEO: = P & B2 & B1 & B0 

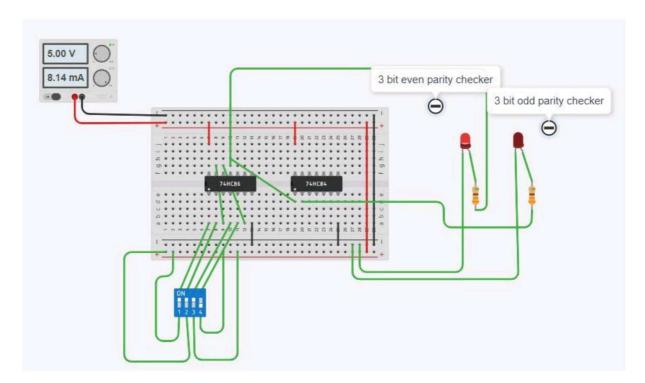
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## **PARITY CHECKER**



## **PARITY GENERATOR**

