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9/11/23

Experiment no 9.

Aim: To design 2 bit synchronous counter using D flip-flop (MOD 4)

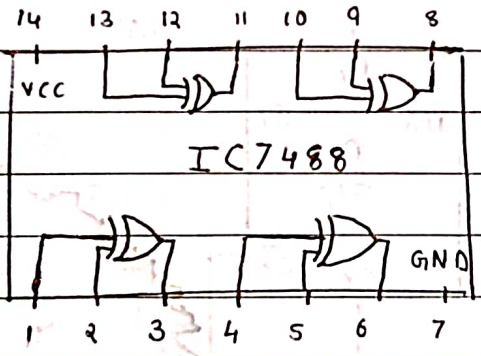
Apparatus: Breadboard, connecting with Led board, power supply, IC7474, IC7486.

Theory:

A counter is a device which stores the number of times a particular event or process has occured, often in relationship to a clock signal. Synchronous counter has one global clock which drives each flip-flop so output changes in parallel.

The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have commelative delay.

Pin diagram :-

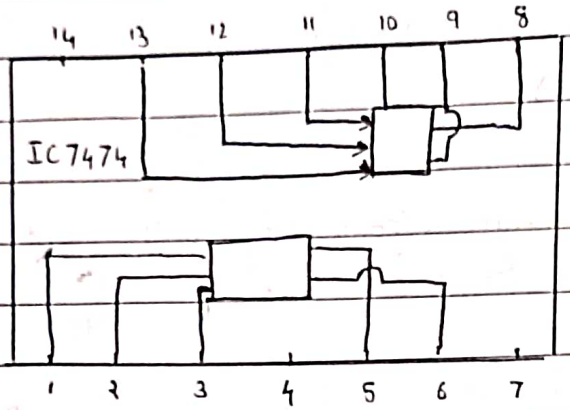


Quad 2 :- Input Exclusive OR gate:

This device contains four independent gates each of which performs the logic exclusive OR fraction.

(A) (i/p) (T) (S)

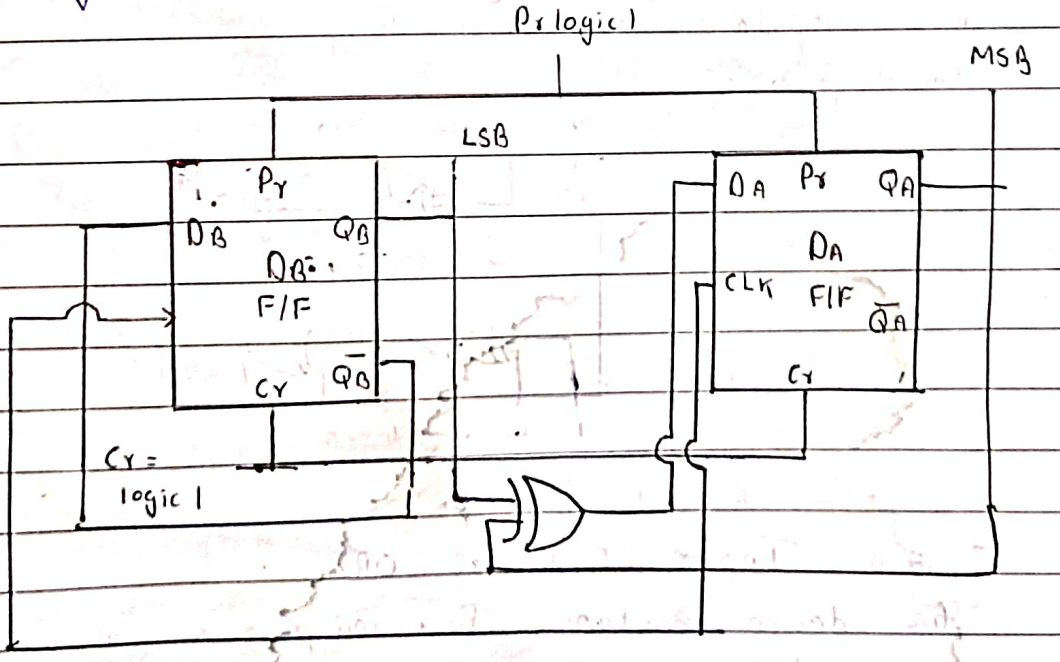
V_{cc} Preset D CLK Clear Q_B $\overline{Q_B}$



Preset D(i/p) CLK Clear Q_A $\overline{Q_A}$ GND

The dual edge triggered flip-flop utilizes circuitry to produce high speed D-type Flip-flops. Each Flip-flop has individual clear and set inputs, and also complementary Q and $\overline{Q}$.

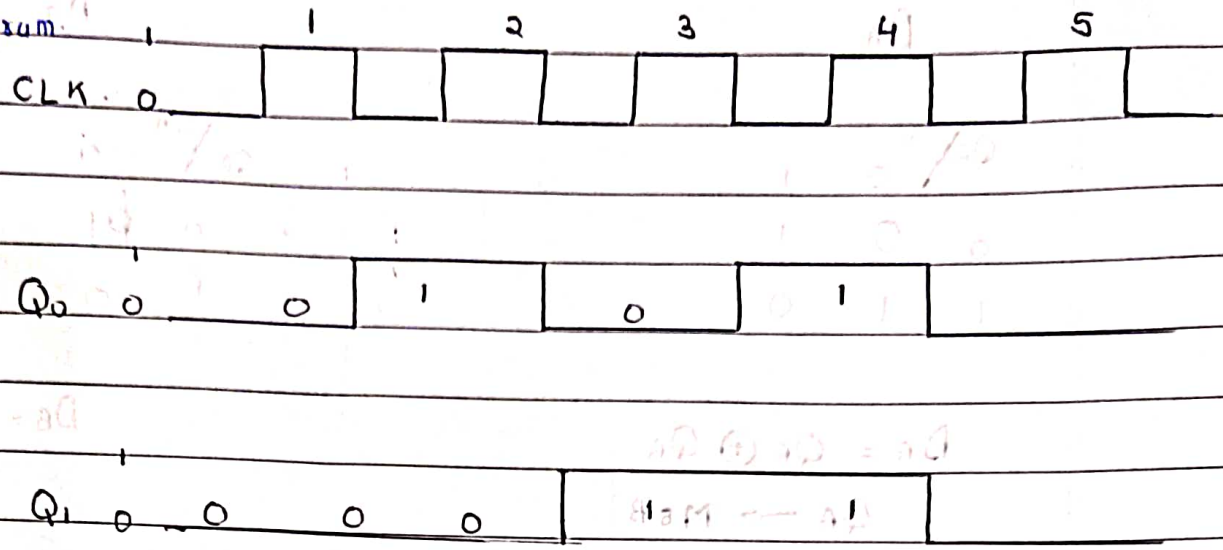
Circuit Diagram.



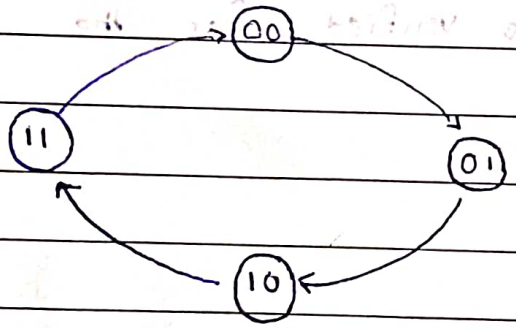
CK

CLK square wave, 1MZ, 5 volts peak to peak.

Timing Diagram



Exact State Diagram.



Execution table of D F/F

Q	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

State Transition Table.

clock	Present State		Next State		F/F control	
	Q_A	Q_B	Q_{A+1}	Q_{B+1}	D_A	D_B
0	0	0	0	1	0	1
1	0	1	1	0	1	0
2	1	0	1	1	1	1
3	1	1	0	0	0	0

D_A

Q_B \ Q_A	0	1
0	0	1
1	1	0

D_B

Q_B \ Q_A	0	1
0	1	1
1	0	0

$D_A = Q_A \oplus Q_B$

$D_B = \overline{Q_B}$

$Q_A \longrightarrow$ MSB

$Q_B \longrightarrow$ LSB

* Output :- Synchronous counter using D Flip Flops
* Conclusion :- Synchronous counter using D Flip Flops has been implemented and truth tables are verified for the same.

7/11/23

Synchronous counter using D flip flop