Ayush Vinod Upadhyay
IO25 I1-1
60003220131

06/11/23

A 7/11/23

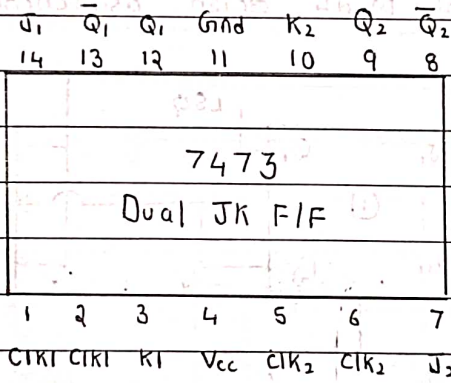
Experiment no 8

Aim:- To design and implement asynchronous counter using J-K flip-flop for MOD-4 [up] and MOD-4 [Down]

Apparatus:- Breadboard, connecting wires, LED, Board, 5 Volts power supply, function generator.

Theory:-

A counter is a device which stores the number of times a particular event or process has occured often in relationship to a clock signal. In asynchronous counter, we don't use universal clock, only first flop is drawn by main clock and the clock input of rest of the following flip-flop is ~~drawn~~ driven by output of previous flip-flops. It is also called as a rippled counter.



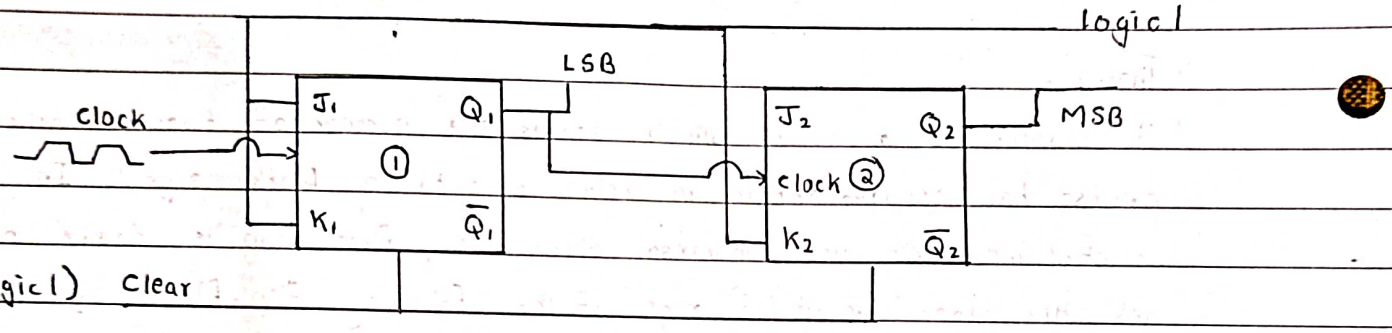
Pin diagram of IC7473

This device (Dual master J-K flip flop), contains 2 independently positive pulse triggered J-K flip flops with complementary output. The J and K data is processed by the flip flop after a complete clock pulse. While the clock is high the J and K inputs are disabled. A low logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

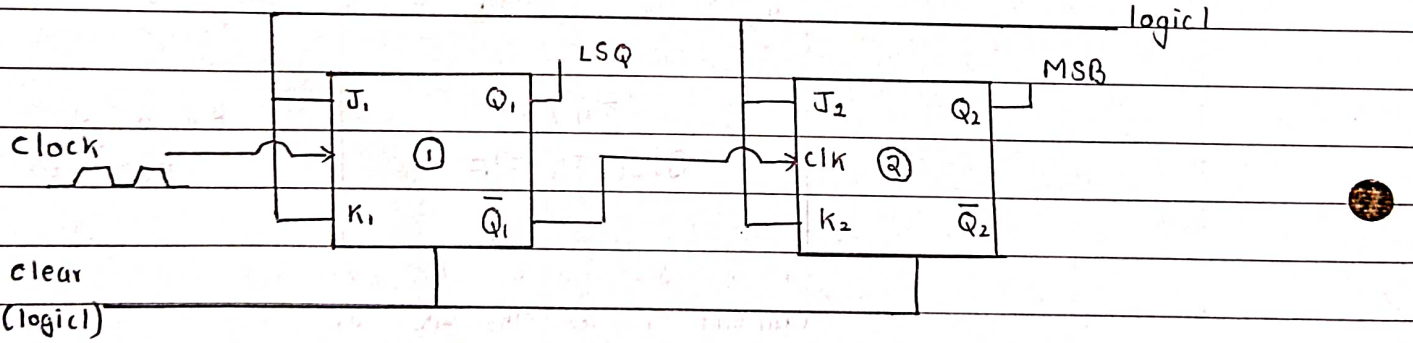
* Mod - 4 Asynchronous up and down counter.

In up counter, it starts counting from low to high, whereas in a down counter, it starts counting from high to low. There is no universal clock, we only use the first flip flop which is driven by the main clock

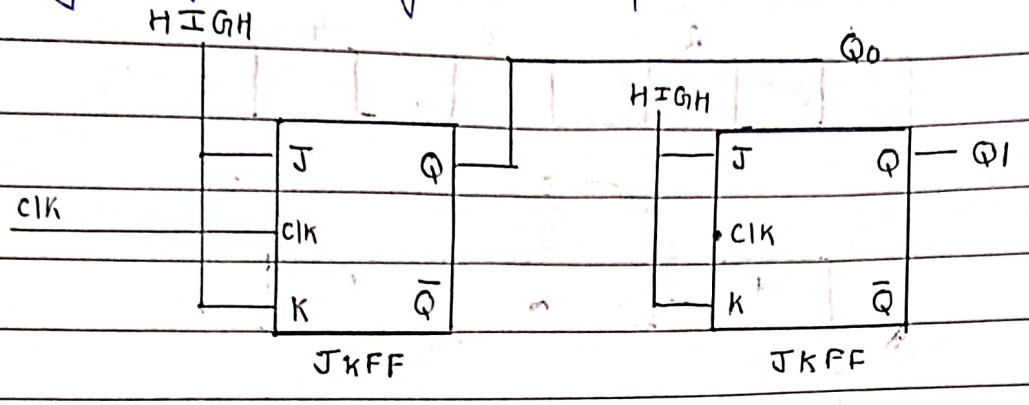
→ Circuit diagram of Mod 4 up asynchronous counter.

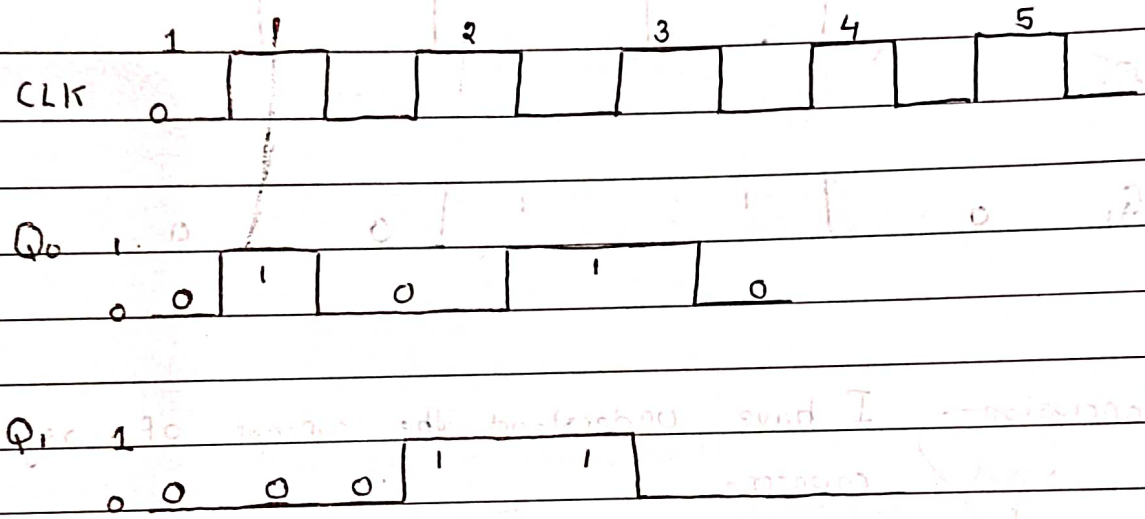


→ Circuit diagram of Mod 4 down asynchronous counter.

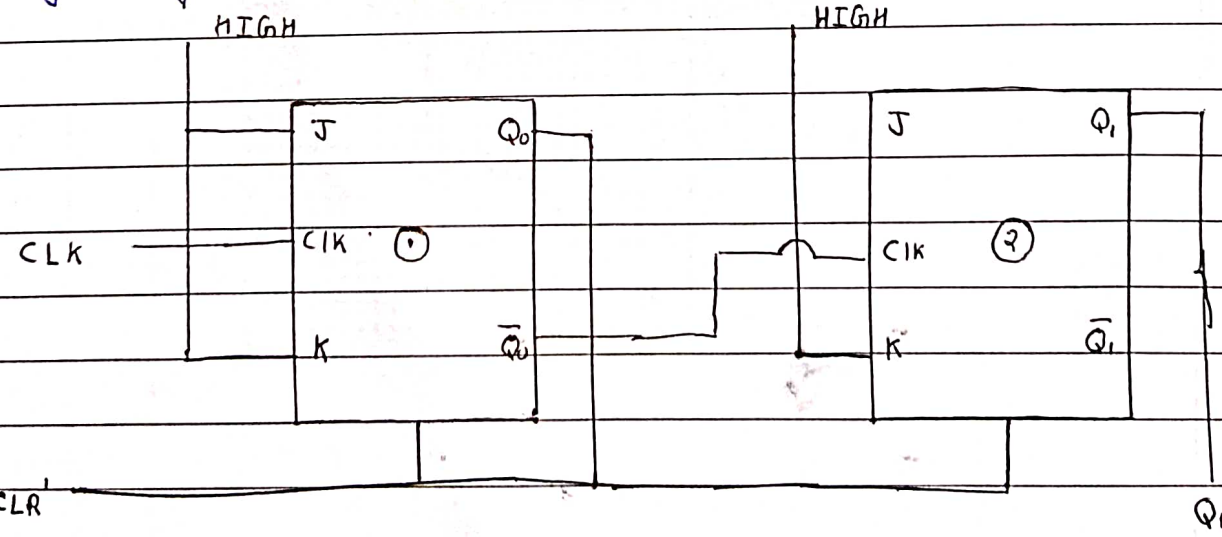


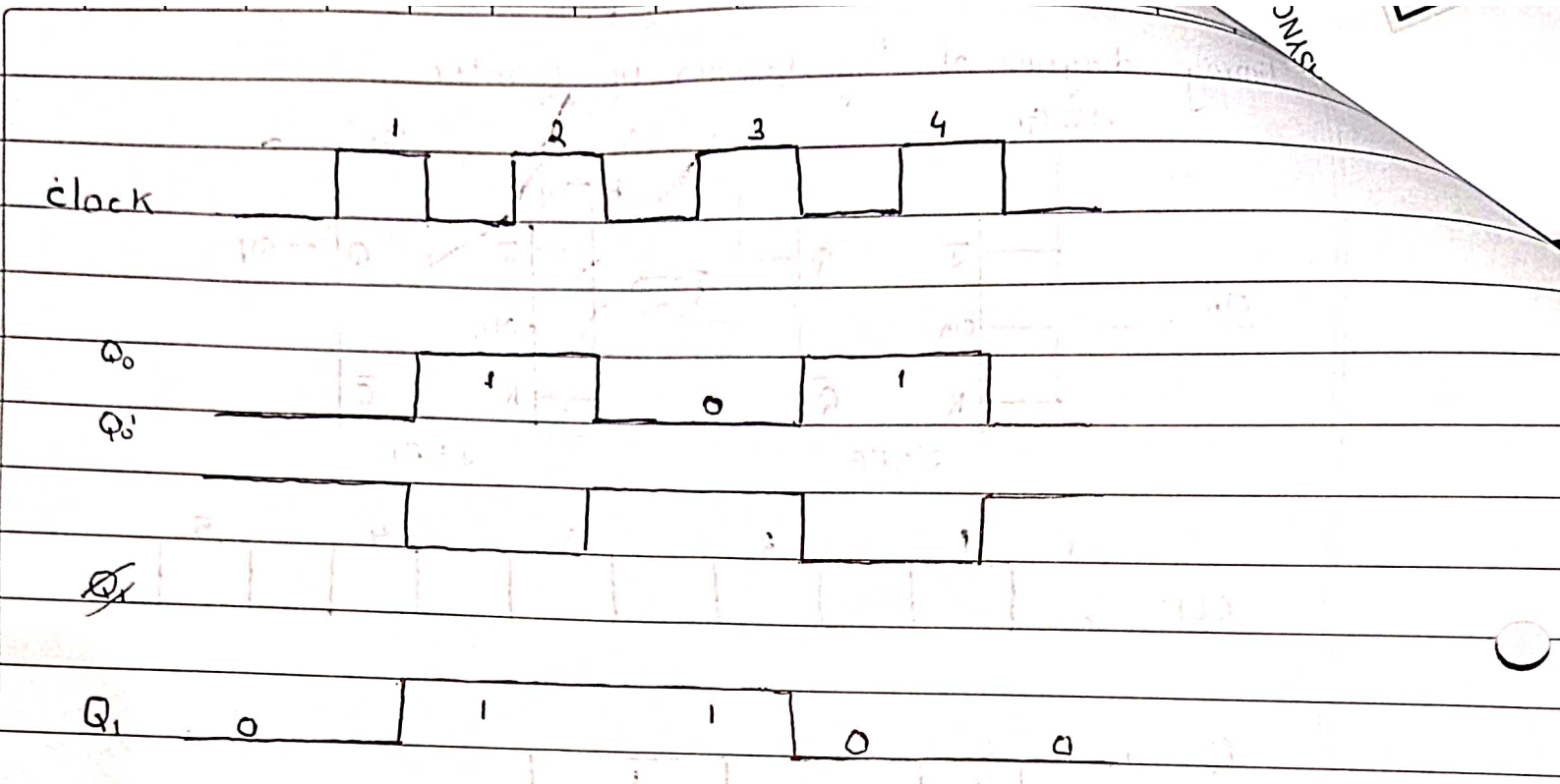
Timing diagram of Asynchronous up counter.





Timing diagram of Asynchronous down counter:-

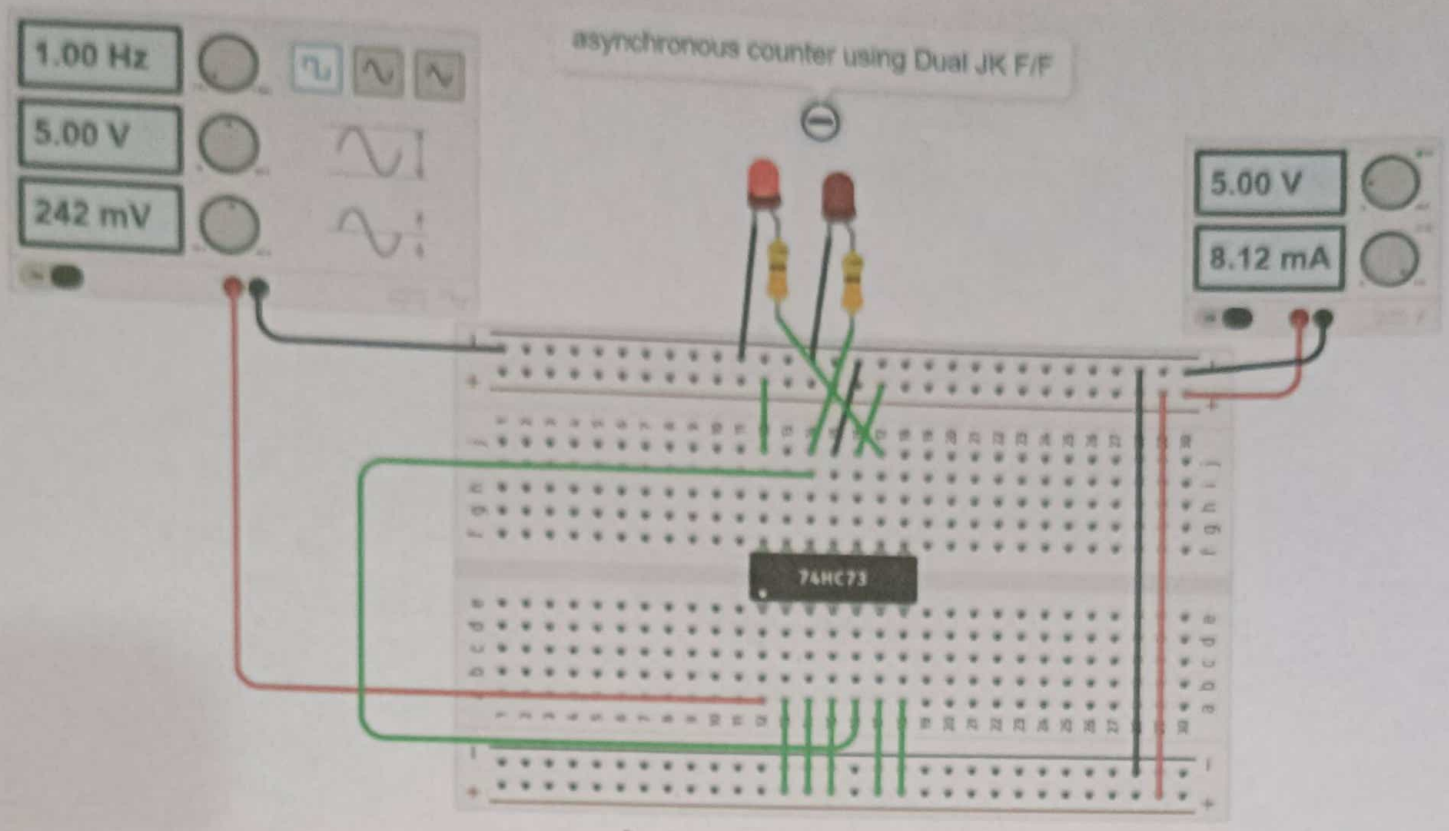




Conclusion:- I have understood the concept of asynchronous counter.

7/11/23

ASYNCHRONOUS COUNTER USING DUAL JK F/F



ASYNCHRONOUS INVERTED COUNTER USING DUAL JK F/F