Ayush Vinod Upadhyay
60003220131
I026 I1-1

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Exp-5 Adder-Subtractor

Aim:- To design and construct half adder, full adder, half subtractor and full subtractor circuits and verify the truthtable using logic gates.

Components:- IC 7408, IC7486, IC7404, IC7482, Bread Board

Apparatus :- Power Supply, O.P switch.

Half Adder.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

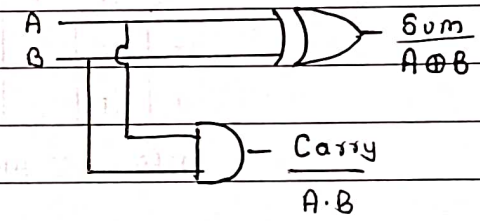
Kmap for Sum

A \ B	0	1
0	·	1
1	1	

Kmap for Carry

A \ B	0	1
0	0	0
1	0	1

Sum :- $\bar{A}B + A\bar{B}$



Full Adder.

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map for sum.

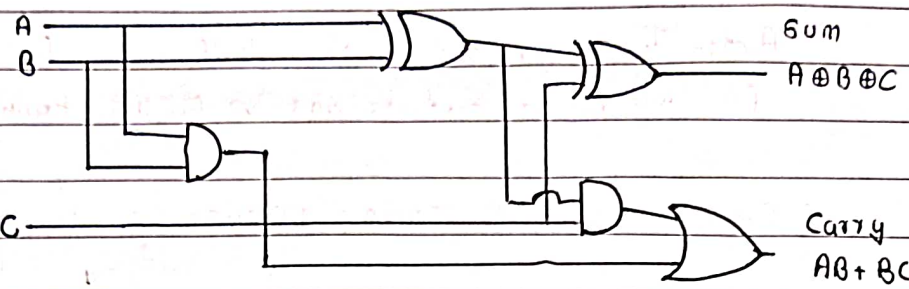
A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$Sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + AB\bar{C} + ABC = A \oplus B \oplus C$

K-map for carry

A \ BC				
			1	
		1	1	1

$Carry = AC + AB + BC$



Half Subtractor.

A	B	Borrow	Difference
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

K-map for difference.

A \ B	0	1
0		1
1	1	

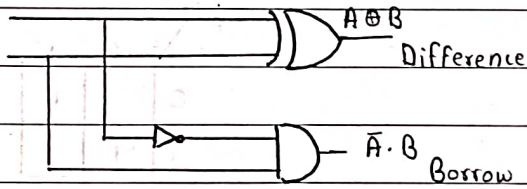
Difference = $\bar{A}B + B\bar{A}$

Kmap for borrow

A \ B	0	1
0		1
1		

Borrow = $\bar{A}B$

Logic.



Full Subtractor.

A	B	C	Borrow	Difference
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-map for difference.

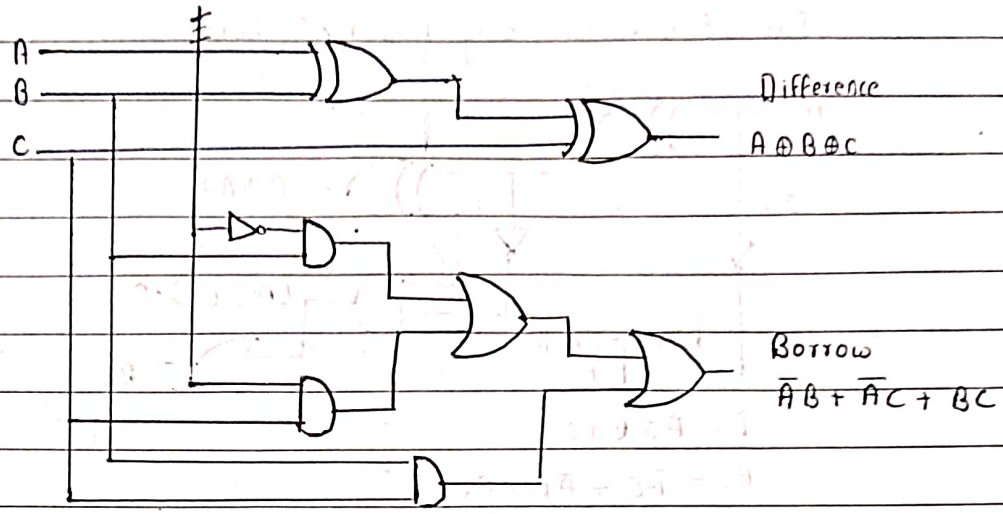
A \ BC	00	01	11	10
0		1		1
1	1		1	

Difference = $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC = A \oplus B \oplus C$

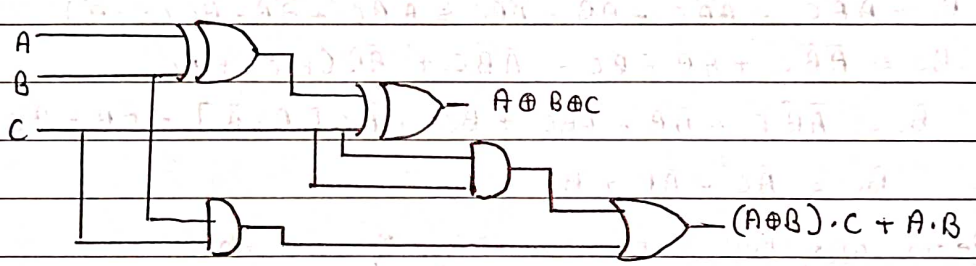
K-map for borrow.

A \ BC	00	01	11	10
0		1	1	1
1			1	

Borrow = $\bar{A}BC + B\bar{C} + \bar{A}C = \bar{A}(B+C) + BC$



Full Adder using two half adder.



To Prove:-

$S = A \oplus B \oplus C$

$C_o = AB + BC + CA$

$= (A \oplus B)C + A \cdot B$

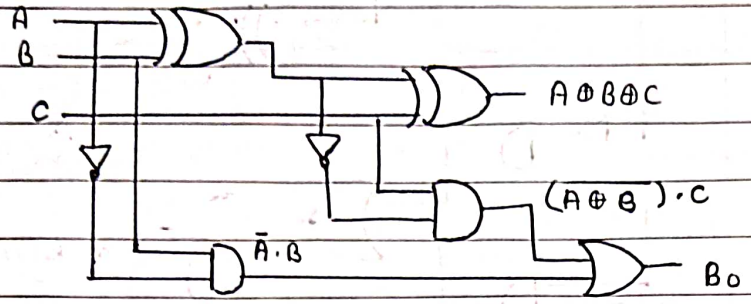
$= (\bar{A}B + B\bar{A})C + A \cdot B$

$= \bar{A}BC + B\bar{A}C + AB$

$= \bar{A}BC + A[\bar{B}C + B] = \bar{A}BC + A[B + C] =$

$= \bar{A}BC + AB + AC = B[\bar{A}C + A] + AC = B[A + C] + AC.$

Full Subtractor using two half subtractors.



$D = A \oplus B \oplus C$

$B_o = \bar{A}C + \bar{A}B + BC$

$B_o = (\overline{A \oplus B}) \cdot C + \bar{A}B = (\bar{A}\bar{B} + AB) \cdot C + \bar{A}B$

$B_o = \bar{A}\bar{B}C + ABC + \bar{A}B = \bar{A}\bar{B}C + ABC + \bar{A}B(1+C)$

$B_o = \bar{A}\bar{B}C + ABC + \bar{A}B + \bar{A}BC = \bar{A}\bar{B}C + \bar{A}B + BC(A+\bar{A})$

$B_o = \bar{A}\bar{B}C + \bar{A}B + BC = \bar{A}\bar{B}C + \bar{A}B(1+C) + BC$

$B_o = \bar{A}\bar{B}C + \bar{A}B + ABC + BC + \bar{A}C[B+\bar{B}] + \bar{A}B + BC$

$B_o = \bar{A}C + \bar{A}B + BC$

Full Adder and Full Subtractor using mode control

M	A	B	C	S/D	Carry B_o
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	0	0
1	1	1	0	0	0

BC \ NA	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	0	1	1	0
10	1	0	0	1

$S/Q = A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C + AB\bar{C}$

$= A(\overline{B \oplus C}) + \bar{A}(B \oplus C)$

$= A \oplus B \oplus C$

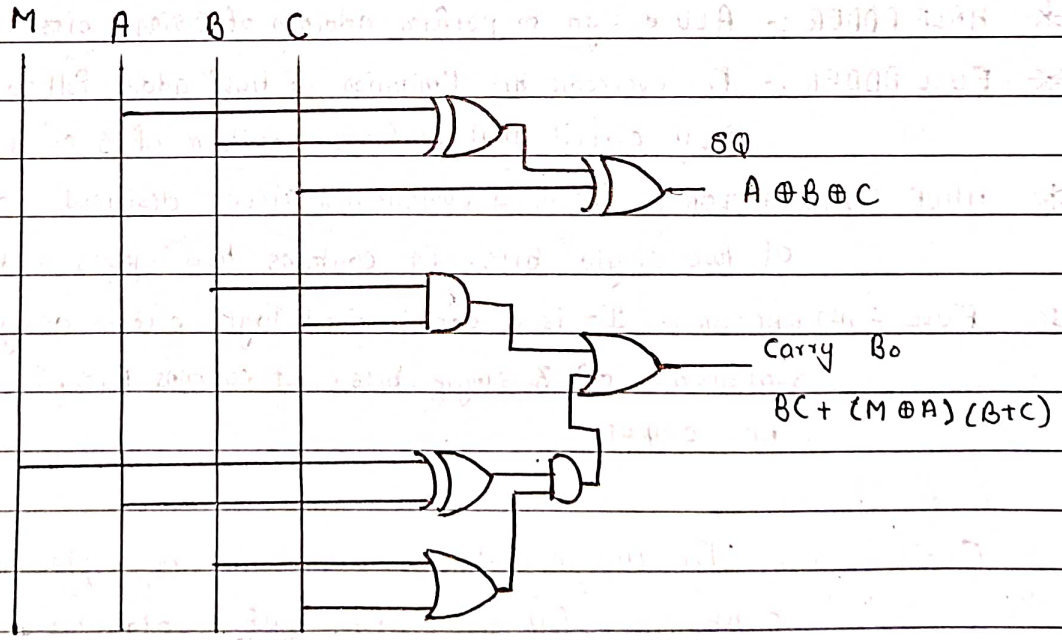
Carry / B_o.

Bc \ MA				
	0	0	0	0
	0	1	0	1
	1	1	1	1
	0	1	0	1

Carry / $B_o = BC + \bar{M}AC + \bar{M}AB + M\bar{A}C + M\bar{A}B$

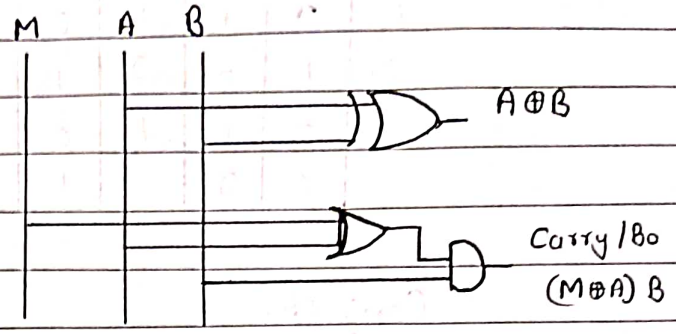
$= BC + C(M \oplus A) + B(M \oplus A)$

$= BC + (M \oplus A)(B + C)$



Half Adder and Half Subtractor.

M	A	B	S/D	Carry/Bo
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	0



B \ MA	00	01	11	10
0	0	1	1	0
1	1	0	0	1

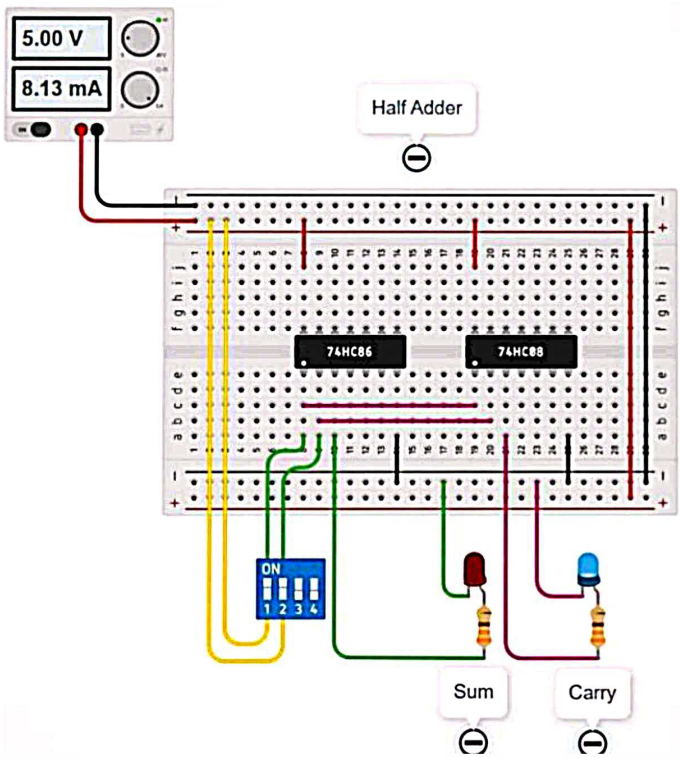
$S/D = A\bar{B} + \bar{A}B = A \oplus B$

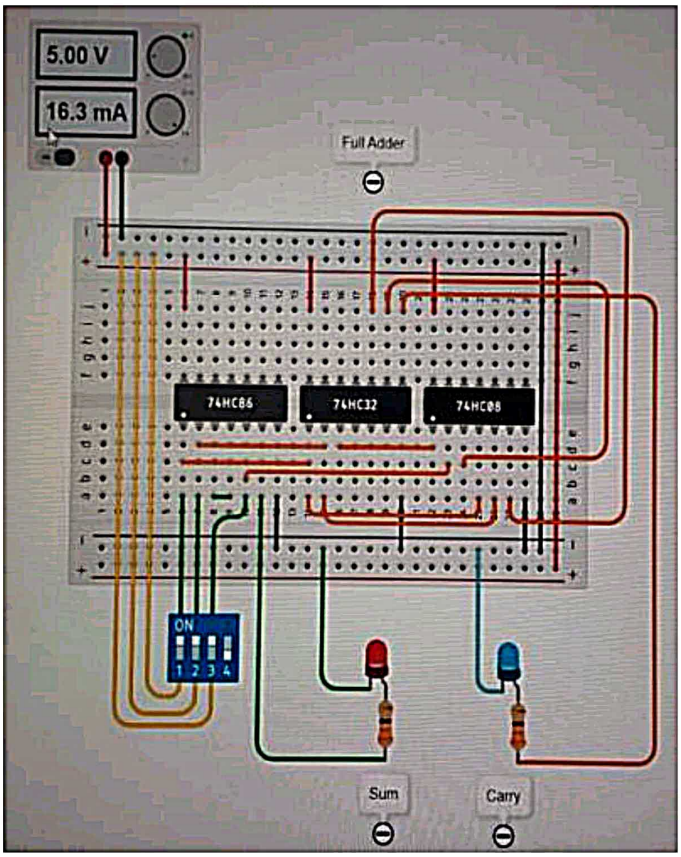
$Carry/B_o = \bar{M}\bar{A}B + M\bar{A}\bar{B} = B(M \oplus A)$

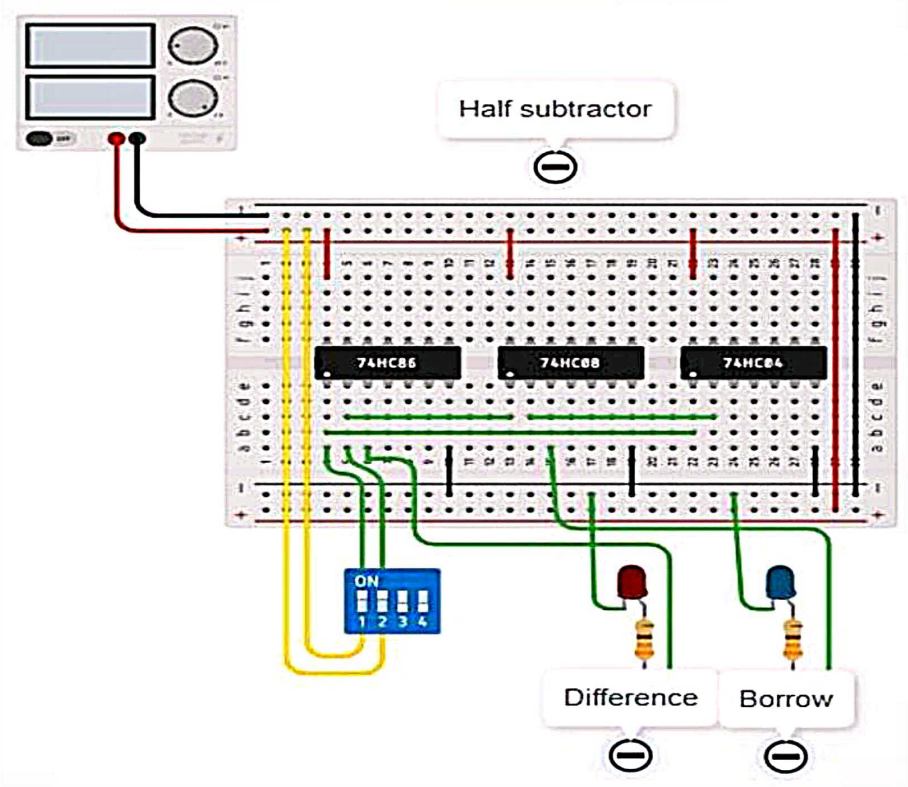
B \ MA				
0	0	0	0	0
1	0	1	0	1

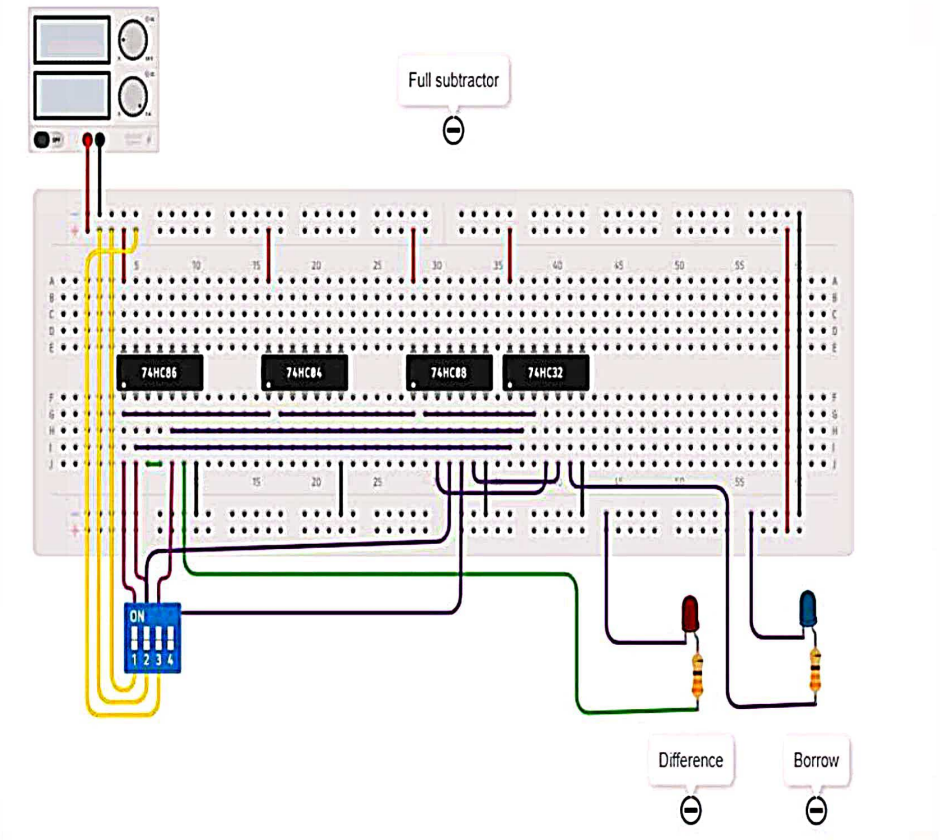
* **HALF ADDER :-** ALU design to perform addition of 2 single bits. 2 iputs - 2 outputs.
* **FULL ADDER :-** For overcome the limitation of half adder, full adder is used. It is a ALU circuit that performs addition of 3 single bits.
* **HALF SUBTRACTOR :-** It is a combination circuit designed to perform subtraction of two single bits. It contains two inputs and produces two output
* **FULL SUBTRACTOR :-** It is a combinational logic circuit designed to perform subtraction of 3 single bits. It contains A, B, 3 inputs and produces two outputs.

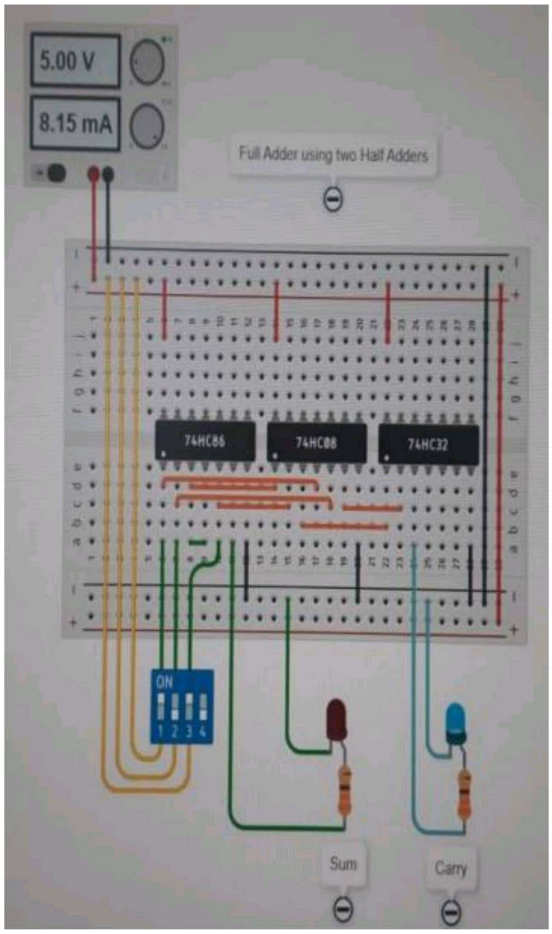
Conclusion :- In this experiment we learnt to implement half adder, half subtractor, full subtractor, half subtractor, and full adder and full subtractor using 2 half adder and subtractor.

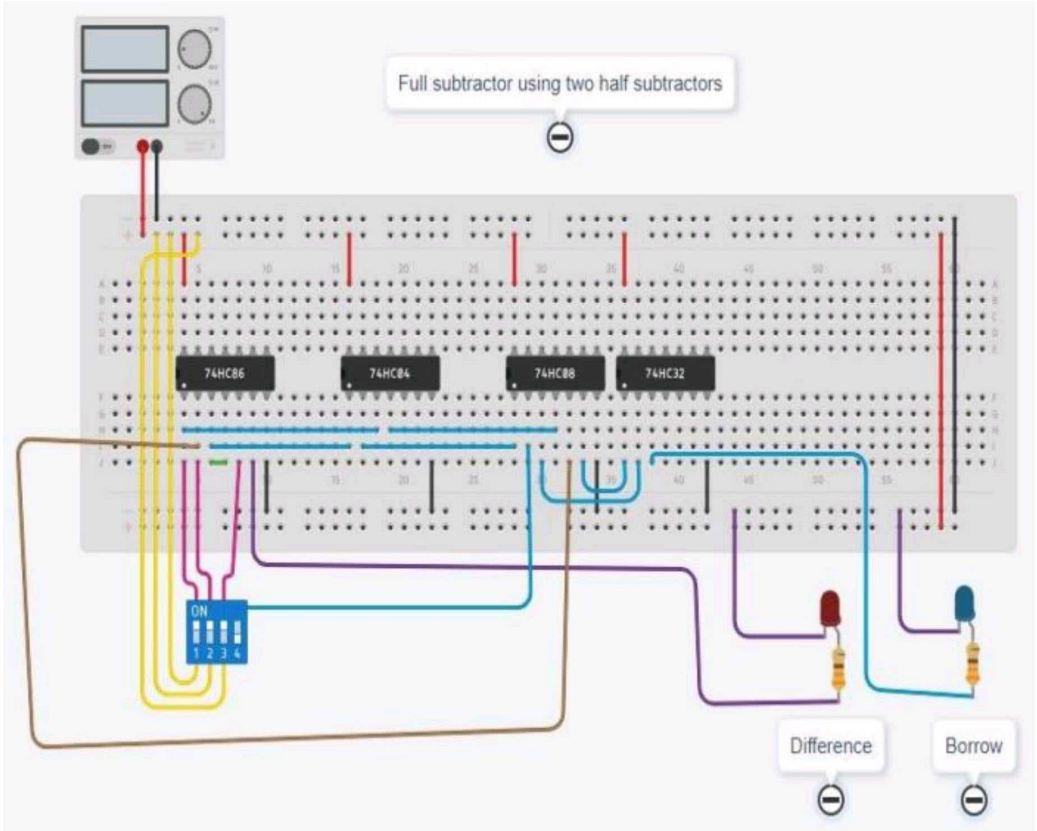

5.00 V
8.13 mA
Half Adder
74HC86
74HC08
ON
1 2 3 4
Sum
Carry

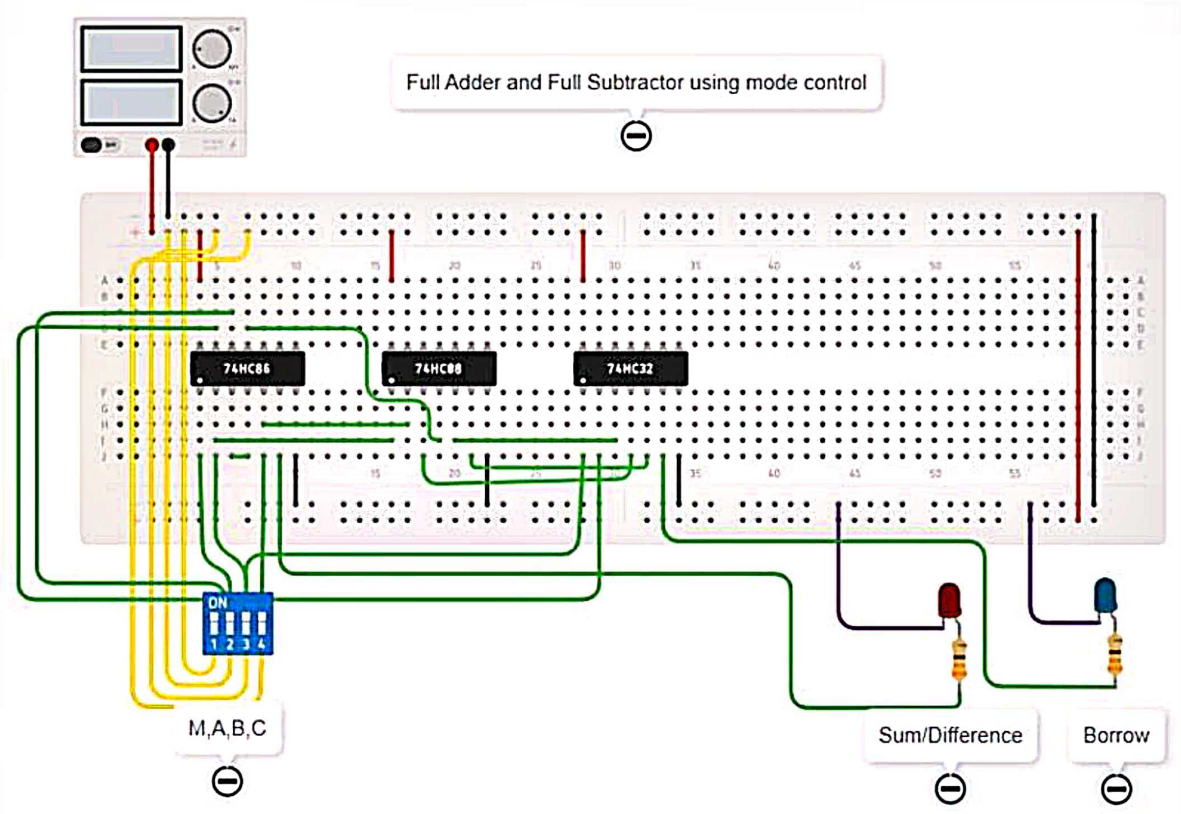

5.00 V
16.3 mA
Full Adder
74HC86
74HC32
74HC08
ON
1 2 3 4
Sum
Carry


Half subtractor
74HC86
74HC08
74HC04
ON
1 2 3 4
Difference
Borrow


Full subtractor
74HC86
74HC04
74HC08
74HC32
ON
1 2 3 4
Difference
Borrow


5.00 V
8.15 mA
Full Adder using two Half Adders
74HC86
74HC08
74HC32
ON
1 2 3 4
Sum
Carry


Full subtractor using two half subtractors
74HC86
74HC04
74HC08
74HC32
ON
1 2 3 4
Difference
Borrow


Full Adder and Full Subtractor using mode control
74HC86
74HC08
74HC32
ON
1 2 3 4
M,A,B,C
Sum/Difference
Borrow