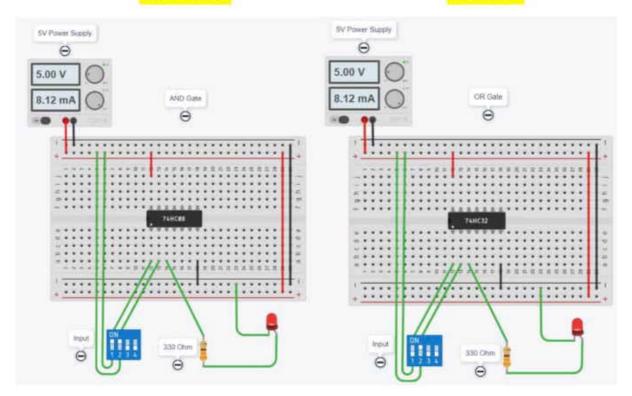
	Name: Ayush Vinod Upadhyay Roll no: IO25 Div: I1-1 SapID: 60003220131 Expe	rimen	t - 1 :	, Baş	ic Gates				
Aim	To study all different types of basic gates								
Apparat	os Tinker Cad	n'							
5100100 11									
Components	330 N resistor, led, 5V po								
ASIL VARIA	IC7408, IC7432, IC740	, I	C7400), I(7402, TC7486				
Infinis					H/H F P				
Description	AND Gate [IC7408]								
		A	В	Y	* Outputs a high signal				
21 20 30	A - Y A	0	0	0	only when both ipput				
1	3	0	1	0	signals are high, Otherwis				
	A 4 4 5 1 4 4 1		0	0	outputs low signal (0)				
	V = A.B		1	1	por side signar (e)				
	- decide di				A+A=v				
7	2) OR Gate: [IC7432]								
	(anx) and (anx)								
		A	B	У	* Outputs high signal if				
0	A-A-Y	0	0	0	atleast one input signal				
1	8-11	0		1	is high, otherwise, it				
		1	0		outputs low signal (0)				
20070175	y = A + B	1	1		out for a see signed				
					8 a A = 8				
	3) NOT Gate: LIC7404]								
The state of the s	Day Sarah Sure Peru		1~		At Trucks the input cional				
	A — V	A			* Inverts the input signal				
	B > 7	1	0		ive high to low and				
	$y = \overline{A}$								
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9 0 7W									
	4) NAND Gate: [IC7400		10000	11.6	He yould of mid				
		A	В	Y	* NAND gate is the opposite				
	A	0	0	1	of AND gate. It outputs				
	B Tool days	0	17	101	low signal when both				
	Conco It These TETHER	T No	0	1	input are high, otherwise,				
	y = A.B	1	1	0	outputs high signal.				
			[804	TCT	Description of AND (material)				
	5) NOR Gate: [IC7402]								
densit no	o stuate 0 * Y 8	A							
Team of	H had a con o	A	В	Y	* The opposite of OR gate				
SOLUMNIE NO	A January 1	0	0	1	It outputs low signal				
(e) Innpia	B 2000	0	1	0	if atleast one input				
			0	0	signal is high, otherwise				
	y = A+B	1	1	0	its outputs high signal.				
			[FEP	TICT	100 20 /				
	6) Exclusive - OR (XOR): [IC7486]								
Fi Toppie	in atomico x v A	4							
lating to	o O atleast one in	A	3	Y	* Outputs high signal				
Ti Seria	A - A	0	0	0	when only one of the				
(0)	8—//	0	1						
				1	inputs is high, otherwis				
	Y = A D B		0		outputs low signal.				
		,							
C . 1	Implementation of all the basic gates have been success fully								
Conclusion		Dasic	gare	S no	ave been success fully				
Sopre Tun	undershood.								
500 mg	Cad World Ser	0							
	0 VICE - VCES								
		-			H - H - H - H - H - H - H - H - H - H -				
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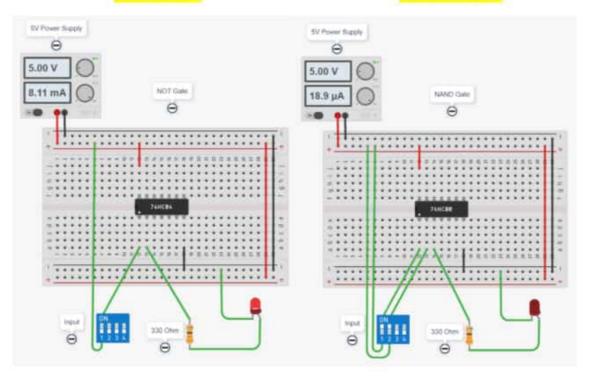
AND GATE

OR GATE



NOT GATE

NAND GATE



NOR GATE

XOR DATE

