Team Members:

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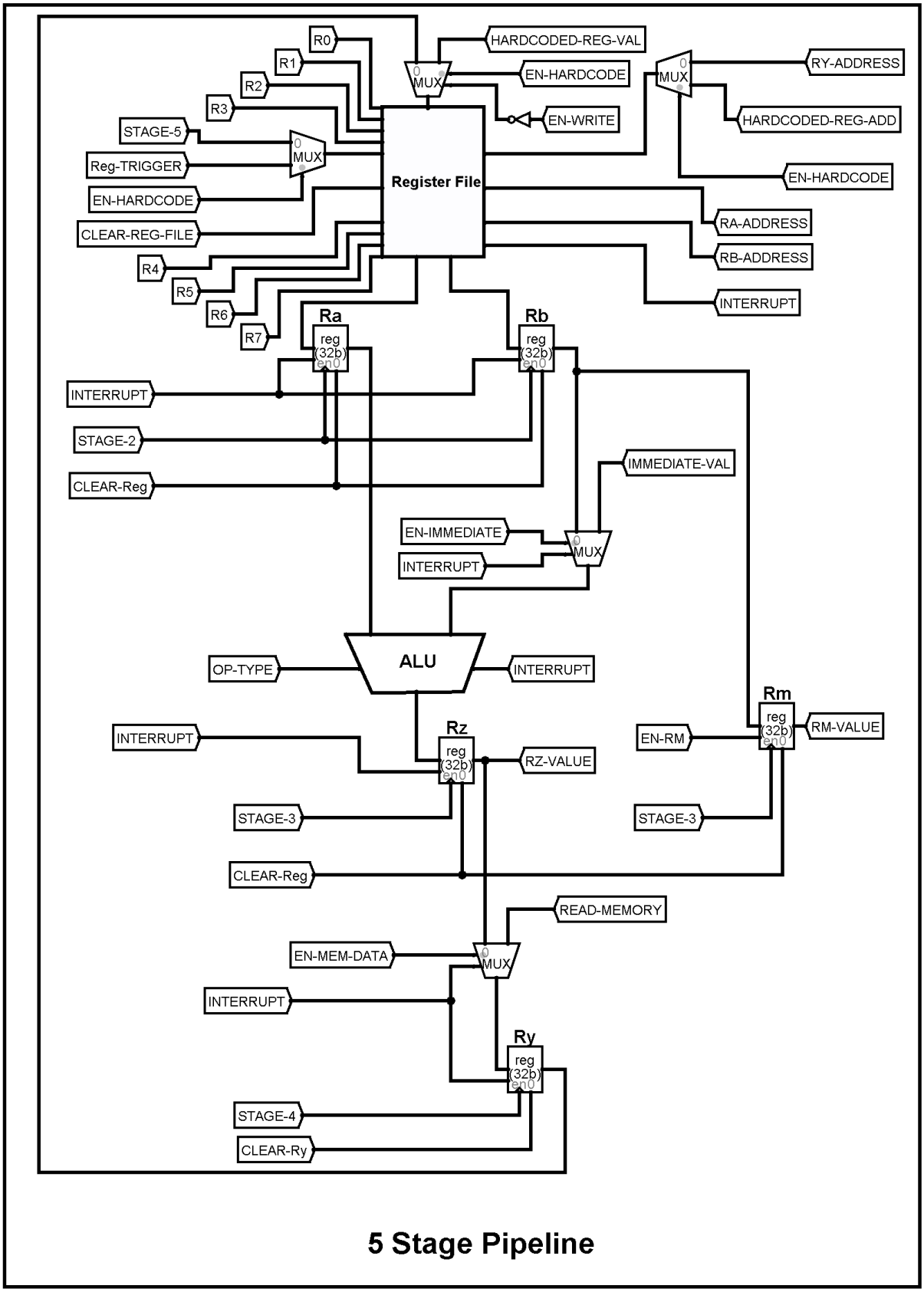
Overall Architecture:

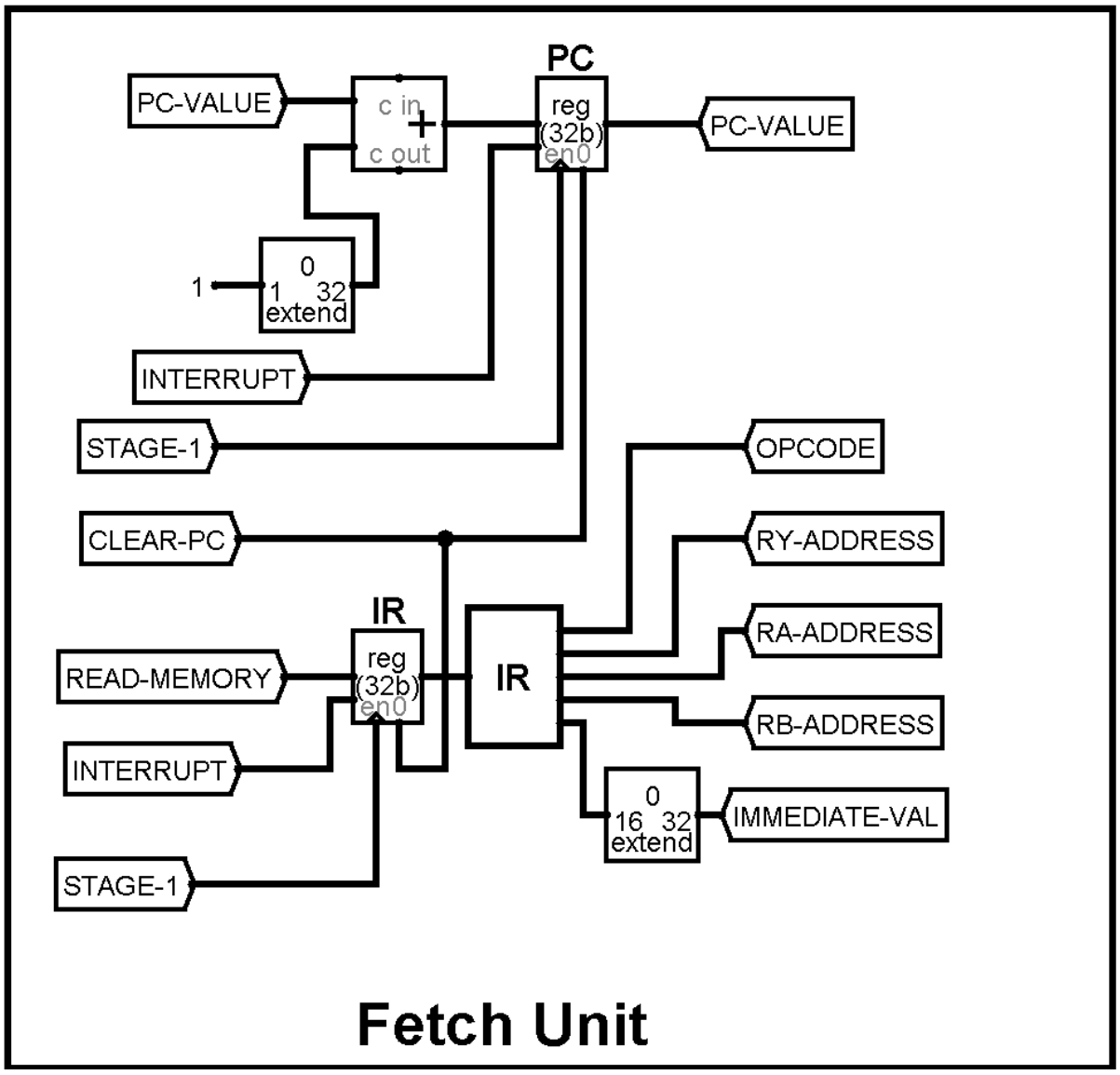
Components	Description
General Purpose Registers (GPRs)	8: R0 – R7
Special Purpose Registers (SPRs)	7: PC, IR, RA, RB, RZ, RM, RY
Memory	RAM: 8 – bit Address Line and 32 – bit Data
Instruction Supported	13

Components:

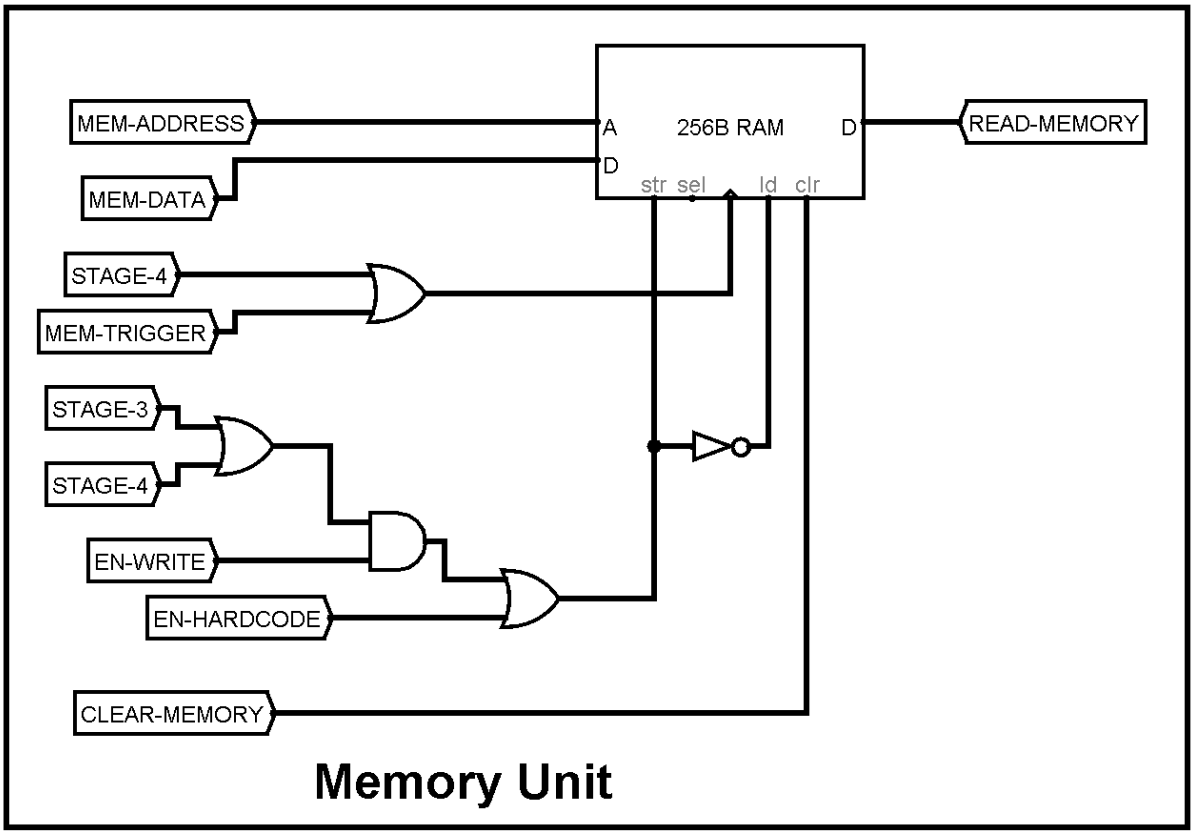
1) Processor Pipeline – 5 stage pipeline



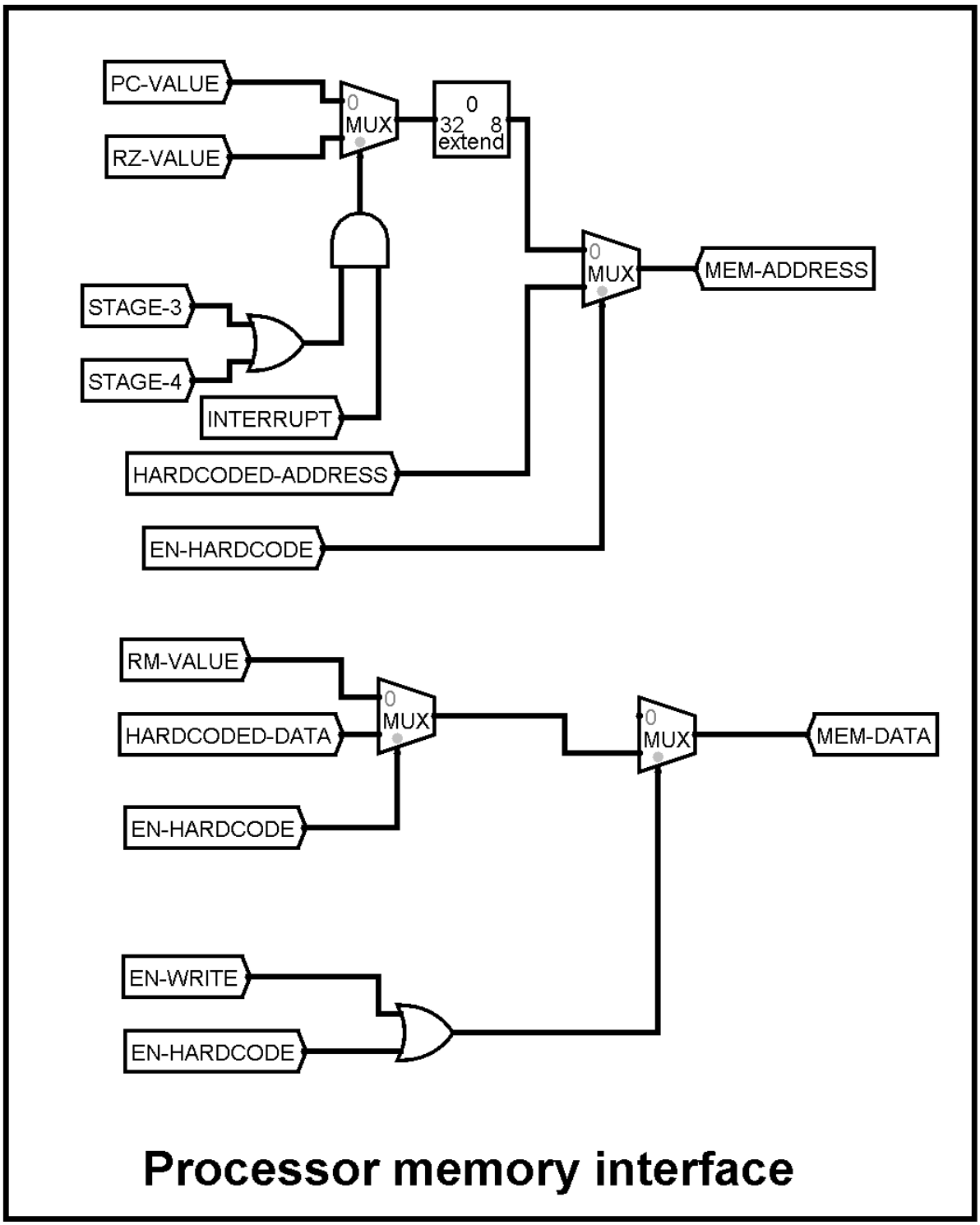
2) Fetch Unit


PC
PC-VALUE
c in
+
c out
reg
(32b)
en0
PC-VALUE
1
0
1 32
extend
INTERRUPT
STAGE-1
OPCODE
CLEAR-PC
RY-ADDRESS
IR
RA-ADDRESS
READ-MEMORY
reg
(32b)
en0
IR
RB-ADDRESS
INTERRUPT
0
16 32
extend
IMMEDIATE-VAL
STAGE-1
Fetch Unit

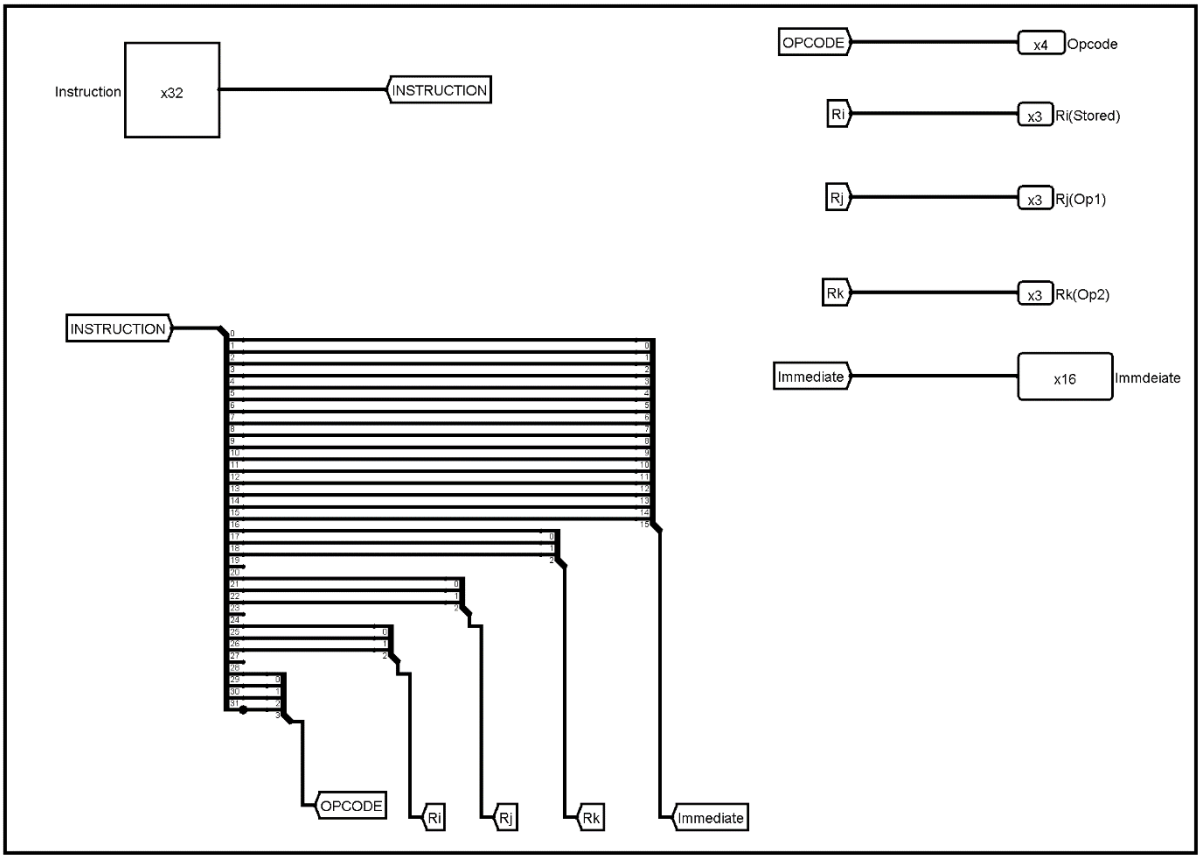
3) Memory Unit



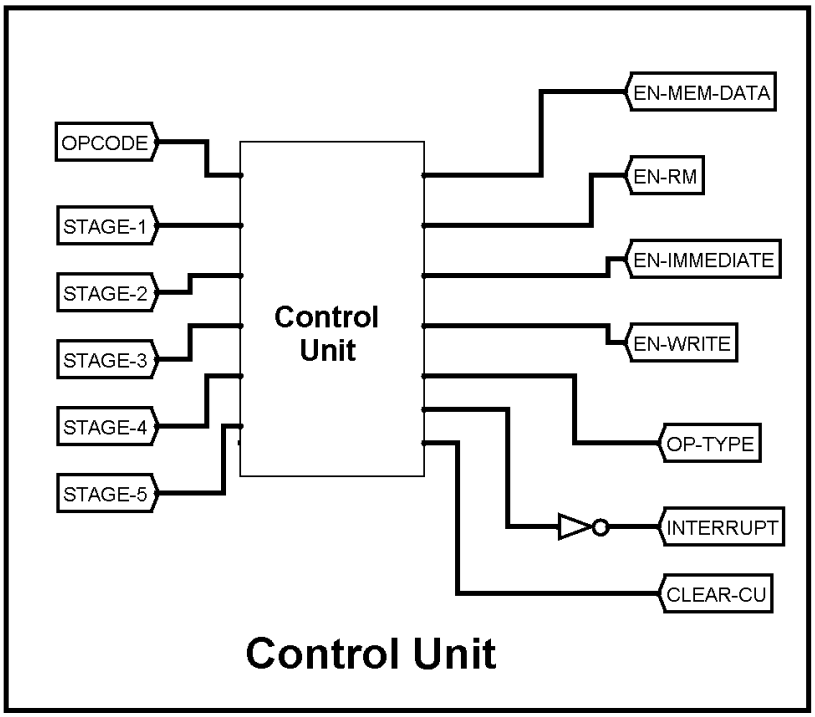
4) Processor Memory Interface

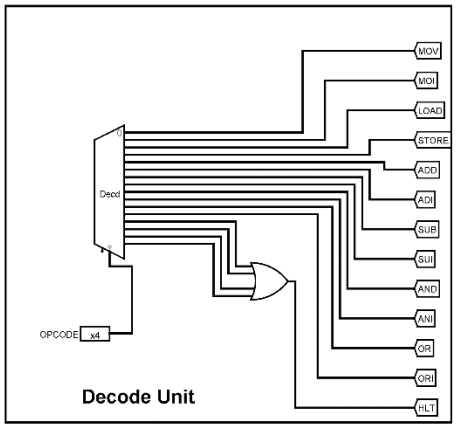


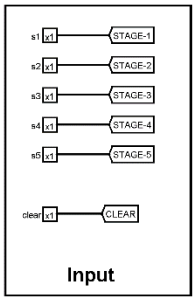
5) Instruction Register – internal circuit

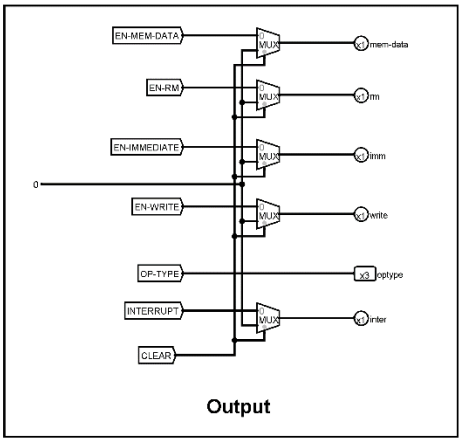


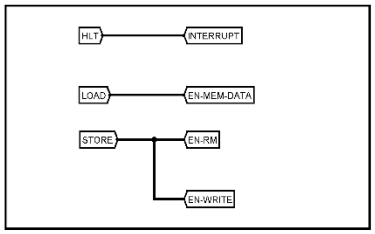
6) Control Unit

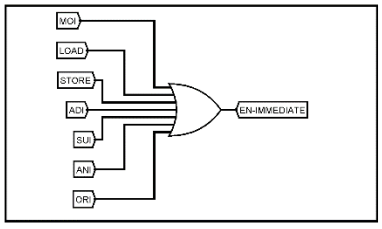


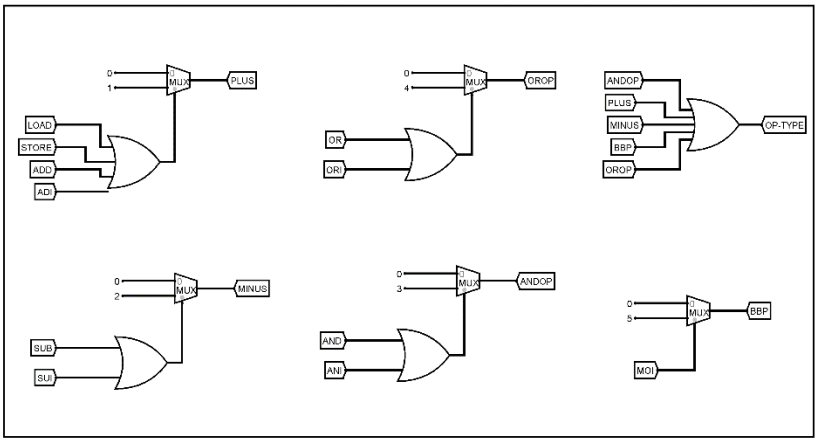




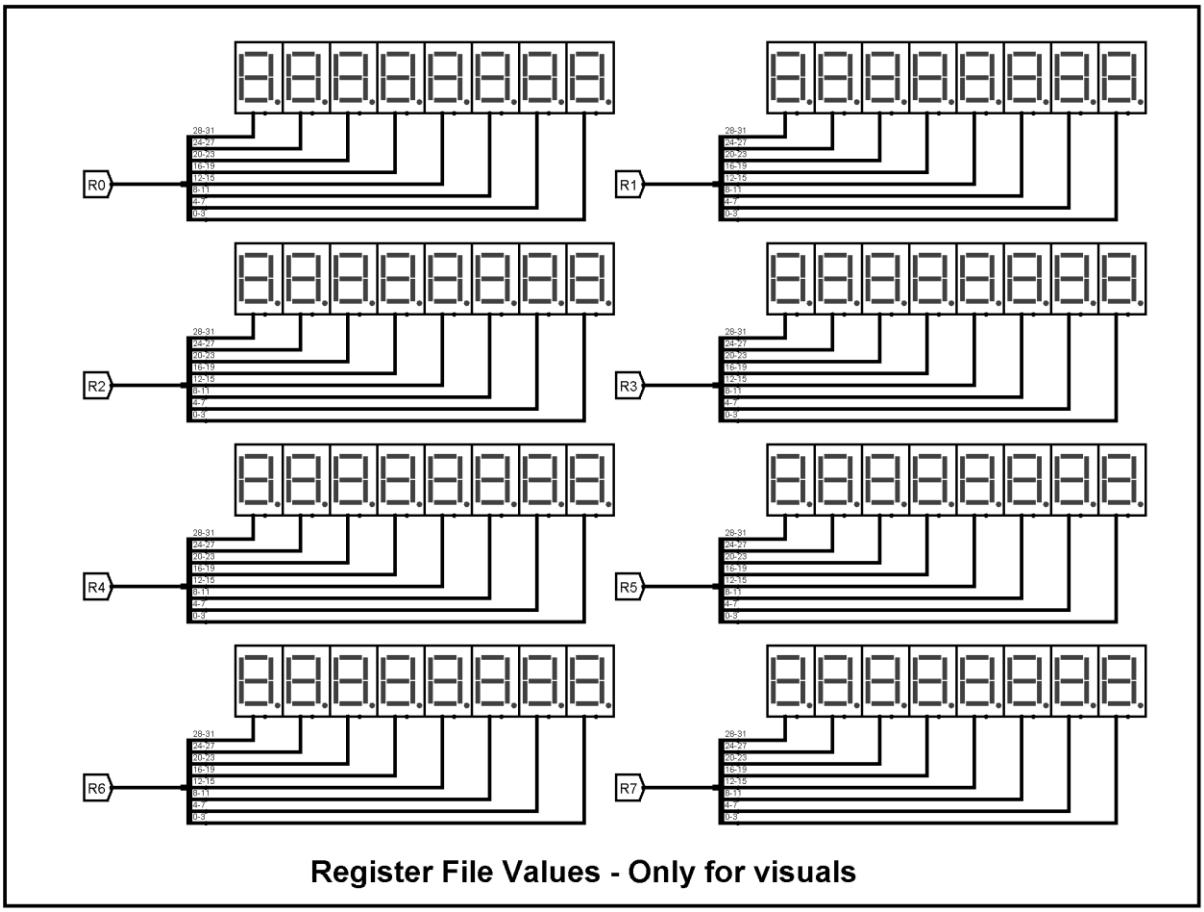


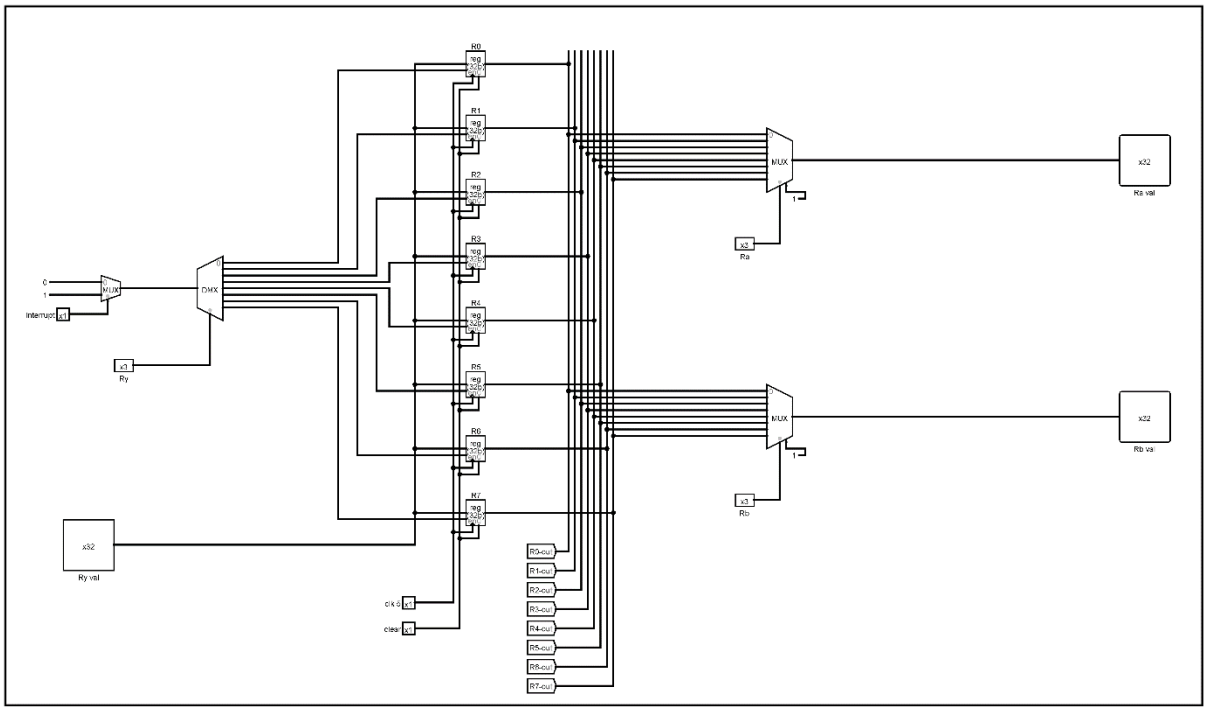




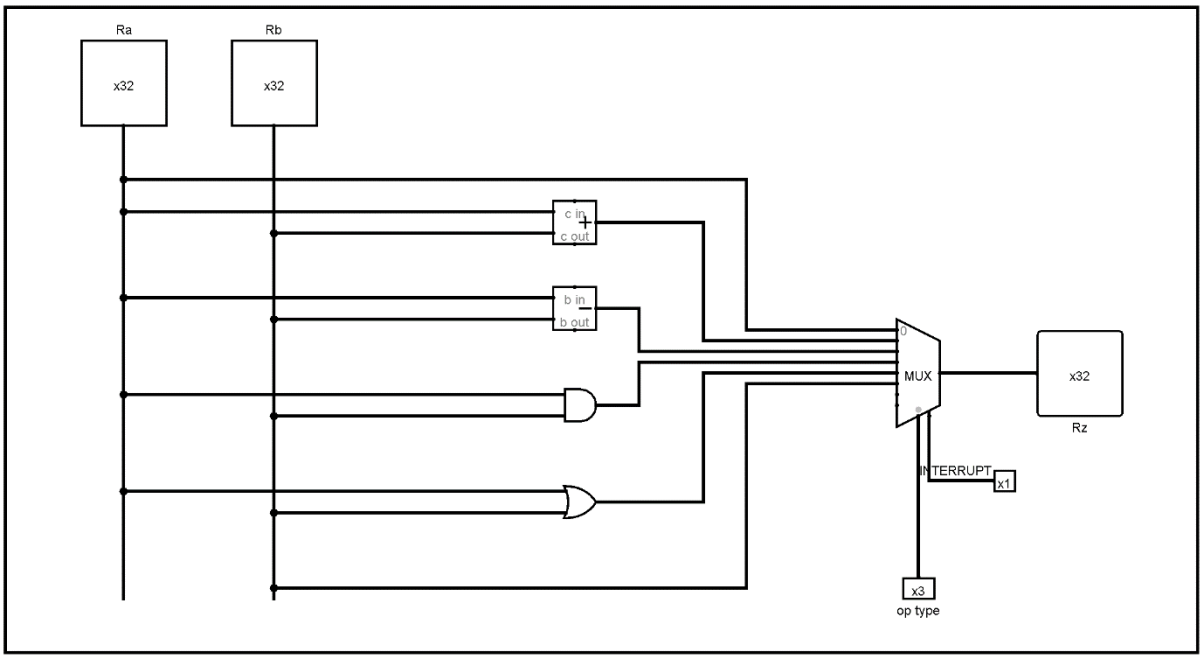


7) Register File





8) ALU – Internal circuit



9) Stage Counter