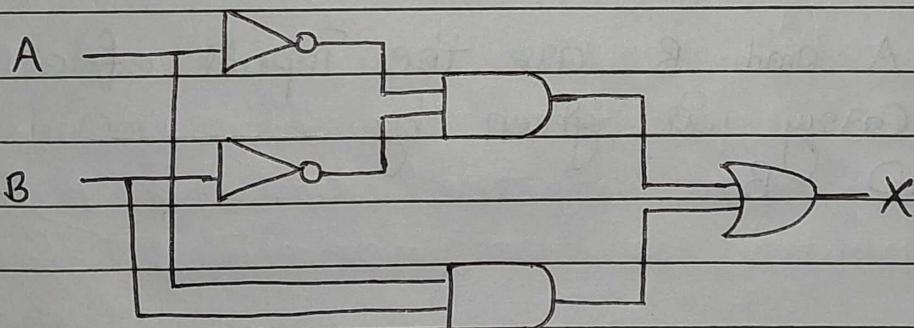


ASSIGNMENT-2

MON	TUE	WED	THR	FRI	SAT	SUN
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A.

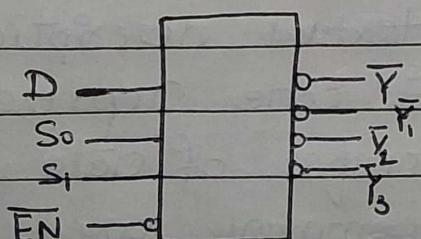
1. There are _____ cells in a 4-variable K-map.
16
2. Each product term of a group, $\bar{w} \cdot x \cdot \bar{y}$ and $w \cdot y$, represents the _____ in that group.
Sum-of-minterms
3. The prime implicant which has at least one element that is not present in any other implicant is known as _____
Essential Prime Implicant
4. Which of the following logic expressions represents the logic diagram shown?



$$X =$$

$$\overline{AB} + AB$$

5. The device shown here is most likely a



Multiplexer

6. 3 bits full adder contains _____
8 Combinational Inputs
7. Which combinational circuit is renowned for selecting a single input from multiple inputs and directing the binary information to output line?
Data Selector (Multiplexes)
8. One multiplexer can take the place of Several SSI Logic Gates (SSI: Small Scale Integration)
9. Total number of inputs in a half adder is _____
9
10. If A and B are the inputs of a half adder, the carry is given by _____
A AND B

[B.]

1. What is Register Transfer Language (RTL)?
RTL is a high-level description language used to specify digital circuits at the register transfer level. RTL is a textual description of a circuit, where each line of code represents a single operation or a transfer of data between registers. RTL is commonly used in digital circuit design and is often used to describe the behavior of hardware modules in hardware.

description languages such as Verilog and VHDL. In RTL, a circuit is typically described in terms of registers and combinational logic blocks, which operate on data stored in registers. RTL also includes statements for specifying the timing of operations and data transfers, such as clock signals and data strobes.

2. Write truth table of Half-adder.

Half adder is a combinational circuit that adds two 1-bit inputs (A and B).

Produces two 1-bit outputs (Sum and Carry)

Sum \rightarrow XOR Operation

Carry \rightarrow AND Operation

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3. What is essential prime implicants.

Prime implicants are the prime implicants of a boolean function, which are the Boolean product terms (AND terms) that are not subsumed by any other product terms.

Essential prime implicants are a subset of prime implicants that are necessary to cover all of the minterms (or maxterms) of the Boolean function.

4. What are maxterm and minterm?

A minterm is a product term in which all of the variables appear exactly once in either true or complemented form. A minterm is also known as a standard conjunction or an element of the product of sums.

Example, the boolean expression $\bar{A}B\bar{C}D$ can be represented as a minterm, since it is the product of the variables \bar{A}, B, \bar{C}, D .

A maxterm is a sum in which all of the variables appear exactly once in either true or complemented form. A maxterm is also known as a standard disjunction or an element of the sum of products.

Example, the boolean expression $A+B+C+\bar{D}$ can be represented as a maxterm, since it is the sum of the variables A, B, C, \bar{D} in complemented or uncomplemented form.

C.

- Difference between Multiplexers and Demultiplexers.
 Multiplexers and Demultiplexers are two important combinational logic circuits that are used to route digital data between multiple inputs and outputs. A multiplexer is a circuit that selects one of several inputs and directs it to a single output, while a demultiplexer takes a single input and routes it to one of several possible outputs.

The Differences between Multiplexers and Demultiplexers are :

* Multiplexer

1. A multiplexer selects one of several inputs and directs it to a single output line, based on the values of a set of control signals.

Demultiplexer

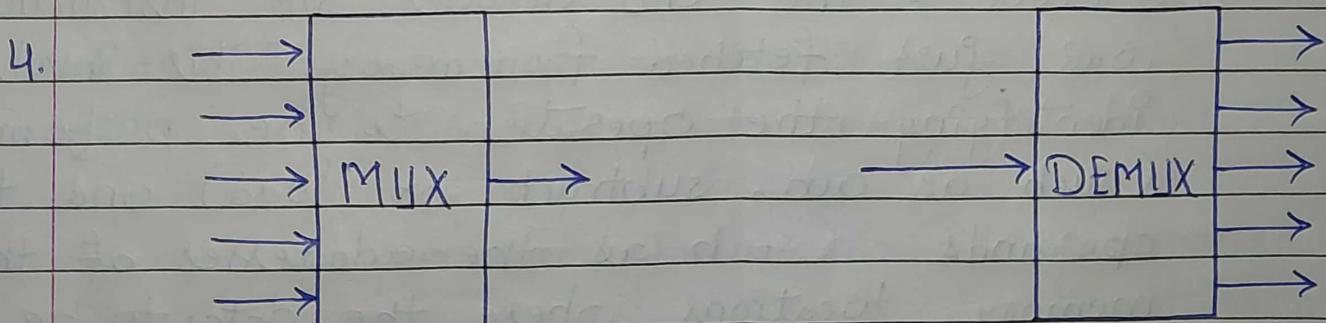
- Demultiplexers takes a single input and routes it to one of several possible output lines.

2. A multiplexer has multiple input lines and a single output line.

- A demultiplexer has a single input line and multiple output lines.

3. Control Signals are used by multiplexers to select which input line to route to the output line.

- Demultiplexers use control signals to select which output line to route the input signal to.



5. Multiplexer is commonly known as Data Selector.

- Demultiplexer is commonly known as a Data Distributor.

6. Works as Digital Switch.

- Works as Digital Circuits.

2. Explain fetch, decode and execute cycle.

The fetch-decode-execute cycle is the fundamental process by which a CPU executes instructions in a program, consisting of fetching the next instruction from memory, decoding it to determine the operation and operands, and executing the operating operation using the specified operands.

Brief :

Fetch-decode-execute cycle consists of three steps:

1. Fetch: The CPU retrieves the next instruction from memory (RAM) and stores it in a register called the Instruction Register (IR). The address of the instruction is stored in the program counter (PC), which is a special register that keeps track of the address of the next instruction to be executed.
2. Decode: The CPU decodes the instruction that was just fetched from memory. This involves identifying the operation to be performed (such as add, subtract, or load) and the operands (such as the addresses of the memory locations where the data to be processed is stored).
3. Execute: The CPU carries out the operation specified by the instruction, using the operands that were decoded in the previous step.

This may involve performing arithmetic or logical operations, reading or writing data to memory, or branching to a different part of the program based on a condition.

Once the execution of the instruction is complete, the program counter is updated to point to the address of the next instruction in the sequence, and the cycle repeats with the fetch step. The process continues until the end of the program is reached or the CPU is interrupted by an external event, such as an input/output operation or an interrupt request from a peripheral device.

[D]

1. Discuss full adder with truth table, K-map and logic diagram

- A full adder is a combinational logic circuit that adds three binary inputs (A, B and Carry-in) and produces a sum (S) and a carry out (C -out).

- Truth table of Full Adder:

A	B	C-in	S	C-out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Karnaugh map (K-map) for sum (S) output is:

C_{in}	AB	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
00	0	0	1	1	0
01	1	1	0	0	1
10					

The K-map for the carry-out (C_{out}) output is:

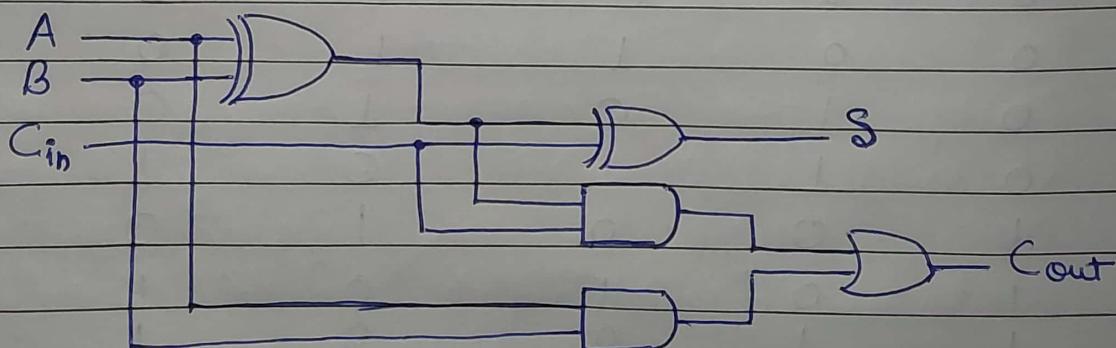
C_{in}	AB	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
00	0	0	1	1	0
01	0	0	0	1	0
10	1	0	1	1	1

→ From these k-maps, the minimum Sum-of-products (SOP) expressions for S and C_{out} are:

$$S = \bar{A}\bar{B}C_{in} + \bar{A}BC_{in} + A\bar{B}C_{in} + ABC_{in}$$

$$C_{out} = AB + AC_{in} + BC_{in}$$

→ Logic Diagram of Full Adder:



The circuit consists of two half adders (HAs) and one OR gate. The first HA adds A and B to produce a partial sum (P) and a partial carry (C_1). The second HA adds the partial sum P and the carry-in C_{in} to produce the final sum S and second partial carry (C_2). The OR gate combines the two partial carries (C_1 and C_2) to produce the final Carry-out (C_{out}).

Q2 Minimize the following boolean function -

$$1. F(A, B, C, D) = \sum m(0, 2, 8, 10, 14) + \sum d(5, 15)$$

Since the given boolean expression has 4 variables
so we draw 4×4 k-map.

		CD			
		$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
		00	01	11	10
$\bar{A}\bar{B}$	00	1	0		
$\bar{A}\bar{B}$	01		4	X	5
AB	11		12	X	13
AB	10	1	3	11	14

Now,

$$\begin{aligned}
 F(A, B, C, D) &= (AB + A\bar{B})(C\bar{D}) + (\bar{A}\bar{B} + A\bar{B})(\bar{C}\bar{D} + \bar{C}D) \\
 &= A(C\bar{D}(B + \bar{B})) + \bar{B}(A + A)(\bar{C}\bar{D} + \bar{C}D) \\
 &= A(C\bar{D}) + \bar{B}\bar{D} \quad \text{or} \quad \bar{D}(AC + \bar{B})
 \end{aligned}$$

$$2. F(A, B, C, D) = \sum m(3, 4, 5, 7, 9, 13, 14, 15)$$

The expression has 4 variable

so we make 4×4 k-map

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$		
$\bar{A}\bar{B}$	00	0	1	1	3	2
$\bar{A}B$	01	1	4	1	7	6
$A\bar{B}$	11	12	13	1	15	14
AB	10	8	9	11	1	10

Now,

$$\begin{aligned}
 F(A, B, C, D) &= \bar{A}B(\bar{C}\bar{D} + \bar{C}D) + (\bar{A}\bar{B} + A\bar{B})(CD) \\
 &\quad + (AB + A\bar{B})(\bar{C}D) + AB(CD + C\bar{D}) \\
 &= \bar{A}B\bar{C}(\bar{D} + D) + \bar{A}CD(\bar{B} + B) \\
 &\quad + A\bar{C}D(B + \bar{B}) + ABC(D + \bar{D}) \\
 &= \bar{A}B\bar{C} + \bar{A}CD + A\bar{C}D + ABC
 \end{aligned}$$