

ASSIGNMENT - III - :

Q-1) Zero address instruction format is used for
Ans - d.) Stack Organised Architecture

Q-2) When an instruction is read from the memory, it is called
Ans - b.) Fetch cycle

Q-3) In Boolean Expression $A + BC$ equals
Ans - b.) $(A+B)(A+C)$

Q-4) Which of the following is not a characteristic of a RISC Architecture
Ans - a.) Large instruction set

Q-5) Which of the following is used for binary multiplication
Ans - b.) Booth's Algorithm

Q-6) The binary no. obtained after applying Arithmetic Right Shift
Ans operation on 11010 will be -
Ans - b.) 11101

Q-7) What does the data transfer instruction STA stand for?
Ans - a.) Store Accumulator

Q-8) How many instruction cycles will be there when we use a 8-bit register for booth's algorithm?
Ans - c.) 8

Q-9) A 2-bit binary multiplier can be implemented using
Ans - b.) 2 input XOR and 6 AND gates in total

Q-10) Sign magnitude is a very simple representation of?

Ans - b) Negative number

Section-B

short

short

Q-1) What is instruction set architecture?

Ans An instruction set architecture is part of the abstract model of a computer that defines how the CPU is controlled by the software. The ISA acts as an interface between the hardware and the software specifying both what the processor is capable of doing as well as how it gets done. In general, an ISA defines the supported instructions, data types, registers, the hardware support for managing main memory, fundamental features (such as the memory consistency, addressing modes, virtual memory) and the input/output model of a family of implementations of the ISA.

Q-2) Briefly explain instruction cycle.

Ans - The instruction cycle (also known as fetch-decode-execute cycle) is the cycle that the CPU follows to execute the instructions regarding the program stored in memory.

- * Fetch - The processor copies the data/instruction captured from RAM
- * Decode - Decoded captured data is transferred to the unit for execution
- * Execute - Instruction is finally executed. The result is then registered in the processor or RAM (memory address)

Q-3) What is zero and one instruction set format?

Ans - * Zero Instruction Set Format -

This instruction does not have an operand field, and the location of operand is implicitly represented. The stacks

organised computer system supports these instructions. To evaluate the arithmetic expression, it is required to convert it into polish notation.

Mode	Opcode
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A - Address

- * ^{Address} One Instruction Set : These instruction lines are implied accumulator for data manipulation operations. An accumulator is a register used by the CPU to perform logical operations. In one address instruction, the accumulator is implied and hence it does not require an explicit reference. For multiplication and division, there is a need for a second register. However, here we will neglect the second register and assume that the accumulator contains the result of all the operations.

Mode	Opcode	Operand
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Q-4. Explain array multiplier with an example.

Ans- An array multiplier is a digital combinational circuit used for multiplying two binary no. by employing an array of half adders and full adders.

Eg - consider multiplication of two 2-bit no.

Multiplication bits $\rightarrow b_1 \& b_0$, Multiplier bits $\rightarrow a_1 \& a_0$

$$\begin{array}{r}
 b_1 \quad b_0 \\
 \times \quad a_1 \quad a_0 \\
 \hline
 a_0 b_1 \quad a_0 b_0
 \end{array}$$

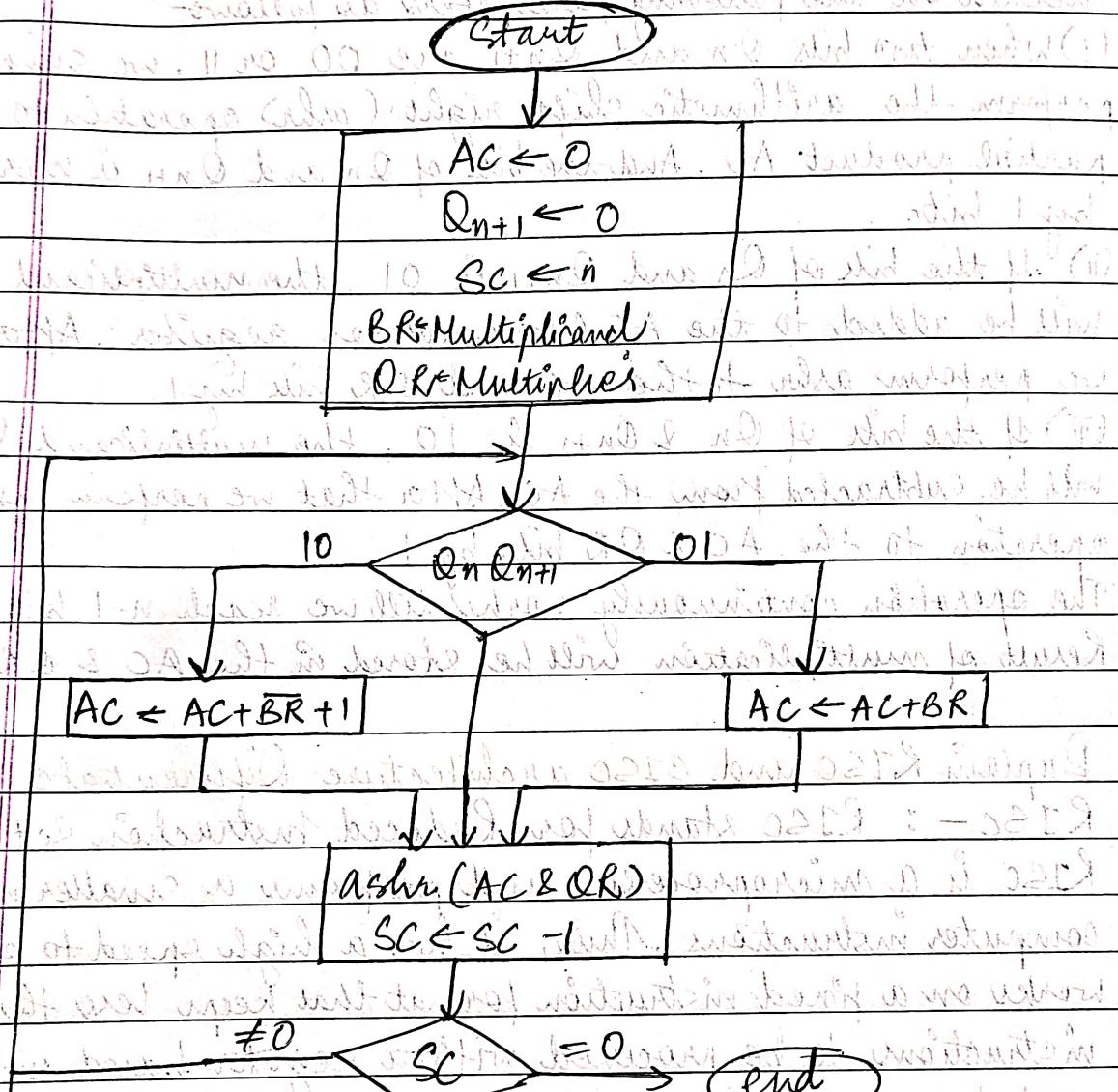
$$\begin{array}{r}
 + \quad a_1 b_1 \quad a_1 b_0 \\
 \hline
 \textcircled{C}_3 \quad c_2 \quad c_1 \quad c_0
 \end{array}$$

$$\text{Product} \rightarrow c_2 c_1 c_0 \quad [c_3 \rightarrow \text{carry (if any)}]$$

Section-C - Implementation of Booth's algorithm

Q-1) Explain Booth's Algorithm in detail.

The Booth's algorithm is a multiplication algorithm that allows us to multiply the two signed binary integers.



→ Set the multiplicand & multiplier binary numbers M & Q respectively.

→ Initially we set the AC and Q_{n+1} registers value to 0.

→ SC represents the no. of multiplier bits (Q) and it is a sequence.

Counter that is continuously decremented till equal to the no. of bits (n) or reached to 0.

- Q_n represents the last bit of the Q, and the Q_{n+1} shows the incremented bit by 1 of Q_n .
- On each cycle of the booth's algorithm, Q_n and Q_{n+1} will be checked on the following parameters as follows:-
- (i) When two bits Q_n and Q_{n+1} are 00 or 11, we simply perform the arithmetic shift right (ashr) operation to the partial product AC. And the bits of Q_n and Q_{n+1} is incremented by 1 bit.
- (ii) If the bits of Q_n and Q_{n+1} is 01, the multiplicand (M) bit will be added to the AC (Accumulator register). After that we perform ashr to the AC and QR bits by 1.
- (iii) If the bits of Q_n & Q_{n+1} is 10, the multiplicand (M) bit will be subtracted from the AC. After that we perform ashr operation to the AC & QR bits by 1.
- The operation continuously works till we reach $n-1$ bit.
- Result of multiplication will be stored in the AC & QR registers.

Q-2.)

Explain RISC and CISC architecture. Differentiate b/w them

Ans - *

RISC - : RISC stands for Reduced Instruction Set Computer. RISC is a microprocessor and performs a smaller no. of computer instructions. Thus, it has a high speed to operate. It works on a fixed instruction format that keeps less than 100 instructions to be processed with a register-based instruction used by a few simple addressing modes. The LOAD/STORE is the only instruction used to access the memory as it is a compiler development mechanism.

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CISC - : CISC stands for Complex Instruction Set Computer. CISC

is the kind of chip that can be easily programmed and makes the best and efficient use of memory. The main motive of CISC is to make compiler development easy & simple. There is no need for machine to generate instructions for the processor as CISC eliminates the need.

RISC

- 1) RISC is a reduced instruction set. |
- 2) The no. of instruction is less as compared to CISC |
- 3) The addressing modes are less. |
- 4) It works in a fixed instruction format. |
- 5) The RISC consumes low power |
- 6) The RISC processors are highly pipelined |
- 7) It optimizes the performance by focusing on software. |
- 8) Requires more RAM |

CISC

- 1) CISC is a complex instruction set. |
- 2) The no. of instruction is more as compared to RISC. |
- 3) The addressing modes are more. |
- 4) It works in a variable instruction format. |
- 5) The CISC consumes high power |
- 6) The CISC processor are less pipelined. |
- 7) It optimizes the performance by focusing on hardware. |
- 8) Requires less RAM |

Section - D :-

Q-1) Using Booth's Algorithm solve the multiplication of $(-2) * (-3)$

Sol: $M = -2 = 110$

$Q = -3 = 101$

$$\left[\begin{array}{l} 2 \rightarrow 010, -2 \rightarrow 110 \\ 3 \rightarrow 011, -3 \rightarrow 101 \end{array} \right] \quad (\text{By } 2\text{'s complement})$$

AC

On ad min Q111-4 to 10

Operation

1st Cycle

000

101

0

$$AC = AC - M = AC + (-M)$$

$$\Rightarrow AC = 000 + (-110)$$

$$\Rightarrow AC = 000 + 010$$

$$\Rightarrow AC = 010$$

010

101

0

↓↓

↓↓

↓↓

001

010

1

Arithmetic
right shift

2nd Cycle

001

+ 2 on 010

1

$$AC = AC + M$$

$$\Rightarrow AC = 001 + 110$$

$$\Rightarrow AC = 111 + 010$$

111

010

0

↓↓

↓↓

0

111

101

0

3rd Cycle

111

101

0

$$AC = AC - M = AC + (-M)$$

$$\Rightarrow AC = 111 + (-110)$$

$$\Rightarrow AC = 111 + 010$$

$$\Rightarrow AC = 001$$

discard carry

001

101

0

↓↓

↓↓

0

000

110

1

101 = 8 = 0

$$\text{Now } n = 0 \quad [01 \leftarrow 1 \rightarrow 010 \leftarrow 2] \quad 010 \leftarrow 2$$

$$[101 \leftarrow 2 \rightarrow 110 \leftarrow 2] \quad 110 \leftarrow 2$$

$$\therefore \text{final answer} \rightarrow 000110 = 6$$