

## Assignment - 4

### Section A

1) The Boot sector files of the system are stored in which computer memory?

Ans - (b) ROM

2) Which memory acts as a buffer between CPU and main memory?

Ans - (c) Cache

3) To overcome the slow operating speeds of the Secondary memory we make use of faster flash drives?

Ans - (a) True

4) In the memory hierarchy, as the speed operation increases the memory size also increase.

Ans - (b) False

5) If we use the flash drives instead of the hard disk, then the secondary storage can go above primary memory in the hierarchy.

Ans - (b) False

6) What is true about memory unit?

Ans - (c) both A and B

7) What is ~~the~~ the formula for Hit Ratio?

Ans- (a) Hit / (Hit + Miss)

8) The memory implemented using the semiconductor chips is \_\_\_\_\_.

Ans- (b) Main Memory

9) Which of the following is independent of the address bus?

Ans- (a) Secondary Memory

10) If  $M$  denotes the number of memory locations and  $N$  denotes the word size, then an expression that denotes the storage capacity is \_\_\_\_\_.

Ans- (a)  $M * N$

## Section-B

1. How we can overcome the speed mismatch between CPU and main memory?

Ans- Speed mismatch between CPU and memory access is reduced by Cache memory.

Cache memory is a small-sized type of volatile computer memory that provides high speed data access to a processor & stores frequently used applications & data.

2) What do you mean by write through and write back technique?

Ans - Write through :- When data is updated, it is written to both the cache & the back-end storage. This mode is easy for operation but is slow in data writing.

Write - Back :- When data is updated, it is written only to the Cache, The modified data is written to the back end storage only when data is removed from the Cache.

3) What are the different types of ROM.

Ans - (1) MROM [Marked read Only memory]

(2) PROM [Programmable read Only memory]

(3) EEPROM [Erasable & programmable read Only memory]

(4) EEPROM [Electrically erasable & programmable read only memory]

(5) Flash Memory

4) Differentiate between static RAM and Dynamic RAM.

Ans-

### Static RAM

### Dynamic RAM

- |   |  |
|---|--|
| <p>1) It has long data life.</p>                  | <p>It has short data life.</p>                       |
| <p>2) They are expensive.</p>                     | <p>They are less expensive.</p>                      |
| <p>3) It is slow density device</p>               | <p>It is a high density device</p>                   |
| <p>4) It is used as cache memory in computer.</p> | <p>It is used as main memory in computer system.</p> |

### Section-c

- 1) Explain the memory Technique?

Ans- There are four primary technologies used today in memory hierarchies -

#### (i) SRAM Technology -

(a) It is simple integrated circuits that are memory arrays with a single access port that can provide either a read or a write.

(b) SRAM's don't need to refresh and so that access time is very close to the cycle time.

#### (ii) DRAM Technology -

(a) In DRAM, as long as power is applied the value kept in a cell is stored as a charge in a capacitor.

(b) DRAMs use only a single transistor per bit of storage, they are cheaper per bit than SRAM.

### (iii) Flash Memory :-

(a) It is a type of EEPROM.

(b) It stores information in an array of memory cell made from floating gate transistors.

(c) Applications are typically prohibited from writing to flash memory in such circumstances

### (iv) Disk Memory or Magnetic Memory -

(a) Magnetic hard disk consist of a collection of platters, which rotate on a spindle at 5400 to 1500 revolution per minute.

(b) To read & write information on a hard disk, a movable arm containing a small electromagnetic coil called read - write head is located just above each surface.

(2) Explain the memory Hierarchy in detail.

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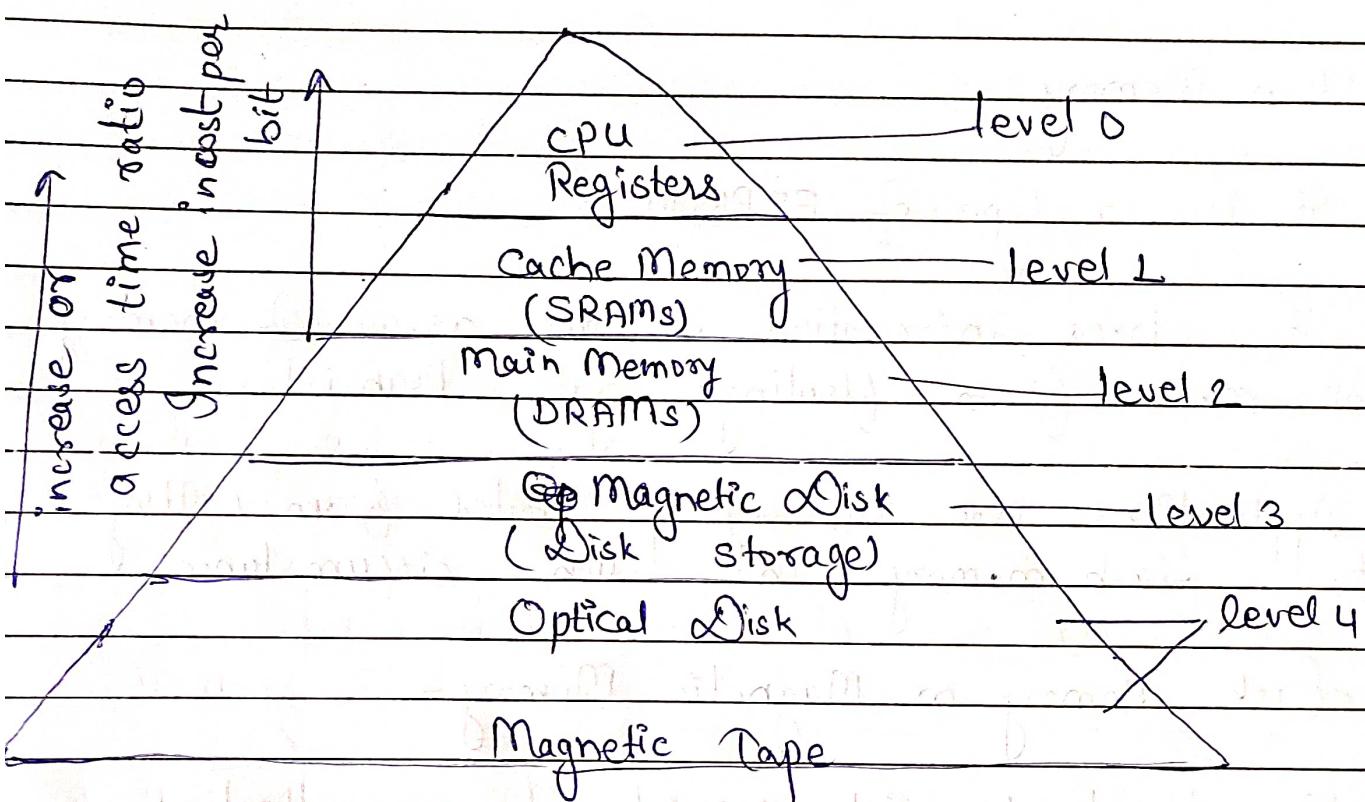
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(2) Explain the memory Hierarchy in detail.

Ans- It is an enhancement that helps in organising the memory so that it can actually minimise the access time.

The development of this occurred on a behaviour of a program known as locality of references.



This Hierarchy Design of memory is divided into two main types. They are

(1) External or Secondary Memory - It consists of Magnetic Tape, Optical Disk, Magnetic Disk i.e. it includes peripheral storage device that are accessible by the system's processor via I/O module.

(2) Internal Memory or Primary Memory - It consists of

CPU Registers, Cache Memory and Main Memory  
It is accessible directly by the processor.

### Section-D

1) Explain the address mapping of the RAM/Rom in detail by using example.

Ans- (a) The addressing of memory can establish by means of a table that specifies the memory address assigned to each chip.

(b) The table called a memory address map, is a pictorial representable of assigned address space for each chip in the System shown in table.

(c) To demonstrate with a particular example - assume that a compute System needs 512 byte of RAM and 512 bytes of Rom.

Component	Hexa address	Address bits									
		10	9	8	7	6	5	4	3	2	1
RAM 1	0000 - 0077	0	0	0	x	x	x	x	x	x	x
RAM 2	0080 - 00FF	0	0	1	x	xx	x	x	x	x	x
RAM 3	0100 - 017F	0	1	0	x	xx	x	x	x	x	x
RAM 4	0180 - 01FF	0	1	1	x	xx	x	x	x	x	x
ROM	0200 - 03FF	1	x	x	x	xx	x	x	x	x	x

(d) The component column specifies whether a RAM or Rom chip used. Moreover, the hexadecimal address column assigns a range of

hexadecimal equivalent address for each chip.

(e) The address bus lines listed in third column

(f) Although there are 16 lines in address bus, table shows only 10 lines because other 6 not used in this example & assumed to be zero.

3) Explain the concept of Associative and Set associative mapping in cache Memory.

Ans- Associative Mapping -

⇒ The fastest & most flexible cache organization uses on associative memory.

⇒ It stores both the address & content (data) of memory word.

⇒ The diagram shows three words presently stored in the cache. The address value of 15 bits is shown as a five octane & its corresponding 12 bit word is shown as four digit octal number.

⇒ A CPU address of 15 bits is placed in the argument register & associate memory is searched for matching address.

CPU address (15 bits)



Argument Registers

Address	Data
01000	3450
02777	6710
22345	1234

### Set Associative Mapping-

- It is an improvement over direct mapping organization in that each word of Cache can stores two or more words of memory under the same index address.
- It can accomodate 1024 words of main memory since each word cache contains two data words.
- In general, a Set- associative cache of set size  $K$  will accomodate  $K$  words of main memory in each word of cache.

Index	Tag	Data	Tag	Data
000	0	3450	02	5670
777	02	6710	00	2340

Fig Two-way Set Associative Mapping Cache.

The octal number listed in above fig are with reference to the Main Memory content.