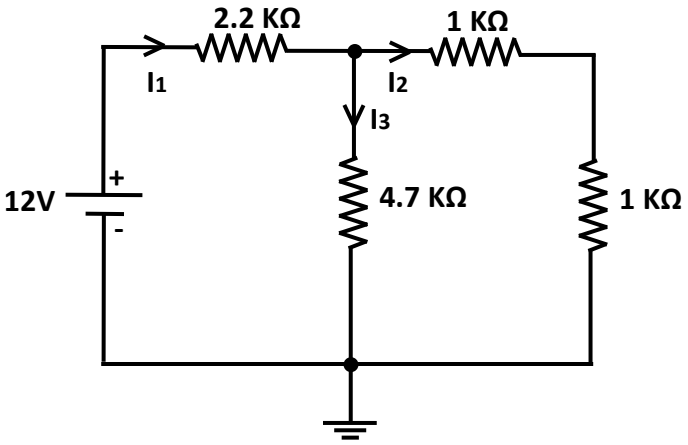
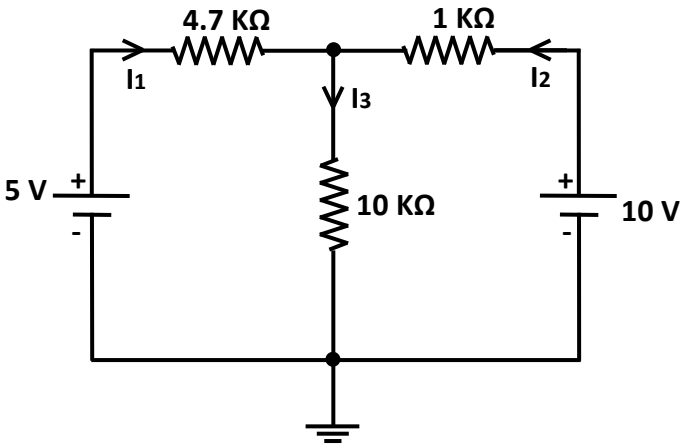
Basic Electronics Circuit's Lab

Experiment no. 2

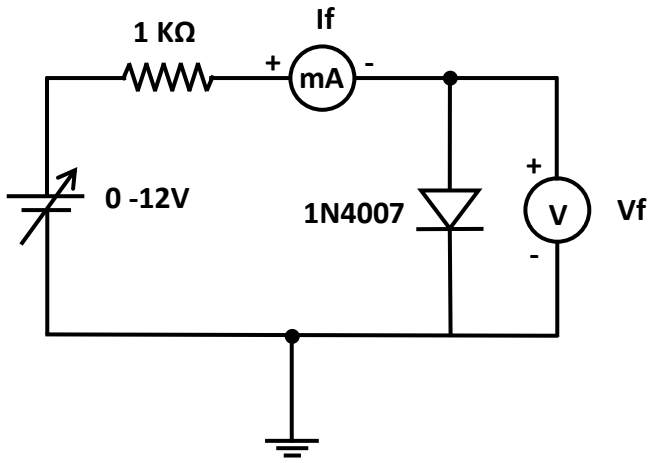
1. (a) verification of voltage and Current Division principles in the resistive circuits.





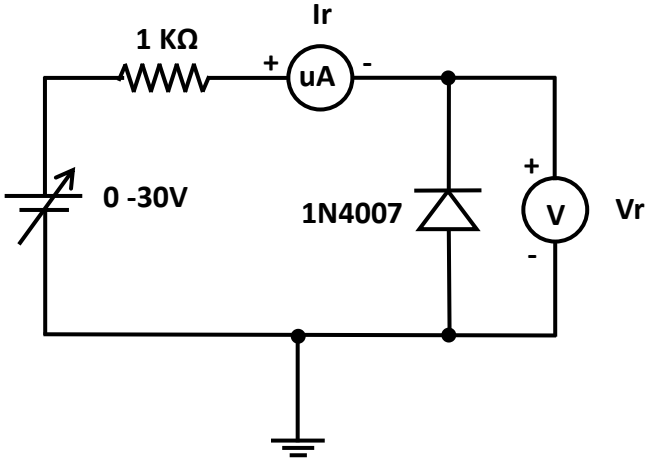
2. (a) PN Junction Diode Characteristics.

Forward Bias :



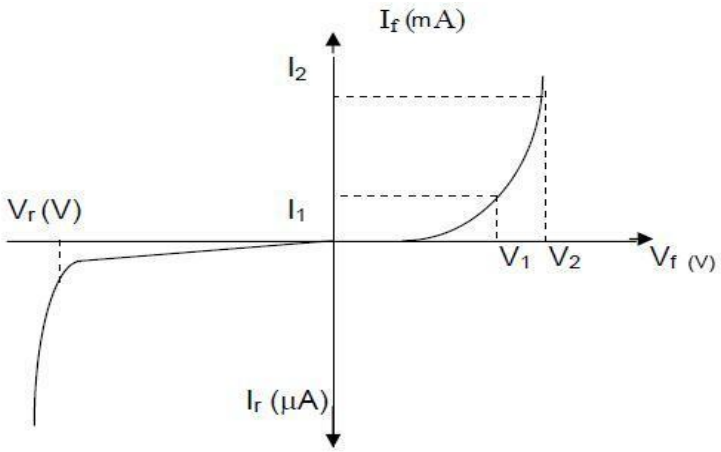
Sl No	Input Voltage	Vf	If
1	0.2		
2	0.4		
3	0.6		
4	0.8		
5	1		
6	2		
7	4		
8	5		
9	7		
10	8		
11	10		
12	12		

Reverse Bias :



Sl No	Input Voltage	Vr	Ir
1	1		
2	2		
3	3		
4	4		
5	5		
6	10		
7	15		
8	18		
9	20		
10	23		
11	26		
12	30		

The model graph for both forward and reverse biased conditions of a PN junction diode is shown below.



Model graph for VI characteristics of a PN junction diode

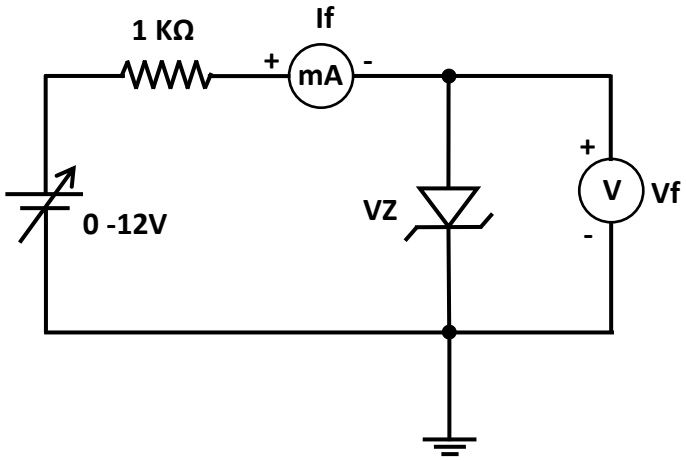
(a) Static resistance = $\frac{Vf}{If}$

(b) Dynamic resistance = $\frac{V2 - V1}{I2 - I1}$

c) Forward voltage drop =

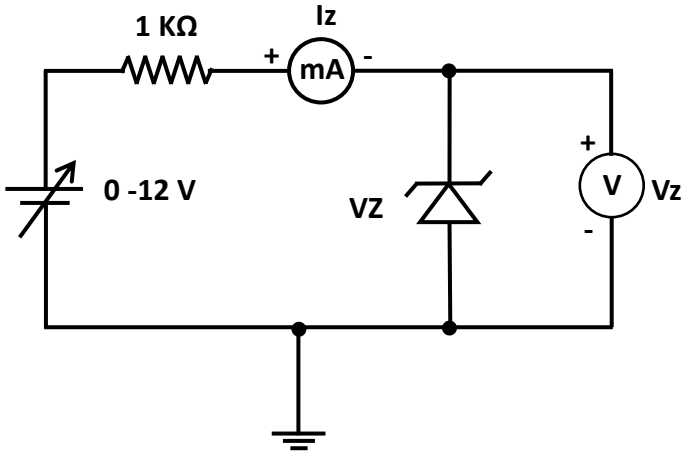
2. (b) Zener Diode Characteristics.

Forward Bias:

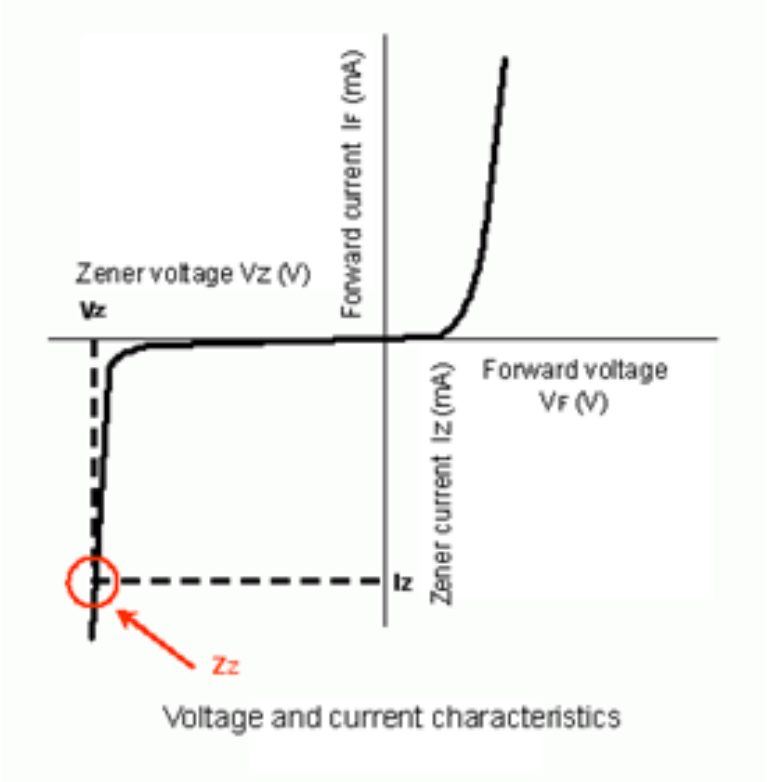


Sl No	Input Voltage	Vf	If
1	0.2		
2	0.4		
3	0.6		
4	0.8		
5	1		
6	2		
7	4		
8	5		
9	7		
10	8		
11	10		
12	12		

Reverse Bias:



Sl No	Input Voltage	Vz	Ir
1	1		
2	2		
3	3		
4	4		
5	5		
6	6		
7	7		
8	8		
9	9		
10	10		
11	11		
12	12		



Model graph for VI characteristics of a Zener diode