Indian Institute of Information Technology, Sri City, Chittoor

Name of the Exam: Digital Design SET2 Duration: 90+30 mins (for uploading) Max. Marks: 28

Question 1 to 5: 5 marks each, Question 6- 3 marks

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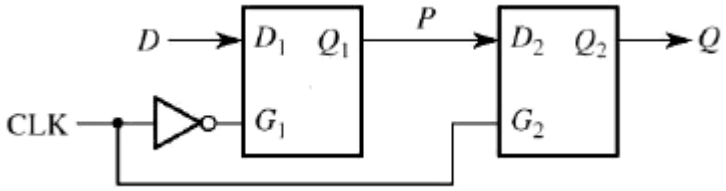
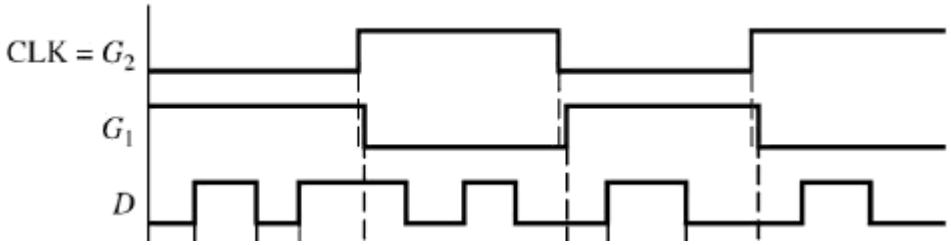
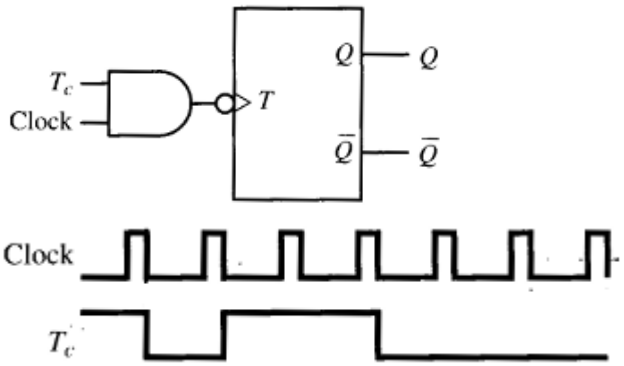
1. A) For the given circuit diagram , draw the waveforms at P and Q. Draw the given waveforms for G1, G2 and D in the answer script. Aligning with the given waveforms, draw the waveforms at P and Q. Assume initial low levels. The given flip-flops are rising edge triggered.





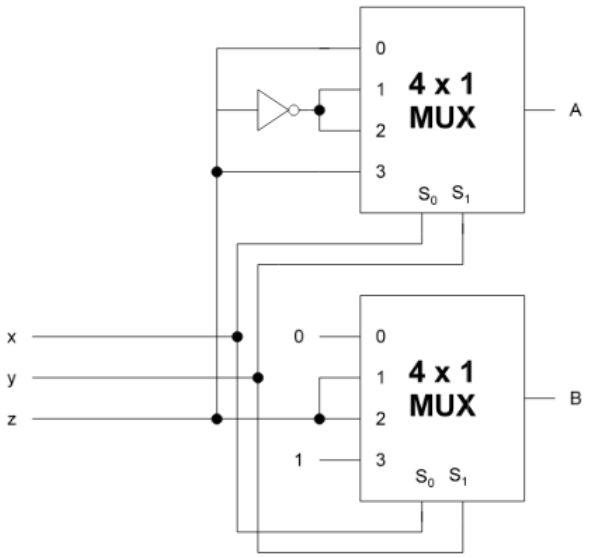
B) Aligning with the given waveforms ,Draw the timing diagram at T, Q and Q'. Assume Q starts from logic low level initially.



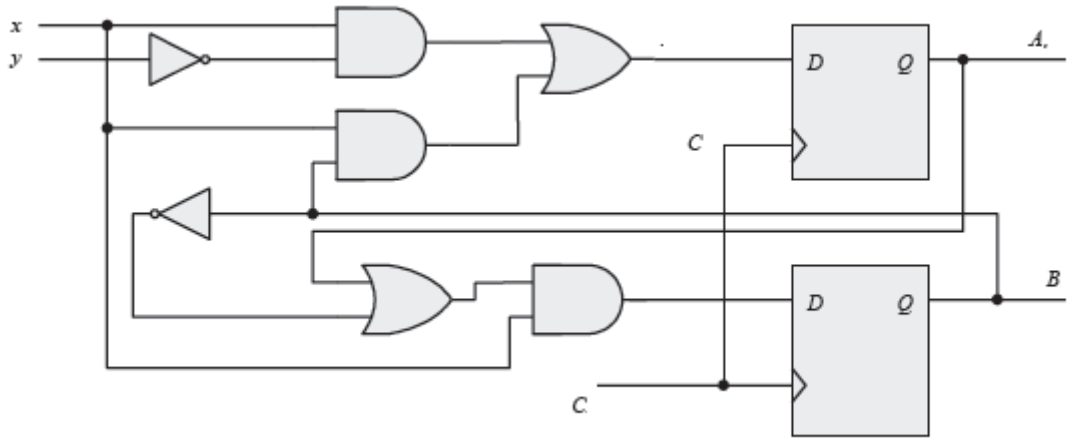
2. For the given circuit, write the complete truth table with (x, y, z) as inputs and (A, B) as outputs and complete the following with numbers.

A=∑(.....) A=∏(.....)
B=∑(.....) B=∏(.....)

S0	S1	x	y	z	A	B



3) Construct the state table and write the state equation for the given sequential circuit diagram



4) Write the complete truth table of a 4x2 priority encoder along with valid bit indicator and draw the circuit diagram. Consider D0, D1, D2, D3 as inputs with D0 as highest priority and D3 as lowest priority. Bit "1" to be encoded.

5) Design a Asynchronous 0-7 counter using negative edge triggered D flip flops. Draw the timing diagram at the output of each flip flop with respect to clock signal.

6) Design a counter that counts from 7-14 and then repeats itself.