CSE Department, IIT Guwahati

CS223: Computer Architecture and Organization

Quiz-1 (03.02.2021)

Submission Link - [submit before 07:30 pm on 03.02.2021]

https://forms.office.com/Pages/ResponsePage.aspx?id=jacKheGUxkuc84wRtTBwHANSILeDKUNOi1YB2VJD6t1UMFVRSEczRjlPQjZUOTJEN1dHUlJJN1o2Wi4u

1. [3] The content of a floating point register is C57A0000. The format of the floating point is IEEE-754 (single precision) and it uses excess-128 for biased exponent. What is the equivalent decimal value?

2. [3] Consider the real number 27.5625 and this number is stored in a 32-bit register using IEEE-754 (Single Precision) format and it uses excess-128 for biased exponent. Write the contents of the register in Hexadecimal format.

3. [3] The content of an 8-bit register is E7 in hexadecimal format. What is the decimal equivalent value stored in this register in:

   (a) Sign Magnitude form:

   (b) 1's complement form :

   (c) 2's complement form :

4. [2] For a memory module, the size of data bus (size of memory location) is 32 bits and size of address bus is 32 bits. What is the capacity of the memory module in GigaByte (GB)?

5. [2] The capacity of a memory module is 8 GB. What are the sizes of address bus and data bus if the size of each memory location is 32 bits?

6. [3] If the last operation performed on a computer with an 8-bit word was an addition (A+B) in which the two operands were A = -86 and B = -25; the numbers are represented in 2's complement form. What would be the value of Carry, Zero, Overflow, Sign, Even Parity, and Half Carry flags? (Show the calculations)

7. [5] The RTL description of the fetch phase of single bus CPU organization is as follows:

T1: MAR <- PC, Read

T2: MBR <- Memory

PC <- PC+1

T3: IR <- MBR

Give the RTL description of the execution phase of the instruction: *MOV M, data* (M = data). M is the address of the memory location to store the given data. It is a three-word instruction – first word is the op-code and the second word is the operand. What are the addressing mode of operands?

8. [1+3+2+1+2] Opcodes of some instructions for 8085 microprocessor are given below. All the numbers are represented in Hexadecimal format

LDA address: 3A, MVI H, data: 26, MVI L, data: 2E, ADD M: 86, MVI A data: 3E,

MVI B data: 06, ADD B: 80 STA address: 32, MOV A, B: 78

Consider the following code segment stored from memory location 357D:

06 3F 3A 01 B0 80 32 10 B0

a) After execution of this code segment, what is the value of the Program Counter (PC)
b) Convert the machine code segment to Assembly code
c) What are the locations of operands before execution of this code segment?
d) Flag bits effected after execution of the last instruction of the code segment
e) The final effect of this code segment after execution.