

Ayush Gaurav

Address:17 Meena Enclave,
Near Shankar Ashram
Jwalapur, Haridwar
Uttrakhand
249407
Contact: +91-9565379408
email-id: ayush23gaurav@gmail.com



CAREER OBJECTIVE: TO WORK HARD IN AN ORGANIZATION OR INDUSTRY WHICH ALLOWS OPPORTUNITY TO INNOVATE, GROW AND DEVELOP

EDUCATION:

Degree	College/School	University/Board	Passing Year	Pass Percentage/Grade
B.Tech(ECE)	MNNIT Allahabad	MNNIT Allahabad	2018	8.36/10
10th	STCS Srinagar Uttrakhand	ICSE	2012	91%
12th	DPS Noida	CBSE	2014	92.4%

PROJECTS:

1. Model A Terrain(eYRC Sponsored by MHRD India)

- Traversal of 5x5 cells.
- Finds all the special paths(Curve,Slope,Bump,And Tunnel),obstacles and different colored objects.
- Map it onto blender animation software in real time.
- Link:[eYRC MT50 Demonstration for original configuration](#)

2. Room Automation

- Automatic Control of
 - Main door entrance (IR sensor)
 - Fan speed according to the temperature(lm35 sensor)
 - Intensity level of bulb according to intensity of the room
 - Curtains according to intensity of outside
- Password protected door lock of the room
- Triacs and optocoupler is used for voltage control by phase angle variation method

3. DCT of 8x8 image using Spartan 3A kit

- IEEE 754 floating point representation
- floating point arithmetic unit
- Vga interfacing and keyboard interfacing

4. 16X2 Lcd Interfacing And UART Implementation On FPGA Kit

- Hyper Terminal was used to communicate with Spartan 3A kit.
- Transmitted character was also displayed on a 16x2 alphanumeric lcd.
- Finite State Machine was created using Verilog HDL.

TRAINING & INTERNSHIP

- iERS(i3indya for Embedded Systems And Robotics) 1 Month
Brief introduction and familiarization with Embedded Systems and Robotics and extensive study about ATmega 16.

AREA OF INTEREST:

- Digital Electronics
- Electronic Devices (BJT, MOSFETS And Operational Amplifiers)
- Circuit Design
- FPGA(Using Verilog)