UNIT – 4

1: Data aquisition method
Block diagram, Analog and digital IO.
2: Counter & Timer
3: ADC (Analog to digital converter)
Successive approximation, Flash, Sigma-Delta
4: DAC (Digital to analog Converter)
weighted resistor and R-2R, inverted R-2R
5: Use of Data Sockets for Network Communication

1: Data Aquisition Method:

Data aquisition, referenced by the acronyms DAS or DAQ, is the digitizing and processing of multiple sensor of signal inputs for the purpose of monitoring, analyzing, and/or controlling system and processes.

Signal or sensor inputs define the behaviour of physical parameters and come from devices such as sensors, timer, relay, and solid-state circuits.

Internal circuitry is used to digitize and process these input in order to monitor, analyze and or control systems & processes.

DAS or DAQ →
- Sensor
- Signal conditioning.
- Multiplexer
- Storage & Display.

DAS or DAQ may be defined as a system used for data processing, data conversion, data transmission & Data storage.

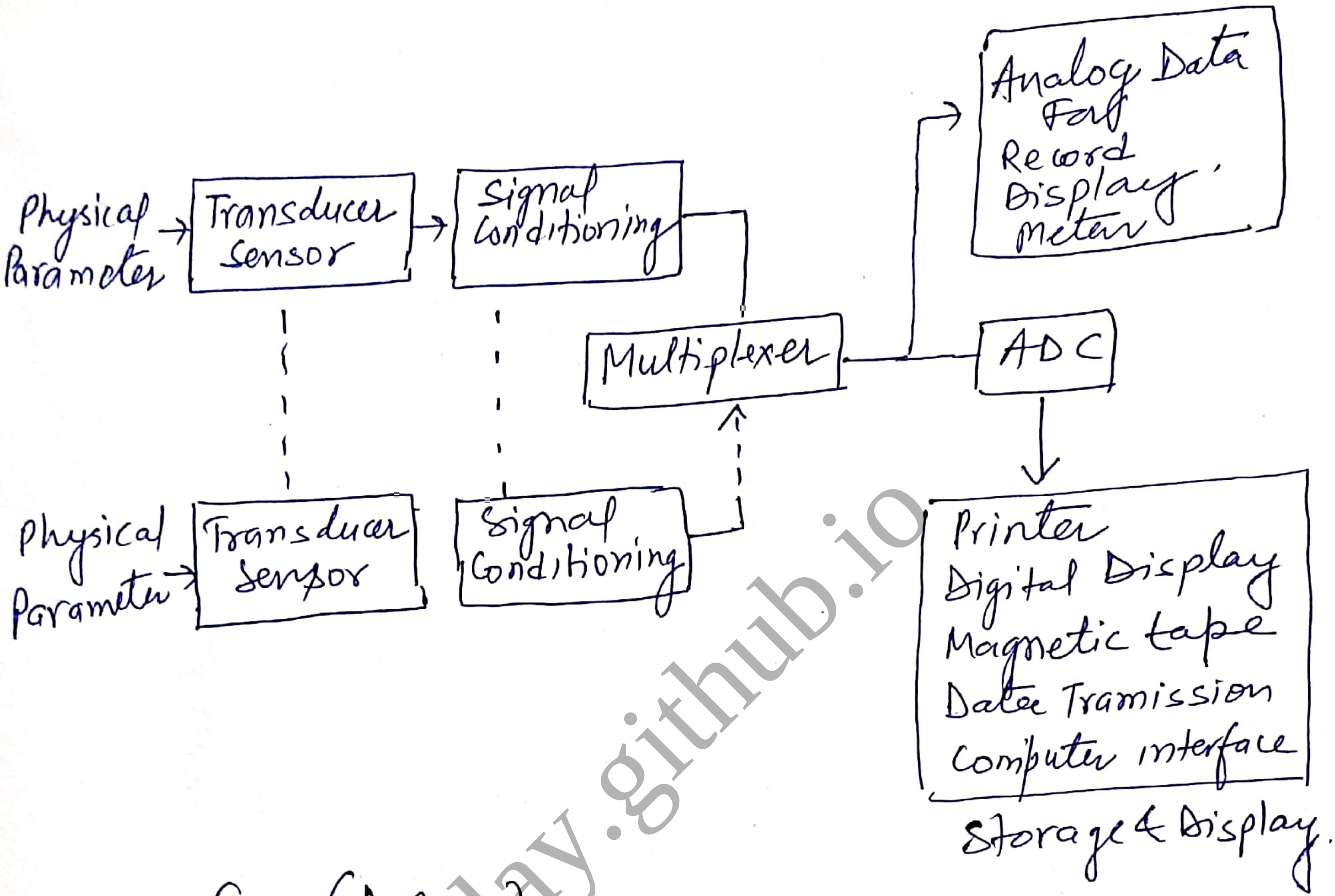


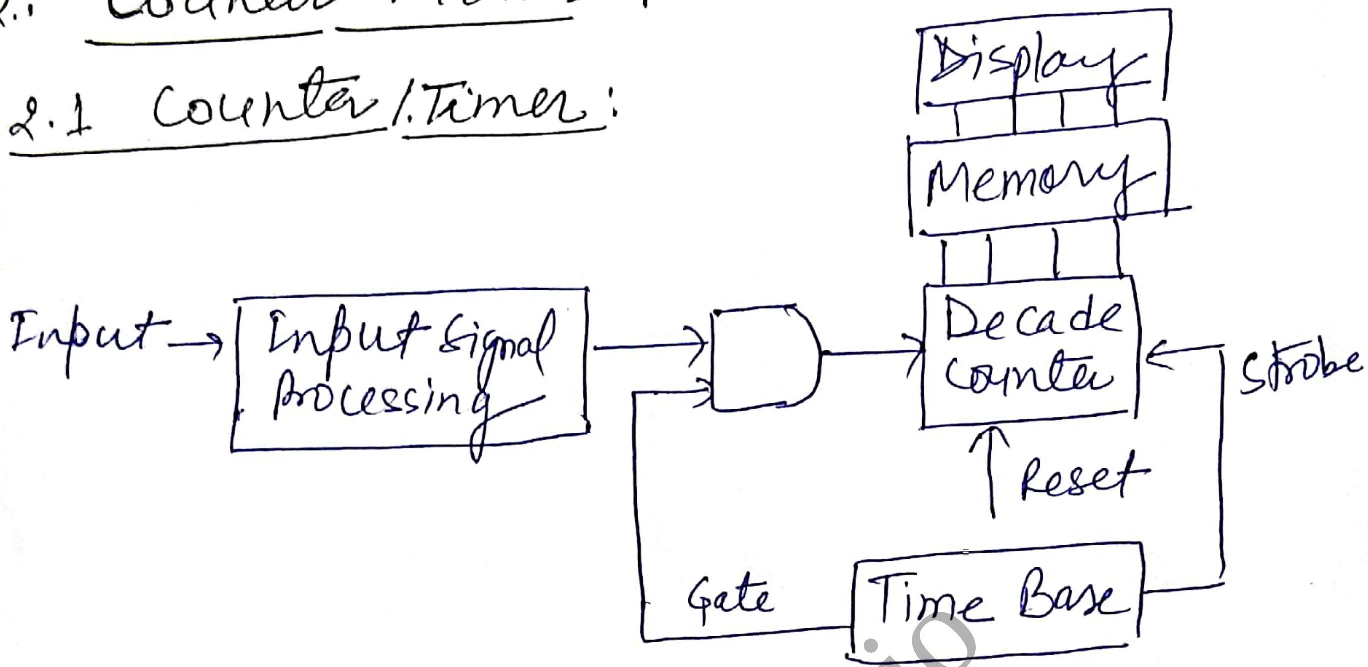
Fig. (DAS)

Objective of DAS:

- ✓ ~~Relatively~~ Reliable & flexible expansion for future requirements.
- ✓ Acquire correct data at correct speed and at correct time.
- ✓ Safe operation
- ✓ To find out the state of plant and inform to operator.
- ✓ Identify the problem area.

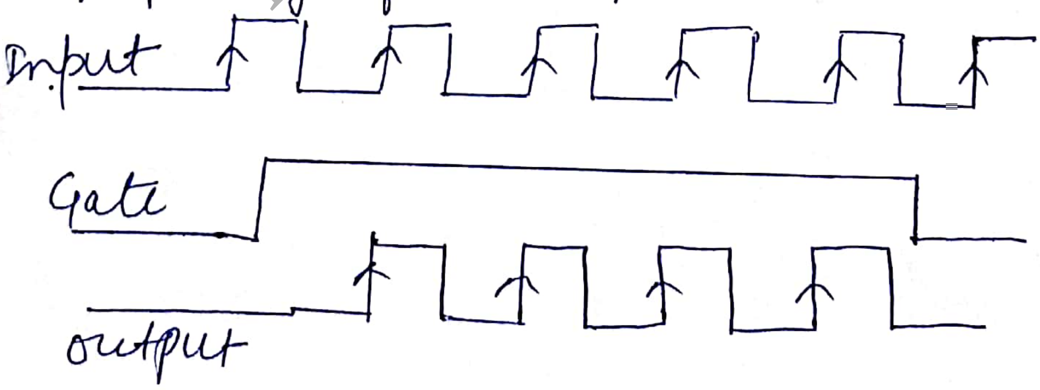
2: Counter & Timer:

2.1 Counter/Timer:



(Basic block diagram of a frequency counter)

The frequency counter operates on the principle of gating the input frequency into the counter for predetermined time.
As an example,
if an unknown frequency were gated into the counter for an exact 1 second(s), the number of count allowed into the counter would be precisely the frequency of the input.



(waveform associated with the gating function of frequency counter)

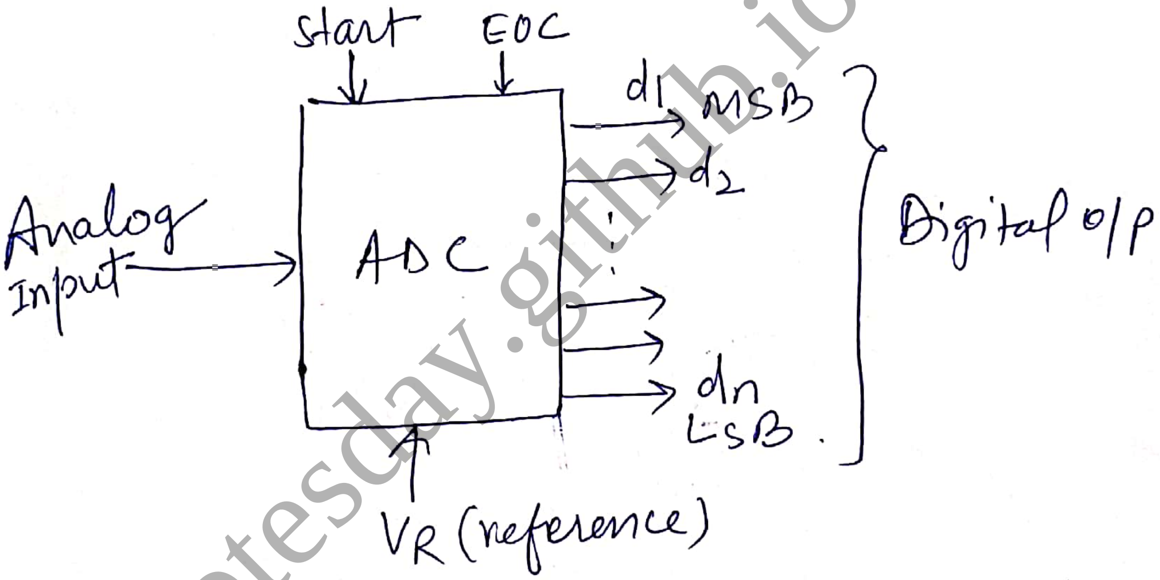
7

3: ADC (Analog to Digital Converter):

- ✓ Function is opposite to DAC.
- ✓ Analog input is converted into binary word $d_1, d_2, \ldots d_n$ of functional value D, so that.

$$D = d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}$$

d_1 – most significant bit
d_n – least significant bit



ADC are classified in two group:

1 – Direct type ADC's
2 – Integrating type ADCs

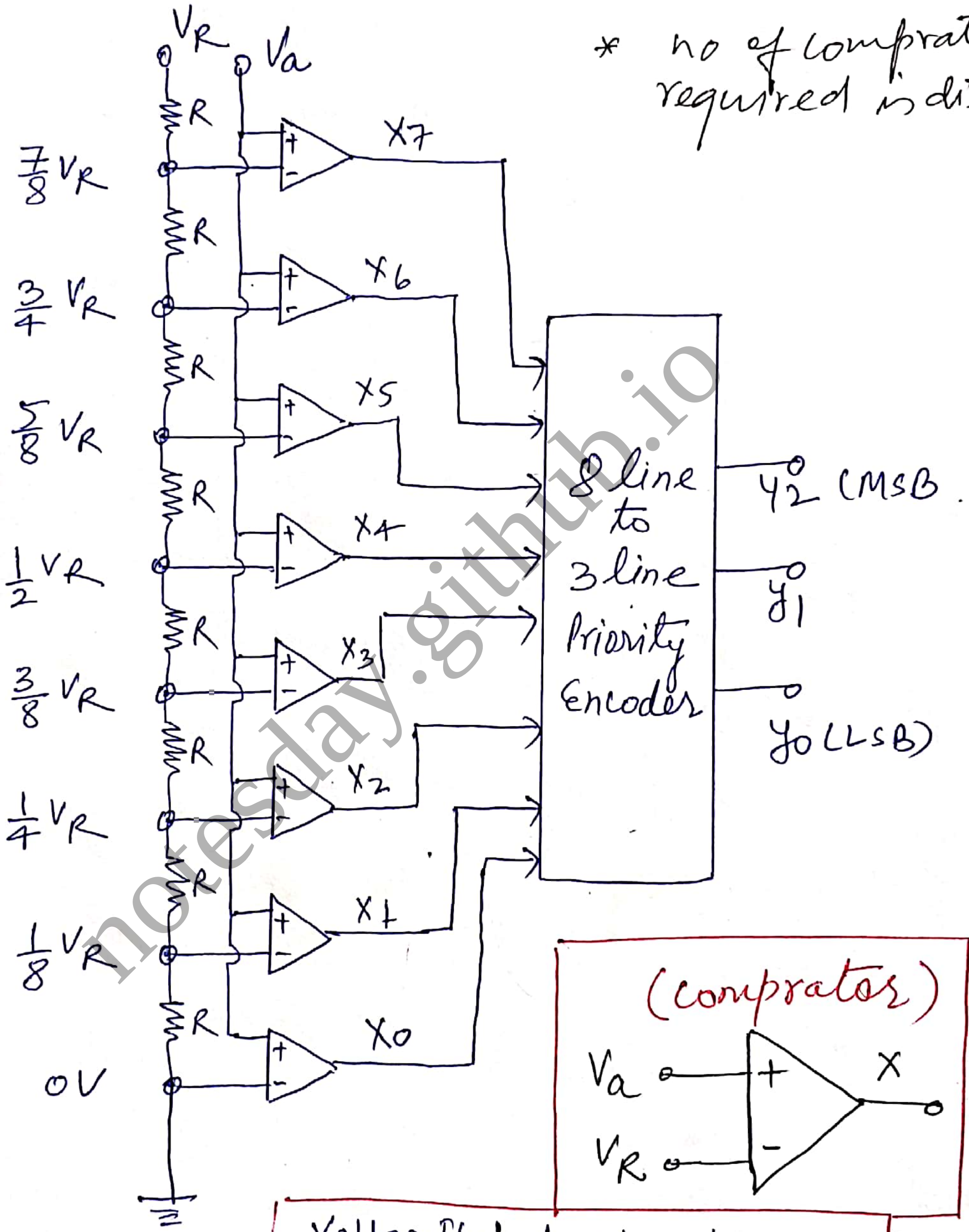
3.1: Direct type ADC:

(a) Flash (comprator) type converter
(b) Counter type converter
(c) Tracking or servo converter
(d) Sucessive approximation type converter.

→ Flash type converter / comprator type :

- Simplest possible A/D converter
- Fastest & expensive (conversion time 100 ns or less)

* no of comprator required is disadv.



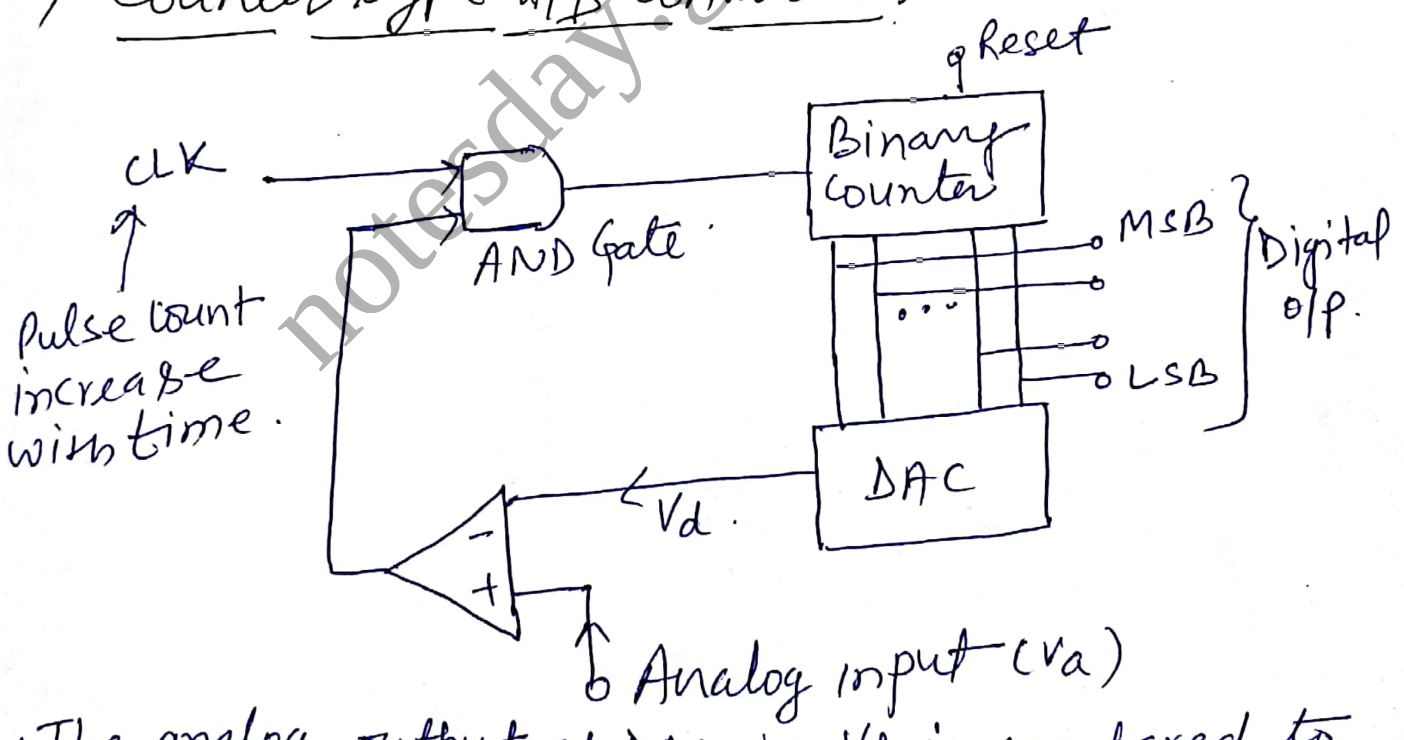
comprator & Truth Table →

Voltage I/p	Logix o/p (X)
$V_a > V_R$	$X = 1$
$V_a < V_R$	$X = 0$
$V_a = V_R$	Previous value.

9

I/p Voltage (V_a)	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to $3V_R/8$	0	0	0	0	0	1	1	1	0	1	0
$3V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to $3V_R/4$	0	0	0	1	1	1	1	1	1	0	1
$5V_R/4$ to $3V_R/4$	0	0	1	0	0	0	0	0	1	1	0
$3V_R/4$ to $7V_R/8$	0	1	1	1	1	1	1	1	1	1	0
$7V_R/8$ V_R	1	1	1	1	1	1	1	1	1	1	1

→ Counter type A/D converter:



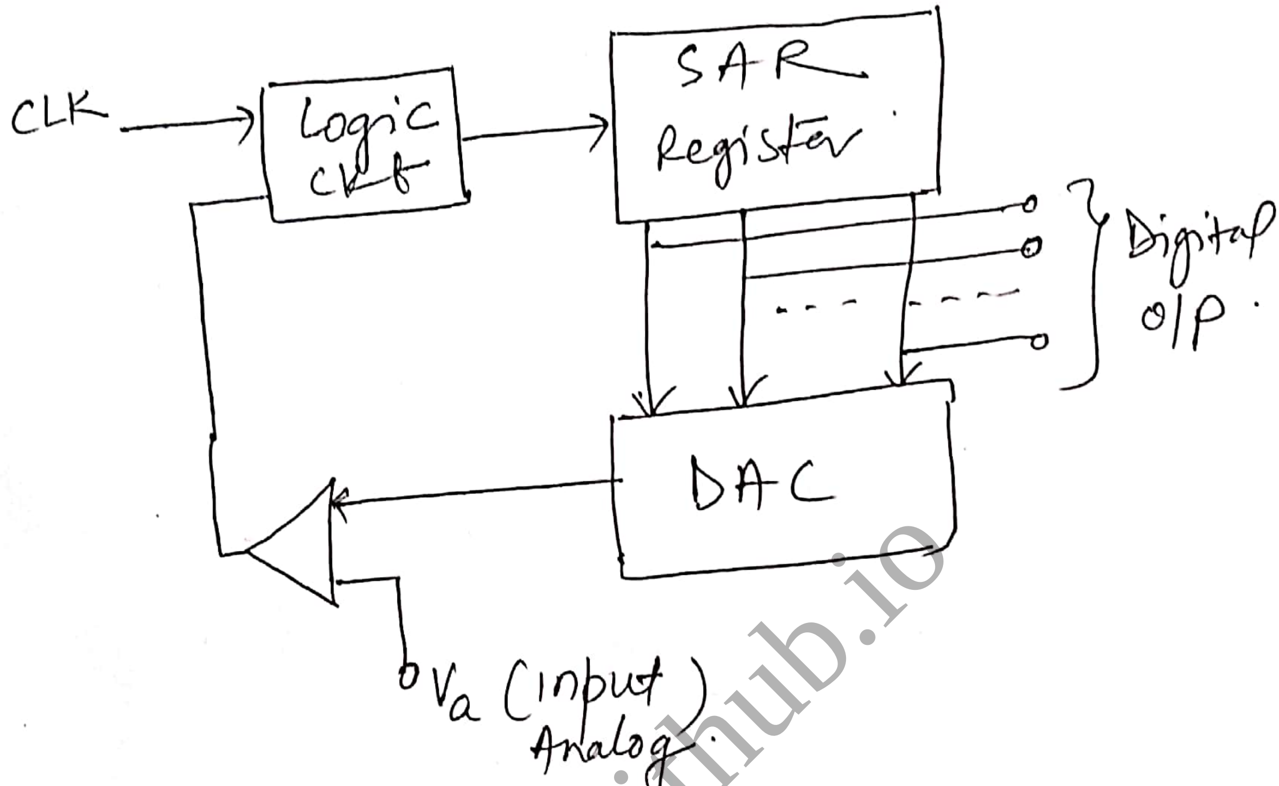
- The analog output of DAC ie Vd is compared to the analog input Va by the comparator.

if $V_a > V_d$ — counting.

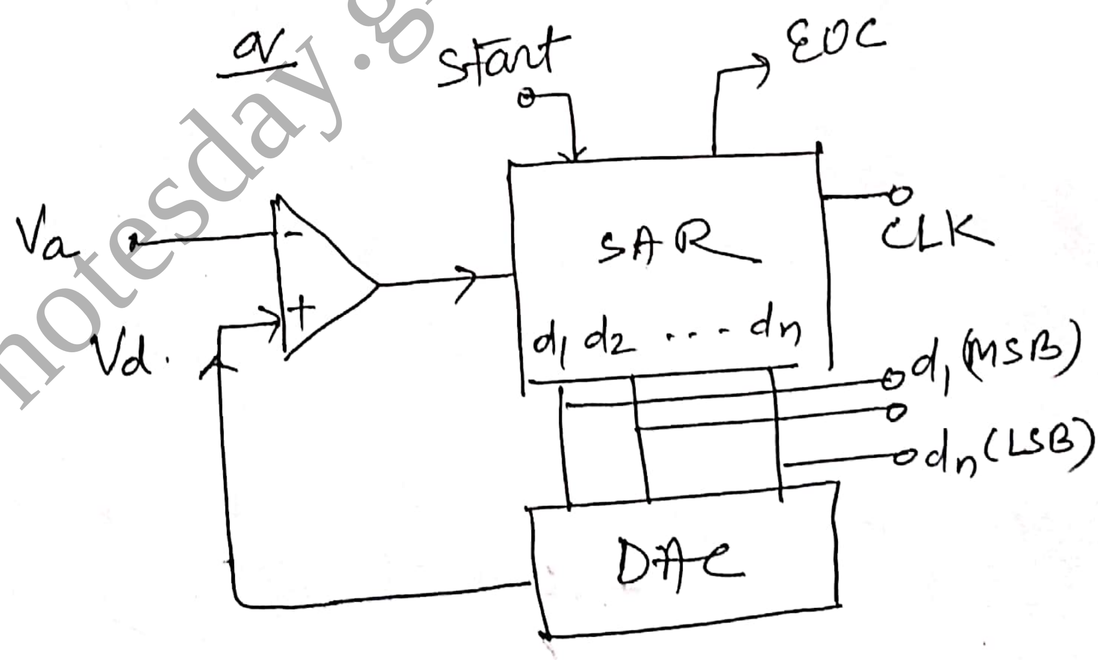
$V_a \le V_d$ — Stop counting & Va = Value of digital counter

$V_a < V_d$ — AND gate is disable, NO counting.

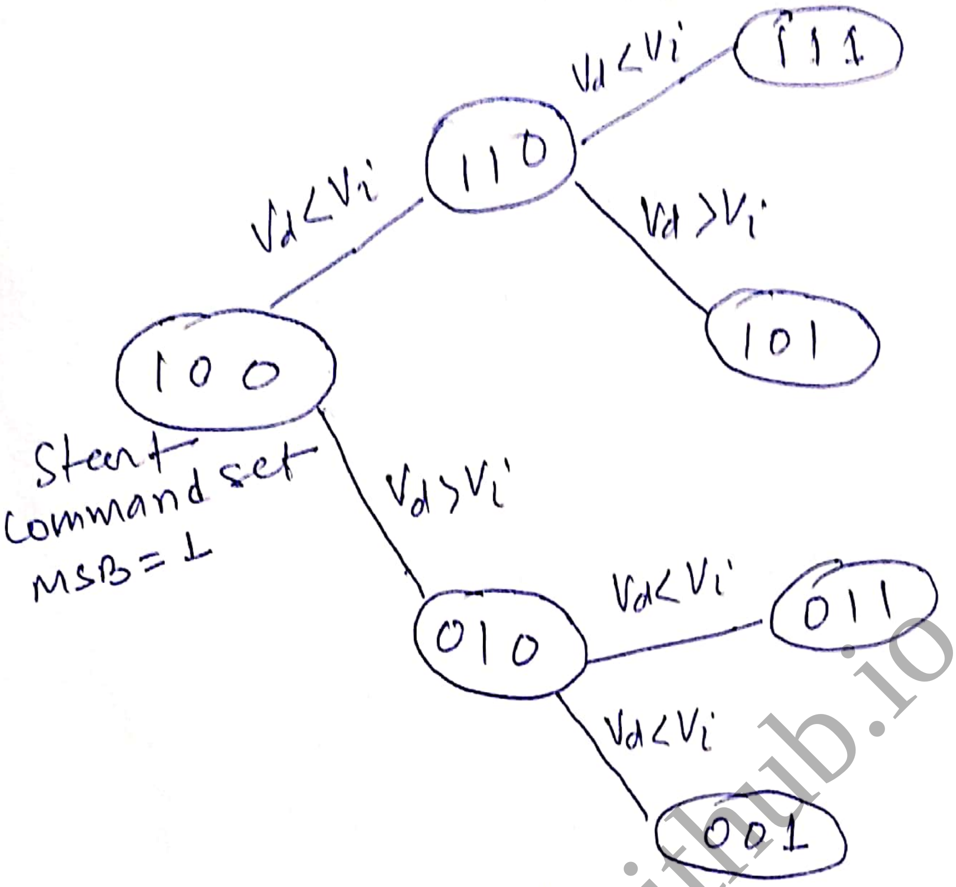
→ Successive approximation ADC :



or



Successive approximation ADC is the advanced version of digital ramp type ADC which is designed to reduce the conversion and to increase speed of operation.



(Tree diagram).

✓ Start command

SAR → set MSB $d_1 = 1$, with all other bit 0

✓ V_d (o/p of DAC) is compared with V_a

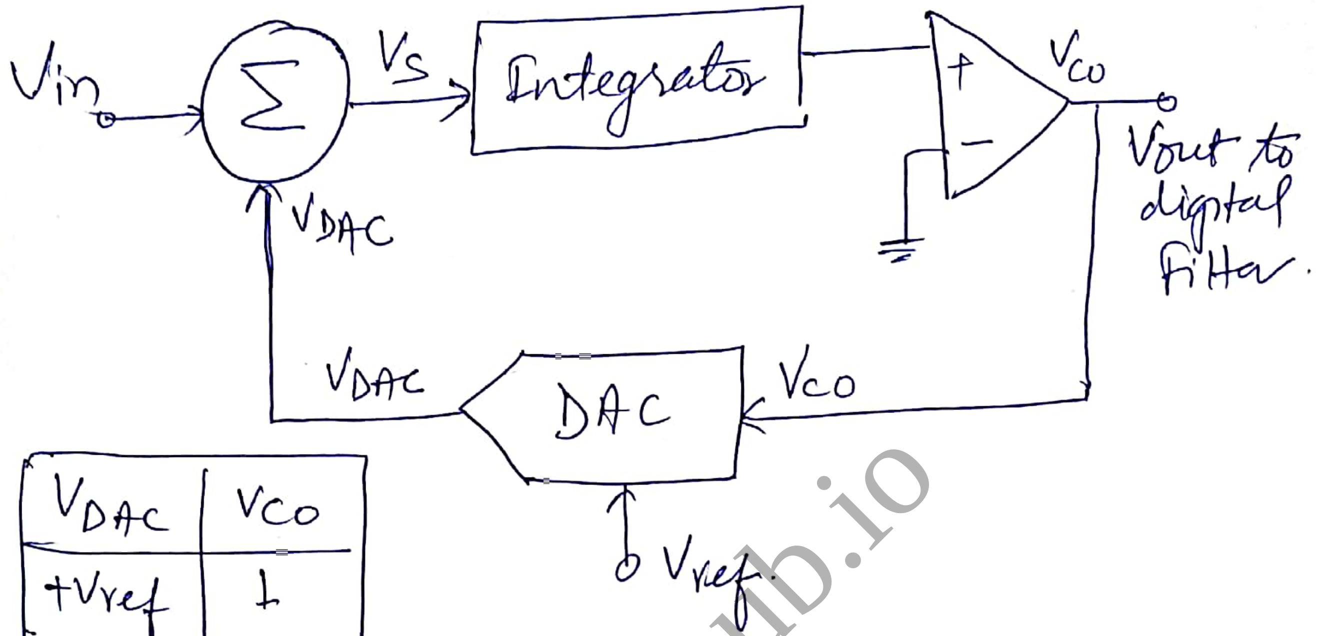
if $V_a > V_d$ → MSB is left 1 and & next lower significant bit made 1

if $V_a < V_d$ → set MSB = 0 and go to next lower significant bit

whenever V_d is crosses the V_a, the comparator change state and this can be taken as the end of conversion.

—o—

3.2 Sigma-Delta ADC;



VDAC	Vco
+Vref	1
−Vref	0

It is another type of integrating ADC. It contains an integrator, a DAC and a comparator and summing junction. Sigma-delta ADCs come in 16 to 24 bit resolution, and they are economical for most data aquisition and instrument applications.

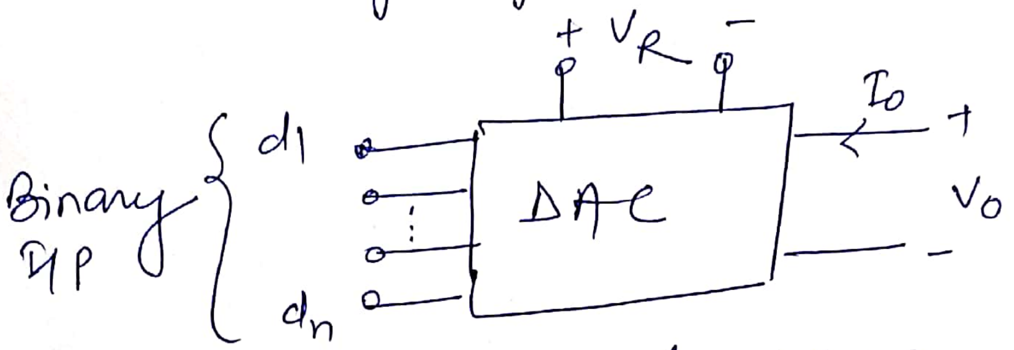
The input voltage sums algebriaically with the o/p voltage of the DAC, and the integrator adds the summing point output V_s to a value it stored previously.

The digital filter averages the series of logic ones and zeros, determines the bandwidth and settling time, and outputs multiple-bit data.

—o—.

4: Digital to Analog Converter (DAC)

DACs are used to convert digital signal into analog signal.



(Schematic of DAC)

$$V_o = K V_{FS} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}) \quad (1)$$

V_o – output voltage

V_{FS} – Full scale voltage

K – Scalling factor usually adjusted to unity

$d_1, d_2, d_3 \dots d_n$ → n-bit binary fractional word with decimal point located at the left.

MSB weight — $V_{FS}/2$

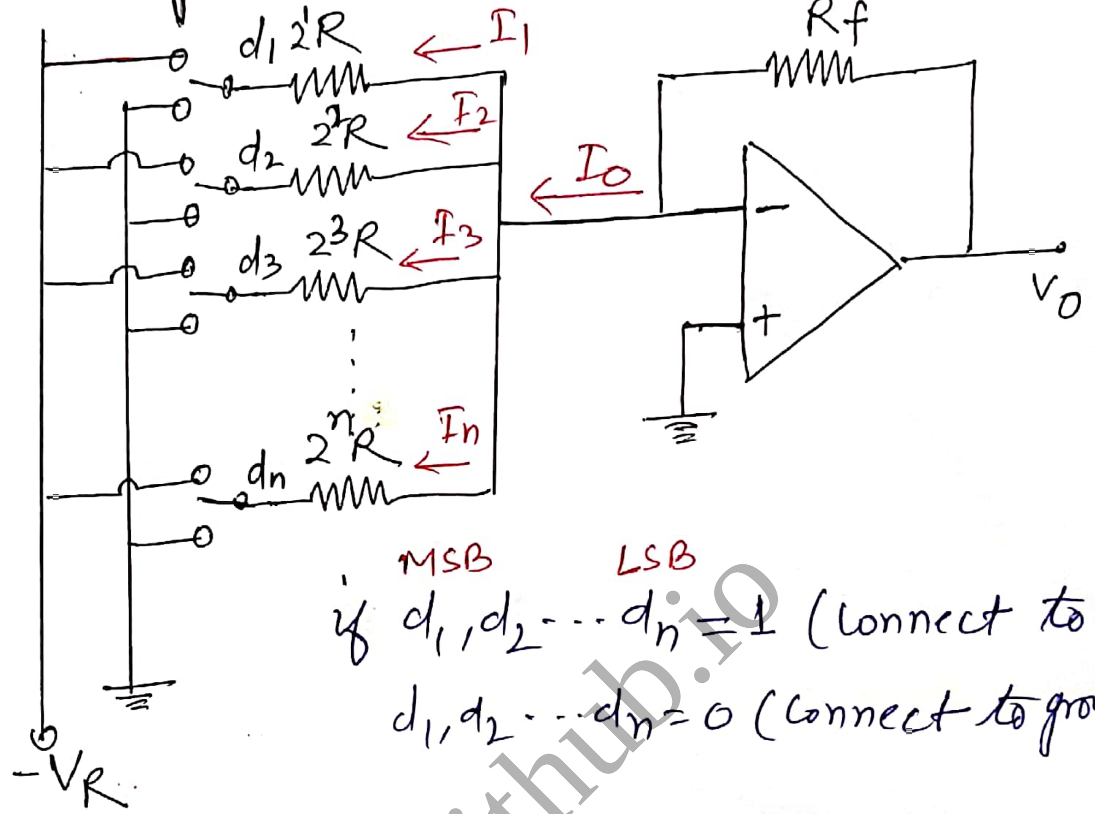
LSB weight — $V_{FS}/2^n$

Types of DAC:

- ✓ The binary-weighted DAC
- ✓ R-2R ladder DAC
- ✓ Inverted R-2R DAC
- ✓ Switched capacitor DAC
- ✓ Switched current source DAC
- ✓ Switched resistor DAC
- ✓ The thermometer-coded DAC
- ✓ Overlapping DACs or interpolating DACs
- ✓ Pulse width modulator

etc.

4.1 Binary weighted Resister DAC :

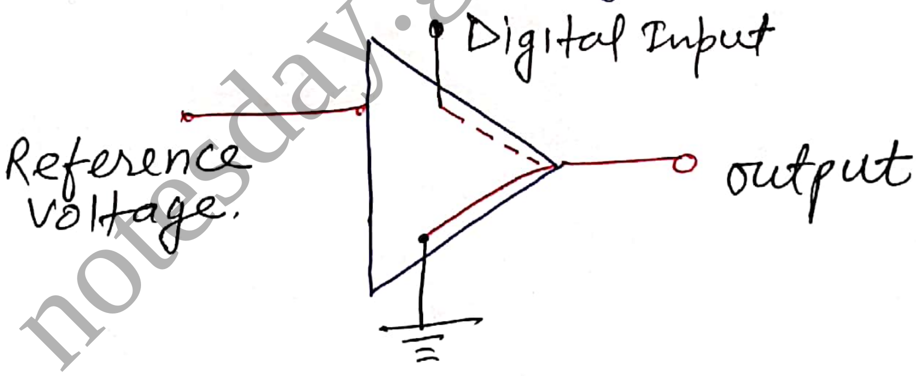


MSB LSB

if $d_1, d_2 \cdots d_n = 1$ (connect to $-V_R$)

$d_1, d_2 \cdots d_n = 0$ (connect to ground).

(Circuit of binary weighted DAC)



(An opamp used in DAC)

✓ use summing amplifier with a binary weighted resister network.

✓ It has n-electronic switches $d_1, d_2 \cdots d_n$ controlled by binary input word.

✓ If the binary input to particular switch is 1, it connects the resistance to the reference voltage ($-V_R$) and if 0, it connects the switch to the ground.

5

The o/p current I_0 for an ideal opamp can be written as.

$$I_0 = I_1 + I_2 + \cdots + I_n$$
$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \cdots + \frac{V_R}{2^n R} d_n$$
$$= \frac{V_R}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right)$$

The o/p voltage,

$$\boxed{V_0 = I_0 \cdot R_f = V_R \frac{R_f}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right)} \quad \text{--- (2)}$$

comparing eqn (1) & (2),
it can be seen that if $R_f = R$, then $K=1$ & $V_{FS} = V_R$

It may be noted that,

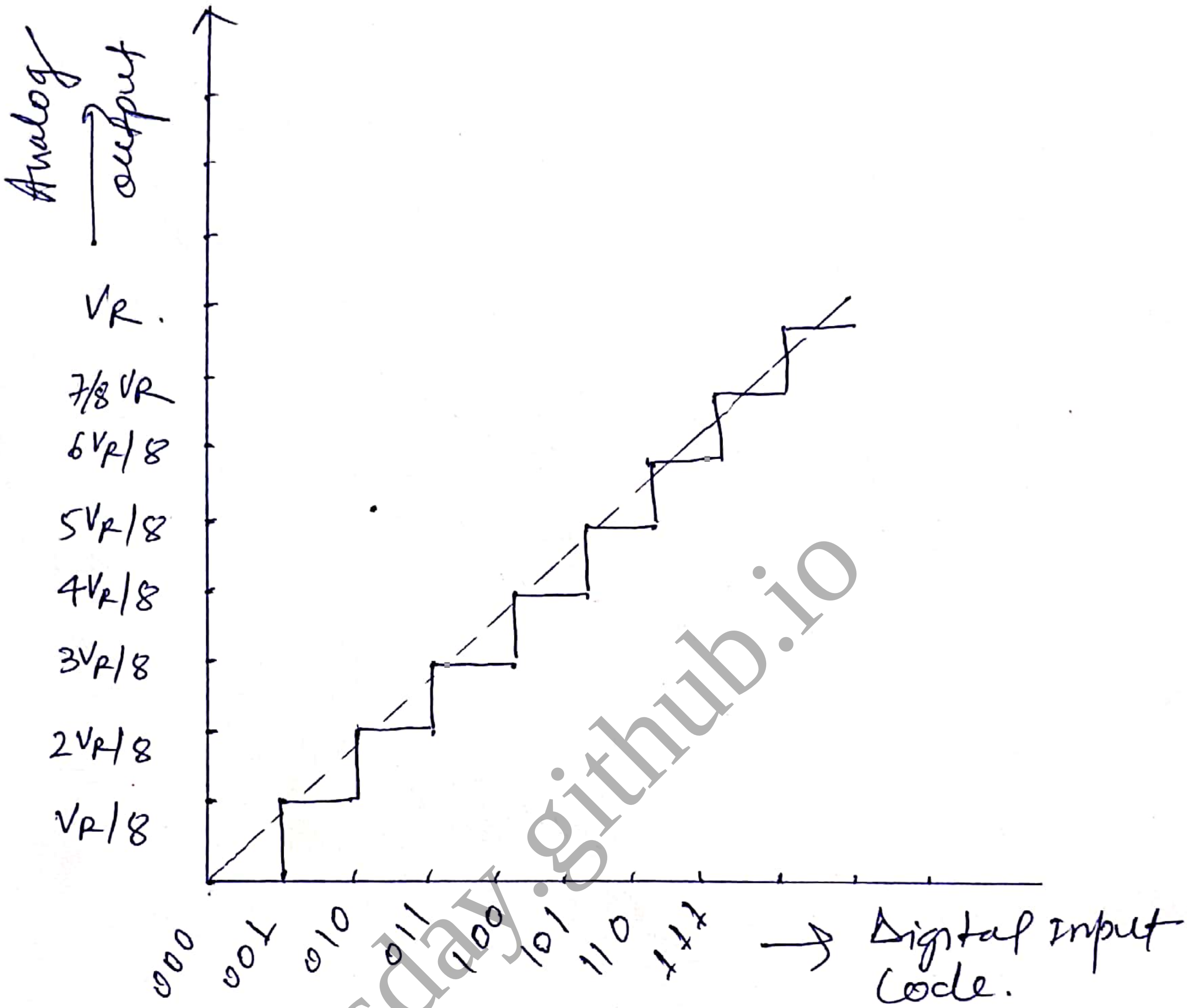
✓ opamp work as current to voltage converter

✓ It is very difficult to fabricate large resistance in IC, It restrict the use of weighted resistance DAC below 8 bit to avoid loading effect.

for 8 bit: $2^0 R, 2^1 R \cdots\cdots 2^7 R \rightarrow 128$ times

for 12 bit: 2^0 —— $2^{12} R \rightarrow$ if $R = 2.5\,k\Omega$
then $2^{12} R = 5.12\,M\Omega$.

✓ Transit (Bipolar) transistor can be replaced by MOSFET to avoid offset voltage across switch resistance.



(Transfer characteristics)
3 bit DAC.

— o —

4.2: R-2R Ladder based DAC :-

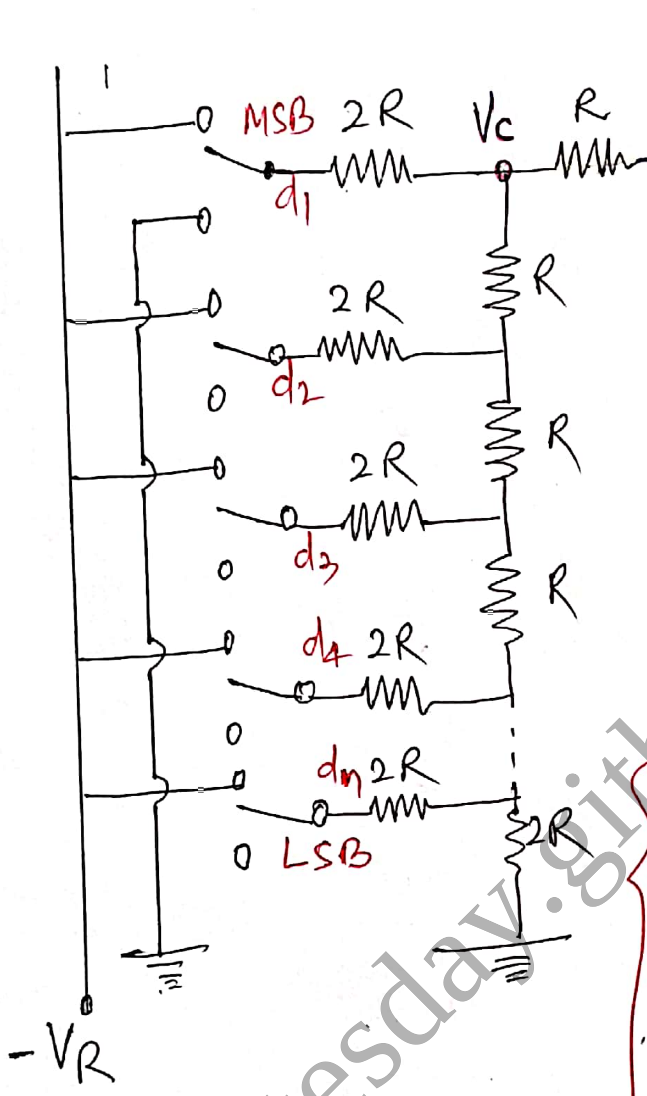
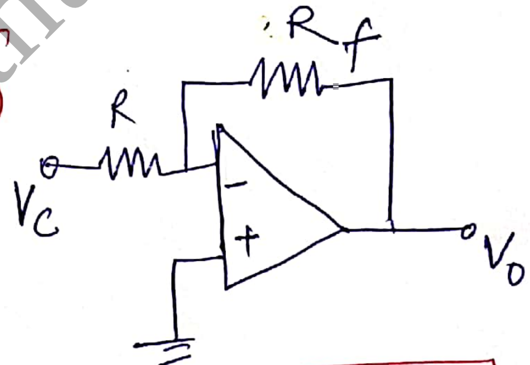


Fig. (R-2R DAC)

MSB LSB

if $d_1, d_2, \ldots d_n = 1$ (Connect to $-V_R$)

$d_1, d_2, \ldots d_n = 0$ (Connect to ground)



$$\boxed{V_o = -\frac{R_f}{R}(V_c)}$$

$$V_o = -\frac{2R}{R}(V_c)$$

Apply voltage division rule and find V_c, then calculate

$$\boxed{V_o = \frac{-R_f}{R}(V_c)}$$

✓ we use only two resistance ie R-2R, so we can avoid manufacture of number of resistance.

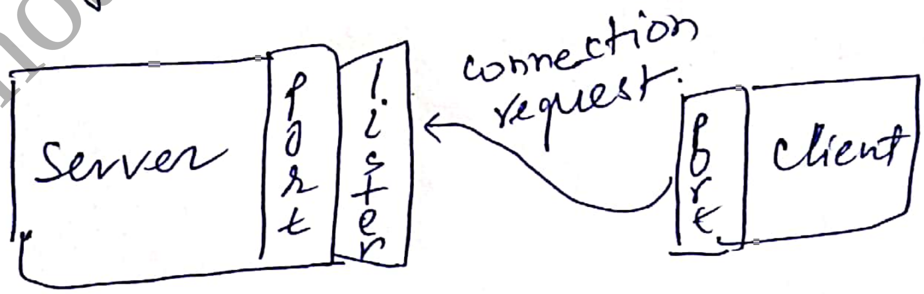
✓ R → range from (2.5kΩ to 10kΩ)

5: <u>Socket</u>? (Use of data socket for N/W comm.)

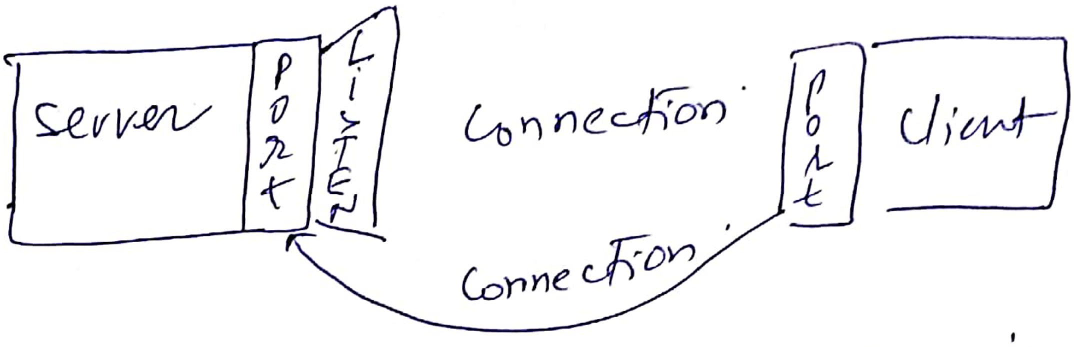
Normally a server runs on specific computer and has a socket that is bound to a specific port number. The server just waits, listening to the socket for a client to make a connection request.

On the client-side: The client knows the host name of the machine on which the server is running and the port number on which the server is listening.

To make the connection request, the client tries to rendezvous with the server's machine & port. The client also needs to identify itself to the server so it binds to a local port number that it will use during this connection. This is usually assigned by the system.



If everything goes well, the server accepts the connection. Upon the acceptance, the server gets a new socket bound to the same local port and also has its remote endpoint set to the address and port of the client. It needs a new socket so that it can continue to listen to the original socket for connection request while tending to needs of the connected client.



on the client side, if the connection is accepted, a socket is successfully created and the client can use the socket to communicate with server.

The client and server can now communicate by writing to or reading from their socket

—o—