Practical No.02: Arithmetic Logic Unit

CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;
entity ALU is
Port (
A: in STD_LOGIC_VECTOR (3 downto 0);
B: in STD_LOGIC_VECTOR (3 downto 0);
Cin : in STD_LOGIC;
Sel : in STD_LOGIC_VECTOR (3 downto 0);
Y : out STD_LOGIC_VECTOR (3 downto 0));
end ALU;
architecture concurrent of ALU is
begin
Y<= AwhenSel ="0000"else
A+1 whenSel="0001" else
B whenSel ="0010" else
B+1 whenSel= "0011" else
A+B whenSel ="0100" else
A+B+Cin whenSel = "0101" else
A-B whenSel ="0110" else
B-1 whenSel = "0111" else
AorBwhenSel="1000"else
```

```
Anor BwhenSel="1001"else
AnandBwhenSel="1010"else
AandBwhenSel="1011"else
not(A) when Sel = "1100" else
Axor BwhenSel ="1101" else
Axnor B whenSel ="1110"else
not(B) ;
end concurrent;
```

TB Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;
entity ALU_tb is-- Port ( );
end ALU_tb;
architecture Behavioral of ALU_tb is
component ALUis
Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
B: in STD_LOGIC_VECTOR (3 downto 0);
Cin : in STD_LOGIC;
Sel : in STD_LOGIC_VECTOR (3 downto 0);
Y : out STD_LOGIC_VECTOR (3 downto 0));
end component;
signal A, B, Y : std_logic_vector (3 downto 0);
```

```
signal Cin : std_logic;
signal Sel : std_logic_vector(3 downto 0) := "0000";
begin
u1: ALUport map (A, B, Cin, Sel, Y);
process
begin
A<="1010";
B <="1111";
Cin <= '0';
Sel <= Sel + 1;
wait for 100 ns;
Cin <= '1';
wait for 100 ns;
end process;
end Behavioral;
```

Port Names	FPGA Pins
a3	R2
a2	T1
a1	U1
a0	W2
b3	R3
b2	T2
b1	T3
b0	V2
s3	W16
s2	V16
s1	V17
y3	L1
y2	P1
y1	N3
y0	P3