① Inverter / NOT Gate

★ Truth Table of NOT

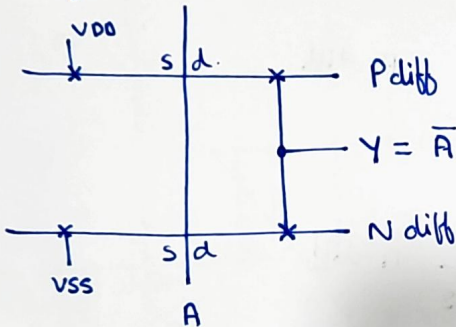| A	Y
0	1
1	0

$\therefore Y = \bar{A}$

★ Circuit Diagram.

PUN (PMOS)

PDN (NMOS)
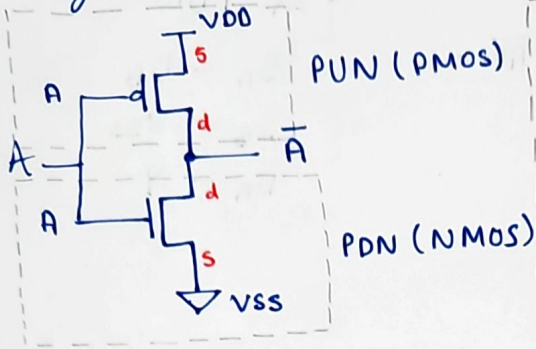
Note: We always take output from the point where the drains of NMOS & PMOS are connected together.

★ ~~Circuit~~ Stick Diagram.

Pdiff

$Y = \bar{A}$

N diff

② NAND Gate

★ Truth Table

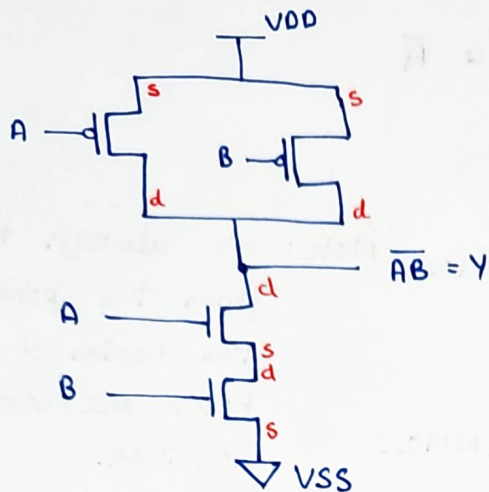| A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$Y = \overline{A \cdot B}$

→ as there is NAND operation present here we will put A & B in <u>series in PDN</u> and parallel in PUN
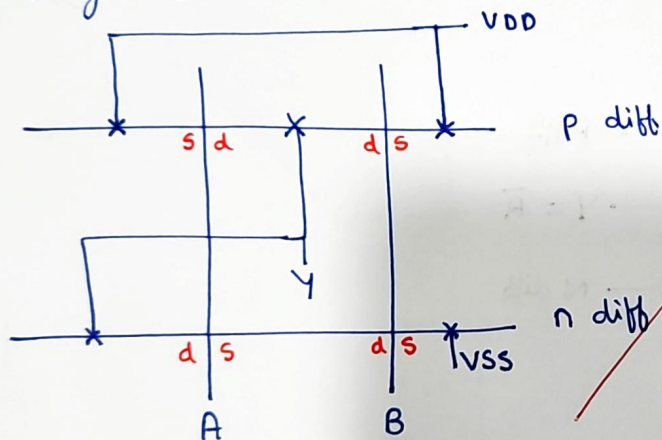
★ Circuit Diagram

★ Circuit Diagram.

- In PUN
  $S_A - S_B - V_{DD}$
  $D_A - D_B - Y$
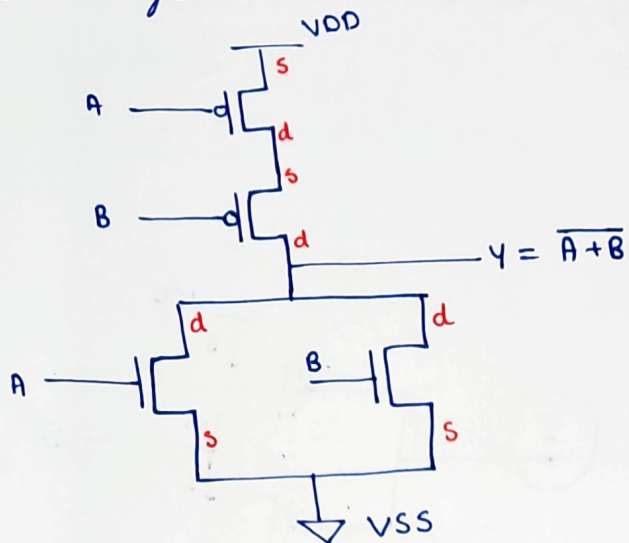
- In PDN
  $S_A - D_B$
  $S_B - V_{SS}$
  $D_A - Y$

$\overline{AB} = Y$

★ Stick Diagram

P. diff

n diff

③ NOR Gate

★ Truth Table.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$$Y = \overline{A + B}$$

↳ As here NOR operation is there so we will connect the nMOS in parallen in the PDN and pMOS in series in PUN
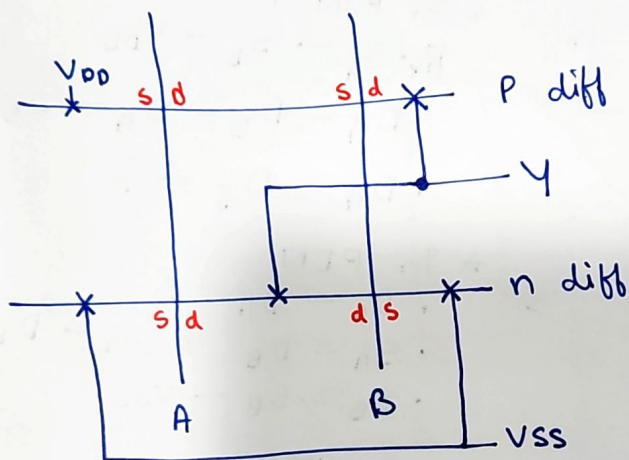
★ Circuit Diagram

$Y = \overline{A+B}$

In PUN:

$S_A - VDD$

$D_A - S_B$

$D_B - Y$

In PDN:

$D_A - D_B - Y$

$S_A - S_B - VSS$

★ Stick Diagram

④ Half Adder

★ Truth Table

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S =$

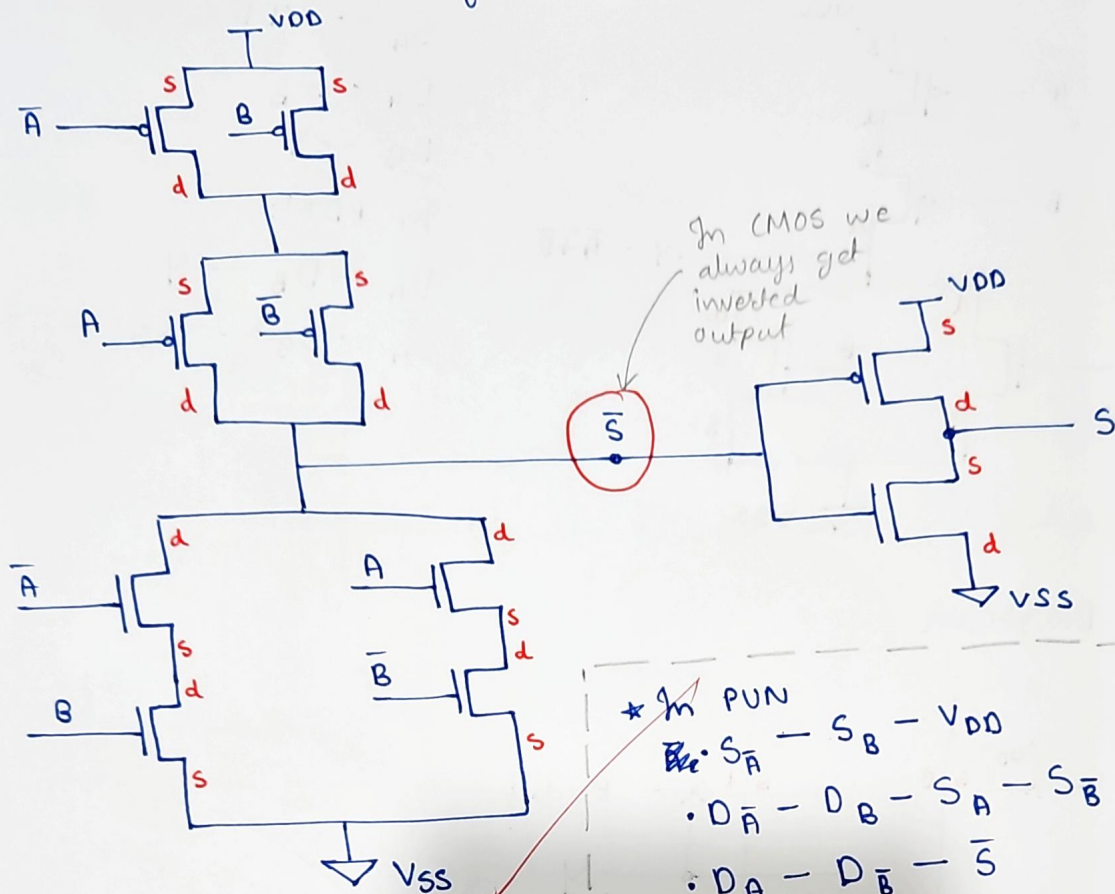$\therefore S = \overline{A}B + A\overline{B}$

$C =$
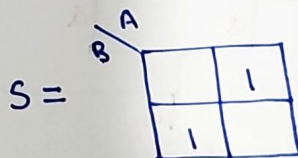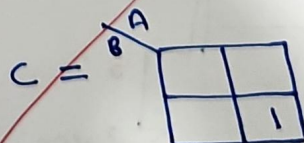
$\therefore C = AB$

As S and C are in SoP form we will first do ANDing then ORing i.e. A and $\overline{B}$, and $\overline{A}$ and B, will be in series in PDN
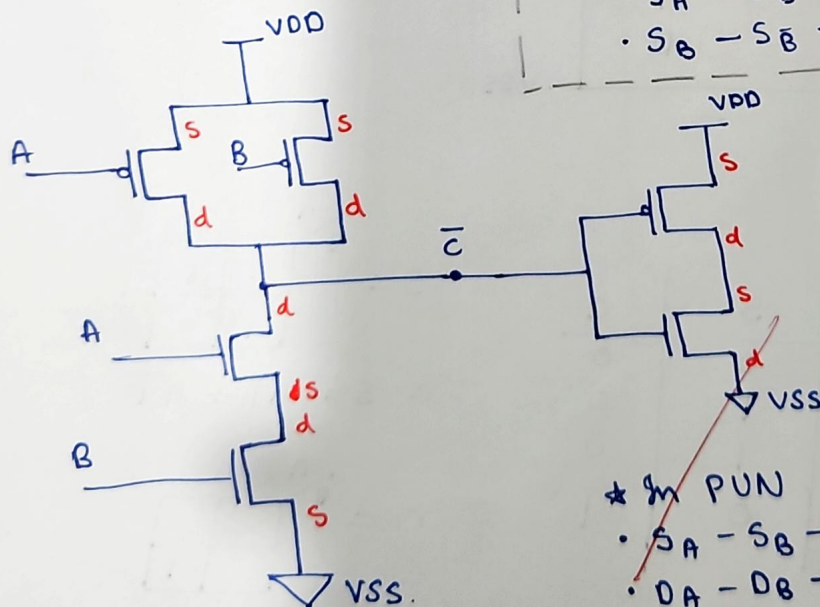
★ Circuit diagram — for Sum

In CMOS we always get inverted output

★ In PUN

Eu: $S_{\bar{A}} - S_B - V_{DD}$

$\cdot D_{\bar{A}} - D_B - S_A - S_{\bar{B}}$

$\cdot D_A - D_{\bar{B}} - \bar{S}$

★ In PDN

$\cdot D_{\bar{A}} - D_A - \bar{S}$

$\cdot S_{\bar{A}} - D_B \quad \& \quad S_A - D_{\bar{B}}$

$\cdot S_B - S_{\bar{B}} - V_{SS}$

✱ for Carry.

★ In PUN

$\cdot S_A - S_B - V_{DD}$

$\cdot D_A - D_B - \bar{C}$

★ In PDN

$\cdot D_A - \bar{C}$ $\cdot S_B - V_{SS}$

$\cdot S_A - D_B$

* Stick Diagram.
— Euler's Path.

For Sum

PDN
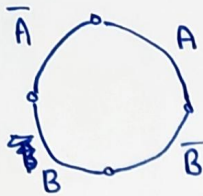
$\overline{A}\ B\ \overline{B}\ A$

PUN
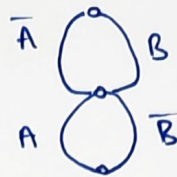
$\overline{A}\ B\ \overline{B}\ A$

→ This sequence is valid in both PUN & PDON.
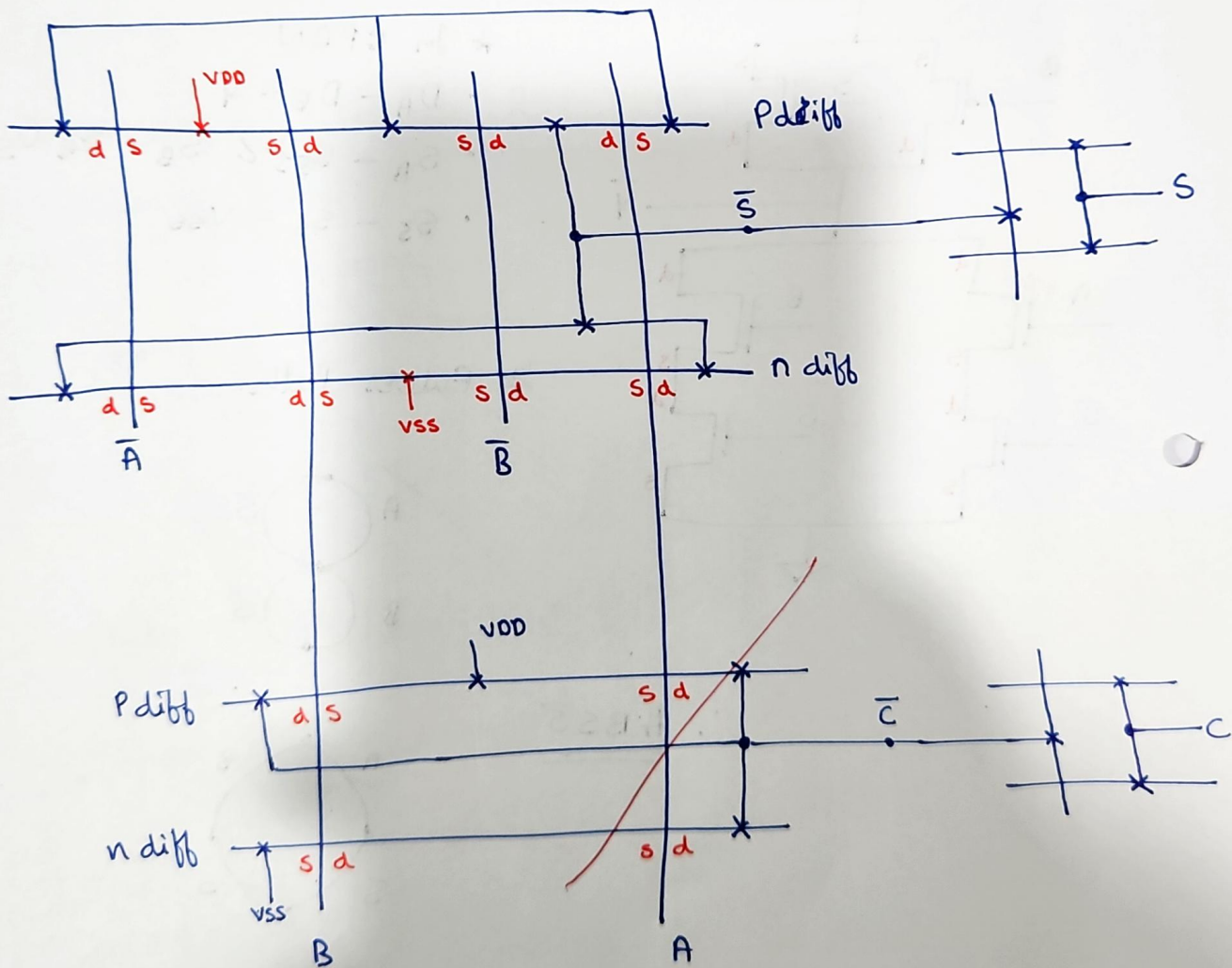
⑤ 2:1 Mux (CMOS)

☆ Truth Table

Input	S	Y
A	0	A
B	1	B

$$\therefore \quad Y = A.\bar{S} + B.S$$

☆ Circuit Diagram
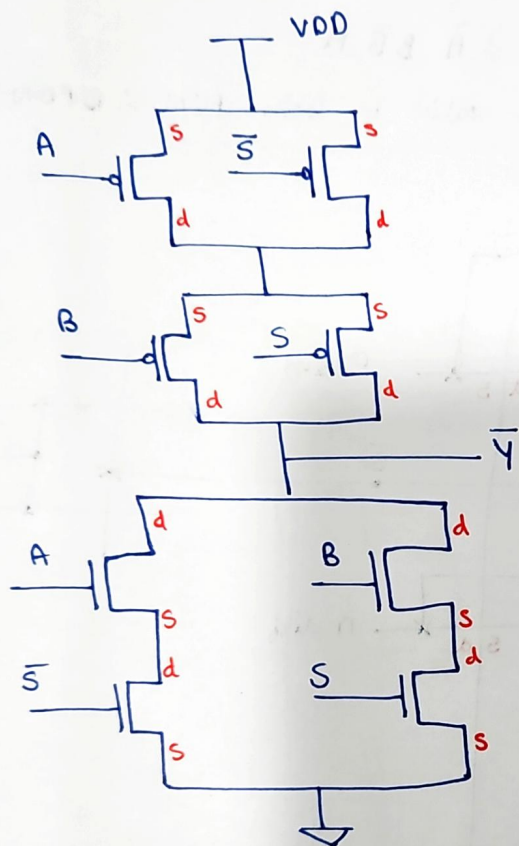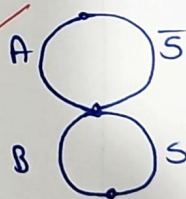

☆ In PUN
- $S_A - S_{\bar{S}} - V_{DD}$
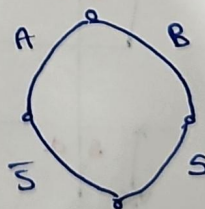- $D_A - D_{\bar{S}} - S_B - S_S$
- $D_B - D_S - \bar{Y}$

☆ In PDN
- $D_A - D_B - \bar{Y}$
- $S_A - \cancel{\text{of}} \ \& \ S_B - \cancel{\text{off}} \ D_S$
- $S_{\bar{S}} - S_S - V_{SS}$

☆ Eulers Path.

$$\therefore \ \underline{\underline{A \ B \ S \ \bar{S}}}$$

★ Stick Diagram

VDD

| s | d | s | d | d | s | d | s |

Y

| s | d | d | s | d | s | s | d |

VSS

A   B   S $\overline{S}$

Y

S

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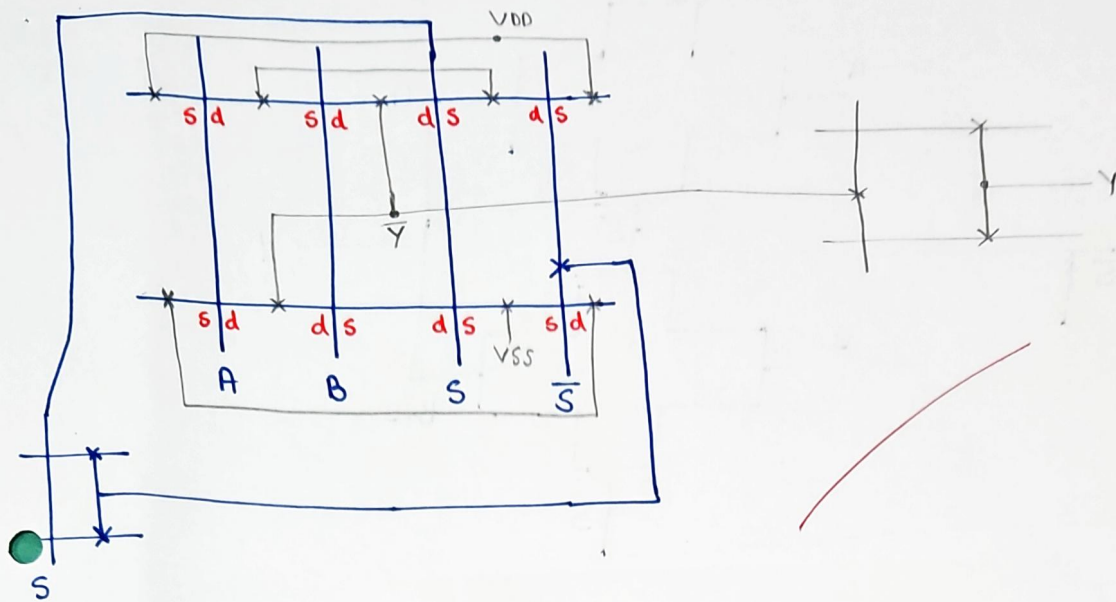
⑥ Transmission Gate & 2:1 Mux using TG

★ Circuit Diagram

g

S   d

I/P   O/P.

S   d

$\overline{g}$

★ Stick Diagram

g

P diff

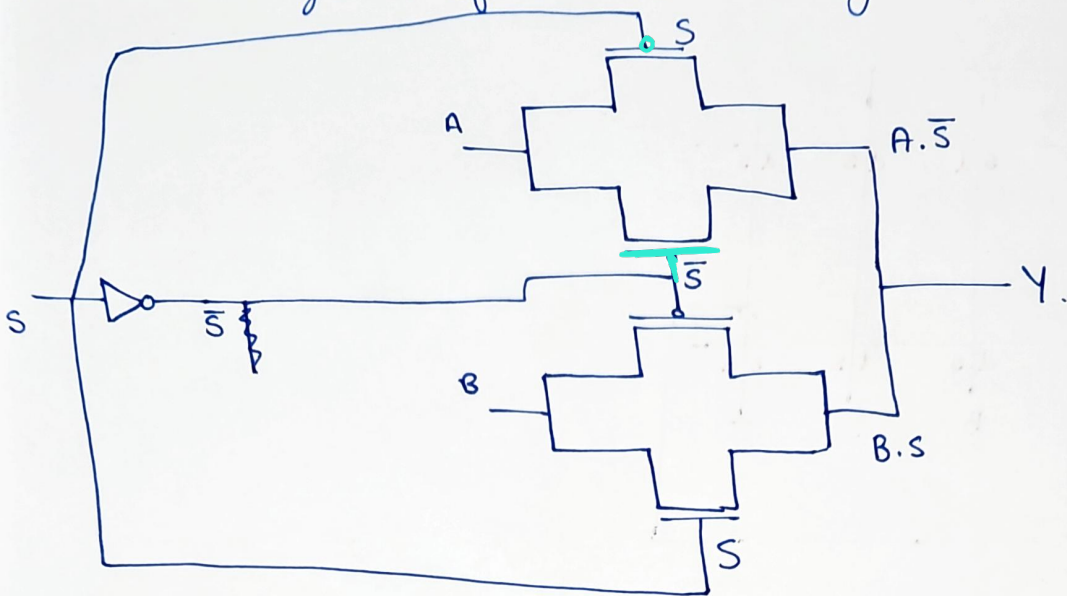clock   O/P

n diff

~g
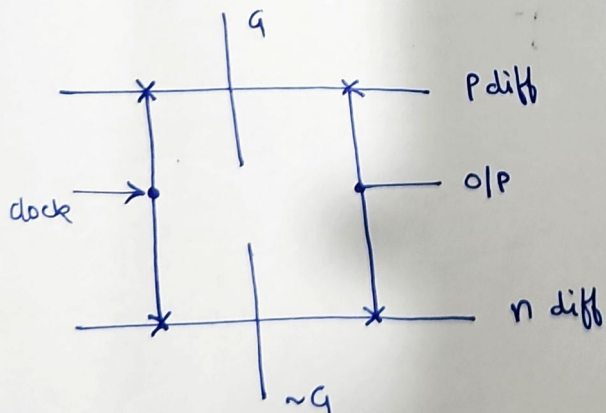
* Circuit Diagram of 2:1 Mux using TG.

* Stick diagram