Project 1
IITB-RISC

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Content

Instructions Encoding

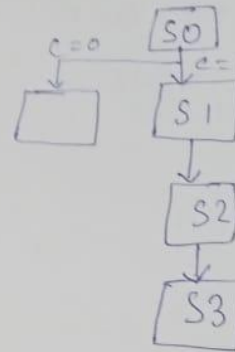|					
ADD:	00_01	RA	RB	RC	0	00
ADC:	00_01	RA	RB	RC	0	10
ADZ:	00_01	RA	RB	RC	0	01
ADL:	00_01	RA	RB	RC	0	11
ADI:	00_00	RA	RB	6 bit Immediate		
NDU:	00_10	RA	RB	RC	0	00
NDC:	00_10	RA	RB	RC	0	10
NDZ:	00_10	RA	RB	RC	0	01
LHI:	00_00	RA	9 bit Immediate			
LW:	01_11	RA	RB	6 bit Immediate		
SW:	01_01	RA	RB	6 bit Immediate		
LM:	11_00	RA	0 + 8 bits corresponding to Reg R0 to R7 (right to left)			
SM:	11_01	RA	0 + 8 bits corresponding to Reg R0 to R7 (right to left)			
BEQ:	10_00	RA	RB	6 bit Immediate		
JAL:	10_01	RA	9 bit Immediate offset			
JLR:	10_10	RA	RB	000_000		
JRI	10_11	RA	9 bit Immediate offset			

Note: Here we will consider op_code of LHI to be "00_11".

Instruction State Flow

7) NDC

S0
c=0 | c=1
[ ]   S1
      S2
      S3

8) NDZ

S0
z=0 | z=1
[ ]   S1
      S2
      S3

9) LHI

S0
S6

10) LW:

S0
S7
S2
S8

11) SW:

S0
S7
S2
S9

14) BEQ

S0
S1
S2
z=0 | z=1
[ ]   S10

15) JAL

```
┌─────┐
│ S11 │
└─────┘
   │
   ▼
┌─────┐
│ S12 │
└─────┘
```

16) JLR

```
┌─────┐
│ S11 │
└─────┘
   │
   ▼
┌─────┐
│ S13 │
└─────┘
```

17)
```
┌─────┐
│ SO  │
└─────┘
   │
   ▼
┌─────┐
│ S14 │
└─────┘
```
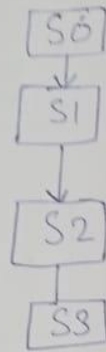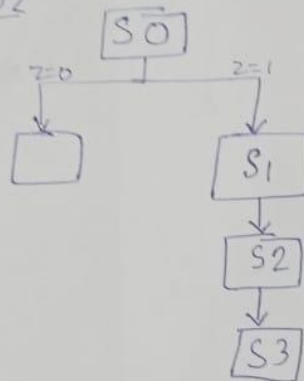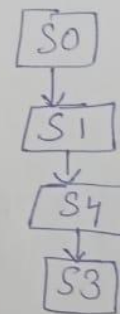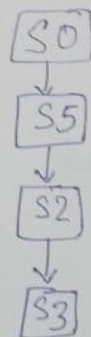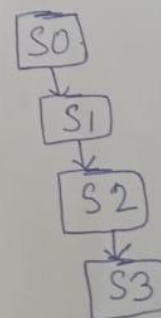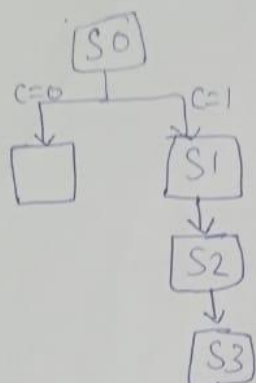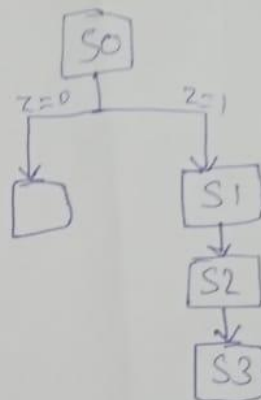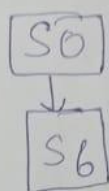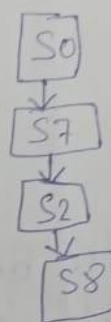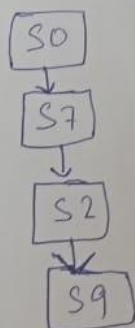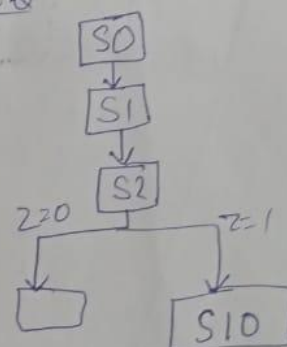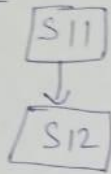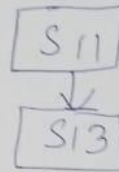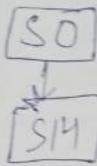
List of States

S0
$$PC \rightarrow mem(A), ALU\text{-}A$$
$$memD \rightarrow iR$$
$$0 + 1 \rightarrow ALU\text{-}B$$
$$ALUout \rightarrow PC$$

S1
$$iR_{1\text{-}9} \rightarrow RF\text{-}A1$$
$$iR_{8\text{-}6} \rightarrow RF\text{-}A2$$
$$RF\text{-}D_1 \rightarrow t_1$$
$$RF\text{-}D_2 \rightarrow t_2$$

S2
$$t_1 \rightarrow ALU\text{-}A$$
$$t_2 \rightarrow ALU\text{-}B$$
$$ALU\text{-}out \rightarrow t_3$$

S3
$$iR_{5\text{-}3} \rightarrow RF\text{-}A3$$
$$t_3 \rightarrow RF\text{-}D3$$

S4
$$t_1 \rightarrow aluA$$
$$t_2 \rightarrow \boxed{LS1} \rightarrow aluB$$
$$alu\text{-}out \rightarrow t_3$$

S5
$$iR_{11\text{-}9} \rightarrow RF A1$$
$$RF\text{-}D_1 \rightarrow t_1$$
$$iR_{50} \rightarrow \boxed{SE6} \rightarrow T_2$$

S6
$$iR_{8\text{-}0} \rightarrow \boxed{SE9\text{-}16} \rightarrow t_1$$
$$iR_{11\text{-}9} \rightarrow RF A3$$
$$t_1 \rightarrow RF\text{-}D3$$

S7
$$iR_{8\text{-}6} \rightarrow RF\text{-}A1$$
$$RF\text{-}D_1 \rightarrow t_1$$
$$iR_{5\text{-}0} \rightarrow \boxed{SE6} \rightarrow t_2$$

S8
$$t_3 \rightarrow mem A$$
$$mem\text{-}D \rightarrow RF\text{-}D3$$
$$IR_{11\text{-}9} \rightarrow RF\text{-}A3$$

S9
$$t_3 \rightarrow mem A$$
$$iR_{11\text{-}9} \rightarrow A1$$
$$RF\text{-}D_1 \rightarrow memD$$

S10
$$PC \rightarrow ALU\text{-}A$$
$$iR_{5\text{-}0} \rightarrow \boxed{SE6} \rightarrow ALUB$$
$$alu\text{-}out \rightarrow PC$$

S11
$$PC \rightarrow mem A, ALUA$$
$$memD \rightarrow iR$$
$$+1 \rightarrow ALUB$$
$$ALUout \rightarrow PC, t_3$$

S12

$t3 \rightarrow RF-D3$
$iR_{11-9} \rightarrow RF-A3$
$PC \rightarrow ALU$
$iR_{8-0} \rightarrow SE_9 \rightarrow ALUB$
$ALU\ out \rightarrow PC$

S13

$t3 \rightarrow RF\ D3$
$LR_{11-9} \rightarrow RFA3$
$iR_{8-6} \rightarrow RFA1$
$RF-D1 \rightarrow PC$

S14

800

$iR_{11-9} \rightarrow RF-A1$
$RF-D1 \rightarrow ALU-A$
$iR80 \rightarrow SE_9 \rightarrow ALUB$
$ALU\cdot out \rightarrow PC$

Data Path

Control Points

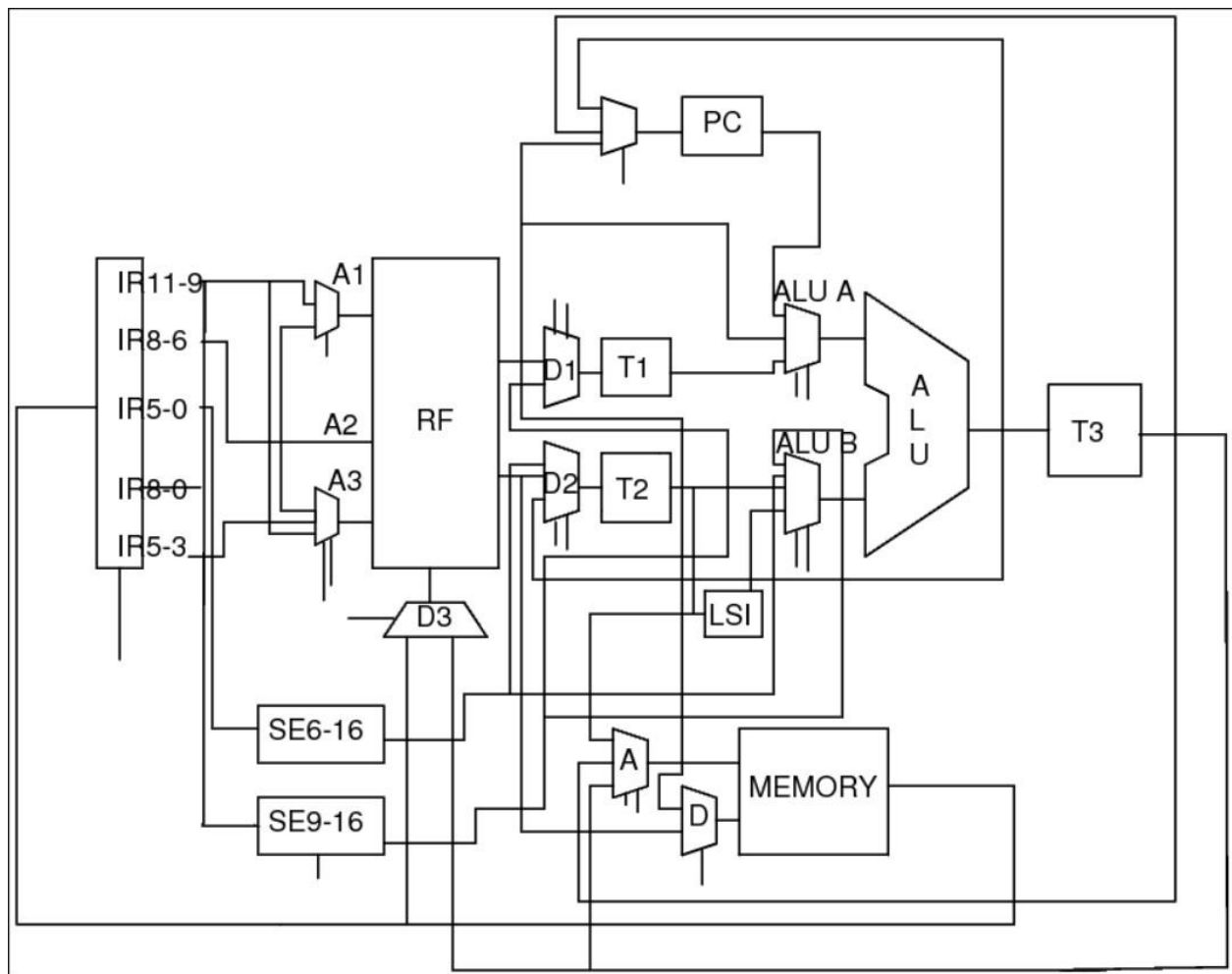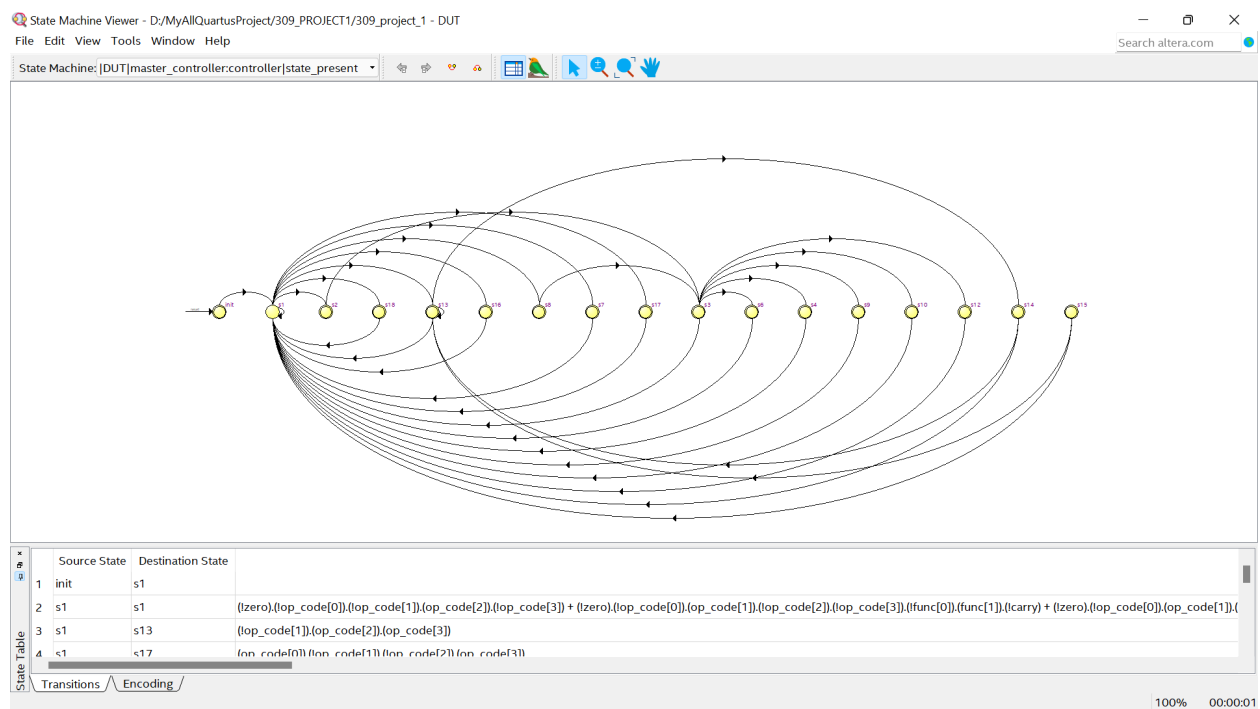| present st	state ID	IR_Wr	Memory		RF			ALU inv	PC-Wr	MUX A1	MUX A2	MUX A3		MUX T1	MUX T2		MUX D3		MUX PC	MUX ALU_A		MUX ALU_B		MX MEMD	MX MEMA		T1_Wr	T2_Wr	SET PE
			READ	WRITE	RF_A1	RF_A2	RF_A3					S1	S0		S1	S0	S1	S0		S1	S0	S1	S0		S1	S0			
sn	#00000																												
s0	#00001	1	1	0	0	0	0	1	1	X	X	X	X	X	X	X	X	X	1	1	0	0	0	X	1	0	0	0	0
s1	#00010	0	0	0	1	1	0	0	0	1	0	X	X	1	0	1	X	X	X	X	X	X	X	X	X	X	1	1	0
s2	#00011	0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	0	0	1	0	X	X	X	0	0	0
s3	#00100	0	0	0	0	0	1	0	0	X	X	0	1	X	X	X	0	1	X	X	X	X	X	X	X	X	0	0	0
s4	#00101																												
s5	#00110	0	0	0	0	0	1	0	0	X	X	1	0	X	X	X	1	0	X	X	X	X	X	X	X	X	0	0	0
s6	#00111	0	0	0	0	0	1	0	0	X	X	0	0	0	X	X	1	1	X	X	X	X	X	X	X	X	0	0	0
s7	#01000	0	0	0	1	0	0	0	0	0	X	X	X	1	1	0	X	X	X	X	X	X	X	X	X	X	1	1	0
s8	#01001	0	1	0	0	0	1	0	0	X	X	0	0	X	X	X	1	0	X	X	X	X	X	X	0	0	0	0	0
s9	#01010	0	0	1	1	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0	0	0
s10	#01011																												
s11	#01100	0	0	0	0	0	0	1	1	X	X	X	X	X	X	X	X	X	1	1	0	1	1	X	X	X	0	0	0
s12	#10000	0	0	0	1	0	1	0	1	0	X	0	0	X	X	X	1	0	0	X	X	X	X	X	X	X	0	0	0
s13	#10001	0	0	0	0	0	1	1	1	X	X	0	0	X	X	X	1	0	1	1	0	0	1	X	X	X	0	0	0
s14	#10010	0	0	0	1	0	0	1	1	1	X	X	X	X	X	X	X	X	1	1	0	0	1	X	X	X	0	0	0

Finite State Map

List of Components

- Program Counter
- Instruction Register
- Sign Extender of 9 bit
- Sign Extender of 6 bit
- Register Selector
- Memory
- Register File
- Temporary Register 1, 2, 3
- ALU
- Left Shifter

These files are added in the zip folder.