**BCA – Semester II**
**Question Bank**

**Multiple Choice Questions:**

***Unit – 1***

**1.** A gate is a logic circuit with one or more input signals but only _____ output signal.

**A. One** B. Two

C. Three D. None of these

**2.** The _____ gate has two or more input signals. All inputs must be high to get a high output.

**A. AND** B. OR

C. NAND D. NOR

**3.** Invert gate has only _____ input and _____ output.

A. Two, One B. One, Two

**C. One, One** D. None of these

**4.** An invert gate is also called a _____ gate.

A. NOR **B. NOT**

C. XNOR D. NAND

**5.** The OR gate has two or more input signals. If any input is _____, the output is high.

**A. High** B. Low

C. Both A and B D. None of these

**6.** The NAND gate has two or more input signals. If all inputs are _____, the output is low.

**A. High** B. Low

C. Both A and B D. None of these

**7.** The NOR gate has two or more input signals. If all inputs are _____, the output is high.

A. High **B. Low**

C. Both A and B D. None of these

**8.** The _____ gate has two or more input signals. All inputs must be same to get a low output.

A. NOR B. XNOR

C. NAND **D. XOR**

**9.** The _____ gate has two or more input signals. All inputs must be same to get a high output.

A. NOR **B. XNOR**

C. NAND D. XOR

**10.** De Morgan's first theorem says that a NOR gate is equivalent to a _____.

A. Bubbled OR B. Bubbled NOR

**C. Bubbled AND** D. Bubbled NAND

**11.** De Morgan's second theorem says that a NAND gate is equivalent to a _____.

**A. Bubbled OR** B. Bubbled NOR

C. Bubbled AND D. Bubbled NAND

**12.** A _____ is a combinational circuit that converts binary information from the "$2^n$" coded inputs to "n" outputs.

A. Half Adder B. Decoder

**C. Encoder** D. Comparator

**13.** A _____ is a combinational circuit that converts binary information from the "n" coded inputs to "$2^n$" unique outputs.

A. Half Adder **B. Decoder**

C. Encoder D. Comparator

**14.** In Comparator, _____ gate is use for comparing bits in word.

A. XOR B. AND

C. NOR D. XNOR

**15.** A combinational circuit that performs the arithmetic addition of two bits is called

A. Full Adder **B. Half Adder**

C. Binary Adder D. Decoder

**16.** A combinational circuit that performs the arithmetic addition of three bits is called

**A. Full Adder** B. Half Adder

C. Binary Adder D. Decoder

**17.** A _____ is logic circuit that can add two binary numbers.

A. Full Adder B. Half Adder

**C. Binary Adder** D. Decoder

**18.** In half adder XOR gate's output is _____

A. Carry **B. Sum**

C. Remainder D. None of these

**19.** In half adder AND gate's output is _____

**A. Carry** B. Sum

C. Remainder D. None of these

**20.** The Full Adder adds _____ digits at a time.

A. 1 B. 2

**C. 3** D. 4

## *Unit – 1 Long Questions*

**1.** What is logic gate? Draw electronic symbol and explain AND, OR, and NOT gates with truth table.

**2.** Explain NOR, NAND, XOR, and XNOR gates with truth table.

**3.** Explain Boolean Addition, Multiplication and Boolean Laws.

**4.** Explain rules of Boolean Algebra.

**5.** Explain Encoder with circuit and truth table

**6.** Explain Decoder with circuit and truth table

**7.** Explain Half – Adder and Full – Adder with circuit and truth table

**8.** Explain Binary Adders – Subtractor with circuit and truth table

### *Unit – 2*

**1.** The basic building block of sequential logic circuit is _____

**A. Flip-Flop** B. OR Gate

C. NAND Gate D. AND Gate

**2.** The truth table for an R-S Flip-Flop has how many VALID entries?

A. 1 B. 2

**C. 3** D. 4

**3.** In which of the following condition the RS Flip-Flop are unstable?

A. S = 0, R = 1 B. S = 1, R = 0

C. S = 0, R = 0 **D. S = 1, R = 1**

**4.** The RS Latch is an example of _____

A. Combinational circuit B. Synchronous sequential circuit

**C. One-bit memory element** D. One-clock delay element

**5.** RS flip-flop can be converted into D flip-flop if S is connected to R through _____.

A. OR Gate **B. AND Gate**

C. Inverters D. None of these

**6.** What is the one disadvantage of an RS Flip-Flop has _____

A. no Enable input **B. a RACE condition**

C. no clock input D. only single output

**7.** Which of the following condition a D Flip-Flop is said to be in a transparent condition?

A. Output is LOW B. Output is HIGH

C. Output follows clock **D. Output follows input**

**8.** The D flip-flop has _____ input.

**A. 1** B. 2

C. 3 D. 4

**9.** In D flip-flop, D stands for _____

A. Distant **B. Data**

C. Desired D. Delay

**10.** The D flip-flop has _____ output/outputs.

A. 1 **B. 2**

C. 3 D. 4

**11.** In D flip-flop, if clock input is LOW, the D input _____

**A. Don't Care** B. High

C. Low D. Not Change

**12.** The length of a register is called _____

A. Word limit **B. Word size**

C. Register limit D. Register size

**13.** A register that is used to store binary information is called _____

A. Data Register **B. Binary Register**

C. Shift Register D. None of these

**14.** A register capable of shifting its binary information either to the right or the left is called a _____.

A. Parallel Register B. Serial Register

**C. Shift Register** D. Storage Register

**15.** Generally, _____ is used to construct shift registers.

**A. D Flip-Flop** B. Half Adder

C. Full Adder D. RS Flip-Flop

**16.** The number of Flip-Flops required to construct 8-bit shift register will be _____.

A. 4 **B. 8**

C. 16 D. 32

## *Unit – 2 Long Questions*

**1.** Explain what is Latch and Flip-Flop and also differentiate them.

**2.** Explain RS Flip-Flop with diagram.

**3.** Explain D Flip-Flop with diagram.

**4.** What is register? Explain buffer and controlled buffer register with diagram.

**5.** Explain Left-Shift and Right-Shift register with diagram.