Project 3

ADC, DMA and DSP

ECEN 5813, Spring 2019

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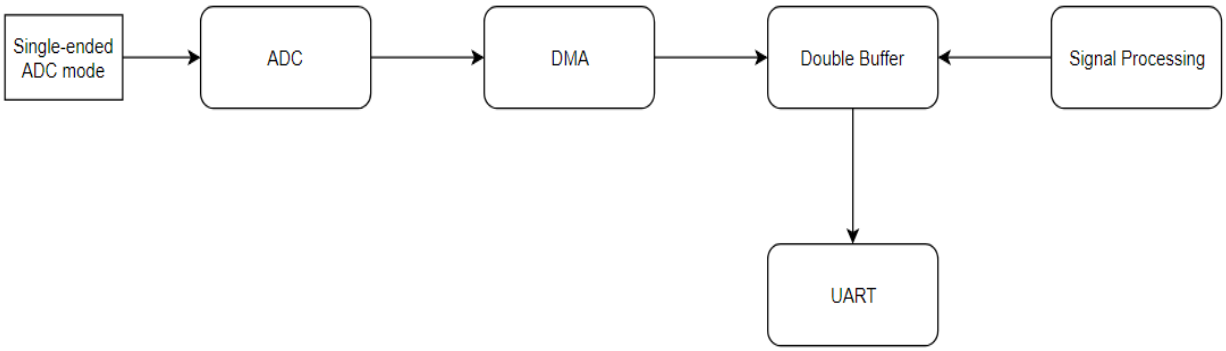
Part 1: Block diagram



BLOCK DIAGRAM

Part 2: ADC setup

Questions

1. What is the behavior of the system when no input signal is applied?

Ans: The system will consider the noise at the pin as the single ended input. The ADC value of the noise ranges between 28000 to 32000.

Part 3: DMA setup

Questions

1. What source and destination DMA read and write size did you choose and why?

Ans: The source and destination DMA read and write size chosen is 2 bytes. We give the size of a buffer element as uint16_t and the resolution of the ADC implemented is of 16 bits. Hence we choose the DMA read and write size as 16 bits (2 byte).

Part 4: Double buffer

One of the two buffers will be used by the DMA process and the other by your application or interrupt service routine which will process the data. The double-buffered implementation is to divide the buffer in half and establish some signaling to swap buffers. We configured the DMA controller to generate an interrupt when half the buffer is filled and reconfigure to generate another interrupt when the other half has been filled repeatedly. We then toggle a LED in the ISR and monitor with an oscilloscope to verify expected frequency and consistency of the interrupt service.

Part 5: Application

Questions

1. What effect does changing the buffer size have on system processing efficiency?

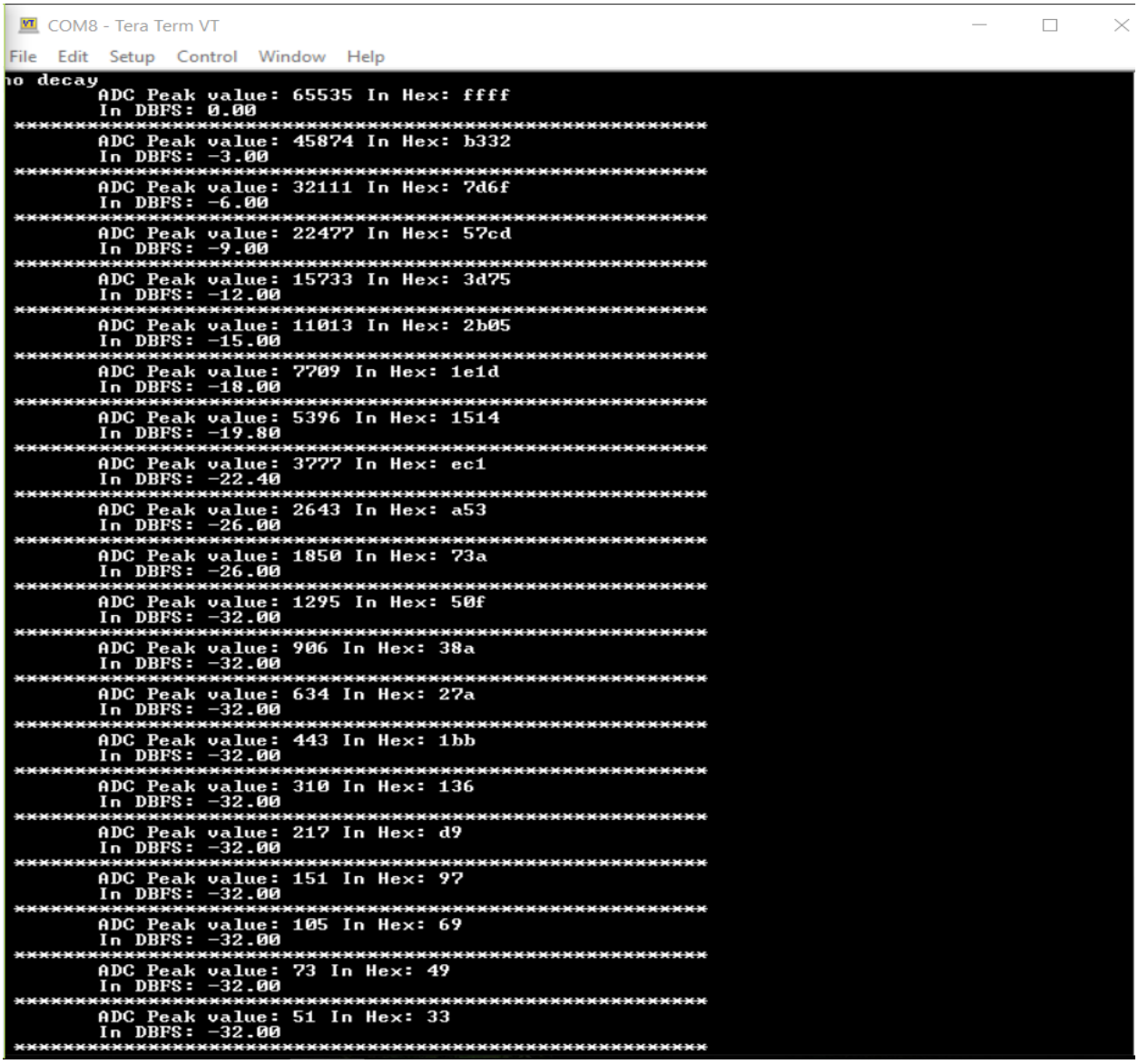
Ans: Changing the buffer size will cause the DMA interrupt to occur accordingly. If we are to decrease the buffer length, the interval between two interrupts will increase causing the IRQ handler to run over the main loop. On the other side, if we increase the buffer length, the interrupts will occur at a larger interval.

2. What other effect(s) does changing the buffer size have on the system?

Ans: There can be a system where the interrupts occur at a very high rate due to a small buffer causing the interrupt handler to fire in between resulting in hindrance in the main loop. This can cause loss of data or getting improper data in the system. If the buffer size is large, then the system will have more time to run the main loop.

Extra credit

Performed a logarithmic calculation of the raw 16-bit ADC data using a lookup table to report signal levels in dBFS units.



APPENDIX:

This report has comprehensively covered all the modules , functions , their description, the different modes implemented in UART and answers to relevant questions. This project covers implementation of 16 bit ADC in single ended mode. The ADC configuration includes selection of proper clock and bits in the ADC register to run it at more than 8 KHz sampling frequency. During the initial phase of the project the ADC reading was obtained using adc_read function to check whether the ADC is properly configured or not. The next step was to configure the ADC to enable the DMA request. The output of the ADC module is directly transferred to the buffer using DMA. The DMA configuration includes clocks, selecting the source and destination registers and selecting DMA write sizes. The data that is written using DMA is of type uint16_t. The DMA byte counter is set to 128 bytes. Hence, the interrupt will be generated after 128 bytes of data write. A double buffer has also been implemented where at a given time a part of the buffer will be used by the processor and a part by the DMA to load the ADC data. The buffer data is processed to calculate peak, logarithmic values and displayed on the terminal using UART.