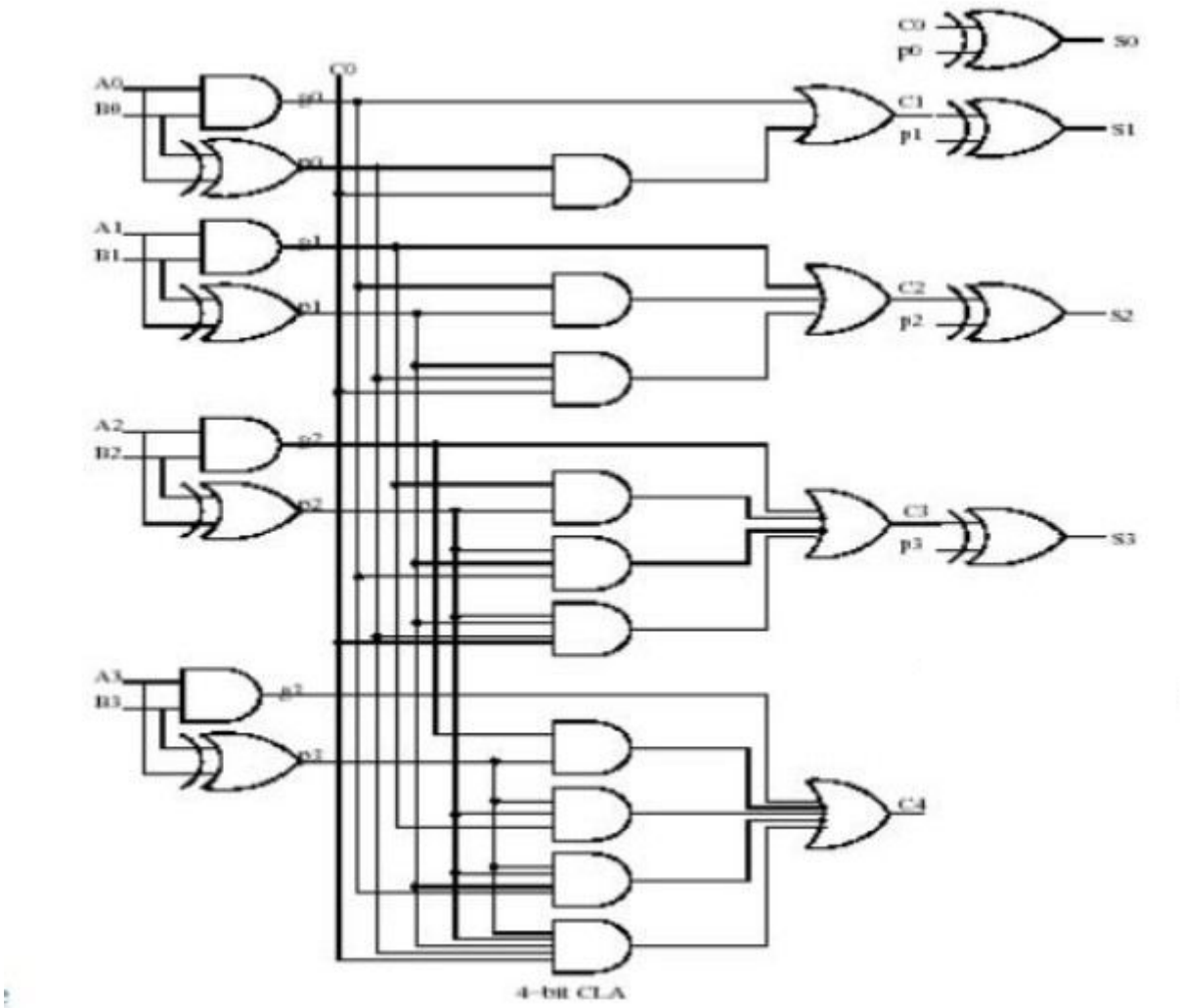
Course Project
VLSI Design

Ayush Kumar Lall – 2020122001

< SECTION 1 > The proposed structure of the adder is based on carry look ahead implementation. In this I have included blocks of D flip flops, propagation and generate block, carry block and adder block.
Initially values that are supposed to be added are loaded in the D flip flops. Since it is addition of 4 bits i.e. first no. Is given as A= A3 A2 A1 A0 and second no. Is given as B = B3 B2 B1 B0. So total of 8 D flip flops will be required to load these values and then there is also an input carry which will also require one D flip flop, to at starting total of 9 D flip flops were used. These values are then passed to the propagate and generate block, such that $P_i = A_i \oplus B_i$ will generate propagated value and $G_i = A_i . B_i$ will give 'generate output. After propagate and generate value were recieved, these were then passed to the carry block which will give output as **Carry = Gi + Pi . Ci** . After we get the carry value, we pass it to the adder block which will generate sum of the values, given by the expression **Sum = Pi ⊕ Ci .**

Structure:

As discussed above I have implemented the CLA adder, whose schematic diagram can be seen as below. So we can see how the input A and B are giving propagate and generate values, which are then used for generating carry values, which finally help us to get the final sum values.



Advantages of CLA :-

- CLA Adders generate the carry-in for each full adder simultaneously, by using simplified equations involving Pi, Gi, and Cin.

- This system reduces the propagation delay. This is because the output carry at any stage is dependent only on the first Carry signal given at the input.

- It is the fastest adder when compared to other addition mechanisms.

Disadvantages of CLA:-

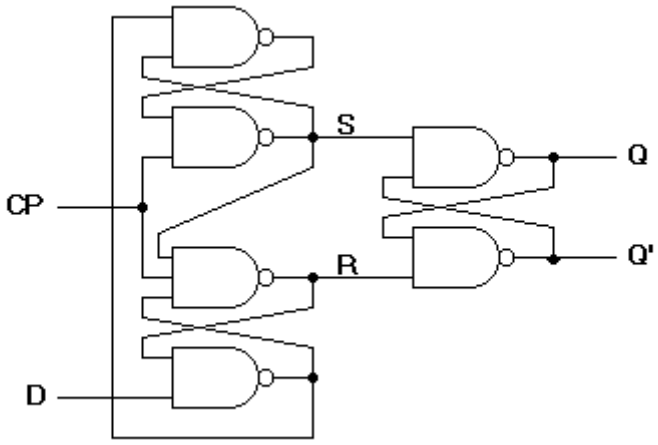
- The carry-lookahead adder circuit gets more complicated as the number of variables increase.

- The circuit for a carry-lookahead adder is expensive as it involves more hardware.

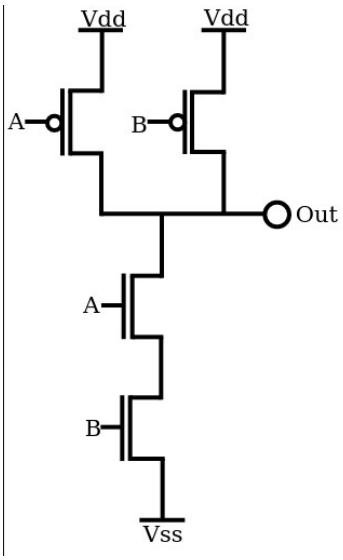
- As the number of variables increases, the circuit implements more hardware. Thus, when the carry-lookahead adder is implemented as an IC, the area is bound to increase.

< SECTION 2 > Based on the above information, I implemented the CLA adder with the required D flip flops and other components.

1st component is D flip flop, whose implementation is as given below:



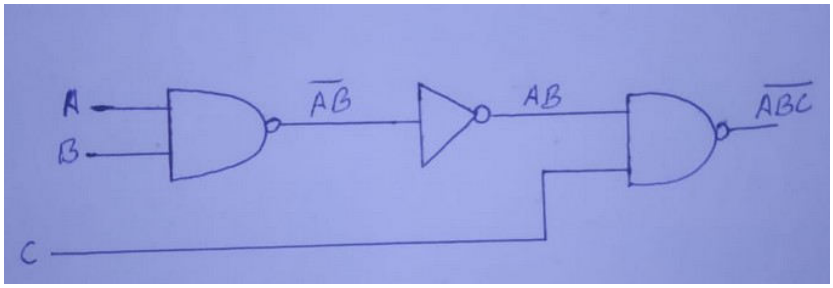
So this the schematic diagram of the positive edge triggered D flip flop that I have used for my implementation. In this when the clock pulse input exceeds a specific threshold level, the inputs are locked out and the flip-flop is not affected by further changes in the inputs until the clock pulse returns to 0 and another pulse occurs.
It can be observed that for the implementation of this nand gates are being used. Whose transister level structure can be observed as :



So, in this taking care of the logical effort the sizes of the NMOS and PMOS were taken as same i.e. of 40 λ each.

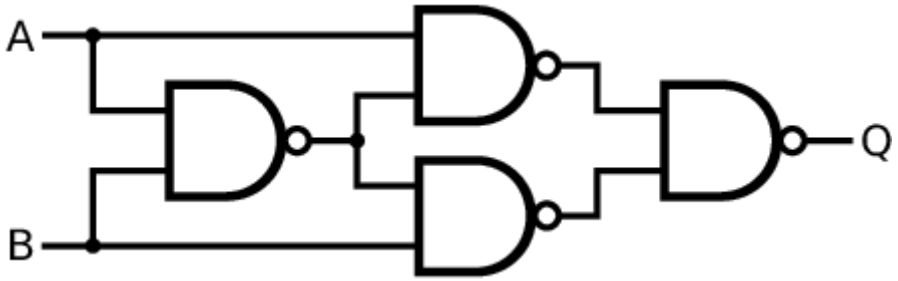
This nand gate is used for the implementation of the D flip flop and keeping the sizes same.

It can be observe that there is also one 3 input nand gate, for which I implemented it using 2 input nand gates and a inverter whose schematic is as given below:



So we can see the 3 input nand gate implementation using 2 input nand gates and an inverter. The size of inverter is choosen keeping in mind value of logical effort that is 1. So, the size of the inverter used is 3.6λ for the PMOS and 1.8λ for the NMOS.

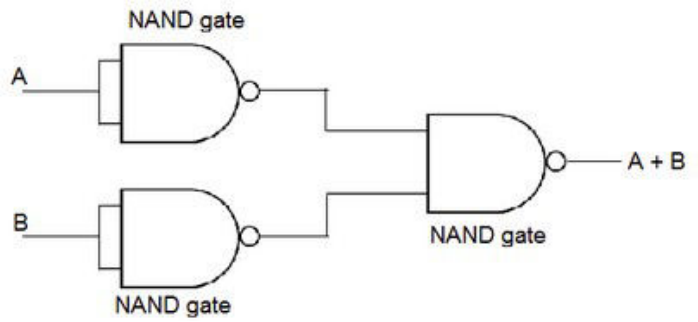
2nd component is propagate and generate block, which are composed of XOR and AND gates respectively. For the implementation of the XOR and AND gates I have used NAND gates only. The schematic for the implementation of XOR gate is as follows:



Here also the size of NAND gates are kept same only, i.e. 40 λ each.
While, for the implementation of the AND gate I kept an inverter infornt of the NAND gate, where the size of the NAND and inverter is same as discussed above.

3rd component is Carry block whose operation is given as

Carry = Gi + Pi . Ci**,** so for this we need AND gate and OR gate. The AND gate implemntation is as discussed above and for the case of OR gate, I have implemented this also using NAND gate and inverter, for general understanding we can see the schematic given below:



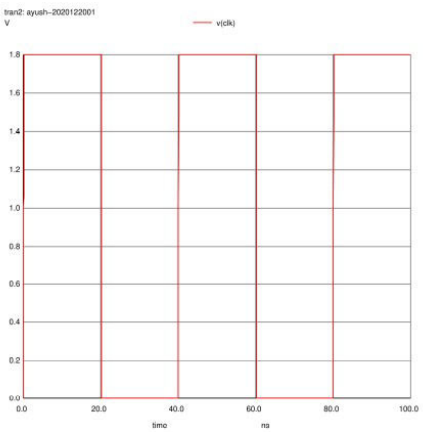
Where I have directly used inverter instead of connecting two inputs of the NAND gates, to make the output inverted.

4th component is adder block. Now, after we got the carry values and propagate values, we can find the corresponding sum values, for which we can use XOR gates, whose implementation is same as discussed above.

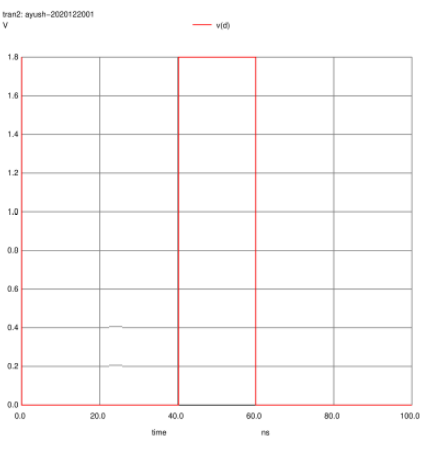
< SECTION 3 > Lets look at the simulation of each of the block.

So, for the D flip flop, the output should give the same value as the supplied input at every positive edge of the clock and if the input changes its value in negetive edge clock then the output will hold the previous value. So below are the simulation results:

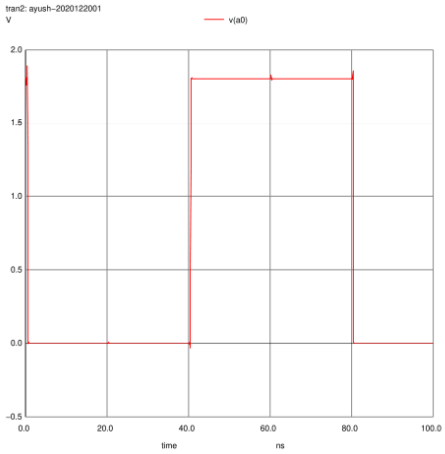
CLOCK



INPUT



OUTPUT



Above we can see the given clock pulses, the input to the D flip flop and the corresponding output. It can be observed that the input at 40ns is transiting to high value which is about 1.8v and at that corresponding time instance we can see that clock pulse is having its positive edge, so the value should reflect at the output, and we can observe the same happening. Now, at time 60ns the input is transiting to low value but the clock pulse is not having its positive edge at that time instance, so the output holds its previous value. At 80ns we can see that clock is having its positive edge and input is having low value at that point, so at time 80ns the output will also reflect this and its value will go down to low value.

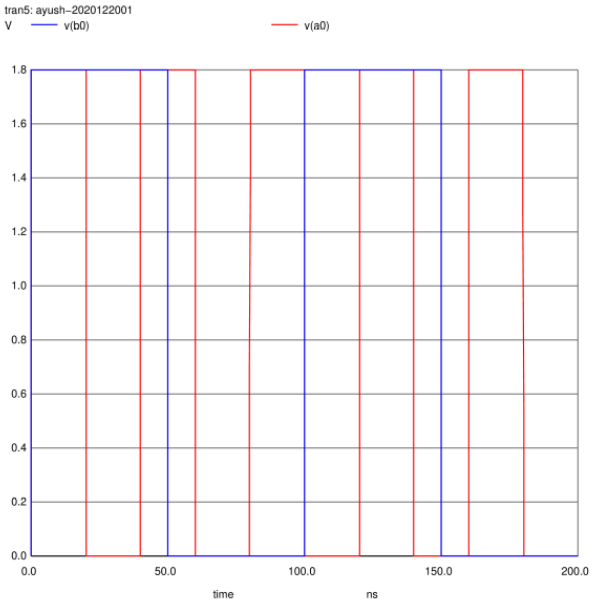
The netlist for this D flip flop is :

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param w = {20*LAMBDA}
.param width_P={2*w}
.param width_N={2*w}
.global gnd vdd

Vdd     vdd     gnd     'SUPPLY'
vin1 D 0 pulse 1.8 0 0n 100p 100p 40.04n 60n
vin2 clk 0 pulse 0 1.8 .044n 100p 100p 20n 40n


.subckt nand A B out vdd gnd
M1      out       A       k     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2      out       A       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3      k       B       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4      out       B       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends nand


.subckt three_nand A B C out vdd gnd
M1      out       A       k     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2      out       A       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3      k       B       p     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4      out       B       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M5      p       C       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M6      out       C       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends three_nand

.subckt inv yi xi vdd gnd
M1      yi      xi      gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2      yi      xi      vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv


x1 ox4 A0_bar A0 vdd gnd nand
x2 ox5 A0 A0_bar vdd gnd nand
x3 ox6 ox4 ox3 vdd gnd nand
x4 ox3 clk ox4 vdd gnd nand
x7 ox4 clk ox7 vdd gnd nand
x8 ox8 ox7 vdd gnd inv
x5 ox8 ox6 ox5 vdd gnd nand
x6 D ox5 ox6 vdd gnd nand


*x5 ox4 ox6 clk ox5 vdd gnd three_nand

.tran 0.1n 100n

.control
set hcopypscolor = 1
set color0=white
set color1=black

run
set curplottitle="Ayush-2020122001"

*plot v(s_bar)
plot v(clk)
plot v(D)
plot v(A0)
set hcopypscolor = 1
*hardcopy DFF_input.eps v(D)
*hardcopy DFF_clock.eps v(clk)
*hardcopy DFF_output.eps v(A0)
.endc
```

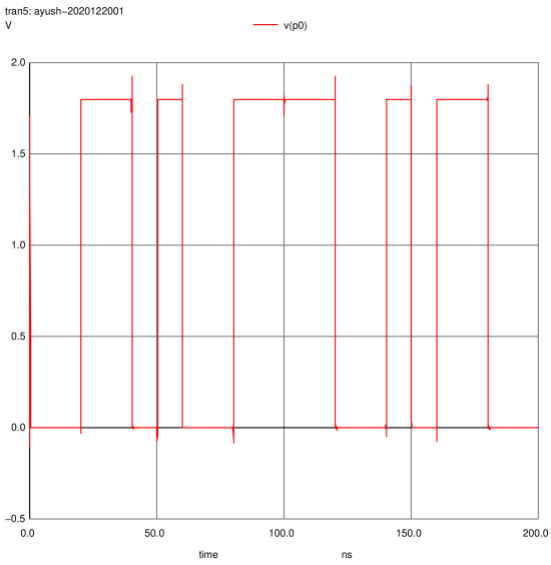
After the D flip flop we have propagate and generate block which will give result same as xor gate for the propagate values and generate will give values same as that of the AND gate.

So the propagate simulation result will give value as:

INPUT



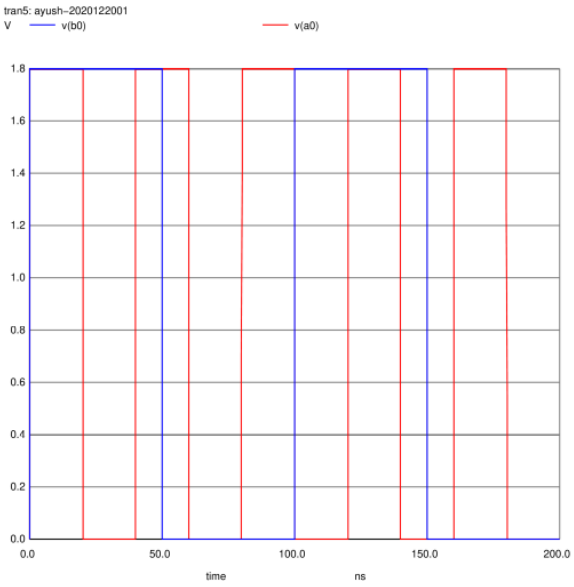
PROPAGATE OUTPUT



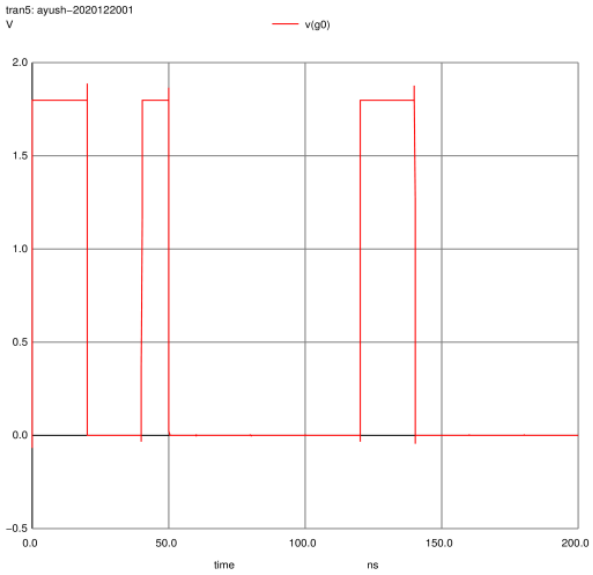
So we can see that for the input A0 and B0 we are getting corresponding propagate value, which reassembles XOR gate value and we can observe that whenever both A0 and B0 are having same value then the propagate will result into low value and when A0 and B0 are complement of eachother, then we will see high value for the propagate.

For generate we should get output similar to that of the AND gate output. So the simulation result is as follows:-

INPUT



GENERATE OUTPUT



So we can see how the generate output is given result simular to that of the AND gate, so whenever the input value A0 and B0 are high, we will get high value at the output also, for rest of the cases we will get low value.

NETLIST for propagate and generate block is as follows:

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param w = {20*LAMBDA}
.param width_P={2*w}
.param width_N={2*w}
.param width_P_i = (LAMBDA*50)
.param width_N_i = (LAMBDA*20)
.global gnd vdd

Vdd     vdd     gnd     'SUPPLY'

vin1 A0 0 pulse 0 1.8 0n 100p 100p 19.9n 40n
vin2 A1 0 pulse 0 1.8 0n 100p 100p 19.9n 40n
vin3 A2 0 pulse 0 1.8 0n 100p 100p 19.9n 40n
vin4 A3 0 pulse 0 1.8 0n 100p 100p 19.9n 40n

vin5 B0 0 pulse 0 1.8 0n 100p 100p 49.9n 100n
vin6 B1 0 pulse 0 1.8 0n 100p 100p 49.9n 100n
vin7 B2 0 pulse 0 1.8 0n 100p 100p 49.9n 100n
vin8 B3 0 pulse 0 1.8 0n 100p 100p 49.9n 100n


.subckt nand A B out vdd gnd
M1      out       A       k       gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2      out       A       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3      k       B       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4      out       B       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends nand

.subckt inv yi xi vdd gnd
M1      yi       xi       gnd     gnd  CMOSN   W={width_N_i}   L={2*LAMBDA}
+ AS={5*width_N_i*LAMBDA} PS={10*LAMBDA+2*width_N_i} AD={5*width_N_i*LAMBDA}
  PD={10*LAMBDA+2*width_N}
M2      yi       xi       vdd     vdd  CMOSP   W={width_P_i}   L={2*LAMBDA}
+ AS={5*width_P_i*LAMBDA} PS={10*LAMBDA+2*width_P_i} AD={5*width_P_i*LAMBDA}
  PD={10*LAMBDA+2*width_P_i}
.ends inv

```

```

**********XOR gate******************
.subckt xor dma dmb outx vdd gnd
xx1 dma dmb outx1 vdd gnd nand
xx2 dma outx1 outx2 vdd gnd nand
xx3 dmb outx1 outx3 vdd gnd nand
xx4 outx2 outx3 outx vdd gnd nand
.ends xor

**************AND GATE******************
.subckt and_g in1 in2 aout vdd gnd
xx5 in1 in2 out_nan vdd gnd nand
xx6 aout out_nan  vdd gnd inv
.ends and_g

****************OR GATE*****************
.subckt or_g inn1 inn2 orout vdd gnd
xx7 ou1 inn1 vdd gnd inv
xx8 ou2 inn2 vdd gnd inv
xx9 ou1 ou2 orout vdd gnd nand
.ends or_g


**********************Generate**********************

x140 A0 B0   g0 vdd gnd and_g
x141 A1 B1  g1 vdd gnd and_g
x142 A2 B2  g2 vdd gnd and_g
x143 A3 B3  g3 vdd gnd and_g

**********************Propagate**********************
x144 A0   B0   p0 vdd gnd xor
x145 A1  B1  p1 vdd gnd xor
x146 A2  B2  p2 vdd gnd xor
x147 A3  B3  p3 vdd gnd xor


.tran 0.1n 200n

.control
set hcopypscolor = 1
set color0=white
set color1=black

run
set curplottitle="Ayush-2020122001"

*plot v(s_bar)
*plot v(clk)
plot v(A0) v(B0)
plot v(p0)
```

After we get the propagate and generate values, we will use them for finding the carry values which is given by the equation **Carry = Gi + Pi . Ci s**o it can be observed that for generating carry we will require both AND gate and OR gate. On expanding the carry we will get the following equations:

C1 = **(C_{in} . P0)** + **G0**

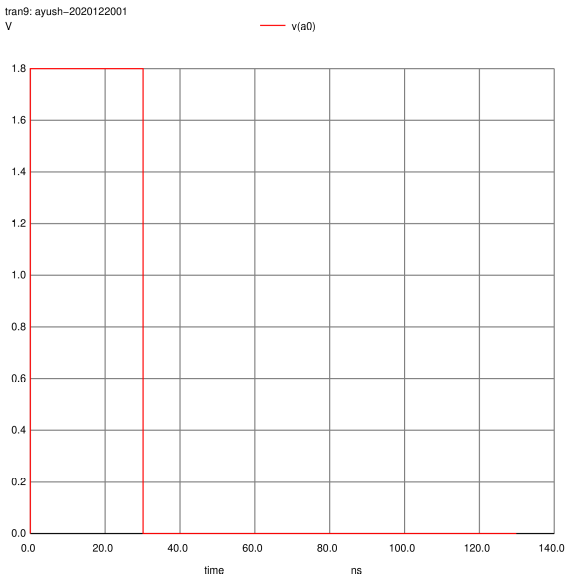
C2 = (**C_{in} . P0 . P1)** + **(G0 . P1)** + **G1**

C3 = **G2 + (P2 . G1) + (P2 . P1 . G0) + (P2 . P1 . P0 . C_{in})**

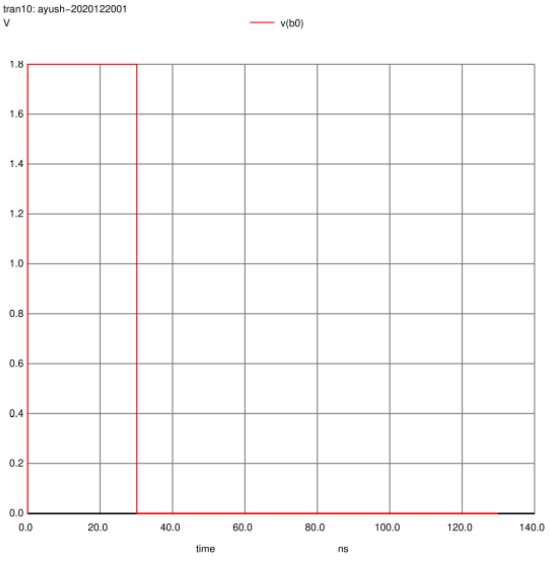
C4 = (**C_{in} . P0 . P1 . P2 . P3**) + (**P3 . P2 . P1 . G0**) + (**P3 . P2 .G1**)
+ (**G2 . P3**) + **G3**

So we can see that in CLA adder we dont have to wait for the carry to generate in order to generate the next carry. All the carry can be generated from the single input carry. Also as we start calculating the values of the carry we will observe that complexity of the carry generation will increase. The simulation result of the carry is as follows:

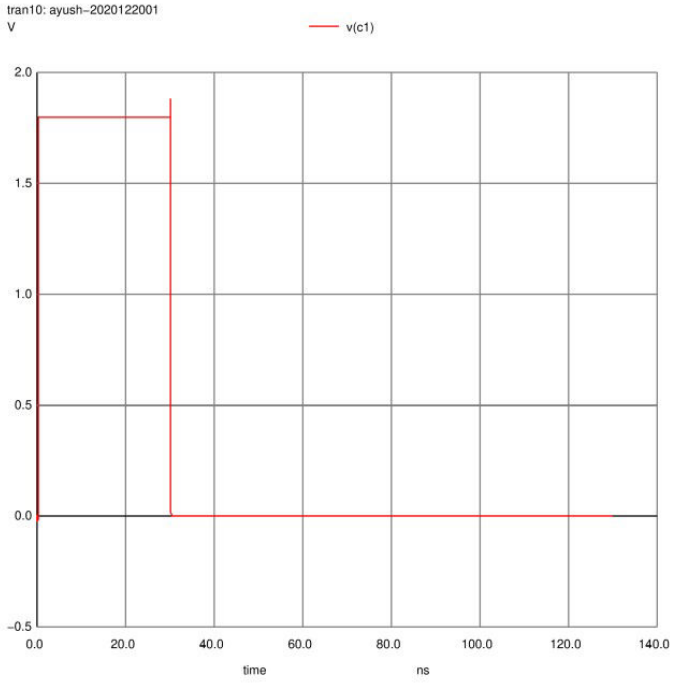
INPUT A0



INPUT B0



OUTPUT CARRY



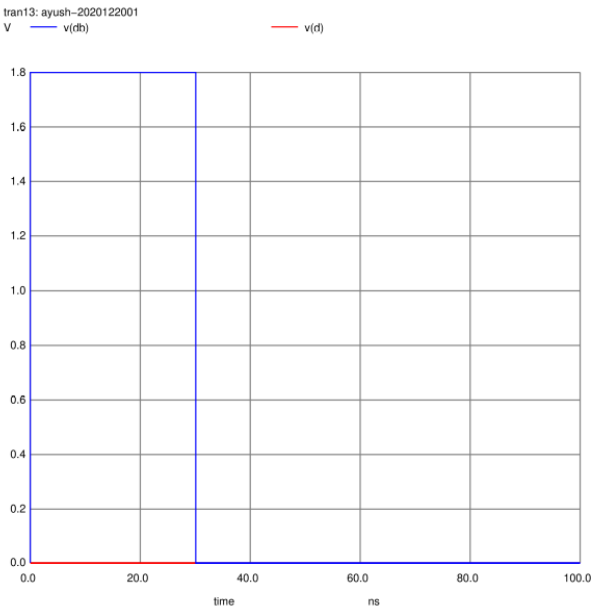
So we can observe that when the input A0 and B0 both are of High bit, we will get high value for carry also. For more analysis we can refer **Carry = Gi + Pi . Ci** So in this case Gi will give high output as both A0 and B0 are high and Gi behave same as that of AND gate while Pi.Ci will result in Low value as Pi behave as XOR gate and so the it will give low value as both A0 and B0 are high. Hence overall the carry will be of high value.
Thus we can see that the carry is working as expected. We can give a look at the corresponding NETLIST for this below :-

NETLIST for carry block

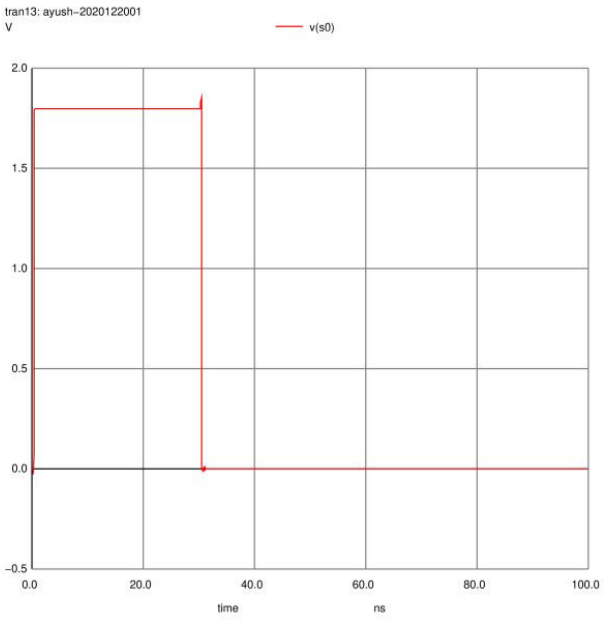
```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param w = {20*LAMBDA}
.param width_P={2*w}
.param width_N={2*w}
.global gnd vdd

Vdd     vdd     gnd     'SUPPLY'


vin1 A0 0 pulse 0 1.8 0n 10p 10p 30n 500n
vin6 A1 0 pulse 0 1.8 0n 10p 10p 30n 500n
vin7 A2 0 pulse 0 0 0n 10p 10p 30n 500n
vin8 A3 0 pulse 0 1.8 0n 10p 10p 30n 500n


vin9 B0 0 pulse 0 1.8 0n 10p 10p 30n 500n
vin10 B1 0 pulse 0 0 0n 10p 10p 30n 500n
vin11 B2 0 pulse 0 1.8 0n 10p 10p 30n 500n
vin12 B3 0 pulse 0 1.8 0n 10p 10p 30n 500n

vin_carry car0 0 0


.subckt nand A B out vdd gnd
M1      out       A       k     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2      out       A       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3      k       B       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4      out       B       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends nand

.subckt inv yi xi vdd gnd
M1      yi       xi       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2      yi       xi       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv


**********XOR gate******************
.subckt xor dda ddb outx vdd gnd
xx1 dda ddb outx1 vdd gnd nand
xx2 dda outx1 outx2 vdd gnd nand
xx3 ddb outx1 outx3 vdd gnd nand
xx4 outx2 outx3 outx vdd gnd nand
.ends xor

**************AND GATE******************
.subckt and_g in1 in2 aout vdd gnd
xx5 in1 in2 out_nan vdd gnd nand
xx6 aout out_nan  vdd gnd inv
.ends and_g

*****************OR GATE*****************
.subckt or_g inn1 inn2 orout vdd gnd
xx7 ou1 inn1 vdd gnd inv
xx8 ou2 inn2 vdd gnd inv
xx9 ou1 ou2 orout vdd gnd nand
.ends or_g


**********************Generate**********************

x140 A0 B0   g0 vdd gnd and_g
x141 A1 B1  g1 vdd gnd and_g
x142 A2 B2  g2 vdd gnd and_g
x143 A3 B3  g3 vdd gnd and_g

**********************Propagate**********************
x144 A0   B0   p0 vdd gnd xor
x145 A1  B1  p1 vdd gnd xor
x146 A2  B2  p2 vdd gnd xor
x147 A3  B3  p3 vdd gnd xor

**********************carry**********************
******c1*********
x148 p0 car0 ccout1 vdd gnd and_g
x149 ccout1 g0 c1 vdd gnd or_g

******c2*********
x150 car0 p1 ccout2 vdd gnd and_g
x151 ccout2 p0 ccout3 vdd gnd and_g
x152 p1 g0 ccout4 vdd gnd and_g
x153 ccout4 ccout3 ccout5 vdd gnd or_g
x154 ccout5 g1 c2 vdd gnd or_g

******c3*********
x155 g1 p2 ccout6 vdd gnd and_g
x156 p2 p1 ccout7 vdd gnd and_g
x157 ccout7 g0 ccout8 vdd gnd and_g
x158 p2 p1 ccout9 vdd gnd and_g
x159 ccout9 p0 ccout10 vdd gnd and_g
x160 ccout10 car0 ccout11 vdd gnd and_g
x161 ccout6 ccout8 ccout12 vdd gnd or_g
x162 ccout11 g2 ccout13 vdd gnd or_g
x163 ccout12 ccout13 c3 vdd gnd or_g

******c4*********
x164 car0 p0 ccout14 vdd gnd and_g
x165 ccout14 p1 ccout15 vdd gnd and_g
x166 ccout15 p2 ccout16 vdd gnd and_g
x167 ccout16 p3 ccout17 vdd gnd and_g
x168 p3 p2 ccout18 vdd gnd and_g
x169 p1 ccout18 ccout19 vdd gnd and_g
x170 ccout19 g0 ccout20 vdd gnd and_g
x171 p3 p2 ccout21 vdd gnd and_g
x172 g1 ccout21 ccout22 vdd gnd and_g
x173 g2 p3 ccout23 vdd gnd and_g
x174 ccout17 ccout20 ccout24 vdd gnd or_g
x175 ccout22 ccout23 ccout25 vdd gnd or_g
x176 ccout25 ccout24 ccout26 vdd gnd or_g
x177 ccout26 g3 c4 vdd gnd or_g


.tran 0.1n 130n

.control
set hcopypscolor = 1
set color0=white
set color1=black

run
set curplottitle="Ayush-2020122001"

plot v(A0) v(B0)
plot v(c1)
plot v(B0)
set hcopypscolor = 1
hardcopy input.eps v(A0)
hardcopy output.eps v(c1)
hardcopy input_B.eps v(B0)
.endc
```

After we generated carry values, we can now use this with ropagate values to generate the sum, which is nothis but XORing the values of carry and propagate. The simulation results for adder block is as follows:

INPUTS



ADDER OUTPUT



So, it can be seen that when two inputs, one of bit value 1 (High voltage value) and other of bit value 0 (LOW voltage value) are added together, will result into bit value 1 (High voltage value). Which is also observable from the above given graphs. Hence the adder block is also working.

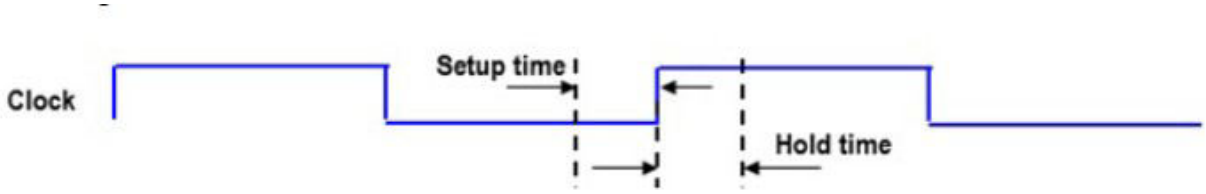
NETLIST for adder block:

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param w = {20*LAMBDA}
.param width_P={2*w}
.param width_N={2*w}
.global gnd vdd

Vdd     vdd     gnd     'SUPPLY'

vin1 D   0 pulse 0 0  0n 100p 100p 30n 500n
vin6 D1 0 pulse 0 1.8   0n 100p 100p 30n 500n
vin7 D2 0 pulse 0 0   0n 100p 100p 30n 500n
vin8 D3 0 pulse 0 1.8 0n 100p 100p 30n 500n

vin9 Db   0 pulse 0 1.8   0n 100p 100p 30n 500n
vin10 Db1 0 pulse 0 0   0n 100p 100p 30n 500n
vin11 Db2 0 pulse 0 1.8 0n 100p 100p 30n 500n
vin12 Db3 0 pulse 0 1.8 0n 100p 100p 30n 500n

vin_carry cinp 0 0

.subckt nand A B out vdd gnd
M1      out       A       k     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2      out       A       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3      k       B       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4      out       B       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends nand

.subckt inv yi xi vdd gnd
M1      yi       xi       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2      yi       xi       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv


**********XOR gate******************
.subckt xor da db outx vdd gnd
xx1 da db outx1 vdd gnd nand
xx2 da outx1 outx2 vdd gnd nand
xx3 db outx1 outx3 vdd gnd nand
xx4 outx2 outx3 outx vdd gnd nand
.ends xor

**************AND GATE******************
.subckt and_g in1 in2 aout vdd gnd
xx5 in1 in2 out_nan vdd gnd nand
xx6 aout out_nan  vdd gnd inv
.ends and_g

****************OR GATE*****************
.subckt or_g inn1 inn2 orout vdd gnd
xx7 ou1 inn1 vdd gnd inv
xx8 ou2 inn2 vdd gnd inv
xx9 ou1 ou2 orout vdd gnd nand
.ends or_g


*********************Generate*********************

x40 D  Db   g0 vdd gnd and_g
x41 D1 Db1  g1 vdd gnd and_g
x42 D2 Db2  g2 vdd gnd and_g
x43 D3 Db3  g3 vdd gnd and_g

*********************Propagate********************
x44 D   Db   p0 vdd gnd xor
x45 D1  Db1  p1 vdd gnd xor
x46 D2  Db2  p2 vdd gnd xor
x47 D3  Db3  p3 vdd gnd xor

*********************carry************************
******c1*********
x148 p0 cinp ccout1 vdd gnd and_g
x149 ccout1 g0 c1 vdd gnd or_g

******c2*********
x150 cinp p1 ccout2 vdd gnd and_g
x151 ccout2 p0 ccout3 vdd gnd and_g
x152 p1 g0 ccout4 vdd gnd and_g
x153 ccout4 ccout3 ccout5 vdd gnd or_g
x154 ccout5 g1 c2 vdd gnd or_g

******c3*********
x155 g1 p2 ccout6 vdd gnd and_g
x156 p2 p1 ccout7 vdd gnd and_g
x157 ccout7 g0 ccout8 vdd gnd and_g
x158 p2 p1 ccout9 vdd gnd and_g
x159 ccout9 p0 ccout10 vdd gnd and_g
x160 ccout10 cinp ccout11 vdd gnd and_g
x161 ccout6 ccout8 ccout12 vdd gnd or_g
x162 ccout11 g2 ccout13 vdd gnd or_g
x163 ccout12 ccout13 c3 vdd gnd or_g

******c4*********
x164 cinp p0 ccout14 vdd gnd and_g
x165 ccout14 p1 ccout15 vdd gnd and_g
x166 ccout15 p2 ccout16 vdd gnd and_g
x167 ccout16 p3 ccout17 vdd gnd and_g
x168 p3 p2 ccout18 vdd gnd and_g
x169 p1 ccout18 ccout19 vdd gnd and_g
x170 ccout19 g0 ccout20 vdd gnd and_g
x171 p3 p2 ccout21 vdd gnd and_g
x172 g1 ccout21 ccout22 vdd gnd and_g
x173 g2 p3 ccout23 vdd gnd and_g
x174 ccout17 ccout20 ccout24 vdd gnd or_g
x175 ccout22 ccout23 ccout25 vdd gnd or_g
x176 ccout25 ccout24 ccout26 vdd gnd or_g
x177 ccout26 g3 c4 vdd gnd or_g


**************sum*******************************
x56 cinp p0 s0 vdd gnd xor
x57 c1 p1 s1 vdd gnd xor
x58 c2 p2 s2 vdd gnd xor
x59 c3 p3 s3 vdd gnd xor




.tran 0.1n 100n

.control
set hcopypscolor = 1
set color0=white
set color1=black

run
set curplottitle="Ayush-2020122001"

*plot v(s_bar)
plot v(s0)
*plot v(Db)
*plot v(D)
plot v(D) v(Db)
*plot v(outs0)
*plot v(c4)
set hcopypscolor = 1
hardcopy input.eps v(D) v(Db)
hardcopy output.eps v(s0)
.endc
```

< SECTION 4 > In this part it is asked to find the setup time, hold time and clock to Q delay, for D flip flop.

Setup time:

Setup Time is the amount of time the synchronous input (D) must show up, and be stable before the capturing edge of clock. This is so that the data can be stored successfully in the storage device.



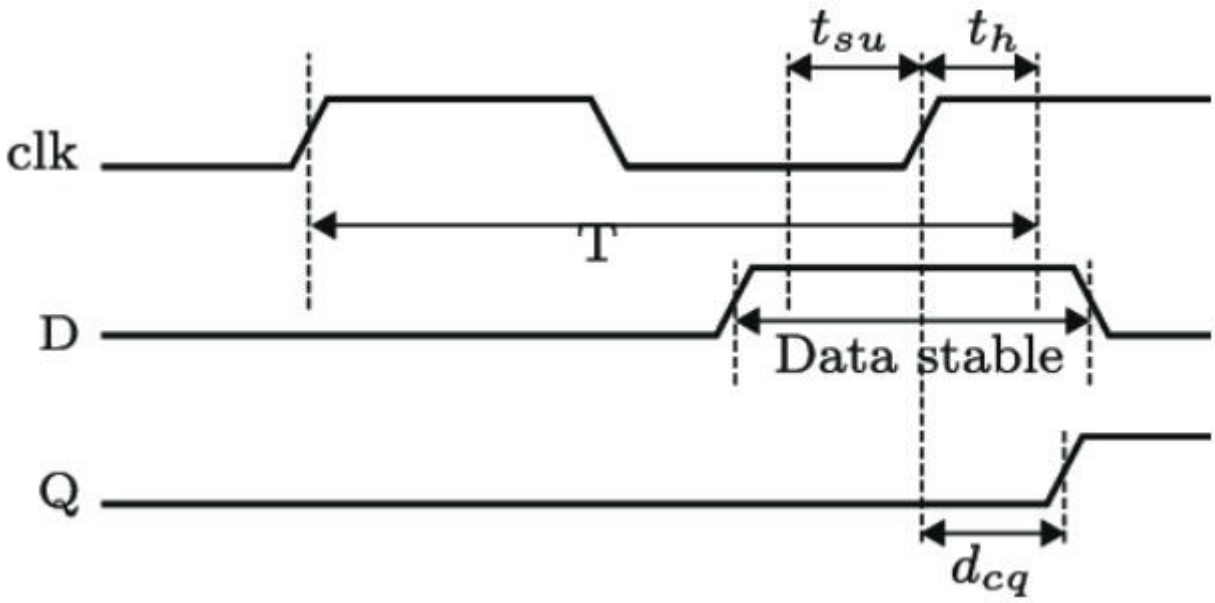
In order to calculate the setup time for the D flip flop, I first gave a delay of 2ns to the clock and then start reducing the delay till I get the absurd value for the given input, on doing so, I got my setup time as 0.044ns.

Hold time:

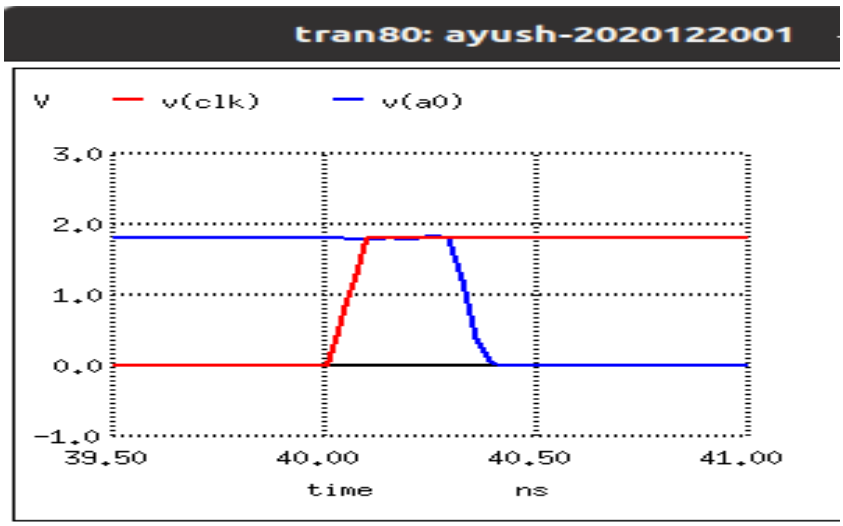
Hold Time is the amount of time the synchronous input (D) stays long enough after the capturing edge of clock so that the data can be stored successfully in the storage device. In order to find this I increased the pulse value, say 40.2 ns (while the clock period is 40ns) and then I start decreasing the value of the pulse till I get the unexpected value at the output, in my case, that occured at 40.05 ns, so the hold time is of 0.05ns

Clock to Q delay:

This delay refer to the delay that occurs when there is a positive edge of the clock which takes the input value and then give out the respective output. For more insight we can give a look at the below timing diagram which give us a general idea of how we can find the delays.



So as per the above timing diagram we can see d_{cq} represent the clock to Q delay. Using the above logic I tried to find the clock to Q delay and the graph given below to justify my approach.

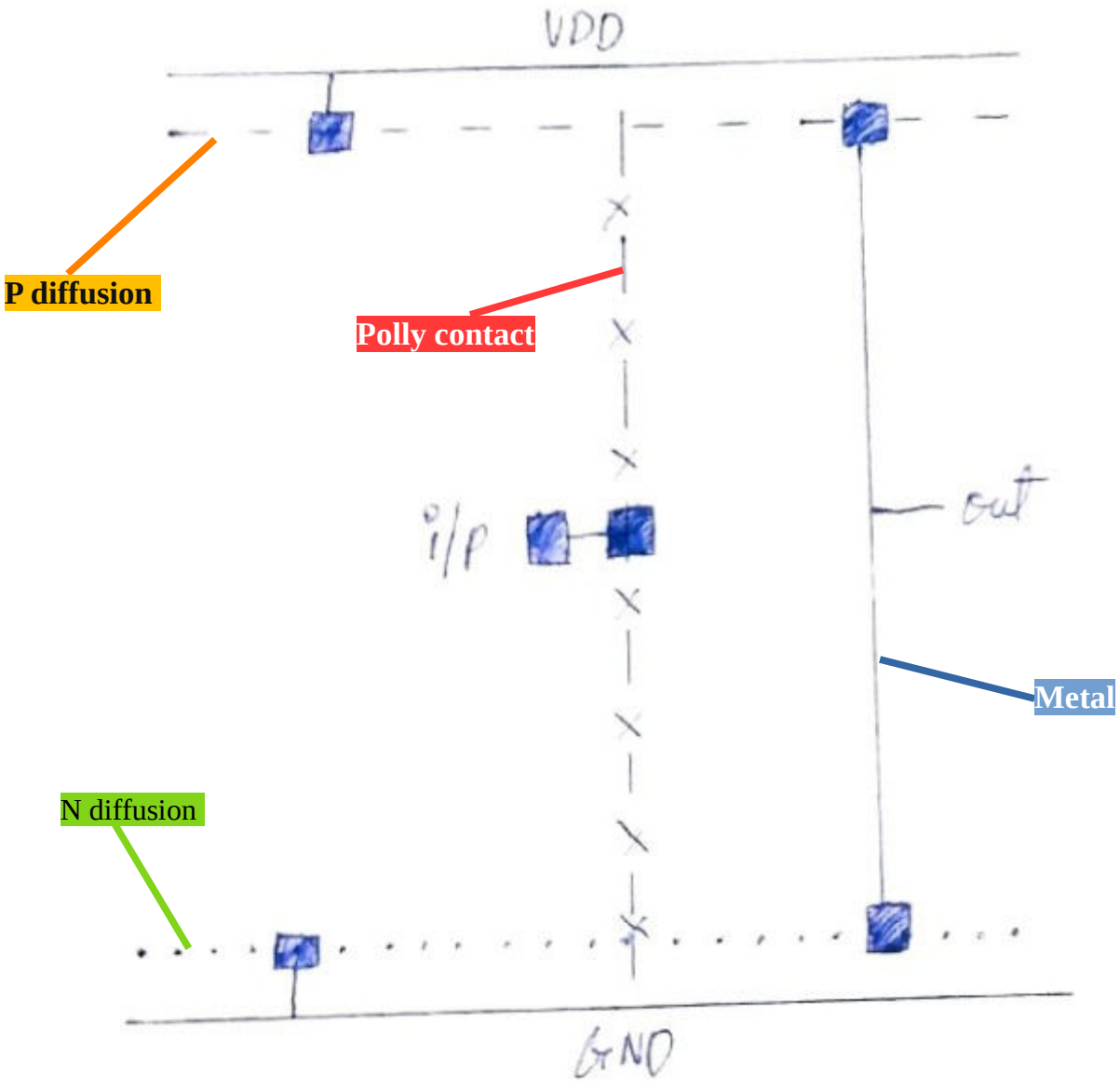


So, here a0 represent the output and clk is given clock pulses. The difference between these pulses will result into the corresponding clock to Q delay.

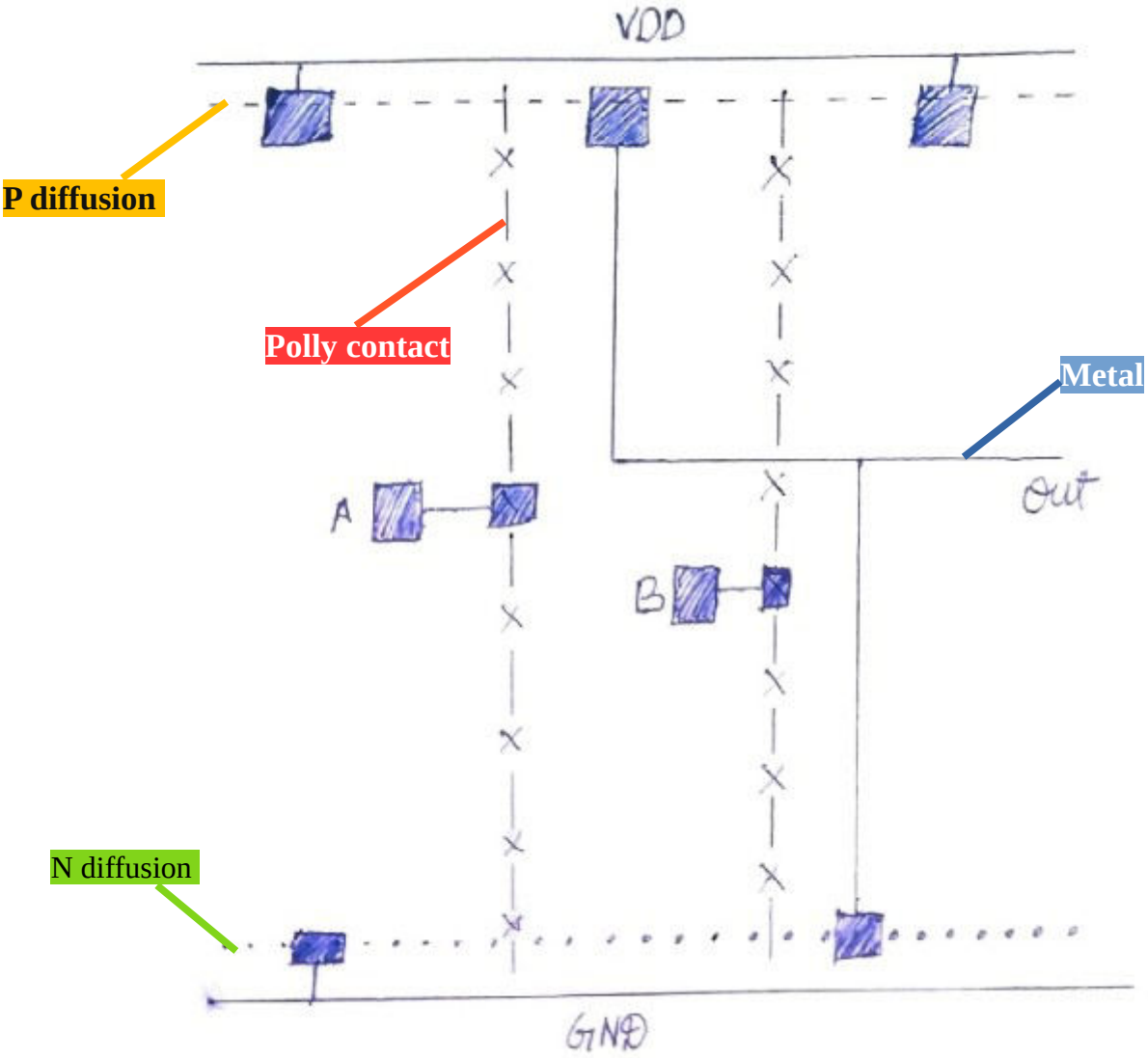
< SECTION 5 > STICK DIAGRAM

For my implementation, I have used NAND gates and inverters to make the rest of the gates so that complications can be reduced. As discussed before we can see how XOR, AND and OR gates were formed with the help of NAND gate and INVERTERS.

Below is the stick diagram for the inverter that I have used



Stick Diagram for NAND gate is as follows:



So we can see the implementation of the NAND gate and inverter with the help of the stick diagram, and every type of line represent some kind of material which are marked accordingly.

In the above section we saw how to implement gates with the help of stick diagrams now the same logic is being used to implement gates and other circuits in the MAGIC tool. In the proceeding section we will see implementation of various blocks in the MAGIC.

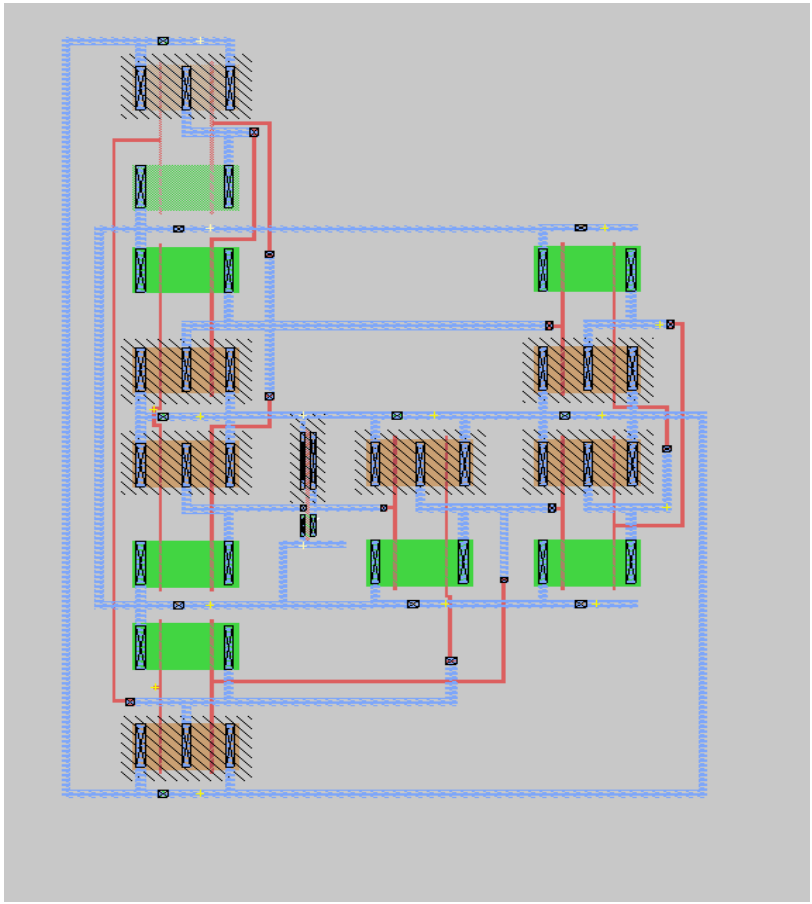
< SECTION 6 > Magic layout of each block

In this part we will look at each block's MAGIC layout output and look at the post layout result.

(A) D flip flop:

As discussed in section 2, I have implemented positive edge triggered D flip flop with the help of NAND gates, its corresponding MAGIC layout is as given below:

D FLIP FLOP MAGIC LAYOUT



D FLIP FLOP SCHEMATIC

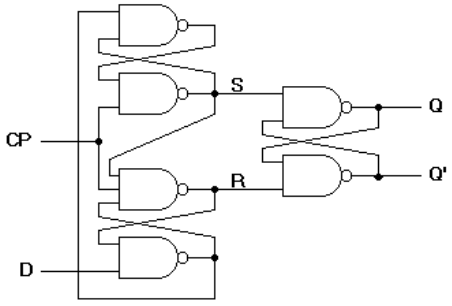
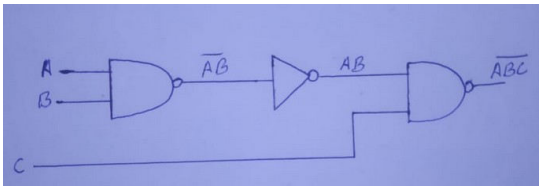
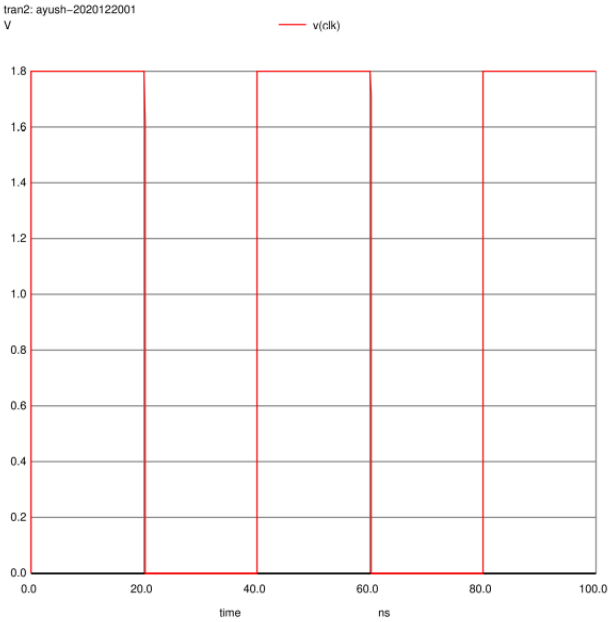


Diagram of three input NAND gate used for making D flip flop

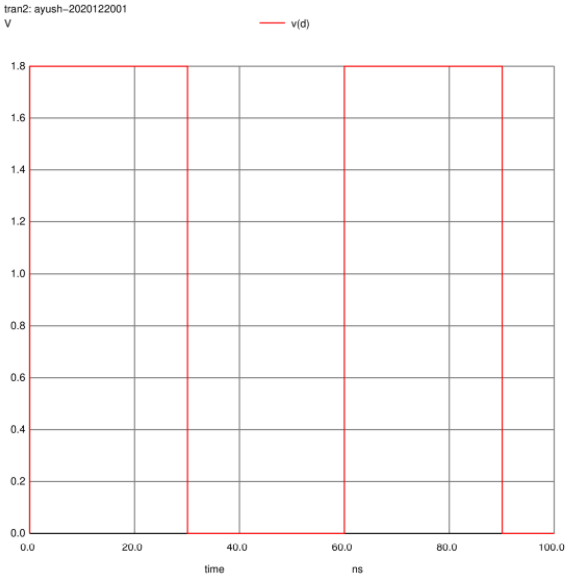


The simulation of the above D flip flop is as follows:

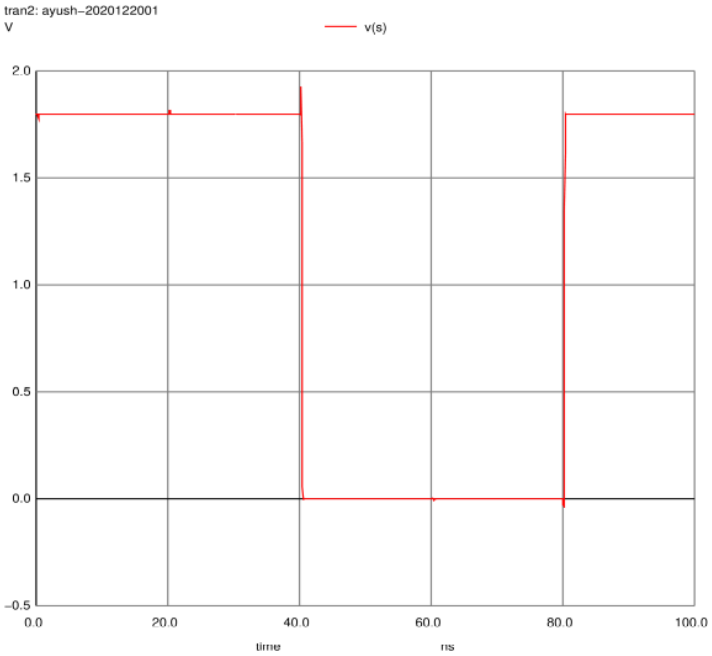
INPUT CLOCK



INPUT VALUE



OUTPUT VALUE



So we can see that when there is positive edge of the clock we will see the output reflecting the value same as that of the input, while at negative edge of the clock the output holds that value. So the D flip flop is performing as expected and giving the correct output. The difference between prelayout and post layout is that, when we make layout in MAGIC, we are using metal wires for inter-connections and also several other diffusion material, so, these material will led to generation of the parasitic capacitances which will add some noise to the original values. This will also increase delay for retrieving the output value.

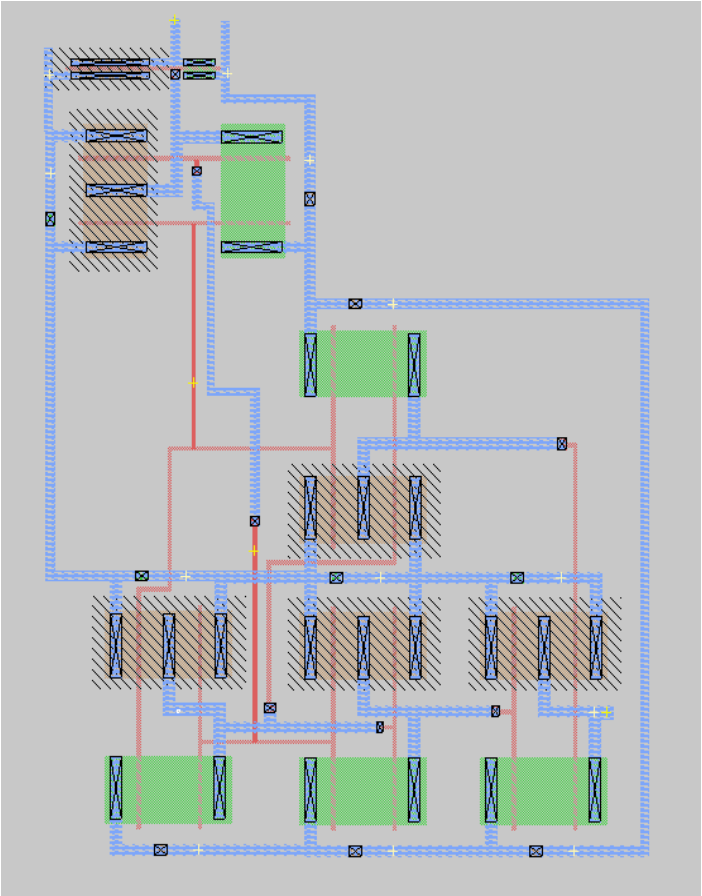
The corresponding **NETLIST** is :

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param w = {20*LAMBDA}
.param width_P={2*w}
.param width_N={2*w}
.global gnd vdd

Vdd     vdd     gnd     'SUPPLY'
vin1 D gnd pulse 0 1.8 0n 100p 100p 30n 60n
vin2 clk gnd pulse 0 1.8 0n 100p 100p 20n 40n


.option scale=0.09u

M1000 a_195_n244# a_30_n223# gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=5700 ps=890
M1001 a_195_n244# a_30_n223# vdd w_86_n4# CMOSP w=50 l=2
+  ad=250 pd=110 as=11170 ps=1776
M1002 a_30_n81# a_n7_n412# gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1003 a_67_n144# a_30_n141# a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1004 a_67_n144# a_n7_n412# vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1005 vdd a_30_n141# a_67_n144# w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1006 vdd a_n7_n412# a_67_n474# w_176_n229# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1007 S a_30_n141# vdd w_302_n149# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1008 a_30_n223# a_30_n141# a_30_n311# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1009 a_n7_n412# a_67_n474# a_30_n383# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1010 vdd S S_bar w_302_n229# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1011 a_332_n52# a_30_n141# gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1012 a_67_n474# a_195_n244# vdd w_176_n229# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1013 S S_bar a_332_n52# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1014 a_30_n311# clk gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1015 a_30_n383# D gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1016 vdd a_67_n144# a_30_n141# w_0_n150# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1017 S_bar a_67_n474# vdd w_302_n229# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1018 a_67_n474# a_n7_n412# a_206_n310# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1019 vdd a_67_n474# a_n7_n412# w_0_n480# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1020 S_bar S a_332_n310# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1021 a_30_n141# clk vdd w_0_n150# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1022 a_30_n53# clk gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1023 vdd a_30_n141# a_30_n223# w_0_n230# CMOSP w=40 l=2
+  ad=0 pd=0 as=1384 ps=122
M1024 a_206_n310# a_195_n244# gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1025 a_n7_n412# D vdd w_0_n480# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1026 a_332_n310# a_67_n474# gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1027 a_30_n141# a_67_n144# a_30_n53# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1028 vdd S_bar S w_302_n149# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1029 a_30_n223# clk vdd w_0_n230# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
C0 a_67_n474# Gnd 3.23fF
C1 S Gnd 2.10fF
C2 w_0_n480# Gnd 5.46fF
C3 w_302_n229# Gnd 5.46fF
C4 w_0_n230# Gnd 5.46fF
C5 w_302_n149# Gnd 5.46fF
C6 w_0_n150# Gnd 5.46fF
C7 gnd Gnd 5.39fF
C8 a_30_n141# Gnd 4.12fF
C9 a_n7_n412# Gnd 5.47fF
C10 vdd Gnd 8.04fF
C11 w_0_0# Gnd 5.46fF

.tran 0.1n 100n

.control
set hcopypscolor = 1
set color0=white
set color1=black

run
set curplottitle="Ayush-2020122001"

*plot v(s_bar)
plot v(clk)
plot v(D)
plot v(S)
set hcopypscolor = 1
```

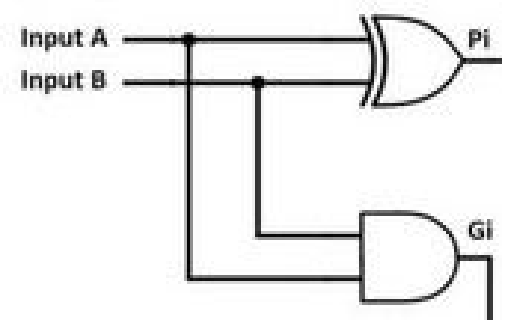
(B) Propagate and generate block:

As discussed in section 2, I have implemented the propagate and generate block with the help of AND and XOR gates, the corresponding MAGIC layout is as follows:

PROPAGATE AND GENERATE MAGIC LAYOUT

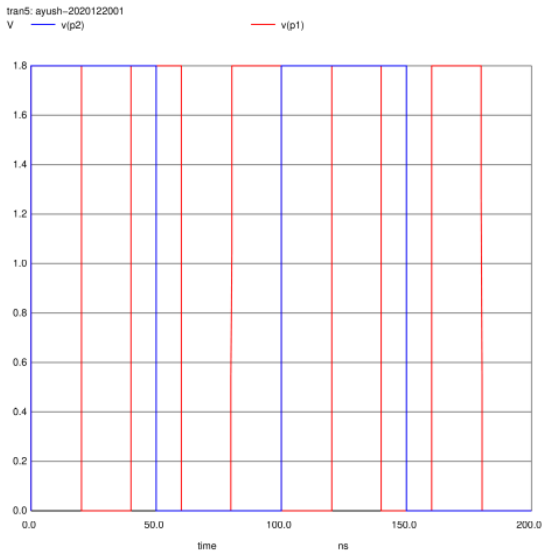


SCHEMATIC DIAGRAM OF PROPAGATE AND GENERATE BLOCK

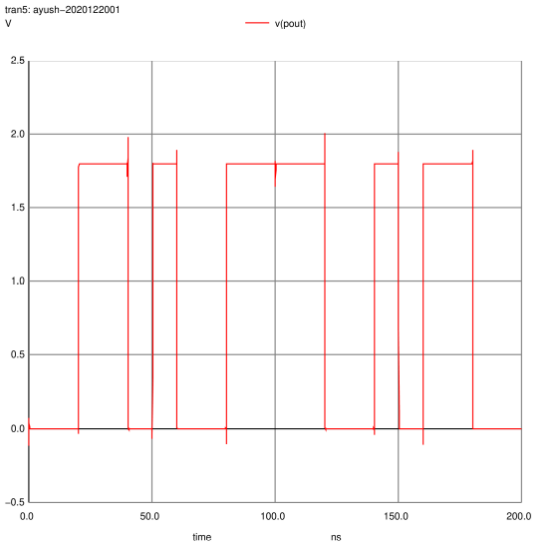


So the output for the **propagate part** is coming as:

INPUT VALUES

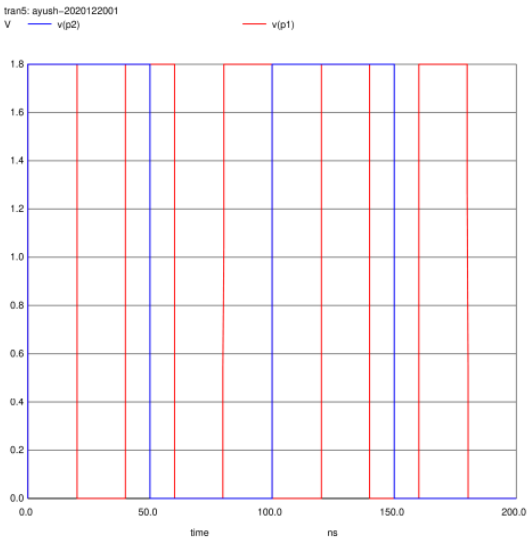


OUTPUT VALUE

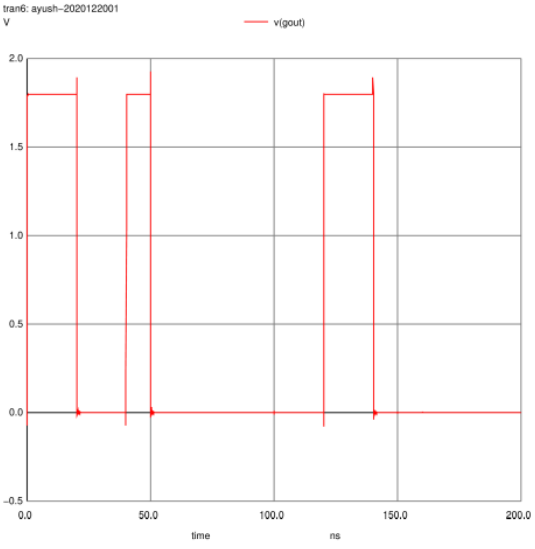


For the **generate part** output will come as:

INPUT VALUES



OUTPUT VALUES



So we can observe that the propagate and generate blocks are giving outputs as expected. Since this is a post-layout simulaton, so we will have effects of parasitic capacitances also, which will led to increase in the delay of the output values.

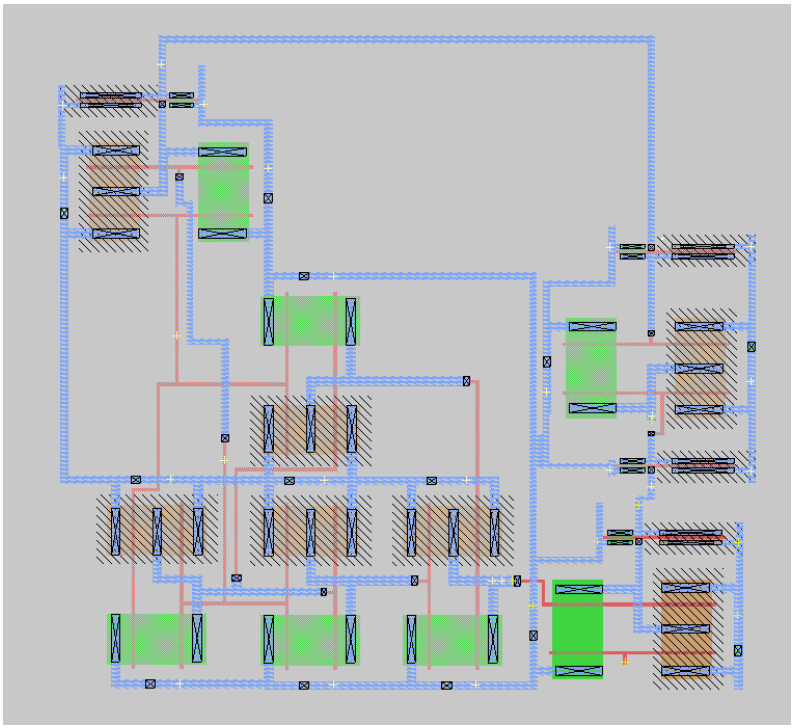
The corresponding **NETLIST** is as follows:

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param w = {20*LAMBDA}
.param width_P={2*w}
.param width_N={2*w}
.global gnd vdd

vin1 p1 0 pulse 0 1.8 0n 100p 100p 19.9n 40n
vin2 p2 0 pulse 0 1.8 0n 100p 100p 49.9n 100n
Vdd     vdd     gnd     'SUPPLY'

.option scale=0.09u

M1000 a_30_n81# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=4100 ps=650
M1001 a_109_86# p2 a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1002 a_109_86# p1 vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=8050 ps=1300
M1003 vdd p2 a_109_86# w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1004 vdd a_154_188# pout w_239_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1005 pout a_154_188# a_269_18# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1006 vdd a_109_86# a_154_106# w_124_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1007 a_154_188# p1 vdd w_124_179# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1008 a_154_106# a_109_86# a_154_18# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1009 vdd a_109_86# a_154_188# w_124_179# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1010 a_154_276# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1011 a_269_18# a_154_106# gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1012 a_154_188# a_109_86# a_154_276# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1013 a_154_18# p2 gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1014 pout a_154_106# vdd w_239_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1015 a_154_106# p2 vdd w_124_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1016 gout m1_83_86# gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1017 gout m1_83_86# vdd w_86_n4# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1018 a_30_n81# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1019 m1_83_86# p2 a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1020 m1_83_86# p1 vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1021 vdd p2 m1_83_86# w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
C0 w_0_0# Gnd 5.46fF
C1 w_239_99# Gnd 5.46fF
C2 w_0_0# Gnd 5.46fF



.tran 0.1n 200n

.control
set hcopypscolor = 1
set color0=white
set color1=black

run
set curplottitle="Ayush-2020122001"

*plot v(a)
plot v(p1) v(p2)
*plot v(db)
plot v(gout)
set hcopypscolor = 1
hardcopy inputs.eps v(p1) v(p2)
hardcopy output.eps v(gout)
.endc
```

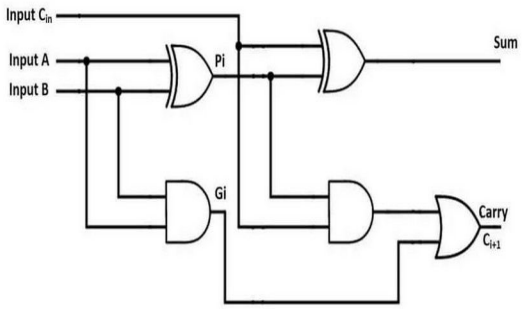
(C) Carry block :

Similar to what discussed in section 2, I have used AND gate and OR gate to implement my carry block. I have kept 1.8v as the initial value of the carry for the simulations. The magic layout of the carry block is as given below:

CARRY BLOCK MAGIC LAYOUT

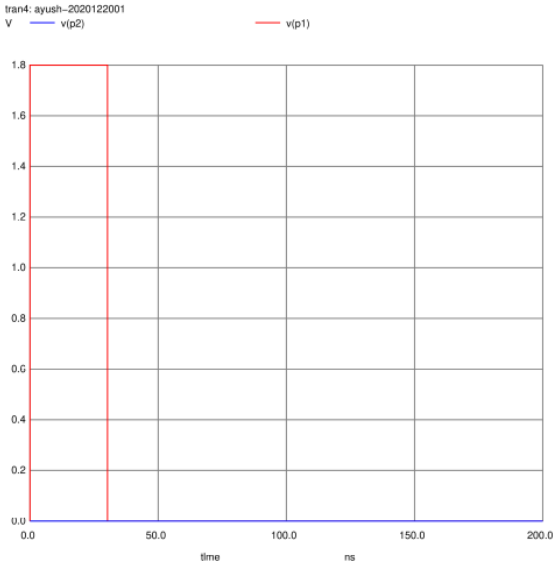


SCHEMATIC DIAGRAM OF CARRY BLOCK AND SUM BLOCK

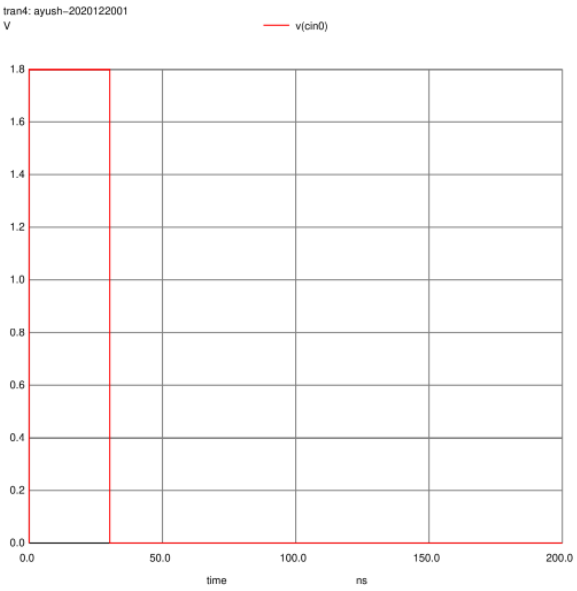


After we get the layout, spice netlist is extracted and we will get the carry output based on the input given.
So in my case I have given input carry value as 1.8v (i.e. high value) and one of the inputs as 1.8v and other as 0v. So the output carry should be of high value as Carry = Gi + Pi . Ci so in this case Pi will result into high value and Ci is also of high value, thus overall the carry output will be high. Below are the corresponding simulation results:

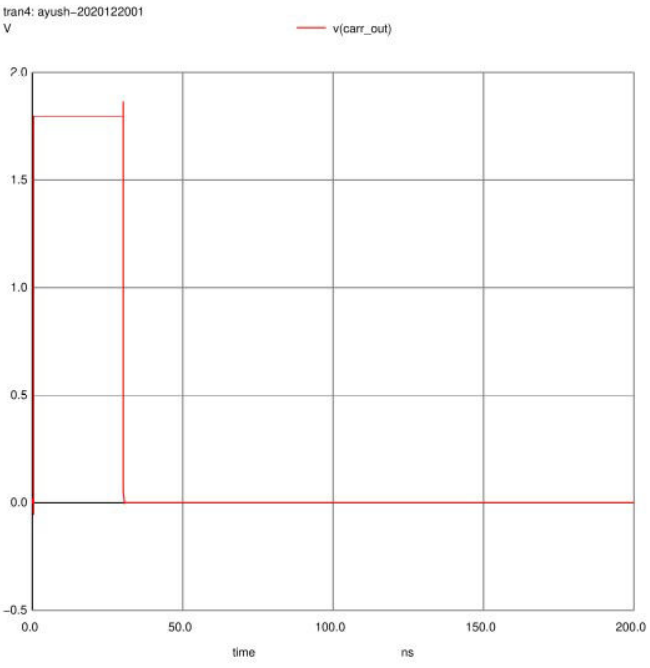
INPUT VALUES



CARRY INPUT



CARRY OUT



So from the above results we can see that the carry block is giving the values as expected. The difference between the prelayout and the postlayout results is the occurance of the parasitic capacitances which introduces some delay in the circuit.

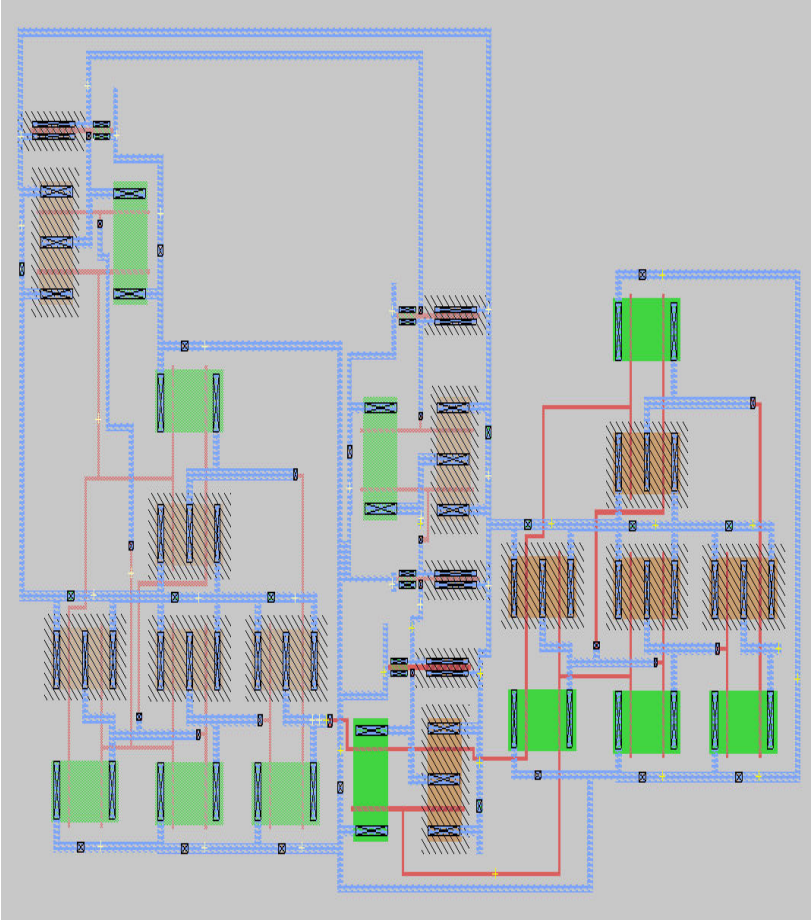
The **NETLIST** for the above carry block is as follows:-

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param w = {20*LAMBDA}
.param width_P={2*w}
.param width_N={2*w}
.global gnd vdd

vin1 p1 0 pulse 0 1.8 0n 100p 100p 30n 600n
vin2 p2 0 pulse 0 0 0n 100p 100p 30n 400n
*vin4 x_in2 0 pulse 0 1.8 0n 100p 100p 29.9n 60n
*vin3 pin 0 pulse 0 1.8 0n 100p 100p 19.9n 40n
vin5 cin0 0 pulse 0 1.8 0n 100p 100p 30n 600n
Vdd     vdd     gnd     'SUPPLY'


* SPICE3 file created from carry_final.ext - technology: scmos

.option scale=0.09u

M1000 a_30_n81# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=5940 ps=994
M1001 a_109_86# p2 a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1002 a_109_86# p1 vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=11920 ps=2106
M1003 vdd p2 a_109_86# w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1004 vdd a_154_188# pin_p w_239_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1005 pin_p a_154_188# a_269_18# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1006 vdd a_109_86# a_154_106# w_124_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1007 a_154_188# p1 vdd w_124_179# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1008 a_154_106# a_109_86# a_154_18# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1009 vdd a_109_86# a_154_188# w_124_179# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1010 a_154_276# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1011 a_269_18# a_154_106# gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1012 a_154_188# a_109_86# a_154_276# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1013 a_154_18# p2 gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1014 pin_p a_154_106# vdd w_239_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1015 a_154_106# p2 vdd w_124_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1016 gout m1_83_86# gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1017 gout m1_83_86# vdd w_0_486# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1018 a_30_n81# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1019 m1_83_86# p2 a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1020 m1_83_86# p1 vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1021 vdd p2 m1_83_86# w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1022 a_18_85# gout gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1023 a_18_85# gout vdd w_86_n4# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1024 a_30_n81# a_18_85# gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1025 carr_out a_69_95# a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1026 carr_out a_18_85# vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1027 vdd a_69_95# carr_out w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1028 gnd o_ca a_69_95# Gnd CMOSN w=20 l=2
+  ad=0 pd=0 as=100 ps=50
M1029 vdd o_ca a_69_95# w_115_92# CMOSP w=50 l=2
+  ad=0 pd=0 as=250 ps=110
M1030 a_399_30# cin0 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1031 a_399_69# pin_p a_399_30# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1032 a_399_69# cin0 vdd w_480_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1033 vdd pin_p a_399_69# w_480_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1034 o_ca a_399_69# gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1035 o_ca a_399_69# vdd w_473_109# CMOSP w=50 l=2
+  ad=75 pd=35 as=0 ps=0
C0 w_480_0# Gnd 5.46fF
C1 gnd Gnd 3.77fF
C2 w_0_0# Gnd 5.46fF
C3 w_0_0# Gnd 5.46fF
C4 w_239_99# Gnd 5.46fF
C5 w_0_0# Gnd 5.46fF


.tran 0.1n 200n

.control
set hcopypscolor = 1
set color0=white
set color1=black

*** x_in1 is g0 and inp2 is p0)

run
set curplottitle="Ayush-2020122001"

*plot v(a)
plot v(p1) v(p2)
*plot v(db)
*plot v(a_car)
*plot v(pin_p)
plot v(carr_out)
plot v(cin0)
*plot v(o_ca)
set hcopypscolor = 1
hardcopy input.eps v(p1) v(p2)
hardcopy out.eps v(carr_out)
hardcopy cin.eps v(cin0)
.endc
```

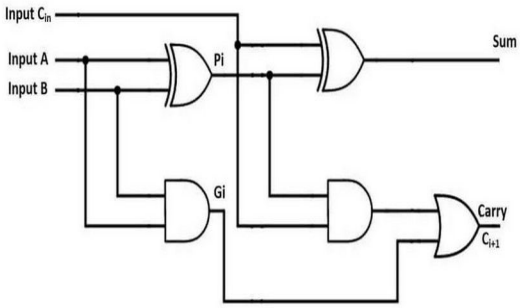
(D) SUM block:

As disscussed in the section 2, I am using XOR gates made with the help of NAND gates to implement my SUM block. The corresponding MAGIC layout is as given below:

MAGIC LAYOUT OF ADDER BLOCK

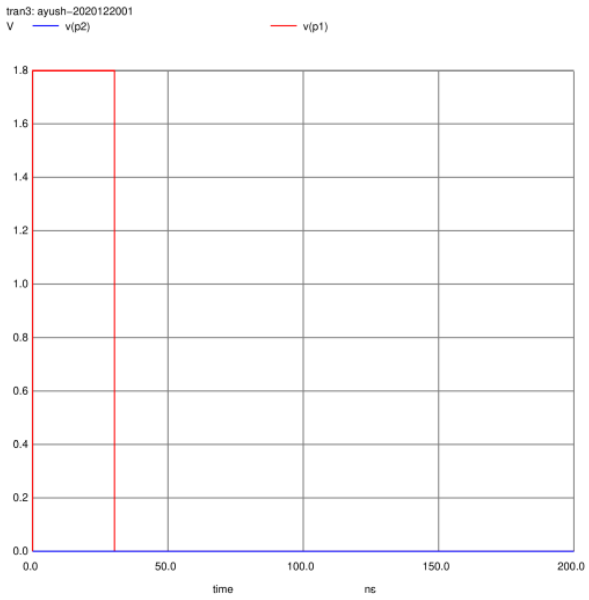


SUM AND CARRY SCHEMATIC

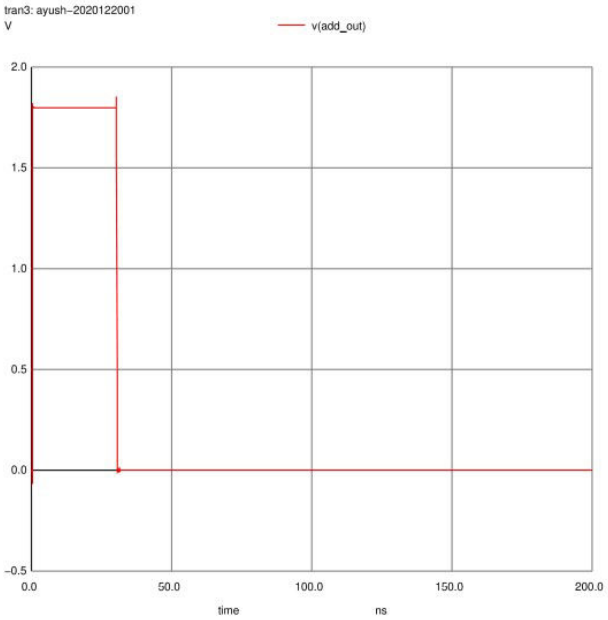


For the simulation of the above ADD block I have used input 1 as low i.e. 0v and input 2 as high i.e. 1.8v and the input carry as 0, so the resulting output should of high value i.e. 1.8v. Lets verify this from the below given simulation graph:

INPUT VALUES



OUTPUT VALUE



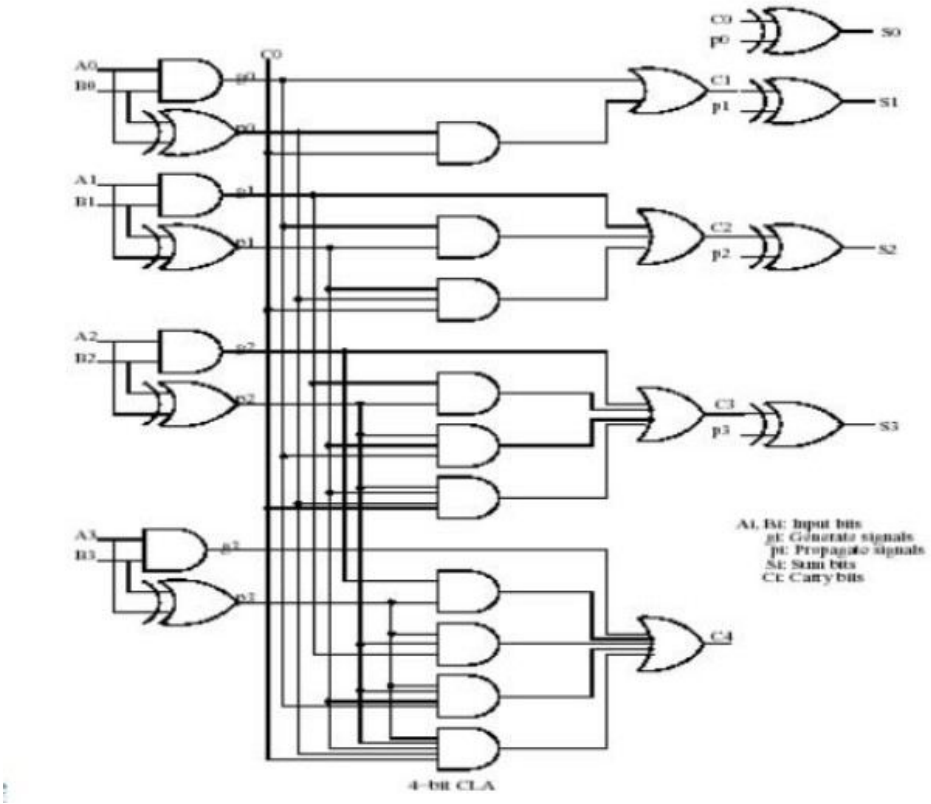
So from the above graphs we can see that output is coming as high value when one of the input is low and other is high and the input carry is low, which is as expected. So the difference between prelayout and the postlayout is the inclusion of parasitic capacitances which ultimately led to increase in the delays. These are generated due to the presence of metals used for connections and other deposition material used.

The **NETLIST** for the above adder is :

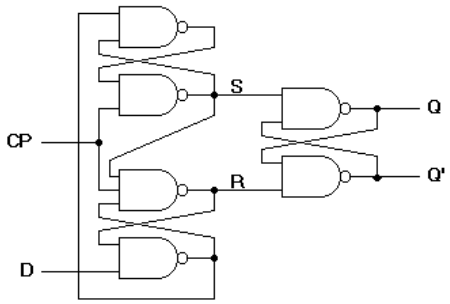
```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param w = {20*LAMBDA}
.param width_P={2*w}
.param width_N={2*w}
.global gnd vdd

vin1 p1 0 pulse 0 1.8 0n 100p 100p 30n 600n
vin2 p2 0 pulse 0 0 0n 100p 100p 30n 400n

vin5 cin0 0 pulse 0 0 0n 100p 100p 30n 600n
Vdd     vdd     gnd     'SUPPLY'


* SPICE3 file created from carry_add.ext - technology: scmos

.option scale=0.09u

M1000 a_30_n81# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=9140 ps=1474
M1001 a_109_86# p2 a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1002 a_109_86# p1 vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=18160 ps=3058
M1003 vdd p2 a_109_86# w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1004 vdd a_154_188# pin_p w_239_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1005 pin_p a_154_188# a_269_18# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1006 vdd a_109_86# a_154_106# w_124_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1007 a_154_188# p1 vdd w_124_179# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1008 a_154_106# a_109_86# a_154_18# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1009 vdd a_109_86# a_154_188# w_124_179# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1010 a_154_276# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1011 a_269_18# a_154_106# gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1012 a_154_188# a_109_86# a_154_276# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1013 a_154_18# p2 gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1014 pin_p a_154_106# vdd w_239_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1015 a_154_106# p2 vdd w_124_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1016 gout m1_83_86# gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1017 gout m1_83_86# vdd w_86_n4# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1018 a_30_n81# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1019 m1_83_86# p2 a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1020 m1_83_86# p1 vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1021 vdd p2 m1_83_86# w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1022 a_18_85# gout gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1023 a_18_85# gout vdd w_86_n4# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1024 a_30_n81# a_18_85# gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1025 carr_out a_69_95# a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1026 carr_out a_18_85# vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1027 vdd a_69_95# carr_out w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1028 gnd o_ca a_69_95# Gnd CMOSN w=20 l=2
+  ad=0 pd=0 as=100 ps=50
M1029 vdd o_ca a_69_95# w_115_92# CMOSP w=50 l=2
+  ad=0 pd=0 as=250 ps=110
M1030 a_844_66# a_729_154# gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1031 add_out a_729_154# vdd w_814_147# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1032 a_729_154# cin0 vdd w_699_147# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1033 a_399_30# cin0 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1034 a_729_66# cin0 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1035 vdd a_729_236# add_out w_814_147# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1036 a_399_69# pin_p a_399_30# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1037 vdd a_605_155# a_729_154# w_699_147# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1038 a_399_69# cin0 vdd w_480_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1039 a_605_155# cin0 a_605_67# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1040 a_729_236# pin_p vdd w_699_227# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1041 vdd pin_p a_399_69# w_480_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1042 add_out a_729_236# a_844_66# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1043 vdd a_605_155# a_729_236# w_699_227# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1044 a_605_155# pin_p vdd w_575_148# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1045 a_729_154# a_605_155# a_729_66# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1046 vdd cin0 a_605_155# w_575_148# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1047 o_ca a_399_69# gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1048 a_729_324# pin_p gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1049 o_ca a_399_69# vdd w_473_109# CMOSP w=50 l=2
+  ad=75 pd=35 as=0 ps=0
M1050 a_605_67# pin_p gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1051 a_729_236# a_605_155# a_729_324# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
C0 cin0 Gnd 3.05fF
C1 a_605_155# Gnd 2.38fF
C2 w_480_0# Gnd 5.46fF
C3 w_814_147# Gnd 5.46fF
C4 w_699_147# Gnd 5.46fF
C5 w_575_148# Gnd 5.46fF
C6 w_699_227# Gnd 5.46fF
C7 gnd Gnd 3.73fF
C8 w_0_0# Gnd 5.46fF
C9 w_0_0# Gnd 5.46fF
C10 vdd Gnd 3.19fF
C11 w_239_99# Gnd 5.46fF
C12 w_0_0# Gnd 5.46fF


.tran 0.1n 200n

.control
set hcopypscolor = 1
set color0=white
set color1=black

*** x_in1 is g0 and inp2 is p0)

run
set curplottitle="Ayush-2020122001"
```

< SECTION 7 >

Now we saw all the components of the CLA adder, now in this section it is asked to combine all these blocks to get the final output.



First the input is given to the D flip flop, so that values will be given to the rest of the CLA adder components only when there is a positive edge. After the bit addition is calculated, resultant value will be passed to the Outter D flip flop, thus the input will be taken at the first positive edge and then the adder output will appear at the second cycle.

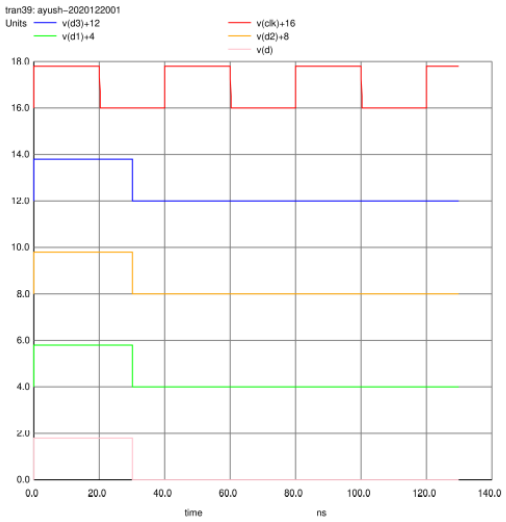


The simulation results are as follows:-

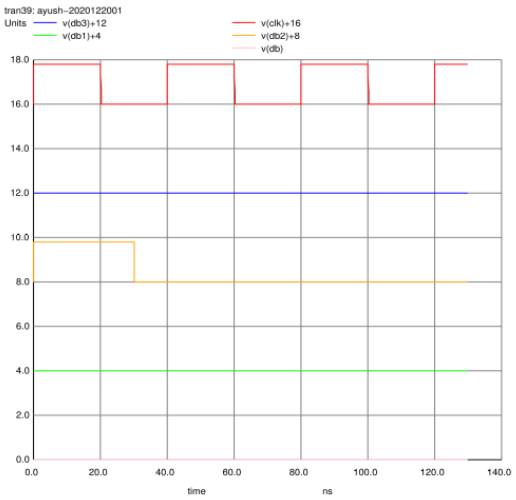
SIMULATIONS
Inputs:
A = 1111
B = 0100
carry_in = 0

Outputs:
S = 0011
Carry_out = 1

INPUT A

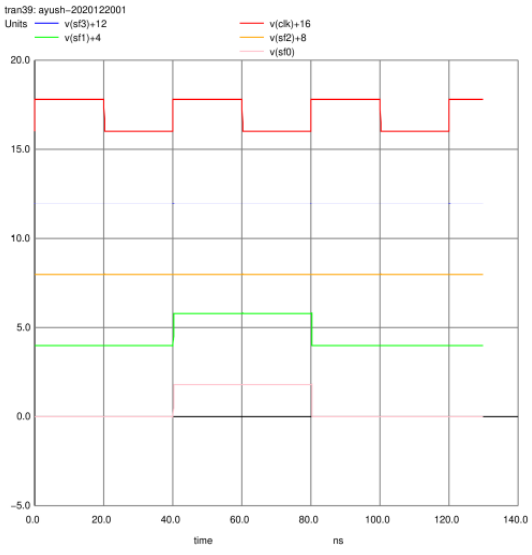


INPUT B



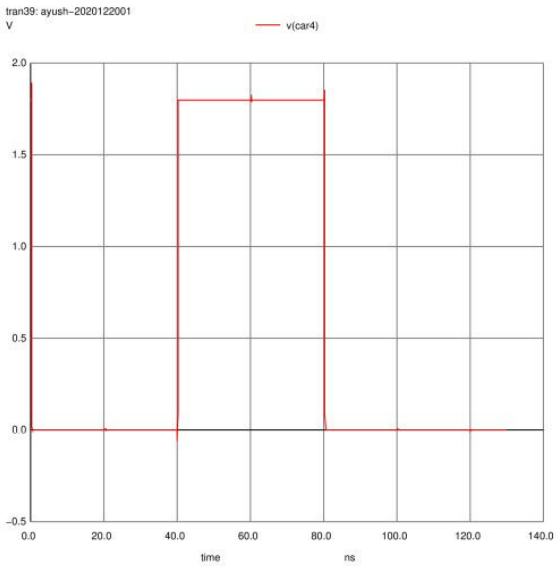
OUTPUT SUM

(Appearing at 2nd cycle)



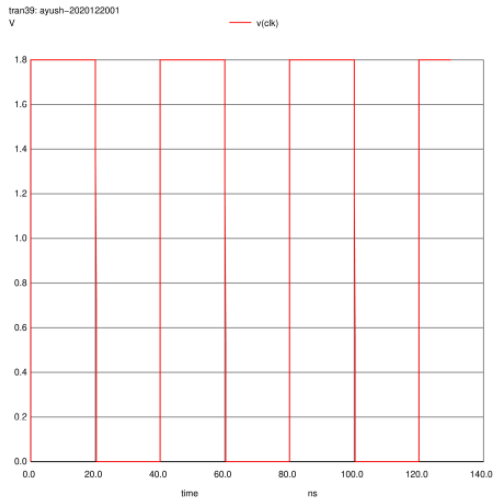
CARRY OUT

(Appearing at 2nd cycle)



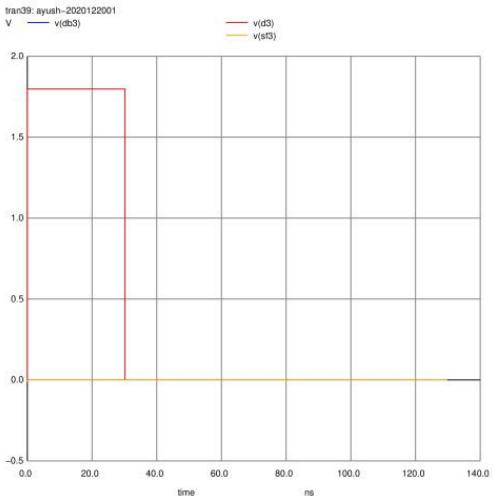
So if we look in a more detail way and analyze bits and their corresponding sums then we would get:

CLOCK



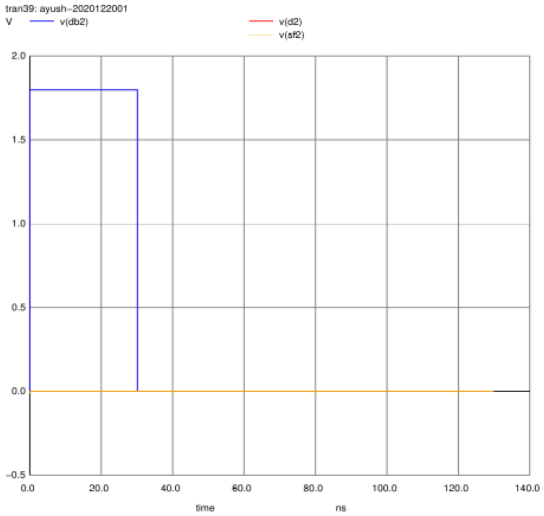
INPUT A3 + B3 = S3

1 + 0 + CARRY = 0, CARRY=1



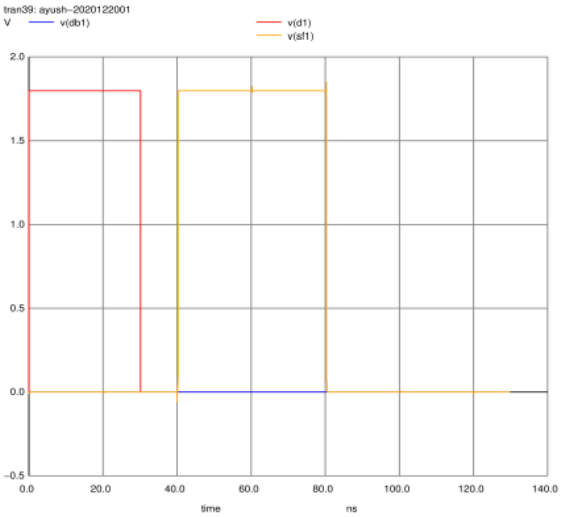
INPUT A2 + B2 = S2

1 + 1 = 0, CARRY =1



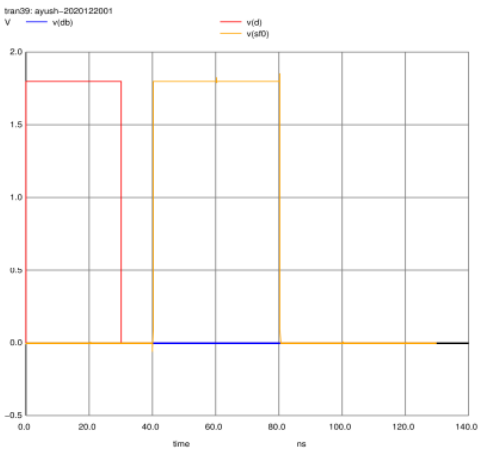
INPUT A1 + B1 = S1

1 + 0 = 1

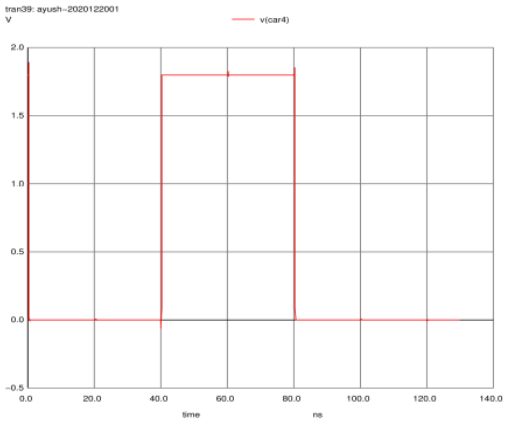


INPUT A0 + B0 = S0

1 + 0 = 1



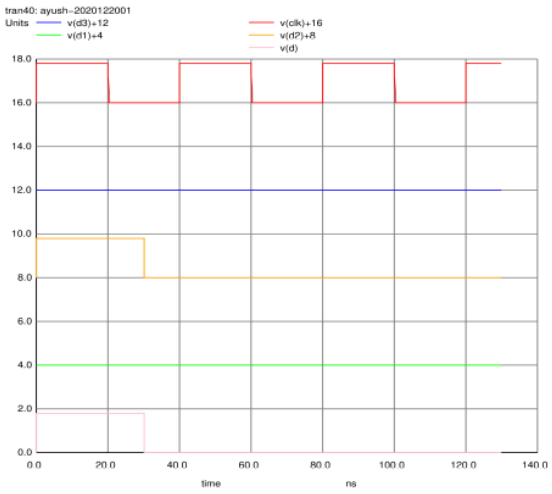
OUTPUT CARRY = 1



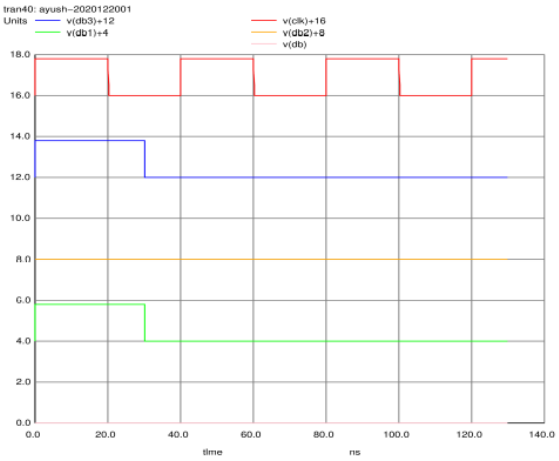
Lets look at one more case:
Inputs:
A = 0101
B = 1010
carry_in = 0

Outputs:
S = 1111
Carry_out = 0

INPUT A

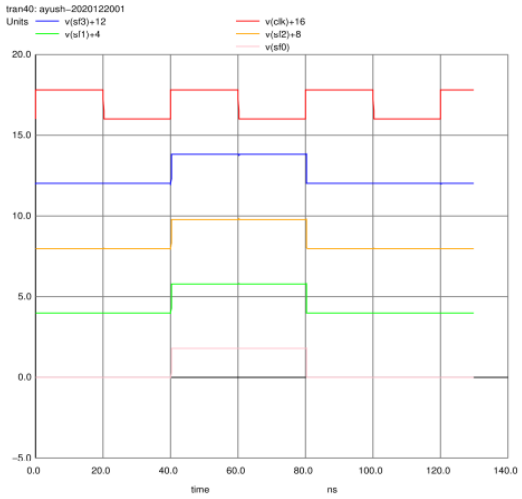


INPUT B



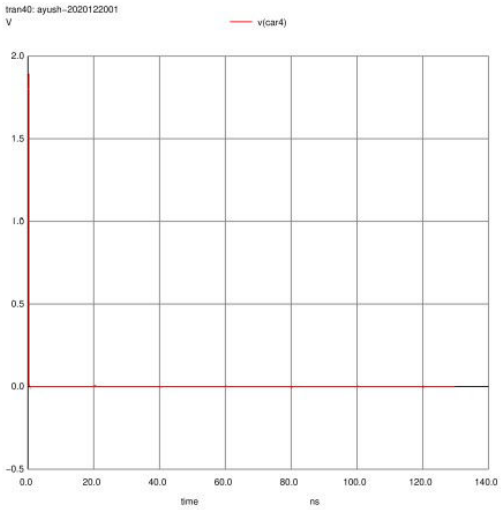
OUTPUT SUM

(Appearing at 2nd cycle)



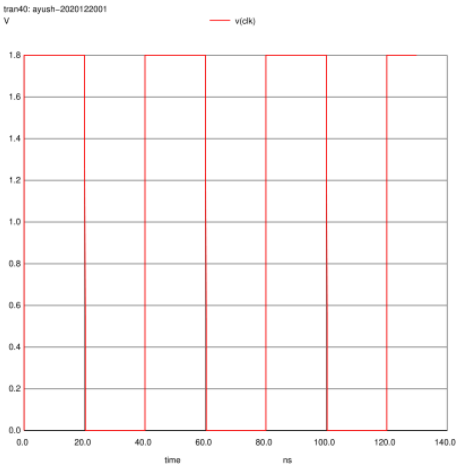
CARRY OUT

(Appearing at 2nd cycle)



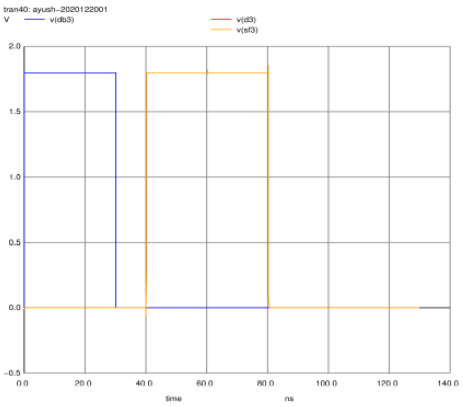
On looking in a more detail way to analyze bits and their corresponding sums then we would get:

CLOCK



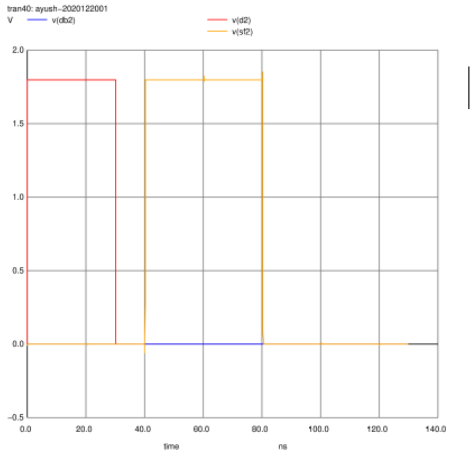
INPUT A3 + B3 = S3

0 + 1 = 1



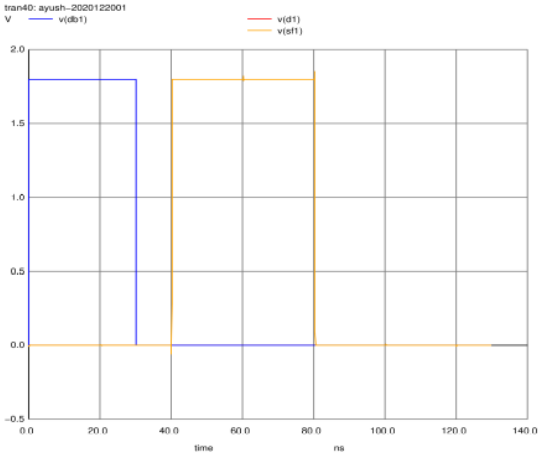
INPUT A2 + B2 = S2

1 + 0 = 1



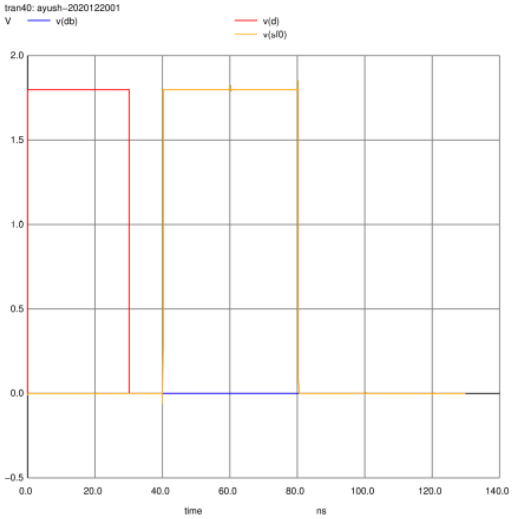
INPUT A1 + B1 = S1

0 + 1 = 1

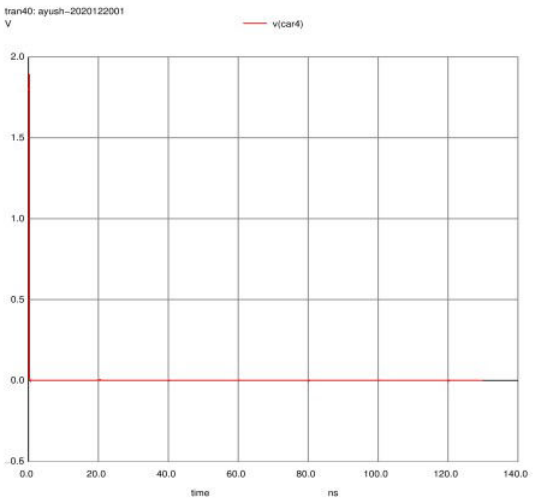


INPUT A0 + B0 = S0

1 + 0 = 1



OUTPUT CARRY = 0



So in the above cases we can see that CLA adder is working as expected and giving the desired value. Also it can be observed that the input is coming at the first positive edge and the corresponding output is at the 2nd positive edge of the clock as per the requirements of the question.

The worst case delay for my circuit is coming out as:

```
  Measurements for Transient Analysis

tprise_i3            =  4.009873e-09 targ=  5.000000e-11 trig=  -3.959873e-09
tpfall_i3            =  4.009873e-09 targ=  5.000000e-11 trig=  -3.959873e-09
tpd_i3               =  4.00987e-09
```

Worst case delay = 4ns

The **maximum clock frequency** till which the output is giving the correct output is 1/0.38ns = **2.63GHz.** On increasing the frequency more than this, leds to incorrect value.

So above we saw the implementation of whole CLA adder with the help of the NGSPICE. We also saw various blocks layout in MAGIC and their corresponding output. Now similar to how I combined all the blocks in NGSPICE to make CLA adder, I will combine all the blocks made in MAGIC to implement the CLA adder. So for that, the proposed floor plan is given below:

The corresponding netlist is given below:

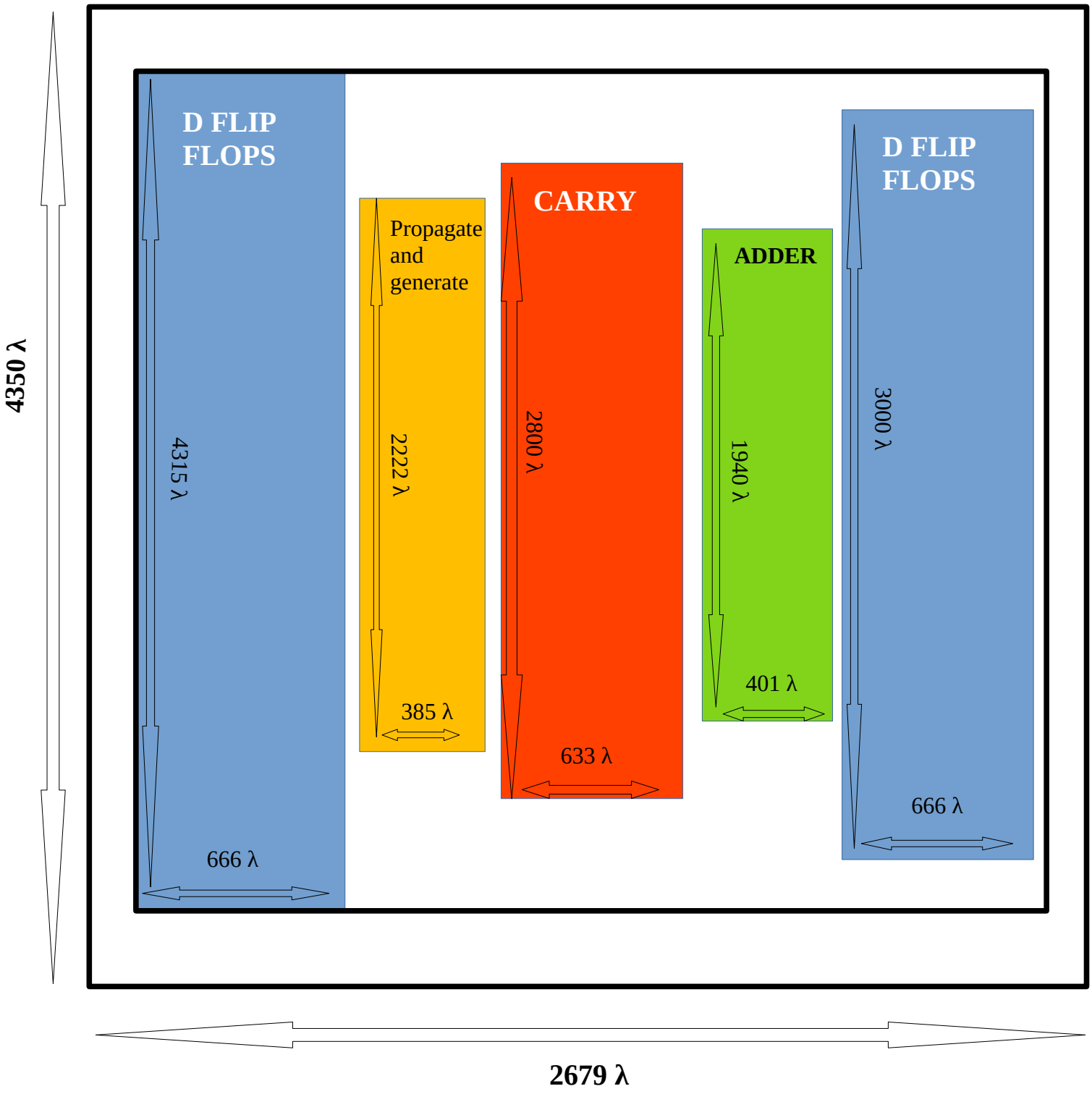
NETLIST of CLA adder with NGSPICE (prelayout):

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param w = {20*LAMBDA}
.param width_P={2*w}
.param width_N={2*w}
.global gnd vdd

Vdd     vdd     gnd     'SUPPLY'


*vin1 D  0 pulse 0 1.8 0n 100p 100p 30n 300n
*vin2 D1 0 pulse 31.1 1.8 0n 100p 100p 60 300n
*vin3 D2 0 pulse 0 1.8 0n 100p 100p 29.9n 60n
*vin4 D3 0 pwl (0 0v 49.9ns 0v 50ns 1.8v 100ns 1.8v)
*vin4 D3 0 pulse 0 1.8 0n 100p 100p 29.9n 60n


*vin5 Db  0 0
*vin6 Db1 0 0
*vin7 Db2 0 0
*vin8 Db3 0 0
**********************************************************************
vin1 D  0 pulse 0 1.8  0n 100p 100p 30n 500n
vin6 D1 0 pulse 0 0  0n 100p 100p 30n 500n
vin7 D2 0 pulse 0 1.8  0n 100p 100p 30n 500n
vin8 D3 0 pulse 0 0  0n 100p 100p 30n 500n


vin9 Db   0 pulse 0 0   0n 100p 10p 30n 500n
vin10 Db1 0 pulse 0 1.8   0n 100p 10p 30n 500n
vin11 Db2 0 pulse 0 0   0n 100p 10p 30n 500n
vin12 Db3 0 pulse 0 1.8   0n 100p 10p 30n 500n


*vin_clk clk 0 pulse 0 1.8 0.044n 100p 100p .2n .4n
vin_clk clk 0 pulse 0 1.8 0n 100p 100p 20n 40n
vin_carry cinp 0 pulse 0 0 0n 100p 10p 30n 500n

.subckt nand A B out vdd gnd
M1      out       A       k     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2      out       A       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3      k       B       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4      out       B       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends nand

.subckt inv yi xi vdd gnd
M1      yi       xi       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2      yi       xi       vdd     vdd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv

*********************************************************A**********************************
********************DFF1************************
x1 ox4 A0_bar A0 vdd gnd nand
x2 ox5 A0 A0_bar vdd gnd nand
x3 ox6 ox4 ox3 vdd gnd nand
x4 ox3 clk ox4 vdd gnd nand
x7 ox4 clk ox7 vdd gnd nand
x8 ox8 ox7 vdd gnd inv
x5 ox8 ox6 ox5 vdd gnd nand
x6 D ox5 ox6 vdd gnd nand
**********************************************************
********************DFF2************************
*** inverter***
x15 ox9 A1_bar A1 vdd gnd nand
x16 ox10 A1 A1_bar vdd gnd nand
x12 ox11 ox9 ox12 vdd gnd nand
x9 ox12 clk ox9 vdd gnd nand
x14 ox9 clk ox14 vdd gnd nand
x13 ox13 ox14 vdd gnd inv
x10 ox13 ox11 ox10 vdd gnd nand
x11 D1 ox10 ox11 vdd gnd nand
**********************************************************
********************DFF3************************
x24 ox17 A2_bar A2 vdd gnd nand
x23 ox18 A2 A2_bar vdd gnd nand
x22 ox19 ox17 ox22 vdd gnd nand
x17 ox22 clk ox17 vdd gnd nand
x20 ox17 clk ox20 vdd gnd nand
x21 ox21 ox20 vdd gnd inv
x18 ox21 ox19 ox18 vdd gnd nand
x19 D2 ox18 ox19 vdd gnd nand
**********************************************************
********************DFF4************************
x33 ox25 A3_bar A3 vdd gnd nand
x32 ox27 A3 A3_bar vdd gnd nand
x31 ox28 ox25 ox31 vdd gnd nand

x25 ox31 clk ox25 vdd gnd nand
x29 ox25 clk ox29 vdd gnd nand
x30 ox30 ox29 vdd gnd inv
x27 ox30 ox28 ox27 vdd gnd nand
x28 D3 ox27 ox28 vdd gnd nand
**********************************************************
*******************************************************************************************



*********************************************************B**********************************
********************DFFb1************************
x41 ox35 B0_bar B0 vdd gnd nand
x40 ox36 B0 B0_bar vdd gnd nand
x34 ox37 ox35 ox34 vdd gnd nand
x35 ox34 clk ox35 vdd gnd nand
x38 ox35 clk ox38 vdd gnd nand
x39 ox39 ox38 vdd gnd inv
x36 ox39 ox37 ox36 vdd gnd nand
x37 Db ox36 ox37 vdd gnd nand
**********************************************************

********************DFFb2************************
x51 ox42 B1_bar B1 vdd gnd nand
x50 ox43 B1 B1_bar vdd gnd nand
x49 ox46 ox42 ox49 vdd gnd nand
x42 ox49 clk ox42 vdd gnd nand
x47 ox42 clk ox47 vdd gnd nand
x48 ox48 ox47 vdd gnd inv
x43 ox48 ox46 ox43 vdd gnd nand
x46 Db1 ox43 ox46 vdd gnd nand
**********************************************************

********************DFFb3************************
x60 ox54 B2_bar B2 vdd gnd nand
x59 ox52 B2 B2_bar vdd gnd nand
x53 ox56 ox54 ox53 vdd gnd nand
x54 ox53 clk ox54 vdd gnd nand
x57 ox54 clk ox57 vdd gnd nand
x58 ox58 ox57 vdd gnd inv
x52 ox58 ox56 ox52 vdd gnd nand
x56 Db2 ox52 ox56 vdd gnd nand
**********************************************************

********************DFFb4************************
x61 ox64 B3_bar B3 vdd gnd nand
x62 ox65 B3 B3_bar vdd gnd nand
x63 ox66 ox64 ox63 vdd gnd nand
x64 ox63 clk ox64 vdd gnd nand

x67 ox64 clk ox67 vdd gnd nand
x68 ox68 ox67 vdd gnd inv
x65 ox68 ox66 ox65 vdd gnd nand
x66 Db3 ox65 ox66 vdd gnd nand
*******************************************************************************************



********************DFFcarr************************
x71 ox74 car0_bar car0 vdd gnd nand
x72 ox75 car0 car0_bar vdd gnd nand
x73 ox76 ox74 ox73 vdd gnd nand
x74 ox73 clk ox74 vdd gnd nand
x77 ox74 clk ox77 vdd gnd nand
x78 ox78 ox77 vdd gnd inv
x75 ox78 ox76 ox75 vdd gnd nand
x76 cinp ox75 ox76 vdd gnd nand


**********XOR gate******************
.subckt xor dda ddb outx vdd gnd
xx1 dda ddb outx1 vdd gnd nand
xx2 dda outx1 outx2 vdd gnd nand
xx3 ddb outx1 outx3 vdd gnd nand
xx4 outx2 outx3 outx vdd gnd nand
.ends xor

**************AND GATE******************
.subckt and_g in1 in2 aout vdd gnd
xx5 in1 in2 out_nan vdd gnd nand
xx6 aout out_nan  vdd gnd inv
.ends and_g

*****************OR GATE*****************
.subckt or_g inn1 inn2 orout vdd gnd
xx7 ou1 inn1 vdd gnd inv
xx8 ou2 inn2 vdd gnd inv
xx9 ou1 ou2 orout vdd gnd nand
.ends or_g


**********************Generate*********************

x140 A0 B0   g0 vdd gnd and_g
x141 A1 B1  g1 vdd gnd and_g
x142 A2 B2  g2 vdd gnd and_g
x143 A3 B3  g3 vdd gnd and_g
```

```
200
201 *********************Propagate*******************
202 x144 A0   B0   p0 vdd gnd xor
203 x145 A1  B1  p1 vdd gnd xor
204 x146 A2  B2  p2 vdd gnd xor
205 x147 A3  B3  p3 vdd gnd xor
206
207 *********************carry***********************
208 ******c1*********
209 x148 p0 car0 ccout1 vdd gnd and_g
210 x149 ccout1 g0 c1 vdd gnd or_g
211
212 ******c2*********
213 x150 car0 p1 ccout2 vdd gnd and_g
214 x151 ccout2 p0 ccout3 vdd gnd and_g
215 x152 p1 g0 ccout4 vdd gnd and_g
216 x153 ccout4 ccout3 ccout5 vdd gnd or_g
217 x154 ccout5 g1 c2 vdd gnd or_g
218
219 ******c3*********
220 x155 g1 p2 ccout6 vdd gnd and_g
221 x156 p2 p1 ccout7 vdd gnd and_g
222 x157 ccout7 g0 ccout8 vdd gnd and_g
223 x158 p2 p1 ccout9 vdd gnd and_g
224 x159 ccout9 p0 ccout10 vdd gnd and_g
225 x160 ccout10 car0 ccout11 vdd gnd and_g
226 x161 ccout6 ccout8 ccout12 vdd gnd or_g
227 x162 ccout11 g2 ccout13 vdd gnd or_g
228 x163 ccout12 ccout13 c3 vdd gnd or_g
229
230 ******c4*********
231 x164 car0 p0 ccout14 vdd gnd and_g
232 x165 ccout14 p1 ccout15 vdd gnd and_g
233 x166 ccout15 p2 ccout16 vdd gnd and_g
234 x167 ccout16 p3 ccout17 vdd gnd and_g
235 x168 p3 p2 ccout18 vdd gnd and_g
236 x169 p1 ccout18 ccout19 vdd gnd and_g
237 x170 ccout19 g0 ccout20 vdd gnd and_g
238 x171 p3 p2 ccout21 vdd gnd and_g
239 x172 g1 ccout21 ccout22 vdd gnd and_g
240 x173 g2 p3 ccout23 vdd gnd and_g
241 x174 ccout17 ccout20 ccout24 vdd gnd or_g
242 x175 ccout22 ccout23 ccout25 vdd gnd or_g
243 x176 ccout25 ccout24 ccout26 vdd gnd or_g
244 x177 ccout26 g3 c4 vdd gnd or_g
245
246 **************sum*******************************
247 x156 car0 p0 s0 vdd gnd xor
248 x157 c1 p1 s1 vdd gnd xor
249 x158 c2 p2 s2 vdd gnd xor
250 x159 c3 p3 s3 vdd gnd xor
```

```
250 x159 c3 p3 s3 vdd gnd xor
251
252
253 *************final out *************************
254 ******************DFFs0*********************
255 x89 ox84 sf0_bar sf0 vdd gnd nand
256 x82 ox85 sf0 sf0_bar vdd gnd nand
257 x83 ox86 ox84 ox83 vdd gnd nand
258 x84 ox83 clk ox84 vdd gnd nand
259 x87 ox84 clk ox87 vdd gnd nand
260 x88 ox88 ox87 vdd gnd inv
261 x85 ox88 ox86 ox85 vdd gnd nand
262 x86 s0 ox85 ox86 vdd gnd nand
263 ******************************************************
264 ******************DFFs1*********************
265 x91 ox94 sf1_bar sf1 vdd gnd nand
266 x92 ox95 sf1 sf1_bar vdd gnd nand
267 x93 ox96 ox94 ox93 vdd gnd nand
268 x94 ox93 clk ox94 vdd gnd nand
269 x97 ox94 clk ox97 vdd gnd nand
270 x98 ox98 ox97 vdd gnd inv
271 x95 ox98 ox96 ox95 vdd gnd nand
272 x96 s1 ox95 ox96 vdd gnd nand
273 ******************************************************
274
275 ******************DFFs2*********************
276 x101 ox104 sf2_bar sf2 vdd gnd nand
277 x102 ox105 sf2 sf2_bar vdd gnd nand
278 x103 ox106 ox104 ox103 vdd gnd nand
279 x104 ox103 clk ox104 vdd gnd nand
280 x107 ox104 clk ox107 vdd gnd nand
281 x108 ox108 ox107 vdd gnd inv
282 x105 ox108 ox106 ox105 vdd gnd nand
283 x106 s2 ox105 ox106 vdd gnd nand
284 ******************************************************
285
286 ******************DFFs3*********************
287 x111 ox114 sf3_bar sf3 vdd gnd nand
288 x112 ox115 sf3 sf3_bar vdd gnd nand
289 x113 ox116 ox114 ox113 vdd gnd nand
290 x114 ox113 clk ox114 vdd gnd nand
291 x117 ox114 clk ox117 vdd gnd nand
292 x118 ox118 ox117 vdd gnd inv
293 x115 ox118 ox116 ox115 vdd gnd nand
294 x116 s3 ox115 ox116 vdd gnd nand
295 ******************************************************
296
297 ******************DFFcarr*********************
298 x121 ox124 car4_bar car4 vdd gnd nand
299 x122 ox125 car4 car4_bar vdd gnd nand
300 x123 ox126 ox124 ox123 vdd gnd nand
300 x123 ox126 ox124 ox123 vdd gnd nand
301 x124 ox123 clk ox124 vdd gnd nand
302 x127 ox124 clk ox127 vdd gnd nand
303 x128 ox128 ox127 vdd gnd inv
304 x125 ox128 ox126 ox125 vdd gnd nand
305 x126 c4 ox125 ox126 vdd gnd nand
306 ******************************************************
307
308
309 .tran 0.1n 130n
310 .measure tran tprise_I3
311 + TRIG v(car4) VAL='SUPPLY*0.5' Fall=0
312 + TARG v(D) VAL='SUPPLY*0.5' RISE=0
313 .measure tran tpfall_I3
314 + TRIG v(car4) VAL='SUPPLY*0.5' RISE=0
315 + TARG v(D) VAL='SUPPLY*0.5' FALL=0
316 .measure tran tpd_I3 param='(tprise_I3+tpfall_I3)/2' goal=0
317
318 .control
319 set hcopypscolor = 1
320 set color0=white
321 set color1=black
322
323 run
324 set curplottitle="Ayush-2020122001"
325
326 *plot v(sf0) v(sf1)+4 v(sf2)+8 v(sf3)+12
327 plot v(clk)
328 *plot v(D) v(D1) v(D2) v(D3)
329 *plot v(Db) v(Db1) v(Db2) v(Db3)
330 *plot v(sf0) v(sf1) v(sf2) v(sf3)
331 *plot v(D) v(outs0) v(Db)
332 *plot v(D1)
333 *plot v(Db)
334 plot v(D) v(Db) v(sf0)
335 plot v(D1) v(Db1) v(sf1)
336 plot v(D2) v(Db2) v(sf2)
337 plot v(D3) v(Db3) v(sf3)
338 *plot v(car4)
339 *plot v(sf2)
340 *plot v(sf1)
341 *plot v(Db1)
342 *plot v(Db2)
343 *plot v(Db3)
344 *plot v(c3) v(p3)
345 *plot v(outs1)
346 *plot v(outs2)
347 *plot v(outs3)
348 plot v(car4)
```

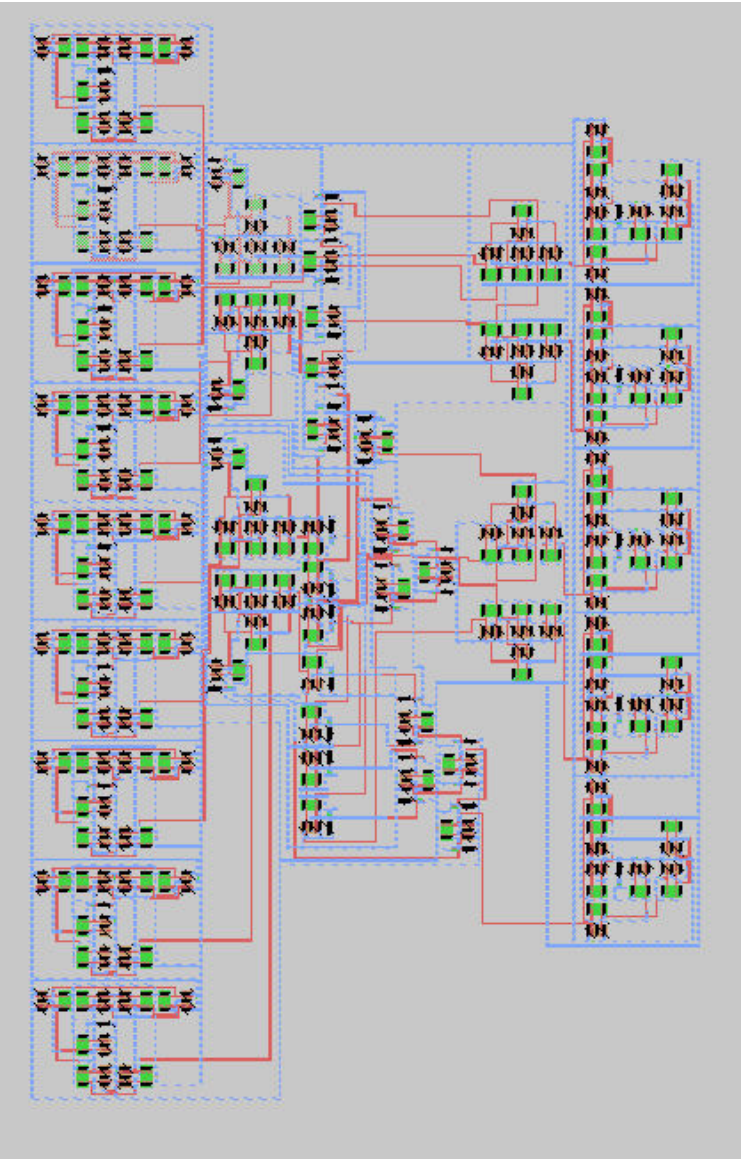
< SECTION 8 > Floor plan :



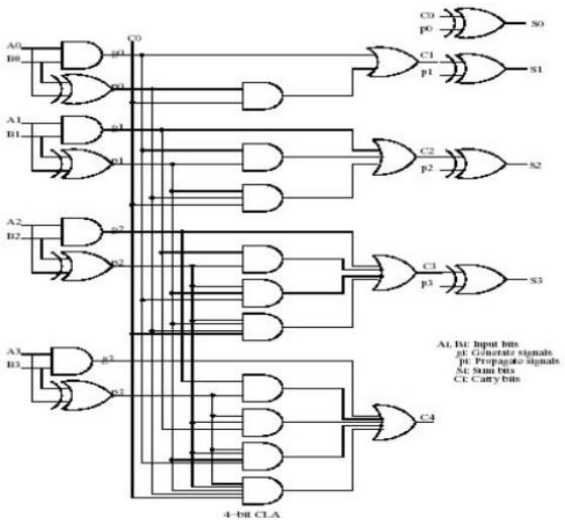
< SECTION 9 > CLA adder layout :

Till now all the simulation results were based on the NGSPICE implementation, now I will show the postlayout simulation results. Based on the above discussed floor plan I have made the CLA layout in MAGIC as given below:

MAGIC LAYOUT OF THE CLA ADDER



SCHEMATIC DIAGRAM OF CLA ADDER



So based on the above layout the corresponding simulation results are as follows:

Inputs:

A = 0101

B = 1010

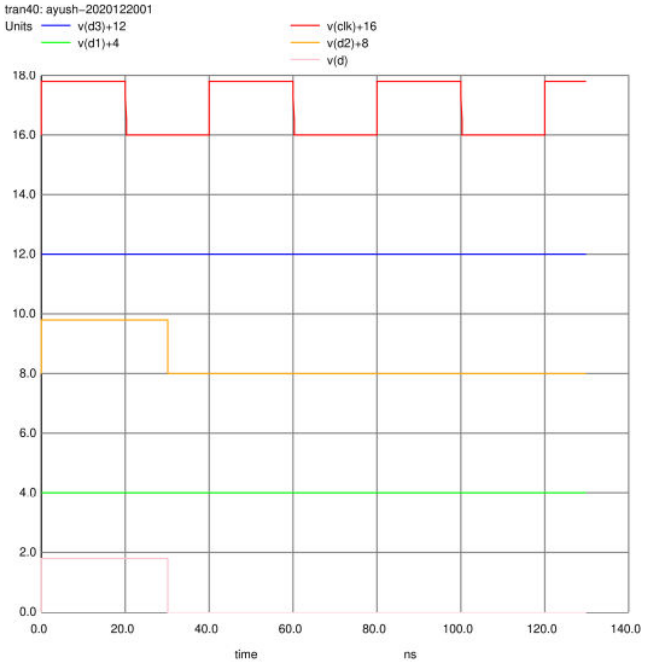
carry_in = 0

Outputs:

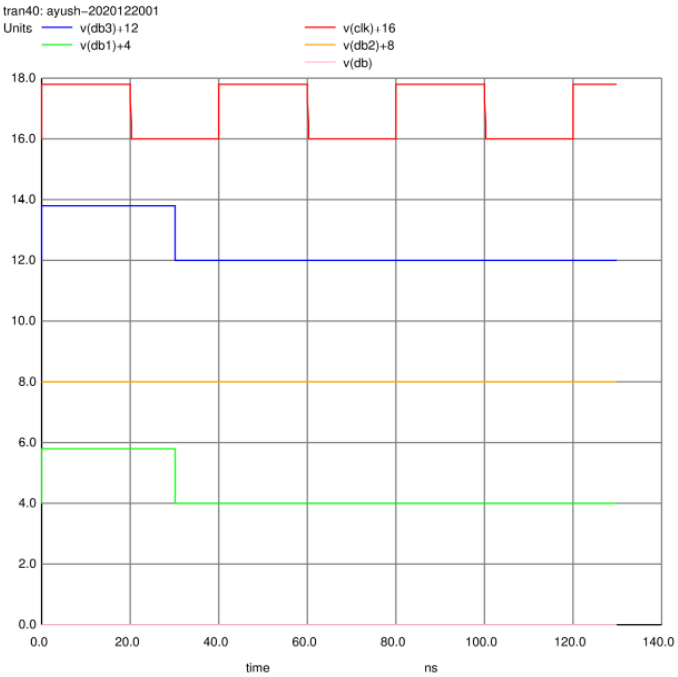
S = 1111

Carry_out = 0

INPUT A

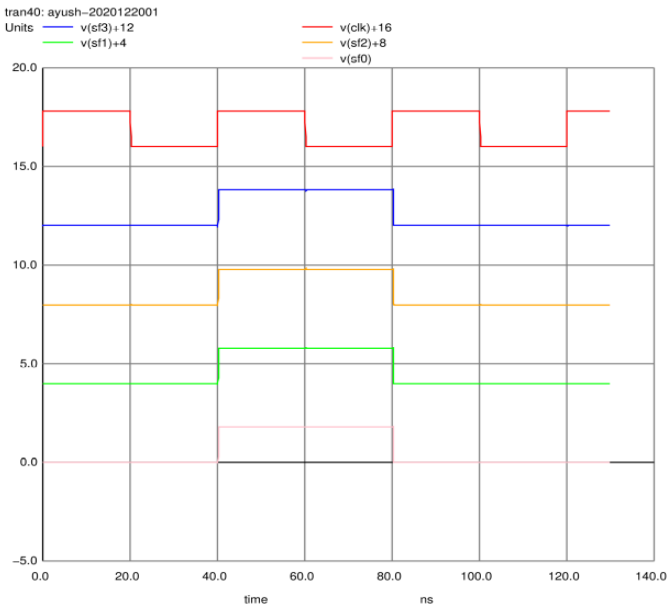


INPUT B



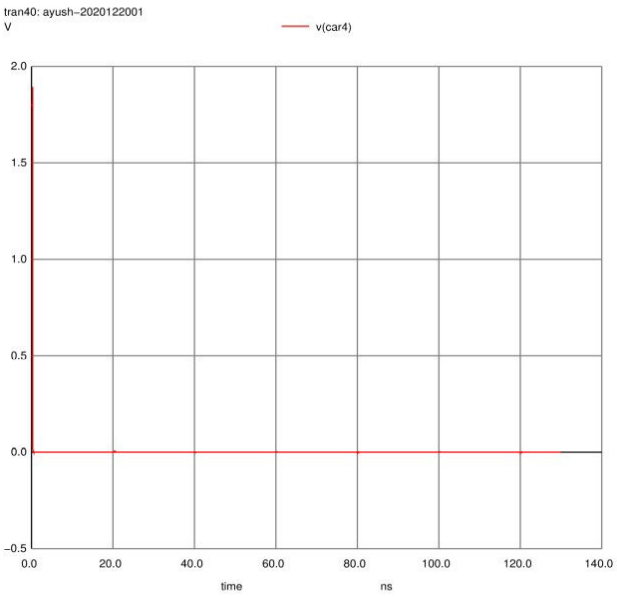
OUTPUT SUM

(Appearing at 2nd cycle)



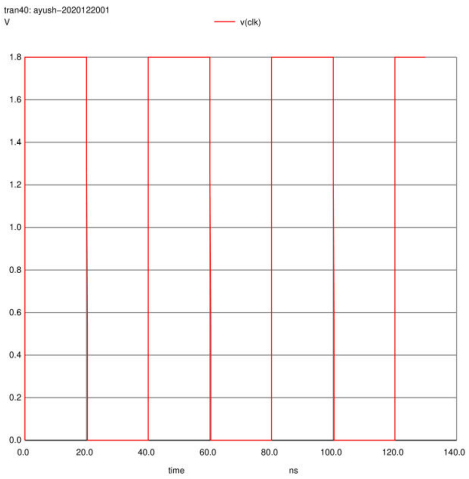
CARRY OUT

(Appearing at 2nd cycle)



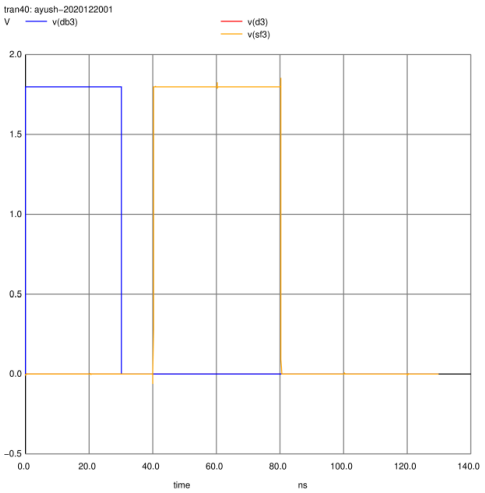
On looking in a more detail way to analyze bits and their corresponding sums then we would get:

CLOCK



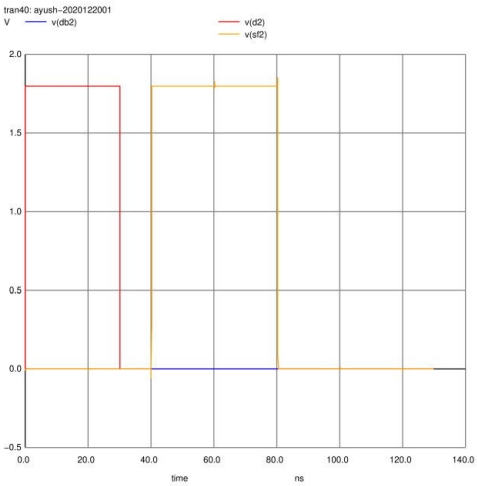
INPUT A3 + B3 = S3

0 + 1 = 1



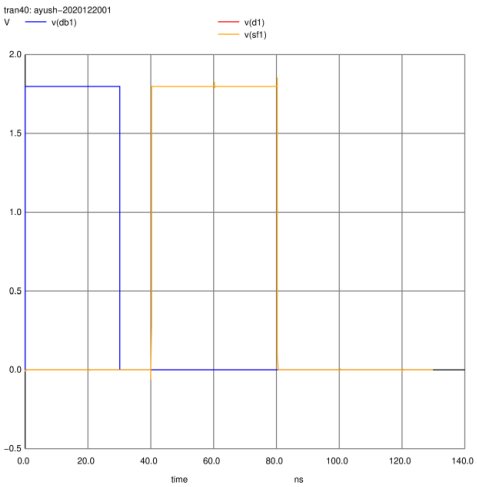
INPUT A2 + B2 = S2

1 + 0 = 1



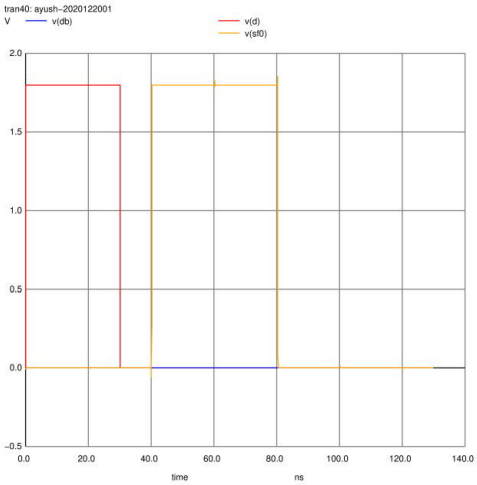
INPUT A1 + B1 = S1

0 + 1 = 1

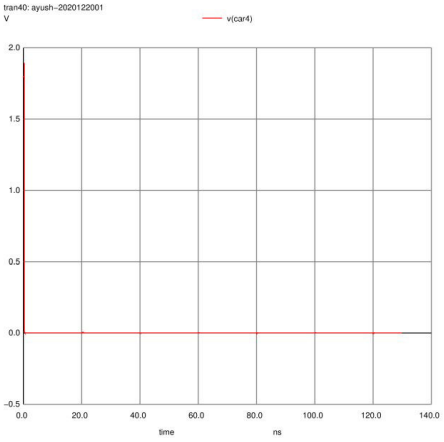


INPUT A0 + B0 = S0

1 + 0 = 1



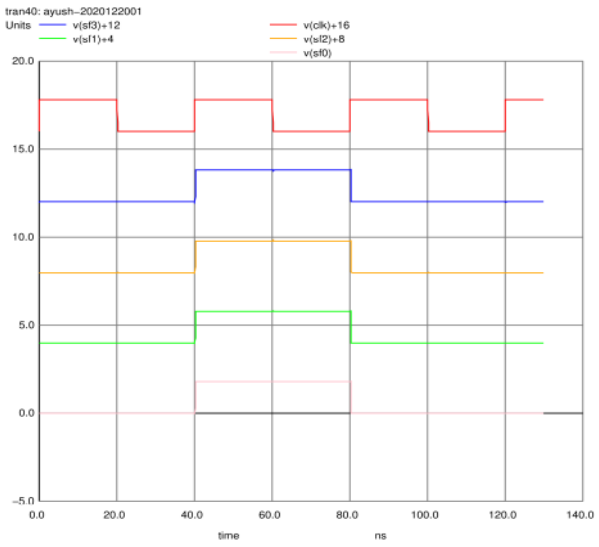
OUTPUT CARRY = 0



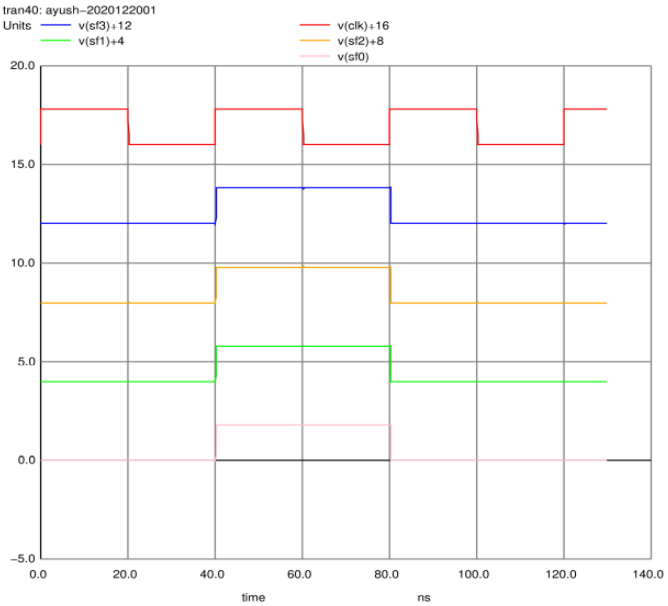
So it can be seen that the output is coming as expected and all the sum bits (yellow colour pulse in the above plot) are coming at the 2nd positive edge of the clock, as required by the question.

Lets look at the prelayout and postlayout result of the CLA adder for the above A = 0101 and B = 1010 :

PRE-LAYOUT SUM OUTPUT



POST-LAYOUT SUM OUTPUT



So we can see that the resulting output for the pre-layout and post-layout are coming out to be same in terms of sum's bit value, i.e. S = 1111 . Also as per the requirement of the question the output is appearing at the 2nd clock cycle. The difference between the pre-layout and post-layout CLA adder is the pressence of the paracitic capacitances in the post-layout implementation, which result in increase of the delay of the output. In the next section, I have compared the parameters of prelayout implementation and postlayout implementation.

NETLIST for post-layout CLA adder :

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param w = {10*LAMBDA}
.param width_P={2*w}
.param width_N={w}
.global gnd vdd


vin18 da0 0 pulse 0 1.8   0n 100p 100p 30n 500n.
vin6 D1 0   pulse 0 0     0n 100p 100p 30n 500n
vin7 D2 0   pulse 0 1.8   0n 100p 100p 30n 500n
vin8 D3 0   pulse 0 1.8   0n 100p 100p 30n 500n

vin14 carry_in 0 pulse 0 0   0n 100p 100p 30n 500n

vin13 D   0 pulse 0 1.8 0n 100p 100p 30n 500n
vin10 Db1 0 pulse 0 0 0n 100p 100p 30n 500n
vin11 Db2 0 pulse 0 0 0n 100p 100p 30n 500n
vin12 Db3 0 pulse 0 1.8 0n 100p 100p 30n 500n


vin5 Dcin 0 pulse 0 0 0n 100p 100p 30n 500n
*vincc cin0 0 1.8
vin_clk clk 0 pulse 0 1.8 0n 100p 100p 20n 40n
Vdd     vdd     gnd     'SUPPLY'




* SPICE3 file created from clafinal_v.ext - technology: scmos

.option scale=0.09u

M1000 a_30_n81# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=127561 ps=20791
M1001 a_109_86# S a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1002 a_109_86# p1 vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=252040 ps=41762
M1003 vdd S a_109_86# w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1004 vdd a_154_188# pin_p w_239_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1005 pin_p a_154_188# a_269_18# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1006 vdd a_109_86# a_154_106# w_124_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1007 a_154_188# p1 vdd w_124_179# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1008 a_154_106# a_109_86# a_154_18# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1009 vdd a_109_86# a_154_188# w_124_179# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1010 a_154_276# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1011 a_269_18# a_154_106# gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1012 a_154_188# a_109_86# a_154_276# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1013 a_154_18# S gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1014 pin_p a_154_106# vdd w_239_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1015 a_154_106# S vdd w_124_99# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1016 gout m1_83_86# gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1017 gout m1_83_86# vdd w_86_n4# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1018 a_30_n81# p1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1019 m1_83_86# S a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1020 m1_83_86# p1 vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1021 vdd S m1_83_86# w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1022 a_195_n244# a_30_n223# gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1023 a_195_n244# a_30_n223# vdd w_86_n4# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1024 a_30_n81# a_n7_n412# gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1025 a_67_n144# a_30_n141# a_30_n81# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1026 a_67_n144# a_n7_n412# vdd w_0_0# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1027 vdd a_30_n141# a_67_n144# w_0_0# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1028 vdd a_n7_n412# a_67_n474# w_176_n229# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1029 S a_30_n141# vdd w_302_n149# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1030 a_30_n223# a_30_n141# a_30_n311# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1031 a_n7_n412# a_67_n474# a_30_n383# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1032 vdd S S_bar w_302_n229# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1033 a_332_n52# a_30_n141# gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1034 a_67_n474# a_195_n244# vdd w_176_n229# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1035 S S_bar a_332_n52# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1036 a_30_n311# clk gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1037 a_30_n383# D gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1038 vdd a_67_n144# a_30_n141# w_0_n150# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1039 S_bar a_67_n474# vdd w_302_n229# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1040 a_67_n474# a_n7_n412# a_206_n310# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1041 vdd a_67_n474# a_n7_n412# w_0_n480# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1042 S_bar S a_332_n310# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1043 a_30_n141# clk vdd w_0_n150# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1044 a_30_n53# clk gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1045 vdd a_30_n141# a_30_n223# w_0_n230# CMOSP w=40 l=2
+  ad=0 pd=0 as=1384 ps=122
M1046 a_206_n310# a_195_n244# gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1047 a_n7_n412# D vdd w_0_n480# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1048 a_332_n310# a_67_n474# gnd Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1049 a_30_n141# a_67_n144# a_30_n53# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=0 ps=0
M1050 vdd S_bar S w_302_n149# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1051 a_30_n223# clk vdd w_0_n230# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1052 a_2252_2303# a_2252_2551# a_2252_2391# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1053 a_112_2288# a_21_2286# a_24_2288# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1054 vdd dfo1 dfo2 w_2222_3284# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1055 a_2363_3497# a_2252_3541# gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1056 a_1108_2669# a_1105_2667# a_1108_2648# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1057 a 2252 901# a 2252 983# a 2252 813# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1058 vdd a_1315_2726# cin2 w_1313_2589# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1059 gnd a_184_3225# a_182_3107# Gnd CMOSN w=20 l=2
+  ad=0 pd=0 as=100 ps=50
M1060 a_2215_712# a_2289_650# a_2252_741# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1061 vdd a_2215_2692# a_2289_2630# w_2398_2875# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1062 a_351_1807# a_181_1807# vdd w_595_1779# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1063 gnd a_21_4201# a_185_3901# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1064 sum_3 a_2252_1643# vdd w_2524_1635# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1065 vdd a_1107_2897# a_1148_2781# w_1181_2851# CMOSP w=50 l=2
+  ad=0 pd=0 as=250 ps=110
M1066 a_811_1702# B3 a_712_1646# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1067 a_514_372# a_181_370# a_351_370# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1068 a_2363_857# a_2252_901# vdd w_2349_887# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1069 vdd carry_4 carry_4_bar w_2524_895# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1070 vdd a_1953_2899# add_out1 w_2038_2972# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1071 gnd gout3 a_1382_2136# Gnd CMOSN w=20 l=2
+  ad=0 pd=0 as=100 ps=50
M1072 vdd a_1108_2648# a_1315_2726# w_1298_2720# CMOSP w=50 l=2
+  ad=0 pd=0 as=250 ps=110
M1073 a_442_2767# a_351_2765# a_181_2765# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1074 vdd a_759_1974# a_883_1975# w_853_1966# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1075 vdd B2 a_759_2277# w_729_2270# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1076 vdd dfi1 a_2252_3871# w_2222_3864# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1077 vdd clk a_184_830# w_265_821# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1078 a_185_1965# B1 vdd w_266_1956# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1079 add_out3 a_1953_1855# vdd w_2038_1846# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1080 B1 a_185_1965# vdd w_346_1956# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1081 gnd a_181_1807# a_443_1507# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1082 a_712_2772# B1 vdd w_714_2798# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
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M1083 gout3 a_712_2643# vdd w_698_2631# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1084 sum_2_bar a_2289_1970# vdd w_2524_2215# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1085 vdd cin1 a_1829_2980# w_1799_2971# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1086 a_1107_2918# a_998_3101# a_1107_2897# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1087 vdd a_182_1191# a_21_1328# w_266_1124# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1088 a_185_1633# a_24_1809# a_21_1807# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1089 pin_p4 a_883_1893# a_998_2063# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1090 vdd cin0 a_1829_3377# w_1799_3370# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1091 a_1829_1854# pin_p4 vdd w_1799_1845# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1092 vdd a_1094_3546# cin1 w_1178_3479# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1093 a_2252_1231# a_2215_712# vdd w_2222_1224# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1094 a_2554_3052# a_2252_2963# gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1095 a_998_3101# a_883_3101# vdd w_968_3092# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1096 a_184_1809# a_181_1807# a_184_1788# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1097 vdd gout3 a_1106_1071# w_1076_1062# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1098 vdd clk a_184_1309# w_265_1300# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1099 a_1829_2251# pin_p3 vdd w_1799_2244# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1100 gnd a_184_351# a_182_233# Gnd CMOSN w=20 l=2
+  ad=0 pd=0 as=100 ps=50
M1101 vdd clk a_181_1328# w_345_1300# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1102 a_1106_3102# a_998_3101# vdd w_1187_3093# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1103 a_759_1974# B3 a_759_2062# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1104 a_2252_2133# clk gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1105 sum_3_bar sum_3 a_2554_1474# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1106 a_1106_1532# pin_p4 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1107 a_1147_1642# a_1113_2276# gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1108 a_2252_2061# add_out2 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1109 a_21_370# a_24_372# vdd w_266_166# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1110 gnd Db1 a_112_2288# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1111 a_759_3100# A1 vdd w_729_3091# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1112 a_24_2767# a_21_2765# vdd w_15_2737# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1113 gnd a_1147_1642# a_1378_2371# Gnd CMOSN w=20 l=2
+  ad=0 pd=0 as=100 ps=50
M1114 a_2252_2963# clk vdd w_2222_2954# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1115 vdd sum_2_bar sum_2 w_2524_2295# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1116 gnd a_1105_2706# a_1108_2669# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1117 a_883_2358# a_759_2277# a_883_2446# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1118 a_21_3244# a_24_3246# vdd w_266_3040# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1119 vdd a_24_1809# a_351_1807# w_595_1779# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1120 a_514_2288# a_181_2286# a_351_2286# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1121 a_1113_2276# a_1148_2567# a_1113_2188# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1122 a_112_851# a_21_849# a_24_851# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1123 a_112_4203# a_21_4201# a_24_4203# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1124 vdd a_184_2746# a_182_2628# w_258_2682# CMOSP w=50 l=2
+  ad=0 pd=0 as=250 ps=110
M1125 a_1113_2028# a_1148_2781# a_1113_2116# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1126 a_2428_3454# a_2363_3497# gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1127 vdd a_184_351# a_182_233# w_258_287# CMOSP w=50 l=2
+  ad=0 pd=0 as=250 ps=110
M1128 gnd A3 a_811_1702# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1129 vdd a_2289_1310# a_2215_1372# w_2222_1304# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1130 a_2363_1517# a_2252_1561# gnd Gnd CMOSN w=20 l=2
+  ad=100 pd=50 as=0 ps=0
M1131 gnd a_24_372# a_514_372# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1132 a_184_3225# a_181_3244# vdd w_265_3216# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1133 a_1110_1733# pin_p4 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1134 a_181_3244# a_351_3244# vdd w_345_3216# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1135 gnd clk a_442_2767# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1136 a_2252_3541# clk vdd w_2222_3534# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1137 a_1644_1059# gout4 vdd w_1720_988# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1138 a_1953_3458# a_1829_3377# a_1953_3546# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1139 vdd sum_1 sum_1_bar w_2524_2875# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1140 a_1953_3069# cin1 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1141 a_185_2465# A1 a_185_2444# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1142 vdd a_21_2286# a_185_1965# w_266_1956# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1143 vdd a_181_2286# B1 w_346_1956# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1144 carry_4 a_2252_983# vdd w_2524_975# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1145 a_1953_2420# pin_p3 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1146 vdd A1 a_712_2772# w_714_2798# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1147 a_1410_2619# a_1315_2560# cin2 Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1148 sum_out dfi2 a_2554_3712# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1149 gnd gout a_1107_2918# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1150 gnd a_182_1670# a_185_1633# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1151 vdd a_2252_1643# a_2252_1891# w_2222_1884# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1152 a_185_3880# p1 vdd w_266_3871# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1153 a_185_675# a_24_851# a_21_849# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1154 p1 a_185_3880# vdd w_346_3871# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1155 gnd clk a_184_1809# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1156 a_2252_2881# a_2252_2963# a_2252_2793# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1157 vdd a_1103_3160# a_1106_3102# w_1187_3093# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1158 a_1647_1061# a_1644_1059# carr4 Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1159 a_2215_2692# a_2289_2630# a_2252_2721# Gnd CMOSN w=40 l=2
+  ad=760 pd=118 as=1480 ps=154
M1160 vdd a_2252_3871# dfi1 w_2222_3614# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1161 a_2554_1072# a_2252_983# gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1162 vdd a_182_233# a_21_370# w_266_166# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1163 vdd D1 a_24_2767# w_15_2737# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1164 vdd a_181_370# B3 w_346_40# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1165 gnd a_184_1788# a_182_1670# Gnd CMOSN w=20 l=2
+  ad=0 pd=0 as=100 ps=50
M1166 a_883_2188# B2 gnd Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1167 gnd gout a_1094_3546# Gnd CMOSN w=20 l=2
+  ad=0 pd=0 as=100 ps=50
M1168 a_1653_1321# a_1486_1258# vdd w_1729_1250# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1169 a_1113_1930# pin_p3 vdd w_1083_1923# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1170 a_181_370# a_351_370# vdd w_345_342# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1171 vdd a_1097_3323# a_1103_3160# w_1171_3277# CMOSP w=50 l=2
+  ad=0 pd=0 as=250 ps=110
M1172 vdd a_182_3107# a_21_3244# w_266_3040# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1173 a_2363_3497# a_2252_3541# vdd w_2349_3527# CMOSP w=50 l=2
+  ad=250 pd=110 as=0 ps=0
M1174 vdd a_1829_2980# a_1953_2899# w_1923_2892# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1175 gnd a_24_2288# a_514_2288# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1176 vdd a_1829_2251# a_1953_2250# w_1923_2243# CMOSP w=40 l=2
+  ad=0 pd=0 as=1480 ps=154
M1177 gnd D3 a_112_851# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1178 gnd da0 a_112_4203# Gnd CMOSN w=40 l=2
+  ad=0 pd=0 as=0 ps=0
M1179 a_1953_1773# pin_p4 vdd w_1923_1766# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1180 a_442_1330# a_351_1328# a_181_1328# Gnd CMOSN w=40 l=2
+  ad=1480 pd=154 as=760 ps=118
M1181 pin_p3 a_883_2276# vdd w_968_2269# CMOSP w=40 l=2
+  ad=1480 pd=154 as=0 ps=0
M1182 vdd clk a_184_3225# w_265_3216# CMOSP w=40 l=2
+  ad=0 pd=0 as=0 ps=0
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404 +  ad=100 pd=50 as=0 ps=0
405 M1184 a_1953_3288# cin0 gnd Gnd CMOSN w=40 l=2
406 +  ad=1480 pd=154 as=0 ps=0
407 M1185 a_1143_1441# a_1113_2028# gnd Gnd CMOSN w=20 l=2
408 +  ad=100 pd=50 as=0 ps=0
409 M1186 a_514_4203# a_181_4201# a_351_4201# Gnd CMOSN w=40 l=2
410 +  ad=1480 pd=154 as=760 ps=118
411 M1187 vdd clk a_181_3244# w_345_3216# CMOSP w=40 l=2
412 +  ad=0 pd=0 as=0 ps=0
413 M1188 a_1143_1441# a_1113_2028# vdd w_1192_2003# CMOSP w=50 l=2
414 +  ad=250 pd=110 as=0 ps=0
415 M1189 gnd a_21_2765# a_185_2465# Gnd CMOSN w=40 l=2
416 +  ad=0 pd=0 as=0 ps=0
417 M1190 a_1486_1258# a_1479_1199# vdd w_1477_1228# CMOSP w=40 l=2
418 +  ad=1480 pd=154 as=0 ps=0
419 M1191 a_2428_1474# a_2363_1517# gnd Gnd CMOSN w=40 l=2
420 +  ad=1480 pd=154 as=0 ps=0
421 M1192 B3 a_185_49# vdd w_346_40# CMOSP w=40 l=2
422 +  ad=0 pd=0 as=0 ps=0
423 M1193 a_1097_3344# cin0 a_1097_3323# Gnd CMOSN w=40 l=2
424 +  ad=1480 pd=154 as=760 ps=118
425 M1194 a_2554_3454# dfo1 gnd Gnd CMOSN w=40 l=2
426 +  ad=1480 pd=154 as=0 ps=0
427 M1195 a_1656_1323# a_1653_1321# a_1656_1302# Gnd CMOSN w=40 l=2
428 +  ad=1480 pd=154 as=760 ps=118
429 M1196 a_883_3019# A1 vdd w_853_3012# CMOSP w=40 l=2
430 +  ad=1480 pd=154 as=0 ps=0
431 M1197 add_out a_1953_3376# vdd w_2038_3369# CMOSP w=40 l=2
432 +  ad=1480 pd=154 as=0 ps=0
433 M1198 a_1108_2648# a_1105_2667# vdd w_1189_2639# CMOSP w=40 l=2
434 +  ad=1480 pd=154 as=0 ps=0
435 M1199 a_2252_1561# clk vdd w_2222_1554# CMOSP w=40 l=2
436 +  ad=1480 pd=154 as=0 ps=0
437 M1200 gnd a_1315_2726# a_1410_2619# Gnd CMOSN w=40 l=2
438 +  ad=0 pd=0 as=0 ps=0
439 M1201 vdd a_21_4201# a_185_3880# w_266_3871# CMOSP w=40 l=2
440 +  ad=0 pd=0 as=0 ps=0
441 M1202 gnd a_182_712# a_185_675# Gnd CMOSN w=40 l=2
442 +  ad=0 pd=0 as=0 ps=0
443 M1203 vdd a_181_4201# p1 w_346_3871# CMOSP w=40 l=2
444 +  ad=0 pd=0 as=0 ps=0
445 M1204 a_2252_2463# a_2215_2032# gnd Gnd CMOSN w=40 l=2
446 +  ad=1480 pd=154 as=0 ps=0
447 M1205 vdd a_1829_1854# a_1953_1855# w_1923_1846# CMOSP w=40 l=2
448 +  ad=0 pd=0 as=1480 ps=154
449 M1206 a_2252_2391# clk gnd Gnd CMOSN w=40 l=2
450 +  ad=0 pd=0 as=0 ps=0
451 M1207 sum_3 sum_3_bar a_2554_1732# Gnd CMOSN w=40 l=2
452 +  ad=760 pd=118 as=1480 ps=154
453 M1208 gnd a_1644_1098# a_1647_1061# Gnd CMOSN w=40 l=2
454 +  ad=0 pd=0 as=0 ps=0

455 M1209 a_1315_2560# gout2 vdd w_1298_2546# CMOSP w=50 l=2
456 +  ad=250 pd=110 as=0 ps=0
457 M1210 a_1382_1970# a_1143_1239# gnd Gnd CMOSN w=20 l=2
458 +  ad=100 pd=50 as=0 ps=0
459 M1211 a_24_1330# a_21_1328# vdd w_15_1300# CMOSP w=40 l=2
460 +  ad=1480 pd=154 as=0 ps=0
461 M1212 dfo2 add_out vdd w_2222_3284# CMOSP w=40 l=2
462 +  ad=0 pd=0 as=0 ps=0
463 M1213 a_1147_1642# a_1113_2276# vdd w_1192_2262# CMOSP w=50 l=2
464 +  ad=250 pd=110 as=0 ps=0
465 M1214 a_443_1986# a_185_1965# B1 Gnd CMOSN w=40 l=2
466 +  ad=1480 pd=154 as=760 ps=118
467 M1215 a_2289_2630# a_2363_2837# vdd w_2398_2875# CMOSP w=40 l=2
468 +  ad=0 pd=0 as=0 ps=0
469 M1216 a_811_2828# B1 a_712_2772# Gnd CMOSN w=40 l=2
470 +  ad=1480 pd=154 as=760 ps=118
471 M1217 a_351_370# a_181_370# vdd w_595_342# CMOSP w=40 l=2
472 +  ad=1480 pd=154 as=0 ps=0
473 M1218 a_1107_2897# a_998_3101# vdd w_1188_2888# CMOSP w=40 l=2
474 +  ad=1480 pd=154 as=0 ps=0
475 M1219 add_out3 a_1953_1773# a_2068_1943# Gnd CMOSN w=40 l=2
476 +  ad=760 pd=118 as=1480 ps=154
477 M1220 a_21_1807# a_24_1809# vdd w_266_1603# CMOSP w=40 l=2
478 +  ad=1480 pd=154 as=0 ps=0
479 M1221 a_1482_1493# a_1475_1434# vdd w_1473_1463# CMOSP w=40 l=2
480 +  ad=1480 pd=154 as=0 ps=0
481 M1222 vdd clk a_181_370# w_345_342# CMOSP w=40 l=2
482 +  ad=0 pd=0 as=0 ps=0
483 M1223 vdd a_184_1309# a_182_1191# w_258_1245# CMOSP w=50 l=2
484 +  ad=0 pd=0 as=250 ps=110
485 M1224 vdd a_759_3100# a_883_3101# w_853_3092# CMOSP w=40 l=2
486 +  ad=0 pd=0 as=1480 ps=154
487 M1225 vdd a_2252_1891# a_2252_1643# w_2222_1634# CMOSP w=40 l=2
488 +  ad=0 pd=0 as=1480 ps=154
489 M1226 add_out1 a_1953_2981# vdd w_2038_2972# CMOSP w=40 l=2
490 +  ad=0 pd=0 as=0 ps=0
491 M1227 a_883_1975# B3 vdd w_853_1966# CMOSP w=40 l=2
492 +  ad=0 pd=0 as=0 ps=0
493 M1228 a_759_2277# A2 vdd w_729_2270# CMOSP w=40 l=2
494 +  ad=0 pd=0 as=0 ps=0
495 M1229 a_184_1788# a_181_1807# vdd w_265_1779# CMOSP w=40 l=2
496 +  ad=1480 pd=154 as=0 ps=0
497 M1230 a_2252_3871# dfo2 vdd w_2222_3864# CMOSP w=40 l=2
498 +  ad=0 pd=0 as=0 ps=0
499 M1231 a_181_1807# a_351_1807# vdd w_345_1779# CMOSP w=40 l=2
500 +  ad=1480 pd=154 as=0 ps=0
501 M1232 a_1829_1854# carry_3 a_1829_1942# Gnd CMOSN w=40 l=2
502 +  ad=760 pd=118 as=1480 ps=154
503 M1233 gnd clk a_442_1330# Gnd CMOSN w=40 l=2
504 +  ad=0 pd=0 as=0 ps=0

505 M1234 a_2363_1517# a_2252_1561# vdd w_2349_1547# CMOSP w=50 l=2
506 +  ad=250 pd=110 as=0 ps=0
507 M1235 a_2252_901# clk vdd w_2222_894# CMOSP w=40 l=2
508 +  ad=1480 pd=154 as=0 ps=0
509 M1236 a_2289_1970# a_2215_2032# a_2428_2134# Gnd CMOSN w=40 l=2
510 +  ad=760 pd=118 as=1480 ps=154
511 M1237 a_998_3101# a_883_3019# a_998_3189# Gnd CMOSN w=40 l=2
512 +  ad=760 pd=118 as=1480 ps=154
513 M1238 a_185_1028# B2 a_185_1007# Gnd CMOSN w=40 l=2
514 +  ad=1480 pd=154 as=760 ps=118
515 M1239 gnd a_24_4203# a_514_4203# Gnd CMOSN w=40 l=2
516 +  ad=0 pd=0 as=0 ps=0
517 M1240 a_1829_2980# a_998_3101# vdd w_1799_2971# CMOSP w=40 l=2
518 +  ad=0 pd=0 as=0 ps=0
519 M1241 a_112_2767# a_21_2765# a_24_2767# Gnd CMOSN w=40 l=2
520 +  ad=1480 pd=154 as=760 ps=118
521 M1242 vdd a_1479_1365# a_1486_1258# w_1477_1228# CMOSP w=40 l=2
522 +  ad=0 pd=0 as=0 ps=0
523 M1243 a_1199_1304# a_1106_1348# gnd Gnd CMOSN w=20 l=2
524 +  ad=100 pd=50 as=0 ps=0
525 M1244 a_998_2063# a_883_1975# gnd Gnd CMOSN w=40 l=2
526 +  ad=0 pd=0 as=0 ps=0
527 M1245 gnd pin_p a_1097_3344# Gnd CMOSN w=40 l=2
528 +  ad=0 pd=0 as=0 ps=0
529 M1246 vdd a_2252_2303# a_2252_2221# w_2222_2214# CMOSP w=40 l=2
530 +  ad=0 pd=0 as=1480 ps=154
531 M1247 a_1378_2205# a_1143_1441# gnd Gnd CMOSN w=20 l=2
532 +  ad=100 pd=50 as=0 ps=0
533 M1248 a_1829_3377# pin_p vdd w_1799_3370# CMOSP w=40 l=2
534 +  ad=0 pd=0 as=0 ps=0
535 M1249 gnd a_1653_1360# a_1656_1323# Gnd CMOSN w=40 l=2
536 +  ad=0 pd=0 as=0 ps=0
537 M1250 vdd a_1105_2706# a_1108_2648# w_1189_2639# CMOSP w=40 l=2
538 +  ad=0 pd=0 as=0 ps=0
539 M1251 a_1106_1071# pin_p4 vdd w_1076_1062# CMOSP w=40 l=2
540 +  ad=0 pd=0 as=0 ps=0
541 M1252 a_759_3100# B1 a_759_3188# Gnd CMOSN w=40 l=2
542 +  ad=760 pd=118 as=1480 ps=154
543 M1253 a_351_2286# a_181_2286# vdd w_595_2258# CMOSP w=40 l=2
544 +  ad=1480 pd=154 as=0 ps=0
545 M1254 a_2252_3211# a_2252_2963# a_2252_3123# Gnd CMOSN w=40 l=2
546 +  ad=760 pd=118 as=1480 ps=154
547 M1255 vdd a_1199_1304# a_1479_1365# w_1462_1359# CMOSP w=50 l=2
548 +  ad=0 pd=0 as=250 ps=110
549 M1256 a_2428_814# a_2363_857# gnd Gnd CMOSN w=40 l=2
550 +  ad=1480 pd=154 as=0 ps=0
551 M1257 a_2252_2963# a_2252_3211# a_2252_3051# Gnd CMOSN w=40 l=2
552 +  ad=760 pd=118 as=1480 ps=154
553 M1258 vdd carry_4_bar carry_4 w_2524_975# CMOSP w=40 l=2
554 +  ad=0 pd=0 as=0 ps=0

556 +  ad=0 pd=0 as=0 ps=0
557 M1260 a_1106_1348# a_1143_1239# a_1106_1260# Gnd CMOSN w=40 l=2
558 +  ad=760 pd=118 as=1480 ps=154
559 M1261 a_2554_1474# a_2289_1310# gnd Gnd CMOSN w=40 l=2
560 +  ad=0 pd=0 as=0 ps=0
561 M1262 a_514_851# a_181_849# a_351_849# Gnd CMOSN w=40 l=2
562 +  ad=1480 pd=154 as=760 ps=118
563 M1263 vdd dfo2 dfo1 w_2398_3535# CMOSP w=40 l=2
564 +  ad=0 pd=0 as=1480 ps=154
565 M1264 a_442_3246# a_351_3244# a_181_3244# Gnd CMOSN w=40 l=2
566 +  ad=1480 pd=154 as=760 ps=118
567 M1265 a_883_1893# a_759_1974# a_883_1805# Gnd CMOSN w=40 l=2
568 +  ad=760 pd=118 as=1480 ps=154
569 M1266 vdd Db2 a_24_1330# w_15_1300# CMOSP w=40 l=2
570 +  ad=0 pd=0 as=0 ps=0
571 M1267 a_185_2444# A1 vdd w_266_2435# CMOSP w=40 l=2
572 +  ad=1480 pd=154 as=0 ps=0
573 M1268 sum_2 a_2252_2303# vdd w_2524_2295# CMOSP w=40 l=2
574 +  ad=0 pd=0 as=0 ps=0
575 M1269 a_883_2446# A2 gnd Gnd CMOSN w=40 l=2
576 +  ad=0 pd=0 as=0 ps=0
577 M1270 add_out2 a_1953_2332# a_2068_2162# Gnd CMOSN w=40 l=2
578 +  ad=760 pd=118 as=1480 ps=154
579 M1271 gnd a_181_2286# a_443_1986# Gnd CMOSN w=40 l=2
580 +  ad=0 pd=0 as=0 ps=0
581 M1272 a_443_70# a_185_49# B3 Gnd CMOSN w=40 l=2
582 +  ad=1480 pd=154 as=760 ps=118
583 M1273 A1 a_185_2444# vdd w_346_2435# CMOSP w=40 l=2
584 +  ad=1480 pd=154 as=0 ps=0
585 M1274 gnd A1 a_811_2828# Gnd CMOSN w=40 l=2
586 +  ad=0 pd=0 as=0 ps=0
587 M1275 a_1113_2188# pin_p3 gnd Gnd CMOSN w=40 l=2
588 +  ad=0 pd=0 as=0 ps=0
589 M1276 a_185_70# B3 a_185_49# Gnd CMOSN w=40 l=2
590 +  ad=1480 pd=154 as=760 ps=118
591 M1277 vdd a_24_372# a_351_370# w_595_342# CMOSP w=40 l=2
592 +  ad=0 pd=0 as=0 ps=0
593 M1278 vdd gout a_1107_2897# w_1188_2888# CMOSP w=40 l=2
594 +  ad=0 pd=0 as=0 ps=0
595 M1279 a_185_2112# a_24_2288# a_21_2286# Gnd CMOSN w=40 l=2
596 +  ad=1480 pd=154 as=760 ps=118
597 M1280 a_1113_2116# pin_p3 gnd Gnd CMOSN w=40 l=2
598 +  ad=0 pd=0 as=0 ps=0
599 M1281 vdd a_182_1670# a_21_1807# w_266_1603# CMOSP w=40 l=2
600 +  ad=0 pd=0 as=0 ps=0
601 M1282 vdd a_1475_1600# a_1482_1493# w_1473_1463# CMOSP w=40 l=2
602 +  ad=0 pd=0 as=0 ps=0
603 M1283 a_2215_1372# add_out3 vdd w_2222_1304# CMOSP w=40 l=2
604 +  ad=0 pd=0 as=0 ps=0

605 M1284 a_443_3901# a_185_3880# p1 Gnd CMOSN w=40 l=2
606 +  ad=1480 pd=154 as=760 ps=118
607 M1285 vdd clk a_184_1788# w_265_1779# CMOSP w=40 l=2
608 +  ad=0 pd=0 as=0 ps=0
609 M1286 a_1953_3546# pin_p gnd Gnd CMOSN w=40 l=2
610 +  ad=0 pd=0 as=0 ps=0
611 M1287 a_184_2288# a_181_2286# a_184_2267# Gnd CMOSN w=40 l=2
612 +  ad=1480 pd=154 as=760 ps=118
613 M1288 gnd a_184_830# a_182_712# Gnd CMOSN w=20 l=2
614 +  ad=0 pd=0 as=100 ps=50
615 M1289 sum_1_bar a_2289_2630# vdd w_2524_2875# CMOSP w=40 l=2
616 +  ad=0 pd=0 as=0 ps=0
617 M1290 carr4 a_1644_1059# vdd w_1728_1031# CMOSP w=40 l=2
618 +  ad=1480 pd=154 as=0 ps=0
619 M1291 vdd clk a_181_1807# w_345_1779# CMOSP w=40 l=2
620 +  ad=0 pd=0 as=0 ps=0
621 M1292 vdd a_1203_1637# a_1475_1600# w_1458_1594# CMOSP w=50 l=2
622 +  ad=0 pd=0 as=250 ps=110
623 M1293 gnd a_21_1328# a_185_1028# Gnd CMOSN w=40 l=2
624 +  ad=0 pd=0 as=0 ps=0
625 M1294 vdd a_1385_2264# a_1556_2131# w_1632_2195# CMOSP w=50 l=2
626 +  ad=0 pd=0 as=250 ps=110
627 M1295 a_21_849# a_24_851# vdd w_266_645# CMOSP w=40 l=2
628 +  ad=1480 pd=154 as=0 ps=0
629 M1296 a_2554_3712# dfl1 gnd Gnd CMOSN w=40 l=2
630 +  ad=0 pd=0 as=0 ps=0
631 M1297 a_2252_1891# a_2215_1372# vdd w_2222_1884# CMOSP w=40 l=2
632 +  ad=0 pd=0 as=0 ps=0
633 M1298 a_24_3246# a_21_3244# vdd w_15_3216# CMOSP w=40 l=2
634 +  ad=1480 pd=154 as=0 ps=0
635 M1299 gnd D1 a_112_2767# Gnd CMOSN w=40 l=2
636 +  ad=0 pd=0 as=0 ps=0
637 M1300 A3 a_185_528# vdd w_346_519# CMOSP w=40 l=2
638 +  ad=1480 pd=154 as=0 ps=0
639 M1301 a_2252_2793# clk gnd Gnd CMOSN w=40 l=2
640 +  ad=0 pd=0 as=0 ps=0
641 M1302 gnd a_1108_2648# a_1315_2726# Gnd CMOSN w=20 l=2
642 +  ad=0 pd=0 as=100 ps=50
643 M1303 a_1094_3507# a_1103_3160# gnd Gnd CMOSN w=20 l=2
644 +  ad=100 pd=50 as=0 ps=0
645 M1304 sum_2_bar sum_2 a_2554_2134# Gnd CMOSN w=40 l=2
646 +  ad=760 pd=118 as=1480 ps=154
647 M1305 a_514_2767# a_181_2765# a_351_2765# Gnd CMOSN w=40 l=2
648 +  ad=1480 pd=154 as=760 ps=118
649 M1306 vdd a_24_2288# a_351_2286# w_595_2258# CMOSP w=40 l=2
650 +  ad=0 pd=0 as=0 ps=0
651 M1307 vdd a_759_2277# a_883_2276# w_853_2269# CMOSP w=40 l=2
652 +  ad=0 pd=0 as=1480 ps=154
653 M1308 a_2252_2721# add_out1 gnd Gnd CMOSN w=40 l=2
654 +  ad=0 pd=0 as=0 ps=0
655 M1309 vdd a_184_3225# a_182_3107# w_258_3161# CMOSP w=50 l=2

656 +  ad=0 pd=0 as=250 ps=110
657 M1310 vdd a_184_830# a_182_712# w_258_766# CMOSP w=50 l=2
658 +  ad=0 pd=0 as=250 ps=110
659 M1311 gnd a_181_370# a_443_70# Gnd CMOSN w=40 l=2
660 +  ad=0 pd=0 as=0 ps=0
661 M1312 dfl1 clk vdd w_2222_3614# CMOSP w=40 l=2
662 +  ad=0 pd=0 as=0 ps=0
663 M1313 gout3 a_712_2643# gnd Gnd CMOSN w=20 l=2
664 +  ad=100 pd=50 as=0 ps=0
665 M1314 gnd a_24_851# a_514_851# Gnd CMOSN w=40 l=2
666 +  ad=0 pd=0 as=0 ps=0
667 M1315 a_712_2643# A2 vdd w_714_2522# CMOSP w=40 l=2
668 +  ad=1480 pd=154 as=0 ps=0
669 M1316 a_442_372# a_351_370# a_181_370# Gnd CMOSN w=40 l=2
670 +  ad=1480 pd=154 as=760 ps=118
671 M1317 vdd sum_1_bar sum_1 w_2524_2955# CMOSP w=40 l=2
672 +  ad=0 pd=0 as=1480 ps=154
673 M1318 a_2252_1231# a_2252_983# a_2252_1143# Gnd CMOSN w=40 l=2
674 +  ad=760 pd=118 as=1480 ps=154
675 M1319 gnd clk a_442_3246# Gnd CMOSN w=40 l=2
676 +  ad=0 pd=0 as=0 ps=0
677 M1320 a_2252_983# a_2252_1231# a_2252_1071# Gnd CMOSN w=40 l=2
678 +  ad=760 pd=118 as=1480 ps=154
679 M1321 a_2215_712# carr4 vdd w_2222_644# CMOSP w=40 l=2
680 +  ad=1480 pd=154 as=0 ps=0
681 M1322 a_1829_2251# cin2 a_1829_2163# Gnd CMOSN w=40 l=2
682 +  ad=760 pd=118 as=1480 ps=154
683 M1323 a_351_4201# a_181_4201# vdd w_595_4173# CMOSP w=40 l=2
684 +  ad=1480 pd=154 as=0 ps=0
685 M1324 gout4 a_712_1646# gout4 w_698_1635# CMOSP w=50 l=2
686 +  ad=0 pd=0 as=250 ps=110
687 M1325 a_1574_1258# a_1479_1199# a_1486_1258# Gnd CMOSN w=40 l=2
688 +  ad=1480 pd=154 as=760 ps=118
689 M1326 a_185_2944# cin0 a_185_2923# Gnd CMOSN w=40 l=2
690 +  ad=1480 pd=154 as=760 ps=118
691 M1327 vdd a_21_2765# a_185_2444# w_266_2435# CMOSP w=40 l=2
692 +  ad=0 pd=0 as=0 ps=0
693 M1328 a_1097_3323# cin0 vdd w_1178_3314# CMOSP w=40 l=2
694 +  ad=1480 pd=154 as=0 ps=0
695 M1329 vdd a_1829_3377# a_1953_3376# w_1923_3369# CMOSP w=40 l=2
696 +  ad=0 pd=0 as=1480 ps=154
697 M1330 vdd a_181_2765# A1 w_346_2435# CMOSP w=40 l=2
698 +  ad=0 pd=0 as=0 ps=0
699 M1331 vdd a_1143_1441# a_1106_1444# w_1076_1435# CMOSP w=40 l=2
700 +  ad=0 pd=0 as=1480 ps=154
701 M1332 a_1953_2899# a_998_3101# vdd w_1923_2892# CMOSP w=40 l=2
702 +  ad=0 pd=0 as=0 ps=0

704 +  ad=0 pd=0 as=100 ps=50
705 M1334 a_1656_1302# a_1653_1321# vdd w_1737_1293# CMOSP w=40 l=2
706 +  ad=1480 pd=154 as=0 ps=0
707 M1335 vdd a_2289_1970# a_2215_2032# w_2222_1964# CMOSP w=40 l=2
708 +  ad=0 pd=0 as=1480 ps=154
709 M1336 a_2363_2177# a_2252_2221# gnd Gnd CMOSN w=20 l=2
710 +  ad=100 pd=50 as=0 ps=0
711 M1337 vdd a_2215_1372# a_2289_1310# w_2398_1555# CMOSP w=40 l=2
712 +  ad=0 pd=0 as=1480 ps=154
713 M1338 a_2554_814# a_2289_650# gnd Gnd CMOSN w=40 l=2
714 +  ad=1480 pd=154 as=0 ps=0
715 M1339 a_1953_2250# cin2 vdd w_1923_2243# CMOSP w=40 l=2
716 +  ad=0 pd=0 as=0 ps=0
717 M1340 gnd a_182_2149# a_185_2112# Gnd CMOSN w=40 l=2
718 +  ad=0 pd=0 as=0 ps=0
719 M1341 vdd sum_out dfl2 w_2524_3535# CMOSP w=40 l=2
720 +  ad=0 pd=0 as=1480 ps=154
721 M1342 gnd a_181_4201# a_443_3901# Gnd CMOSN w=40 l=2
722 +  ad=0 pd=0 as=0 ps=0
723 M1343 gnd clk a_184_2288# Gnd CMOSN w=40 l=2
724 +  ad=0 pd=0 as=0 ps=0
725 M1344 vdd a_1644_1098# carr4 w_1728_1031# CMOSP w=40 l=2
726 +  ad=0 pd=0 as=0 ps=0
727 M1345 a_185_4027# a_24_4203# a_21_4201# Gnd CMOSN w=40 l=2
728 +  ad=1480 pd=154 as=760 ps=118
729 M1346 vdd a_2252_2303# a_2252_2551# w_2222_2544# CMOSP w=40 l=2
730 +  ad=0 pd=0 as=1480 ps=154
731 M1347 a_112_1330# a_21_1328# a_24_1330# Gnd CMOSN w=40 l=2
732 +  ad=1480 pd=154 as=760 ps=118
733 M1348 vdd a_1147_1642# a_1110_1645# w_1080_1636# CMOSP w=40 l=2
734 +  ad=0 pd=0 as=1480 ps=154
735 M1349 vdd a_182_712# a_21_849# w_266_645# CMOSP w=40 l=2
736 +  ad=0 pd=0 as=0 ps=0
737 M1350 a_184_4203# a_181_4201# a_184_4182# Gnd CMOSN w=40 l=2
738 +  ad=1480 pd=154 as=760 ps=118
739 M1351 vdd carry_in a_24_3246# w_15_3216# CMOSP w=40 l=2
740 +  ad=0 pd=0 as=0 ps=0
741 M1352 a_2252_3541# dfl1 a_2252_3453# Gnd CMOSN w=40 l=2
742 +  ad=760 pd=118 as=1480 ps=154
743 M1353 gnd a_21_370# a_185_70# Gnd CMOSN w=40 l=2
744 +  ad=0 pd=0 as=0 ps=0
745 M1354 a_1199_1304# a_1106_1348# vdd w_1185_1334# CMOSP w=50 l=2
746 +  ad=250 pd=110 as=0 ps=0
747 M1355 vdd a_181_849# A3 w_346_519# CMOSP w=40 l=2
748 +  ad=0 pd=0 as=0 ps=0
749 M1356 dfo2 dfo1 a_2252_3381# Gnd CMOSN w=40 l=2
750 +  ad=760 pd=118 as=1480 ps=154
751 M1357 vdd a_1829_2980# a_1953_2981# w_1923_2972# CMOSP w=40 l=2
752 +  ad=0 pd=0 as=1480 ps=154
753 M1358 gnd a_184_2267# a_182_2149# Gnd CMOSN w=20 l=2

754 +  ad=0 pd=0 as=100 ps=50
755 M1359 vdd a_2252_983# a_2252_901# w_2222_894# CMOSP w=40 l=2
756 +  ad=0 pd=0 as=0 ps=0
757 M1360 a_1570_1493# a_1475_1434# a_1482_1493# Gnd CMOSN w=40 l=2
758 +  ad=1480 pd=154 as=760 ps=118
759 M1361 a_185_49# B3 vdd w_266_40# CMOSP w=40 l=2
760 +  ad=1480 pd=154 as=0 ps=0
761 M1362 a_184_372# a_181_370# a_184_351# Gnd CMOSN w=40 l=2
762 +  ad=1480 pd=154 as=760 ps=118
763 M1363 vdd a_1829_2251# a_1953_2332# w_1923_2323# CMOSP w=40 l=2
764 +  ad=0 pd=0 as=1480 ps=154
765 M1364 a_181_849# a_351_849# vdd w_345_821# CMOSP w=40 l=2
766 +  ad=1480 pd=154 as=0 ps=0
767 M1365 a_1953_1855# carry_3 vdd w_1923_1846# CMOSP w=40 l=2
768 +  ad=0 pd=0 as=0 ps=0
769 M1366 gnd a_24_2767# a_514_2767# Gnd CMOSN w=40 l=2
770 +  ad=0 pd=0 as=0 ps=0
771 M1367 a_2554_1732# a_2252_1643# gnd Gnd CMOSN w=40 l=2
772 +  ad=0 pd=0 as=0 ps=0
773 M1368 a_442_1809# a_351_1807# a_181_1807# Gnd CMOSN w=40 l=2
774 +  ad=1480 pd=154 as=760 ps=118
775 M1369 add_out1 a_1953_2899# a_2068_3069# Gnd CMOSN w=40 l=2
776 +  ad=760 pd=118 as=1480 ps=154
777 M1370 gnd a_1106_3102# a_1148_2567# Gnd CMOSN w=20 l=2
778 +  ad=0 pd=0 as=100 ps=50
779 M1371 a_883_1975# a_759_1974# a_883_2063# Gnd CMOSN w=40 l=2
780 +  ad=760 pd=118 as=1480 ps=154
781 M1372 vdd B2 a_712_2643# w_714_2522# CMOSP w=40 l=2
782 +  ad=0 pd=0 as=0 ps=0
783 M1373 gnd clk a_442_372# Gnd CMOSN w=40 l=2
784 +  ad=0 pd=0 as=0 ps=0
785 M1374 a_185_1007# B2 vdd w_266_998# CMOSP w=40 l=2
786 +  ad=1480 pd=154 as=0 ps=0
787 M1375 vdd a_24_4203# a_351_4201# w_595_4173# CMOSP w=40 l=2
788 +  ad=0 pd=0 as=0 ps=0
789 M1376 a_2289_650# a_2215_712# a_2428_814# Gnd CMOSN w=40 l=2
790 +  ad=760 pd=118 as=0 ps=0
791 M1377 a_2068_1943# a_1953_1855# gnd Gnd CMOSN w=40 l=2
792 +  ad=0 pd=0 as=0 ps=0
793 M1378 B2 a_185_1007# vdd w_346_998# CMOSP w=40 l=2
794 +  ad=1480 pd=154 as=0 ps=0
795 M1379 gnd a_1479_1365# a_1574_1258# Gnd CMOSN w=40 l=2
796 +  ad=0 pd=0 as=0 ps=0
797 M1380 a_883_3101# B1 vdd w_853_3092# CMOSP w=40 l=2
798 +  ad=0 pd=0 as=0 ps=0
799 M1381 gnd a_21_3244# a_185_2944# Gnd CMOSN w=40 l=2
800 +  ad=0 pd=0 as=0 ps=0
801 M1382 a_1143_1239# a_1113_1930# gnd Gnd CMOSN w=20 l=2
802 +  ad=100 pd=50 as=0 ps=0
803 M1383 vdd pin_p a_1097_3323# w_1178_3314# CMOSP w=40 l=2

804 +  ad=0 pd=0 as=0 ps=0
805 M1384 a_2252_1643# clk vdd w_2222_1634# CMOSP w=40 l=2
806 +  ad=0 pd=0 as=0 ps=0
807 M1385 vdd a_1653_1360# a_1656_1302# w_1737_1293# CMOSP w=40 l=2
808 +  ad=0 pd=0 as=0 ps=0
809 M1386 a_1829_2980# cin1 a_1829_3068# Gnd CMOSN w=40 l=2
810 +  ad=760 pd=118 as=1480 ps=154
811 M1387 a_1829_1942# pin_p4 gnd Gnd CMOSN w=40 l=2
812 +  ad=0 pd=0 as=0 ps=0
813 M1388 a_2428_2134# a_2363_2177# gnd Gnd CMOSN w=40 l=2
814 +  ad=0 pd=0 as=0 ps=0
815 M1389 a_998_3189# a_883_3101# gnd Gnd CMOSN w=40 l=2
816 +  ad=0 pd=0 as=0 ps=0
817 M1390 a_1479_1199# a_1199_1063# vdd w_1462_1185# CMOSP w=50 l=2
818 +  ad=250 pd=110 as=0 ps=0
819 M1391 a_1106_1071# gout3 a_1106_1159# Gnd CMOSN w=40 l=2
820 +  ad=760 pd=118 as=1480 ps=154
821 M1392 a_1113_1930# gout2 a_1113_1842# Gnd CMOSN w=40 l=2
822 +  ad=760 pd=118 as=1480 ps=154
823 M1393 gnd a_182_406# a_185_4027# Gnd CMOSN w=40 l=2
824 +  ad=0 pd=0 as=0 ps=0
825 M1394 a_1953_1773# a_1829_1854# a_1953_1685# Gnd CMOSN w=40 l=2
826 +  ad=760 pd=118 as=1480 ps=154
827 M1395 a_2252_2221# clk vdd w_2222_2214# CMOSP w=40 l=2
828 +  ad=0 pd=0 as=0 ps=0
829 M1396 vdd sum_3 sum_3_bar w_2524_1555# CMOSP w=40 l=2
830 +  ad=0 pd=0 as=1480 ps=154
831 M1397 a_24_1809# a_21_1807# vdd w_15_1779# CMOSP w=40 l=2
832 +  ad=1480 pd=154 as=0 ps=0
833 M1398 gnd Db2 a_112_1330# Gnd CMOSN w=40 l=2
834 +  ad=0 pd=0 as=0 ps=0
835 M1399 pin_p3 a_883_2358# a_998_2188# Gnd CMOSN w=40 l=2
836 +  ad=760 pd=118 as=1480 ps=154
837 M1400 a_759_3188# A1 gnd Gnd CMOSN w=40 l=2
838 +  ad=0 pd=0 as=0 ps=0
839 M1401 a_443_2465# a_185_2444# A1 Gnd CMOSN w=40 l=2
840 +  ad=1480 pd=154 as=760 ps=118
841 M1402 a_2252_3123# a_2215_2692# gnd Gnd CMOSN w=40 l=2
842 +  ad=0 pd=0 as=0 ps=0
843 M1403 gnd clk a_184_4203# Gnd CMOSN w=40 l=2
844 +  ad=0 pd=0 as=0 ps=0
845 M1404 a_351_849# a_181_849# vdd w_595_821# CMOSP w=40 l=2
846 +  ad=1480 pd=154 as=0 ps=0
847 M1405 a_2252_3051# clk gnd Gnd CMOSN w=40 l=2
848 +  ad=0 pd=0 as=0 ps=0
849 M1406 sum_2 sum_2_bar a_2554_2392# Gnd CMOSN w=40 l=2
850 +  ad=760 pd=118 as=1480 ps=154
851 M1407 a_21_2286# a_24_2288# vdd w_266_2082# CMOSP w=40 l=2
852 +  ad=1480 pd=154 as=0 ps=0
853 M1408 a_514_1330# a_181_1328# a_351_1328# Gnd CMOSN w=40 l=2
854 +  ad=1480 pd=154 as=760 ps=118
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855 M1409 gnd a_1475_1608# a_1570_1493# Gnd CMOSN w=40 l=2
856 +  ad=0 pd=0 as=0 ps=0
857 M1410 a_1106_1260# pin_p4 gnd Gnd CMOSN w=40 l=2
858 +  ad=0 pd=0 as=0 ps=0
859 M1411 gnd clk a_184_372# Gnd CMOSN w=40 l=2
860 +  ad=0 pd=0 as=0 ps=0
861 M1412 vdd clk a_181_849# w_345_821# CMOSP w=40 l=2
862 +  ad=0 pd=0 as=0 ps=0
863 M1413 vdd a_184_1788# a_182_1670# w_258_1724# CMOSP w=50 l=2
864 +  ad=0 pd=0 as=250 ps=110
865 M1414 vdd a_1148_2567# a_1113_2276# w_1083_2269# CMOSP w=40 l=2
866 +  ad=0 pd=0 as=1480 ps=154
867 M1415 a_883_3019# a_759_3100# a_883_2931# Gnd CMOSN w=40 l=2
868 +  ad=760 pd=118 as=1480 ps=154
869 M1416 vdd gout a_1094_3546# w_1170_3610# CMOSP w=50 l=2
870 +  ad=0 pd=0 as=250 ps=110
871 M1417 dfo1 a_2363_3497# vdd w_2398_3535# CMOSP w=40 l=2
872 +  ad=0 pd=0 as=0 ps=0
873 M1418 add_out a_1953_3458# a_2068_3288# Gnd CMOSN w=40 l=2
874 +  ad=760 pd=118 as=1480 ps=154
875 M1419 a_2252_1561# a_2252_1643# a_2252_1473# Gnd CMOSN w=40 l=2
876 +  ad=760 pd=118 as=1480 ps=154
877 M1420 gnd a_1656_1302# a_1644_1098# Gnd CMOSN w=20 l=2
878 +  ad=0 pd=0 as=100 ps=50
879 M1421 a_184_2267# a_181_2286# vdd w_265_2258# CMOSP w=40 l=2
880 +  ad=1480 pd=154 as=0 ps=0
881 M1422 a_2215_1372# a_2289_1310# a_2252_1401# Gnd CMOSN w=40 l=2
882 +  ad=760 pd=118 as=1480 ps=154
883 M1423 a_2252_983# clk vdd w_2222_974# CMOSP w=40 l=2
884 +  ad=1480 pd=154 as=0 ps=0
885 M1424 a_883_1805# A3 gnd Gnd CMOSN w=40 l=2
886 +  ad=0 pd=0 as=0 ps=0
887 M1425 gnd a_184_4182# a_182_4064# Gnd CMOSN w=20 l=2
888 +  ad=0 pd=0 as=100 ps=50
889 M1426 a_181_2286# a_351_2286# vdd w_345_2258# CMOSP w=40 l=2
890 +  ad=1480 pd=154 as=0 ps=0
891 M1427 gnd clk a_442_1809# Gnd CMOSN w=40 l=2
892 +  ad=0 pd=0 as=0 ps=0
893 M1428 a_2068_2162# a_1953_2250# gnd Gnd CMOSN w=40 l=2
894 +  ad=0 pd=0 as=0 ps=0
895 M1429 a_1475_1434# a_1199_1436# vdd w_1458_1420# CMOSP w=50 l=2
896 +  ad=250 pd=110 as=0 ps=0
897 M1430 vdd a_21_1328# a_185_1007# w_266_998# CMOSP w=40 l=2
898 +  ad=0 pd=0 as=0 ps=0
899 M1431 a_185_1507# A2 a_185_1486# Gnd CMOSN w=40 l=2
900 +  ad=1480 pd=154 as=760 ps=118
901 M1432 vdd a_2252_2551# a_2252_2303# w_2222_2294# CMOSP w=40 l=2
902 +  ad=0 pd=0 as=1480 ps=154
903 M1433 a_1556_2092# a_1389_2029# vdd w_1632_2021# CMOSP w=50 l=2
904 +  ad=250 pd=110 as=0 ps=0
905 M1434 vdd a_181_1328# B2 w_346_998# CMOSP w=40 l=2
906 +  ad=0 pd=0 as=0 ps=0
907 M1435 a_112_3246# a_21_3244# a_24_3246# Gnd CMOSN w=40 l=2
908 +  ad=1480 pd=154 as=760 ps=118
909 M1436 vdd a_2289_650# a_2215_712# w_2222_644# CMOSP w=40 l=2
910 +  ad=0 pd=0 as=0 ps=0
911 M1437 a_2289_2630# a_2215_2692# a_2428_2794# Gnd CMOSN w=40 l=2
912 +  ad=760 pd=118 as=1480 ps=154
913 M1438 a_2363_2177# a_2252_2221# vdd w_2349_2207# CMOSP w=50 l=2
914 +  ad=250 pd=110 as=0 ps=0
915 M1439 a_1315_2560# gout2 gnd Gnd CMOSN w=20 l=2
916 +  ad=100 pd=50 as=0 ps=0
917 M1440 a_351_2765# a_181_2765# vdd w_595_2737# CMOSP w=40 l=2
918 +  ad=1480 pd=154 as=0 ps=0
919 M1441 a_1389_2029# a_1382_1970# vdd w_1380_1999# CMOSP w=40 l=2
920 +  ad=1480 pd=154 as=0 ps=0
921 M1442 vdd a_2252_2963# a_2252_2881# w_2222_2874# CMOSP w=40 l=2
922 +  ad=0 pd=0 as=1480 ps=154
923 M1443 a_443_549# a_185_528# A3 Gnd CMOSN w=40 l=2
924 +  ad=1480 pd=154 as=760 ps=118
925 M1444 carry_4 bar carry_4 a_2554_814# Gnd CMOSN w=40 l=2
926 +  ad=760 pd=118 as=0 ps=0
927 M1445 a_811_2552# A2 gnd Gnd CMOSN w=40 l=2
928 +  ad=1480 pd=154 as=0 ps=0
929 M1446 a_759_2277# B2 a_759_2189# Gnd CMOSN w=40 l=2
930 +  ad=760 pd=118 as=1480 ps=154
931 M1447 a_1559_2094# a_1556_2092# carry_3 Gnd CMOSN w=40 l=2
932 +  ad=1480 pd=154 as=760 ps=118
933 M1448 a_2252_3871# dfi1 a_2252_3783# Gnd CMOSN w=40 l=2
934 +  ad=760 pd=118 as=1480 ps=154
935 M1449 a_1199_1063# a_1106_1071# gnd Gnd CMOSN w=20 l=2
936 +  ad=100 pd=50 as=0 ps=0
937 M1450 a_24_372# a_21_370# vdd w_15_342# CMOSP w=40 l=2
938 +  ad=1480 pd=154 as=0 ps=0
939 M1451 vdd D2 a_24_1809# w_15_1779# CMOSP w=40 l=2
940 +  ad=0 pd=0 as=0 ps=0
941 M1452 dfi1 a_2252_3871# a_2252_3711# Gnd CMOSN w=40 l=2
942 +  ad=760 pd=118 as=1480 ps=154
943 M1453 a_1199_1063# a_1106_1071# vdd w_1185_1046# CMOSP w=50 l=2
944 +  ad=250 pd=110 as=0 ps=0
945 M1454 a_185_2923# cin0 vdd w_266_2914# CMOSP w=40 l=2
946 +  ad=1480 pd=154 as=0 ps=0
947 M1455 gnd a_1482_1493# a_1653_1360# Gnd CMOSN w=20 l=2
948 +  ad=0 pd=0 as=100 ps=50
949 M1456 cin0 a_185_2923# vdd w_346_2914# CMOSP w=40 l=2
950 +  ad=1480 pd=154 as=0 ps=0
951 M1457 gnd a_181_2765# a_443_2465# Gnd CMOSN w=40 l=2
952 +  ad=0 pd=0 as=0 ps=0
953 M1458 a_2554_2134# a_2289_1970# gnd Gnd CMOSN w=40 l=2
954 +  ad=0 pd=0 as=0 ps=0
955 M1459 a_883_2276# B2 vdd w_853_2269# CMOSP w=40 l=2
956 +  ad=0 pd=0 as=0 ps=0
957 M1460 a_1105_2667# a_1148_2567# gnd Gnd CMOSN w=20 l=2
958 +  ad=100 pd=50 as=0 ps=0
959 M1461 vdd a_24_851# a_351_849# w_595_821# CMOSP w=40 l=2
960 +  ad=0 pd=0 as=0 ps=0
961 M1462 vdd a_182_2149# a_21_2286# w_266_2082# CMOSP w=40 l=2
962 +  ad=0 pd=0 as=0 ps=0
963 M1463 vdd a_883_1893# pin_p4 w_968_1966# CMOSP w=40 l=2
964 +  ad=0 pd=0 as=1480 ps=154
965 M1464 a_185_2591# a_24_2767# a_21_2765# Gnd CMOSN w=40 l=2
966 +  ad=1480 pd=154 as=760 ps=118
967 M1465 gnd a_24_1330# a_514_1330# Gnd CMOSN w=40 l=2
968 +  ad=0 pd=0 as=0 ps=0
969 M1466 a_1829_3377# cin0 a_1829_3289# Gnd CMOSN w=40 l=2
970 +  ad=760 pd=118 as=1480 ps=154
971 M1467 vdd a_712_2772# gout2 w_698_2761# CMOSP w=50 l=2
972 +  ad=0 pd=0 as=250 ps=110
973 M1468 sum_1 a_2252_2963# vdd w_2524_2955# CMOSP w=40 l=2
974 +  ad=0 pd=0 as=0 ps=0
975 M1469 a_2252_1143# a_2215_712# gnd Gnd CMOSN w=40 l=2
976 +  ad=0 pd=0 as=0 ps=0
977 M1470 a_2252_1071# clk gnd Gnd CMOSN w=40 l=2
978 +  ad=0 pd=0 as=0 ps=0
979 M1471 a_1829_2163# pin_p3 gnd Gnd CMOSN w=40 l=2
980 +  ad=0 pd=0 as=0 ps=0
981 M1472 a_184_2767# a_181_2765# a_184_2746# Gnd CMOSN w=40 l=2
982 +  ad=1480 pd=154 as=760 ps=118
983 M1473 vdd clk a_184_2267# w_265_2258# CMOSP w=40 l=2
984 +  ad=0 pd=0 as=0 ps=0
985 M1474 a_21_4201# a_24_4203# vdd w_266_3997# CMOSP w=40 l=2
986 +  ad=1480 pd=154 as=0 ps=0
987 M1475 vdd clk a_181_2286# w_345_2258# CMOSP w=40 l=2
988 +  ad=0 pd=0 as=0 ps=0
989 M1476 vdd B3 a_759_1974# w_729_1965# CMOSP w=40 l=2
990 +  ad=0 pd=0 as=1480 ps=154
991 M1477 a_1953_3376# cin0 vdd w_1923_3369# CMOSP w=40 l=2
992 +  ad=0 pd=0 as=0 ps=0
993 M1478 a_1106_1444# pin_p4 vdd w_1076_1435# CMOSP w=40 l=2
994 +  ad=0 pd=0 as=0 ps=0
995 M1479 a_2215_2032# add_out2 vdd w_2222_1964# CMOSP w=40 l=2
996 +  ad=0 pd=0 as=0 ps=0
997 M1480 a_185_2264# a_1378_2205# vdd w_1376_2234# CMOSP w=40 l=2
998 +  ad=1480 pd=154 as=0 ps=0
999 M1481 gnd a_21_1807# a_185_1507# Gnd CMOSN w=40 l=2
1000 +  ad=0 pd=0 as=0 ps=0
1001 M1482 a_2289_1310# a_2363_1517# vdd w_2398_1555# CMOSP w=40 l=2
1002 +  ad=0 pd=0 as=0 ps=0
1003 M1483 a_184_4182# a_181_4201# vdd w_265_4173# CMOSP w=40 l=2
1004 +  ad=1480 pd=154 as=0 ps=0
1005 M1484 gnd carry_in a_112_3246# Gnd CMOSN w=40 l=2
1006 +  ad=0 pd=0 as=0 ps=0
1006 +  ad=0 pd=0 as=0 ps=0
1007 M1485 gnd a_1199_1304# a_1479_1365# Gnd CMOSN w=20 l=2
1008 +  ad=0 pd=0 as=100 ps=50
1009 M1486 a_185_549# A3 a_185_528# Gnd CMOSN w=40 l=2
1010 +  ad=1480 pd=154 as=760 ps=118
1011 M1487 dfi2 dfo1 vdd w_2524_3535# CMOSP w=40 l=2
1012 +  ad=0 pd=0 as=0 ps=0
1013 M1488 a_1143_1239# a_1113_1930# vdd w_1192_1916# CMOSP w=50 l=2
1014 +  ad=250 pd=110 as=0 ps=0
1015 M1489 a_181_4201# a_351_4201# vdd w_345_4173# CMOSP w=40 l=2
1016 +  ad=1480 pd=154 as=0 ps=0
1017 M1490 vdd a_759_2277# a_883_2358# w_853_2349# CMOSP w=40 l=2
1018 +  ad=0 pd=0 as=1480 ps=154
1019 M1491 gnd a_1107_2897# a_1148_2781# Gnd CMOSN w=20 l=2
1020 +  ad=0 pd=0 as=100 ps=50
1021 M1492 vdd a_24_2767# a_351_2765# w_595_2737# CMOSP w=40 l=2
1022 +  ad=0 pd=0 as=0 ps=0
1023 M1493 a_514_3246# a_181_3244# a_351_3244# Gnd CMOSN w=40 l=2
1024 +  ad=1480 pd=154 as=760 ps=118
1025 M1494 vdd a_1148_2781# a_1113_2028# w_1083_2019# CMOSP w=40 l=2
1026 +  ad=0 pd=0 as=1480 ps=154
1027 M1495 vdd a_21_370# a_185_49# w_266_40# CMOSP w=40 l=2
1028 +  ad=0 pd=0 as=0 ps=0
1029 M1496 a_2252_2551# a_2215_2032# vdd w_2222_2544# CMOSP w=40 l=2
1030 +  ad=0 pd=0 as=0 ps=0
1031 M1497 vdd a_1382_2136# a_1389_2029# w_1380_1999# CMOSP w=40 l=2
1032 +  ad=0 pd=0 as=0 ps=0
1033 M1498 a_1953_1855# a_1829_1854# a_1953_1943# Gnd CMOSN w=40 l=2
1034 +  ad=760 pd=118 as=1480 ps=154
1035 M1499 gnd a_181_849# a_443_549# Gnd CMOSN w=40 l=2
1036 +  ad=0 pd=0 as=0 ps=0
1037 M1500 a_712_2643# B2 a_811_2552# Gnd CMOSN w=40 l=2
1038 +  ad=760 pd=118 as=0 ps=0
1039 M1501 a_1110_1645# pin_p4 vdd w_1080_1636# CMOSP w=40 l=2
1040 +  ad=0 pd=0 as=0 ps=0
1041 M1502 a_184_351# a_181_370# vdd w_265_342# CMOSP w=40 l=2
1042 +  ad=1480 pd=154 as=0 ps=0
1043 M1503 a_2252_3453# clk gnd Gnd CMOSN w=40 l=2
1044 +  ad=0 pd=0 as=0 ps=0
1045 M1504 gnd a_1556_2131# a_1559_2094# Gnd CMOSN w=40 l=2
1046 +  ad=0 pd=0 as=0 ps=0
1047 M1505 a_442_851# a_351_849# a_181_849# Gnd CMOSN w=40 l=2
1048 +  ad=1480 pd=154 as=760 ps=118
1049 M1506 vdd a_1829_3377# a_1953_3458# w_1923_3449# CMOSP w=40 l=2
1050 +  ad=0 pd=0 as=1480 ps=154
1051 M1507 sum_1_bar sum_1 a_2554_2794# Gnd CMOSN w=40 l=2
1052 +  ad=760 pd=118 as=1480 ps=154
1053 M1508 a_2252_3381# add_out gnd Gnd CMOSN w=40 l=2
1054 +  ad=0 pd=0 as=0 ps=0
1055 M1509 vdd Db3 a_24_372# w_15_342# CMOSP w=40 l=2
1056 +  ad=0 pd=0 as=0 ps=0
1057 M1510 a 443 1028# a 185 1007# B2 Gnd CMOSN w=40 l=2
1058 +  ad=1480 pd=154 as=760 ps=118
1059 M1511 a_1953_2981# cin1 vdd w_1923_2972# CMOSP w=40 l=2
1060 +  ad=0 pd=0 as=0 ps=0
1061 M1512 vdd a_21_3244# a_185_2923# w_266_2914# CMOSP w=40 l=2
1062 +  ad=0 pd=0 as=0 ps=0
1063 M1513 vdd gout3 a_1382_2136# w_1365_2130# CMOSP w=50 l=2
1064 +  ad=0 pd=0 as=250 ps=110
1065 M1514 a_1953_2332# pin_p3 vdd w_1923_2323# CMOSP w=40 l=2
1066 +  ad=0 pd=0 as=0 ps=0
1067 M1515 vdd a_181_3244# cin0 w_346_2914# CMOSP w=40 l=2
1068 +  ad=0 pd=0 as=0 ps=0
1069 M1516 vdd dfi2 sum_out w_2524_3615# CMOSP w=40 l=2
1070 +  ad=0 pd=0 as=1480 ps=154
1071 M1517 a_883_3101# a_759_3100# a_883_3189# Gnd CMOSN w=40 l=2
1072 +  ad=760 pd=118 as=1480 ps=154
1073 M1518 gnd a_182_2628# a_185_2591# Gnd CMOSN w=40 l=2
1074 +  ad=0 pd=0 as=0 ps=0
1075 M1519 a_2252_1891# a_2252_1643# a_2252_1803# Gnd CMOSN w=40 l=2
1076 +  ad=760 pd=118 as=1480 ps=154
1077 M1520 a_2252_1643# a_2252_1891# a_2252_1731# Gnd CMOSN w=40 l=2
1078 +  ad=760 pd=118 as=1480 ps=154
1079 M1521 gnd a_1203_1637# a_1475_1600# Gnd CMOSN w=20 l=2
1080 +  ad=0 pd=0 as=100 ps=50
1081 M1522 a_2068_3069# a_1953_2981# gnd Gnd CMOSN w=40 l=2
1082 +  ad=0 pd=0 as=0 ps=0
1083 M1523 a_883_2063# B3 gnd Gnd CMOSN w=40 l=2
1084 +  ad=0 pd=0 as=0 ps=0
1085 M1524 vdd a_2289_2630# a_2215_2692# w_2222_2624# CMOSP w=40 l=2
1086 +  ad=0 pd=0 as=1480 ps=154
1087 M1525 gnd clk a_184_2767# Gnd CMOSN w=40 l=2
1088 +  ad=0 pd=0 as=0 ps=0
1089 M1526 a_2363_2837# a_2252_2881# gnd Gnd CMOSN w=20 l=2
1090 +  ad=100 pd=50 as=0 ps=0
1091 M1527 vdd a_2215_2032# a_2289_1970# w_2398_2215# CMOSP w=40 l=2
1092 +  ad=0 pd=0 as=1480 ps=154
1093 M1528 vdd a_182_4064# a_21_4201# w_266_3997# CMOSP w=40 l=2
1094 +  ad=0 pd=0 as=0 ps=0
1095 M1529 a_112_1809# a_21_1807# a_24_1809# Gnd CMOSN w=40 l=2
1096 +  ad=1480 pd=154 as=760 ps=118
1097 M1530 a_1829_3068# a_998_3101# gnd Gnd CMOSN w=40 l=2
1098 +  ad=0 pd=0 as=0 ps=0
1099 M1531 vdd a_1378_2371# a_1385_2264# w_1376_2234# CMOSP w=40 l=2
1100 +  ad=0 pd=0 as=0 ps=0
1101 M1532 vdd a_2252_1231# a_2252_983# w_2222_974# CMOSP w=40 l=2
1102 +  ad=0 pd=0 as=0 ps=0
1103 M1533 vdd clk a_184_4182# w_265_4173# CMOSP w=40 l=2
1104 +  ad=0 pd=0 as=0 ps=0
1105 M1534 gnd a_21_849# a_185_549# Gnd CMOSN w=40 l=2
1106 +  ad=0 pd=0 as=0 ps=0
1107 M1535 vdd clk a_181_4201# w_345_4173# CMOSP w=40 l=2
1108 +  ad=0 pd=0 as=0 ps=0
1109 M1536 gnd a_184_2746# a_182_2628# Gnd CMOSN w=20 l=2
1110 +  ad=0 pd=0 as=100 ps=50
1111 M1537 a_351_1328# a_181_1328# vdd w_595_1300# CMOSP w=40 l=2
1112 +  ad=1480 pd=154 as=0 ps=0
1113 M1538 a_1106_1159# pin_p4 gnd Gnd CMOSN w=40 l=2
1114 +  ad=0 pd=0 as=0 ps=0
1115 M1539 a_1113_1842# pin_p3 gnd Gnd CMOSN w=40 l=2
1116 +  ad=0 pd=0 as=0 ps=0
1117 M1540 a_184_851# a_181_849# a_184_830# Gnd CMOSN w=40 l=2
1118 +  ad=1480 pd=154 as=760 ps=118
1119 M1541 vdd a_2252_2963# a_2252_3211# w_2222_3204# CMOSP w=40 l=2
1120 +  ad=0 pd=0 as=1480 ps=154
1121 M1542 vdd a_1147_1642# a_1378_2371# w_1361_2365# CMOSP w=50 l=2
1122 +  ad=0 pd=0 as=250 ps=110
1123 M1543 a_1953_2899# a_1829_2980# a_1953_2811# Gnd CMOSN w=40 l=2
1124 +  ad=760 pd=118 as=1480 ps=154
1125 M1544 gnd a_24_3246# a_514_3246# Gnd CMOSN w=40 l=2
1126 +  ad=0 pd=0 as=0 ps=0
1127 M1545 a_2289_650# a_2363_857# vdd w_2398_895# CMOSP w=40 l=2
1128 +  ad=1480 pd=154 as=0 ps=0
1129 M1546 a_1953_2250# a_1829_2251# a_1953_2162# Gnd CMOSN w=40 l=2
1130 +  ad=760 pd=118 as=1480 ps=154
1131 M1547 a_1953_1685# pin_p4 gnd Gnd CMOSN w=40 l=2
1132 +  ad=0 pd=0 as=0 ps=0
1133 M1548 vdd a_1143_1239# a_1106_1348# w_1076_1341# CMOSP w=40 l=2
1134 +  ad=0 pd=0 as=1480 ps=154
1135 M1549 gnd a_712_1646# gout4 Gnd CMOSN w=20 l=2
1136 +  ad=0 pd=0 as=100 ps=50
1137 M1550 a_1094_3507# a_1103_3160# vdd w_1170_3436# CMOSP w=50 l=2
1138 +  ad=250 pd=110 as=0 ps=0
1139 M1551 sum_3_bar a_2289_1310# vdd w_2524_1555# CMOSP w=40 l=2
1140 +  ad=0 pd=0 as=0 ps=0
1141 M1552 a_1644_1059# gout4 gnd Gnd CMOSN w=20 l=2
1142 +  ad=100 pd=50 as=0 ps=0
1143 M1553 a_998_2188# a_883_2276# gnd Gnd CMOSN w=40 l=2
1144 +  ad=0 pd=0 as=0 ps=0
1145 M1554 a_442_2288# a_351_2286# a_181_2286# Gnd CMOSN w=40 l=2
1146 +  ad=1480 pd=154 as=760 ps=118
1147 M1555 vdd clk a_184_351# w_265_342# CMOSP w=40 l=2
1148 +  ad=0 pd=0 as=0 ps=0
1149 M1556 gnd clk a_442_851# Gnd CMOSN w=40 l=2
1150 +  ad=0 pd=0 as=0 ps=0
1151 M1557 a_185_1486# A2 vdd w_266_1477# CMOSP w=40 l=2
1152 +  ad=1480 pd=154 as=0 ps=0
1153 M1558 vdd a_759_1974# a_883_1893# w_853_1886# CMOSP w=40 l=2
1154 +  ad=0 pd=0 as=1480 ps=154
1155 M1559 a_2554_2392# a_2252_2303# gnd Gnd CMOSN w=40 l=2
1156 +  ad=0 pd=0 as=0 ps=0
1157 M1560 vdd a_1953_2332# add_out2 w_2038_2243# CMOSP w=40 l=2
1158 +  ad=0 pd=0 as=1480 ps=154
1159 M1561 gnd a_181_1328# a_443_1028# Gnd CMOSN w=40 l=2
1160 +  ad=0 pd=0 as=0 ps=0
1161 M1562 A2 a_185_1486# vdd w_346_1477# CMOSP w=40 l=2
1162 +  ad=1480 pd=154 as=0 ps=0
1163 M1563 a_1113_2276# pin_p3 vdd w_1083_2269# CMOSP w=40 l=2
1164 +  ad=0 pd=0 as=0 ps=0
1165 M1564 a_185_1154# a_24_1330# a_21_1328# Gnd CMOSN w=40 l=2
1166 +  ad=1480 pd=154 as=760 ps=118
1167 M1565 a_883_2931# A1 gnd Gnd CMOSN w=40 l=2
1168 +  ad=0 pd=0 as=0 ps=0
1169 M1566 a_2068_3288# a_1953_3376# gnd Gnd CMOSN w=40 l=2
1170 +  ad=0 pd=0 as=0 ps=0
1171 M1567 a_2252_1473# clk gnd Gnd CMOSN w=40 l=2
1172 +  ad=0 pd=0 as=0 ps=0
1173 M1568 vdd a_1148_2781# a_1105_2706# w_1181_2770# CMOSP w=50 l=2
1174 +  ad=0 pd=0 as=250 ps=110
1175 M1569 a_2252_1401# add_out3 gnd Gnd CMOSN w=40 l=2
1176 +  ad=0 pd=0 as=0 ps=0
1177 M1570 a_1097_3509# a_1094_3507# cin1 Gnd CMOSN w=40 l=2
1178 +  ad=1480 pd=154 as=760 ps=118
1179 M1571 a_184_1330# a_181_1328# a_184_1309# Gnd CMOSN w=40 l=2
1180 +  ad=1480 pd=154 as=760 ps=118
1181 M1572 a_1477_2029# a_1382_1970# a_1389_2029# Gnd CMOSN w=40 l=2
1182 +  ad=1480 pd=154 as=760 ps=118
1183 M1573 a_2252_2303# clk vdd w_2222_2294# CMOSP w=40 l=2
1184 +  ad=0 pd=0 as=0 ps=0
1185 M1574 vdd sum_3_bar sum_3 w_2524_1635# CMOSP w=40 l=2
1186 +  ad=0 pd=0 as=0 ps=0
1187 M1575 carry_3 a_1556_2092# vdd w_1640_2064# CMOSP w=40 l=2
1188 +  ad=1480 pd=154 as=0 ps=0
1189 M1576 a_24_2288# a_21_2286# vdd w_15_2258# CMOSP w=40 l=2
1190 +  ad=1480 pd=154 as=0 ps=0
1191 M1577 gnd D2 a_112_1809# Gnd CMOSN w=40 l=2
1192 +  ad=0 pd=0 as=0 ps=0
1193 M1578 a_2428_2794# a_2363_2837# gnd Gnd CMOSN w=40 l=2
1194 +  ad=0 pd=0 as=0 ps=0
1195 M1579 gnd a_1097_3323# a_1103_3160# Gnd CMOSN w=20 l=2
1196 +  ad=0 pd=0 as=100 ps=50
1197 M1580 a_443_2944# a_185_2923# cin0 Gnd CMOSN w=40 l=2
1198 +  ad=1480 pd=154 as=760 ps=118
1199 M1581 a_1653_1321# a_1486_1258# gnd Gnd CMOSN w=20 l=2
1200 +  ad=100 pd=50 as=0 ps=0
1201 M1582 vdd a_1953_1773# add_out3 w_2038_1846# CMOSP w=40 l=2
1202 +  ad=0 pd=0 as=0 ps=0
1203 M1583 a_21_2765# a_24_2767# vdd w_266_2561# CMOSP w=40 l=2
1204 +  ad=1480 pd=154 as=0 ps=0
1205 M1584 a_514_1809# a_181_1807# a_351_1807# Gnd CMOSN w=40 l=2
1206 +  ad=1480 pd=154 as=760 ps=118
1207 M1585 vdd a_24_1330# a_351_1328# w_595_1300# CMOSP w=40 l=2
1208 +  ad=0 pd=0 as=0 ps=0
1209 M1586 gnd clk a_184_851# Gnd CMOSN w=40 l=2
1210 +  ad=0 pd=0 as=0 ps=0
1211 M1587 a_2252_2881# clk vdd w_2222_2874# CMOSP w=40 l=2
1212 +  ad=0 pd=0 as=0 ps=0
1213 M1588 vdd a_184_2267# a_182_2149# w_258_2203# CMOSP w=50 l=2
1214 +  ad=0 pd=0 as=250 ps=110
1215 M1589 vdd sum_2 sum_2_bar w_2524_2215# CMOSP w=40 l=2
1216 +  ad=0 pd=0 as=0 ps=0
1217 M1590 a_112_372# a_21_370# a_24_372# Gnd CMOSN w=40 l=2
1218 +  ad=1480 pd=154 as=760 ps=118
1219 M1591 a_759_2189# A2 gnd Gnd CMOSN w=40 l=2
1220 +  ad=0 pd=0 as=0 ps=0
1221 M1592 a_712_1646# B3 vdd w_714_1672# CMOSP w=40 l=2
1222 +  ad=1480 pd=154 as=0 ps=0
1223 M1593 a_2252_3783# dfo2 gnd Gnd CMOSN w=40 l=2
1224 +  ad=0 pd=0 as=0 ps=0
1225 M1594 a_184_2746# a_181_2765# vdd w_265_2737# CMOSP w=40 l=2
1226 +  ad=1480 pd=154 as=0 ps=0
1227 M1595 vdd carry_3 a_1829_1854# w_1799_1845# CMOSP w=40 l=2
1228 +  ad=0 pd=0 as=0 ps=0
1229 M1596 a_2252_3711# clk gnd Gnd CMOSN w=40 l=2
1230 +  ad=0 pd=0 as=0 ps=0
1231 M1597 sum_1 sum_1_bar a_2554_3052# Gnd CMOSN w=40 l=2
1232 +  ad=760 pd=118 as=0 ps=0
1233 M1598 a_181_2765# a_351_2765# vdd w_345_2737# CMOSP w=40 l=2
1234 +  ad=1480 pd=154 as=0 ps=0
1235 M1599 gnd clk a_442_2288# Gnd CMOSN w=40 l=2
1236 +  ad=0 pd=0 as=0 ps=0
1237 M1600 vdd a_2252_983# a_2252_1231# w_2222_1224# CMOSP w=40 l=2
1238 +  ad=0 pd=0 as=0 ps=0
1239 M1601 a_2252_813# clk gnd Gnd CMOSN w=40 l=2
1240 +  ad=0 pd=0 as=0 ps=0
1241 M1602 vdd a_883_3019# a_998_3101# w_968_3092# CMOSP w=40 l=2
1242 +  ad=0 pd=0 as=0 ps=0
1243 M1603 a_185_1986# B1 a_185_1965# Gnd CMOSN w=40 l=2
1244 +  ad=1480 pd=154 as=760 ps=118
1245 M1604 a_2252_741# carr4 gnd Gnd CMOSN w=40 l=2
1246 +  ad=0 pd=0 as=0 ps=0
1247 M1605 vdd cin2 a_1829_2251# w_1799_2244# CMOSP w=40 l=2
1248 +  ad=0 pd=0 as=0 ps=0
1249 M1606 vdd a_21_1807# a_185_1486# w_266_1477# CMOSP w=40 l=2
1250 +  ad=0 pd=0 as=0 ps=0
1251 M1607 vdd a_1106_3102# a_1148_2567# w_1180_3056# CMOSP w=50 l=2
1252 +  ad=0 pd=0 as=250 ps=110
1253 M1608 a_1473_2264# a_1378_2205# a_1385_2264# Gnd CMOSN w=40 l=2
1254 +  ad=1480 pd=154 as=760 ps=118
1255 M1609 vdd a_181_1807# A2 w_346_1477# CMOSP w=40 l=2
1256 +  ad=0 pd=0 as=0 ps=0
1257 M1610 pin_p4 a_883_1975# vdd w_968_1966# CMOSP w=40 l=2
1258 +  ad=0 pd=0 as=0 ps=0
1258 +  ad=0 pd=0 as=0 ps=0
1259 M1611 a_2252_2221# a_2252_2303# a_2252_2133# Gnd CMOSN w=40 l=2
1260 +  ad=760 pd=118 as=0 ps=0
1261 M1612 a_1106_1444# a_1143_1441# a_1106_1532# Gnd CMOSN w=40 l=2
1262 +  ad=760 pd=118 as=0 ps=0
1263 M1613 a_2215_2032# a_2289_1970# a_2252_2061# Gnd CMOSN w=40 l=2
1264 +  ad=760 pd=118 as=0 ps=0
1265 M1614 a_1829_3289# pin_p gnd Gnd CMOSN w=40 l=2
1266 +  ad=0 pd=0 as=0 ps=0
1267 M1615 a_1479_1199# a_1199_1063# gnd Gnd CMOSN w=20 l=2
1268 +  ad=100 pd=50 as=0 ps=0
1269 M1616 gnd a_182_1191# a_185_1154# Gnd CMOSN w=40 l=2
1270 +  ad=0 pd=0 as=0 ps=0
1271 M1617 a_442_4203# a_351_4201# a_181_4201# Gnd CMOSN w=40 l=2
1272 +  ad=1480 pd=154 as=760 ps=118
1273 M1618 carry_4 bar a_2289_650# vdd w_2524_895# CMOSP w=40 l=2
1274 +  ad=0 pd=0 as=0 ps=0
1275 M1619 vdd B1 a_759_3100# w_729_3091# CMOSP w=40 l=2
1276 +  ad=0 pd=0 as=0 ps=0
1277 M1620 a_185_196# a_24_372# a_21_370# Gnd CMOSN w=40 l=2
1278 +  ad=1480 pd=154 as=760 ps=118
1279 M1621 vdd a_2252_3211# a_2252_2963# w_2222_2954# CMOSP w=40 l=2
1280 +  ad=0 pd=0 as=0 ps=0
1281 M1622 gnd a_1094_3546# a_1097_3509# Gnd CMOSN w=40 l=2
1282 +  ad=0 pd=0 as=0 ps=0
1283 M1623 a_351_3244# a_181_3244# vdd w_595_3216# CMOSP w=40 l=2
1284 +  ad=1480 pd=154 as=0 ps=0
1285 M1624 a_759_1974# A3 vdd w_729_1965# CMOSP w=40 l=2
1286 +  ad=0 pd=0 as=0 ps=0
1287 M1625 gnd clk a_184_1330# Gnd CMOSN w=40 l=2
1288 +  ad=0 pd=0 as=0 ps=0
1289 M1626 a_2363_857# a_2252_901# gnd Gnd CMOSN w=20 l=2
1290 +  ad=100 pd=50 as=0 ps=0
1291 M1627 a_185_528# A3 vdd w_266_519# CMOSP w=40 l=2
1292 +  ad=1480 pd=154 as=0 ps=0
1293 M1628 a_1106_3123# a_998_3101# a_1106_3102# Gnd CMOSN w=40 l=2
1294 +  ad=1480 pd=154 as=760 ps=118
1295 M1629 gnd a_1382_2136# a_1477_2029# Gnd CMOSN w=40 l=2
1296 +  ad=0 pd=0 as=0 ps=0
1297 M1630 dfo1 dfo2 a_2428_3454# Gnd CMOSN w=40 l=2
1298 +  ad=760 pd=118 as=0 ps=0
1299 M1631 vdd a_1556_2131# carry_3 w_1640_2064# CMOSP w=40 l=2
1300 +  ad=0 pd=0 as=0 ps=0
1301 M1632 a_2363_2837# a_2252_2881# vdd w_2349_2867# CMOSP w=50 l=2
1302 +  ad=250 pd=110 as=0 ps=0
1303 M1633 a_24_851# a_21_849# vdd w_15_821# CMOSP w=40 l=2
1304 +  ad=1480 pd=154 as=0 ps=0
1305 M1634 vdd Db1 a_24_2288# w_15_2258# CMOSP w=40 l=2
1306 +  ad=0 pd=0 as=0 ps=0
1307 M1635 a_883_2358# A2 vdd w_853_2349# CMOSP w=40 l=2
1308 +  ad=0 pd=0 as=0 ps=0
1309 M1636 a_1110_1645# a_1147_1642# a_1110_1733# Gnd CMOSN w=40 l=2
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1310 +  ad=760 pd=118 as=0 ps=0
1311 M1637 vdd dfl1 a_2252_3541# w_2222_3534# CMOSP w=40 l=2
1312 +  ad=0 pd=0 as=0 ps=0
1313 M1638 gnd a_184_1309# a_182_1191# Gnd CMOSN w=20 l=2
1314 +  ad=0 pd=0 as=100 ps=50
1315 M1639 gnd a_181_3244# a_443_2944# Gnd CMOSN w=40 l=2
1316 +  ad=0 pd=0 as=0 ps=0
1317 M1640 a_1382_1970# a_1143_1239# vdd w_1365_1956# CMOSP w=50 l=2
1318 +  ad=250 pd=110 as=0 ps=0
1319 M1641 a_1113_2028# pln_p3 vdd w_1083_2019# CMOSP w=40 l=2
1320 +  ad=0 pd=0 as=0 ps=0
1321 M1642 a_1953_2981# a_1829_2980# a_1953_3069# Gnd CMOSN w=40 l=2
1322 +  ad=760 pd=118 as=0 ps=0
1323 M1643 a_185_3070# a_24_3246# a_21_3244# Gnd CMOSN w=40 l=2
1324 +  ad=1480 pd=154 as=760 ps=118
1325 M1644 vdd a_182_2628# a_21_2765# w_266_2561# CMOSP w=40 l=2
1326 +  ad=0 pd=0 as=0 ps=0
1327 M1645 gnd a_24_1809# a_514_1809# Gnd CMOSN w=40 l=2
1328 +  ad=0 pd=0 as=0 ps=0
1329 M1646 a_1953_2332# a_1829_2251# a_1953_2420# Gnd CMOSN w=40 l=2
1330 +  ad=760 pd=118 as=0 ps=0
1331 M1647 a_1953_1943# carry_3 gnd Gnd CMOSN w=40 l=2
1332 +  ad=0 pd=0 as=0 ps=0
1333 M1648 gnd Db3 a_112_372# Gnd CMOSN w=40 l=2
1334 +  ad=0 pd=0 as=0 ps=0
1335 M1649 a_24_4203# a_21_4201# vdd w_15_4173# CMOSP w=40 l=2
1336 +  ad=1480 pd=154 as=0 ps=0
1337 M1650 a_1475_1434# a_1199_1436# gnd Gnd CMOSN w=20 l=2
1338 +  ad=100 pd=50 as=0 ps=0
1339 M1651 vdd A3 a_712_1646# w_714_1672# CMOSP w=40 l=2
1340 +  ad=0 pd=0 as=0 ps=0
1341 M1652 a_1953_3458# pin_p vdd w_1923_3449# CMOSP w=40 l=2
1342 +  ad=0 pd=0 as=0 ps=0
1343 M1653 a_2554_2794# a_2289_2630# gnd Gnd CMOSN w=40 l=2
1344 +  ad=0 pd=0 as=0 ps=0
1345 M1654 a_184_3246# a_181_3244# a_184_3225# Gnd CMOSN w=40 l=2
1346 +  ad=1480 pd=154 as=760 ps=118
1347 M1655 vdd clk a_184_2746# w_265_2737# CMOSP w=40 l=2
1348 +  ad=0 pd=0 as=0 ps=0
1349 M1656 vdd clk a_181_2765# w_345_2737# CMOSP w=40 l=2
1350 +  ad=0 pd=0 as=0 ps=0
1351 M1657 vdd a_1656_1302# a_1644_1098# w_1720_1162# CMOSP w=50 l=2
1352 +  ad=0 pd=0 as=250 ps=110
1353 M1658 vdd a_2215_712# a_2289_650# w_2398_895# CMOSP w=40 l=2
1354 +  ad=0 pd=0 as=0 ps=0
1355 M1659 vdd a_184_4182# a_182_4064# w_258_4118# CMOSP w=50 l=2
1356 +  ad=0 pd=0 as=250 ps=110
1357 M1660 gnd a_21_2286# a_185_1986# Gnd CMOSN w=40 l=2
1358 +  ad=0 pd=0 as=0 ps=0
1359 M1661 gnd a_1378_2371# a_1473_2264# Gnd CMOSN w=40 l=2
1360 +  ad=0 pd=0 as=0 ps=0
1361 M1662 sum_out dfl1 vdd w_2524_3615# CMOSP w=40 l=2
1362 +  ad=0 pd=0 as=0 ps=0
1363 M1663 a_2252_1803# a_2215_1372# gnd Gnd CMOSN w=40 l=2
1364 +  ad=0 pd=0 as=0 ps=0
1365 M1664 a_883_3189# B1 gnd Gnd CMOSN w=40 l=2
1366 +  ad=0 pd=0 as=0 ps=0
1367 M1665 a_2252_1731# clk gnd Gnd CMOSN w=40 l=2
1368 +  ad=0 pd=0 as=0 ps=0
1369 M1666 carry_4 carry_4_bar a_2554_1072# Gnd CMOSN w=40 l=2
1370 +  ad=760 pd=118 as=0 ps=0
1371 M1667 cin2 a_1315_2560# vdd w_1313_2589# CMOSP w=40 l=2
1372 +  ad=0 pd=0 as=0 ps=0
1373 M1668 gnd clk a_442_4203# Gnd CMOSN w=40 l=2
1374 +  ad=0 pd=0 as=0 ps=0
1375 M1669 a_185_3901# p1 a_185_3880# Gnd CMOSN w=40 l=2
1376 +  ad=0 pd=0 as=760 ps=118
1377 M1670 a_2215_2692# add_out1 vdd w_2222_2624# CMOSP w=40 l=2
1378 +  ad=0 pd=0 as=0 ps=0
1379 M1671 a_883_2276# a_759_2277# a_883_2188# Gnd CMOSN w=40 l=2
1380 +  ad=760 pd=118 as=0 ps=0
1381 M1672 a_1199_1436# a_1106_1444# gnd Gnd CMOSN w=20 l=2
1382 +  ad=100 pd=50 as=0 ps=0
1383 M1673 a_1378_2205# a_1143_1441# vdd w_1361_2191# CMOSP w=50 l=2
1384 +  ad=250 pd=110 as=0 ps=0
1385 M1674 gnd a_182_233# a_185_196# Gnd CMOSN w=40 l=2
1386 +  ad=0 pd=0 as=0 ps=0
1387 M1675 vdd a_24_3246# a_351_3244# w_595_3216# CMOSP w=40 l=2
1388 +  ad=0 pd=0 as=0 ps=0
1389 M1676 a_2289_1970# a_2363_2177# vdd w_2398_2215# CMOSP w=40 l=2
1390 +  ad=0 pd=0 as=0 ps=0
1391 M1677 a_1199_1436# a_1106_1444# vdd w_1185_1419# CMOSP w=50 l=2
1392 +  ad=250 pd=110 as=0 ps=0
1393 M1678 vdd gout2 a_1113_1930# w_1083_1923# CMOSP w=40 l=2
1394 +  ad=0 pd=0 as=0 ps=0
1395 M1679 vdd a_21_849# a_185_528# w_266_519# CMOSP w=40 l=2
1396 +  ad=0 pd=0 as=0 ps=0
1397 M1680 gnd a_1103_3160# a_1106_3123# Gnd CMOSN w=40 l=2
1398 +  ad=0 pd=0 as=0 ps=0
1399 M1681 vdd a_1829_1854# a_1953_1773# w_1923_1766# CMOSP w=40 l=2
1400 +  ad=0 pd=0 as=0 ps=0
1401 M1682 a_184_830# a_181_849# vdd w_265_821# CMOSP w=40 l=2
1402 +  ad=0 pd=0 as=0 ps=0
1403 M1683 vdd a_883_2358# pin_p3 w_968_2269# CMOSP w=40 l=2
1404 +  ad=0 pd=0 as=0 ps=0
1405 M1684 vdd D3 a_24_851# w_15_821# CMOSP w=40 l=2
1406 +  ad=0 pd=0 as=0 ps=0
1407 M1685 a_443_1507# a_185_1486# A2 Gnd CMOSN w=40 l=2
1408 +  ad=0 pd=0 as=760 ps=118
1409 M1686 a_1953_3376# a_1829_3377# a_1953_3288# Gnd CMOSN w=40 l=2
1410 +  ad=760 pd=118 as=0 ps=0
1411 M1687 a_2252_3211# a_2215_2692# vdd w_2222_3204# CMOSP w=40 l=2
1412 +  ad=0 pd=0 as=0 ps=0
1413 M1688 gnd a_712_2772# gout2 Gnd CMOSN w=20 l=2
1414 +  ad=0 pd=0 as=100 ps=50
1415 M1689 a_1953_2811# a_998_3101# gnd Gnd CMOSN w=40 l=2
1416 +  ad=0 pd=0 as=0 ps=0
1417 M1690 a_21_1328# a_24_1330# vdd w_266_1124# CMOSP w=40 l=2
1418 +  ad=0 pd=0 as=0 ps=0
1419 M1691 a_1953_2162# cin2 gnd Gnd CMOSN w=40 l=2
1420 +  ad=0 pd=0 as=0 ps=0
1421 M1692 vdd a_1482_1493# a_1653_1360# w_1729_1424# CMOSP w=50 l=2
1422 +  ad=0 pd=0 as=250 ps=110
1423 M1693 a_2289_1310# a_2215_1372# a_2428_1474# Gnd CMOSN w=40 l=2
1424 +  ad=760 pd=118 as=0 ps=0
1425 M1694 a_1106_1348# pln_p4 vdd w_1076_1341# CMOSP w=40 l=2
1426 +  ad=0 pd=0 as=0 ps=0
1427 M1695 cin1 a_1094_3507# vdd w_1178_3479# CMOSP w=40 l=2
1428 +  ad=0 pd=0 as=0 ps=0
1429 M1696 gnd a_182_3107# a_185_3070# Gnd CMOSN w=40 l=2
1430 +  ad=0 pd=0 as=0 ps=0
1431 M1697 dfl2 sum_out a_2554_3454# Gnd CMOSN w=40 l=2
1432 +  ad=760 pd=118 as=0 ps=0
1433 M1698 a_1105_2667# a_1148_2567# vdd w_1181_2596# CMOSP w=50 l=2
1434 +  ad=250 pd=110 as=0 ps=0
1435 M1699 a_1203_1637# a_1110_1645# gnd Gnd CMOSN w=20 l=2
1436 +  ad=100 pd=50 as=0 ps=0
1437 M1700 vdd da0 a_24_4203# w_15_4173# CMOSP w=40 l=2
1438 +  ad=0 pd=0 as=0 ps=0
1439 M1701 vdd a_759_3100# a_883_3019# w_853_3012# CMOSP w=40 l=2
1440 +  ad=0 pd=0 as=0 ps=0
1441 M1702 a_1203_1637# a_1110_1645# vdd w_1189_1620# CMOSP w=50 l=2
1442 +  ad=250 pd=110 as=0 ps=0
1443 M1703 a_184_1309# a_181_1328# vdd w_265_1300# CMOSP w=40 l=2
1444 +  ad=0 pd=0 as=0 ps=0
1445 M1704 vdd a_1953_3458# add_out w_2038_3369# CMOSP w=40 l=2
1446 +  ad=0 pd=0 as=0 ps=0
1447 M1705 vdd a_2252_1643# a_2252_1561# w_2222_1554# CMOSP w=40 l=2
1448 +  ad=0 pd=0 as=0 ps=0
1449 M1706 gnd a_1385_2264# a_1556_2131# Gnd CMOSN w=20 l=2
1450 +  ad=0 pd=0 as=100 ps=50
1451 M1707 a_181_1328# a_351_1328# vdd w_345_1300# CMOSP w=40 l=2
1452 +  ad=0 pd=0 as=0 ps=0
1453 M1708 a_883_1893# A3 vdd w_853_1886# CMOSP w=40 l=2
1454 +  ad=0 pd=0 as=0 ps=0
1455 M1709 gnd clk a_184_3246# Gnd CMOSN w=40 l=2
1456 +  ad=0 pd=0 as=0 ps=0
1457 M1710 add_out2 a_1953_2250# vdd w_2038_2243# CMOSP w=40 l=2
1458 +  ad=0 pd=0 as=0 ps=0
1459 M1711 a_2252_2551# a_2252_2303# a_2252_2463# Gnd CMOSN w=40 l=2
1459 M1711 a_2252_2551# a_2252_2303# a_2252_2463# Gnd CMOSN w=40 l=2
1460 +  ad=760 pd=118 as=0 ps=0
1461 C0 vdd gnd 2.08fF
1462 C1 B2 A2 2.17fF
1463 C2 a_2289_650# Gnd 3.23fF
1464 C3 carry_4 Gnd 2.10fF
1465 C4 carr4 Gnd 6.43fF
1466 C5 a_2252_983# Gnd 4.11fF
1467 C6 a_2215_712# Gnd 5.47fF
1468 C7 a_2289_1310# Gnd 3.23fF
1469 C8 sum_3 Gnd 2.10fF
1470 C9 a_1656_1302# Gnd 3.05fF
1471 C10 a_2252_1643# Gnd 4.11fF
1472 C11 a_2215_1372# Gnd 5.47fF
1473 C12 a_1199_1063# Gnd 2.07fF
1474 C13 a_1199_1304# Gnd 2.03fF
1475 C14 a_1199_1436# Gnd 2.05fF
1476 C15 add_out3 Gnd 4.52fF
1477 C16 a_1203_1637# Gnd 2.24fF
1478 C17 a_1829_1854# Gnd 2.38fF
1479 C18 a_2289_1970# Gnd 3.23fF
1480 C19 sum_2 Gnd 2.10fF
1481 C20 add_out2 Gnd 2.54fF
1482 C21 a_1829_2251# Gnd 2.38fF
1483 C22 a_21_370# Gnd 3.23fF
1484 C23 a_181_370# Gnd 4.11fF
1485 C24 a_24_372# Gnd 5.47fF
1486 C25 a_21_849# Gnd 3.23fF
1487 C26 a_181_849# Gnd 4.11fF
1488 C27 a_24_851# Gnd 5.47fF
1489 C28 a_21_1328# Gnd 3.23fF
1490 C29 a_181_1328# Gnd 4.11fF
1491 C30 a_24_1330# Gnd 5.47fF
1492 C31 a_1143_1441# Gnd 5.54fF
1493 C32 pln_p4 Gnd 16.00fF
1494 C33 a_759_1974# Gnd 2.37fF
1495 C34 B3 Gnd 19.53fF
1496 C35 A3 Gnd 14.45fF
1497 C36 a_2252_2303# Gnd 4.11fF
1498 C37 a_2215_2032# Gnd 5.47fF
1499 C38 cin2 Gnd 9.50fF
1500 C39 a_2289_2630# Gnd 3.23fF
1501 C40 sum_1 Gnd 2.10fF
1502 C41 a_1147_1642# Gnd 5.31fF
1503 C42 a_21_1807# Gnd 3.23fF
1504 C43 a_181_1807# Gnd 4.11fF
1505 C44 a_24_1809# Gnd 5.47fF
1506 C45 pln_p3 Gnd 10.33fF
1507 C46 a_759_2277# Gnd 2.37fF
1508 C47 A2 Gnd 10.60fF
1509 C48 B2 Gnd 14.37fF
1510 C49 a_21_2286# Gnd 3.23fF
1511 C50 a_181_2286# Gnd 4.11fF
1512 C51 a_24_2288# Gnd 5.47fF
1513 C52 a_1148_2781# Gnd 5.77fF
1514 C53 a_1148_2567# Gnd 4.54fF
1515 C54 add_out1 Gnd 3.42fF
1516 C55 a_1829_2980# Gnd 2.38fF
1517 C56 a_21_2765# Gnd 3.23fF
1518 C57 a_181_2765# Gnd 4.11fF
1519 C58 a_24_2767# Gnd 5.47fF
1520 C59 a_2252_2963# Gnd 4.11fF
1521 C60 a_2215_2692# Gnd 5.47fF
1522 C61 dfo1 Gnd 3.23fF
1523 C62 a_998_3101# Gnd 7.94fF
1524 C63 a_759_3100# Gnd 2.37fF
1525 C64 B1 Gnd 14.98fF
1526 C65 A1 Gnd 9.74fF
1527 C66 a_21_3244# Gnd 3.23fF
1528 C67 cin0 Gnd 14.32fF
1529 C68 a_1103_3160# Gnd 2.62fF
1530 C69 a_181_3244# Gnd 4.11fF
1531 C70 a_24_3246# Gnd 5.47fF
1532 C71 a_1829_3377# Gnd 2.38fF
1533 C72 dfl1 Gnd 4.11fF
1534 C73 dfo2 Gnd 5.47fF
1535 C74 a_21_4201# Gnd 3.23fF
1536 C75 a_181_4201# Gnd 4.11fF
1537 C76 a_24_4203# Gnd 5.47fF
1538 C77 w_346_40# Gnd 5.46fF
1539 C78 w_266_40# Gnd 5.46fF
1540 C79 w_266_166# Gnd 5.46fF
1541 C80 w_595_342# Gnd 5.46fF
1542 C81 w_345_342# Gnd 5.46fF
1543 C82 w_265_342# Gnd 5.46fF
1544 C83 w_15_342# Gnd 5.46fF
1545 C84 w_346_519# Gnd 5.46fF
1546 C85 w_266_519# Gnd 5.46fF
1547 C86 w_2222_644# Gnd 5.46fF
1548 C87 w_266_645# Gnd 5.46fF
1549 C88 w_2524_895# Gnd 5.46fF
1550 C89 w_2398_895# Gnd 5.46fF
1551 C90 w_2222_894# Gnd 5.46fF
1552 C91 w_595_821# Gnd 5.46fF
1553 C92 w_345_821# Gnd 5.46fF
1554 C93 w_265_821# Gnd 5.46fF
1555 C94 w_15_821# Gnd 5.46fF
1556 C95 w_2524_975# Gnd 5.46fF
1557 C96 w_2222_974# Gnd 5.46fF
1558 C97 w_1728_1031# Gnd 5.46fF
1560 C99 w_346_998# Gnd 5.46fF
1561 C100 w_266_998# Gnd 5.46fF
1562 C101 w_266_1124# Gnd 5.46fF
1563 C102 w_2222_1224# Gnd 5.46fF
1564 C103 w_2222_1304# Gnd 5.46fF
1565 C104 w_1737_1293# Gnd 5.46fF
1566 C105 w_1477_1228# Gnd 5.46fF
1567 C106 w_1076_1341# Gnd 5.46fF
1568 C107 w_595_1300# Gnd 5.46fF
1569 C108 w_345_1300# Gnd 5.46fF
1570 C109 w_265_1300# Gnd 5.46fF
1571 C110 w_15_1300# Gnd 5.46fF
1572 C111 w_2524_1555# Gnd 5.46fF
1573 C112 w_2398_1555# Gnd 5.46fF
1574 C113 w_2222_1554# Gnd 5.46fF
1575 C114 w_1473_1463# Gnd 5.46fF
1576 C115 w_1076_1435# Gnd 5.46fF
1577 C116 w_346_1477# Gnd 5.46fF
1578 C117 w_266_1477# Gnd 5.46fF
1579 C118 w_2524_1635# Gnd 5.46fF
1580 C119 w_2222_1634# Gnd 5.46fF
1581 C120 w_1080_1636# Gnd 5.46fF
1582 C121 w_1923_1766# Gnd 5.46fF
1583 C122 w_714_1672# Gnd 5.46fF
1584 C123 w_266_1603# Gnd 5.46fF
1585 C124 w_2222_1884# Gnd 5.46fF
1586 C125 w_2038_1846# Gnd 5.46fF
1587 C126 w_1923_1846# Gnd 5.46fF
1588 C127 w_1799_1845# Gnd 5.46fF
1589 C128 w_595_1779# Gnd 5.46fF
1590 C129 w_345_1779# Gnd 5.46fF
1591 C130 w_265_1779# Gnd 5.46fF
1592 C131 w_15_1779# Gnd 5.46fF
1593 C132 w_2222_1964# Gnd 5.46fF
1594 C133 w_1083_1923# Gnd 5.46fF
1595 C134 w_853_1886# Gnd 5.46fF
1596 C135 w_1640_2064# Gnd 5.46fF
1597 C136 w_1380_1999# Gnd 5.46fF
1598 C137 w_1083_2019# Gnd 5.46fF
1599 C138 w_968_1966# Gnd 5.46fF
1600 C139 w_853_1966# Gnd 5.46fF
1601 C140 w_729_1965# Gnd 5.46fF
1602 C141 w_346_1956# Gnd 5.46fF
1603 C142 w_266_1956# Gnd 5.46fF
1604 C143 w_266_2082# Gnd 5.46fF
1605 C144 w_2524_2215# Gnd 5.46fF
1606 C145 w_2398_2215# Gnd 5.46fF
1607 C146 w_2222_2214# Gnd 5.46fF
1608 C147 w_2524_2295# Gnd 5.46fF
1609 C148 w_2222_2294# Gnd 5.46fF
1610 C149 w_2038_2243# Gnd 5.46fF
1611 C150 w_1923_2243# Gnd 5.46fF
1612 C151 w_1799_2244# Gnd 5.46fF
1613 C152 w_1923_2323# Gnd 5.46fF
1614 C153 w_1376_2234# Gnd 5.46fF
1615 C154 w_1083_2269# Gnd 5.46fF
1616 C155 w_968_2269# Gnd 5.46fF
1617 C156 w_853_2269# Gnd 5.46fF
1618 C157 w_729_2270# Gnd 5.46fF
1619 C158 w_853_2349# Gnd 5.46fF
1620 C159 w_595_2258# Gnd 5.46fF
1621 C160 w_345_2258# Gnd 5.46fF
1622 C161 w_265_2258# Gnd 5.46fF
1623 C162 w_15_2258# Gnd 5.46fF
1624 C163 w_2222_2544# Gnd 5.46fF
1625 C164 w_2222_2624# Gnd 5.46fF
1626 C165 w_714_2522# Gnd 5.46fF
1627 C166 w_346_2435# Gnd 5.46fF
1628 C167 w_266_2435# Gnd 5.46fF
1629 C168 w_1189_2639# Gnd 5.46fF
1630 C169 w_266_2561# Gnd 5.46fF
1631 C170 w_2524_2875# Gnd 5.46fF
1632 C171 w_2398_2875# Gnd 5.46fF
1633 C172 w_2222_2874# Gnd 5.46fF
1634 C173 w_1923_2892# Gnd 5.46fF
1635 C174 w_2524_2955# Gnd 5.46fF
1636 C175 w_2222_2954# Gnd 5.46fF
1637 C176 w_2038_2972# Gnd 5.46fF
1638 C177 w_1923_2972# Gnd 5.46fF
1639 C178 w_1799_2971# Gnd 5.46fF
1640 C179 w_1188_2888# Gnd 5.46fF
1641 C180 w_714_2798# Gnd 5.46fF
1642 C181 w_595_2737# Gnd 5.46fF
1643 C182 w_345_2737# Gnd 5.46fF
1644 C183 w_265_2737# Gnd 5.46fF
1645 C184 w_15_2737# Gnd 5.46fF
1646 C185 w_346_2914# Gnd 5.46fF
1647 C186 w_266_2914# Gnd 5.46fF
1648 C187 w_853_3012# Gnd 5.46fF
1649 C188 w_1187_3093# Gnd 5.46fF
1650 C189 w_968_3092# Gnd 5.46fF
1651 C190 w_853_3092# Gnd 5.46fF
1652 C191 w_729_3091# Gnd 5.46fF
1653 C192 w_266_3040# Gnd 5.46fF
1654 C193 w_2222_3204# Gnd 5.46fF
1655 C194 w_2222_3284# Gnd 5.46fF
1656 C195 w_595_3216# Gnd 5.46fF
1657 C196 w_345_3216# Gnd 5.46fF
1658 C197 w_265_3216# Gnd 5.46fF
1659 C198 w_15_3216# Gnd 5.46fF
1660 C199 w_2038_3369# Gnd 5.46fF
1661 C200 w_1923_3369# Gnd 5.46fF
1662 C201 w_1799_3370# Gnd 5.46fF
1663 C202 w_1178_3314# Gnd 5.46fF
1664 C203 w_1923_3449# Gnd 5.46fF
1665 C204 w_2524_3535# Gnd 5.46fF
1666 C205 w_2398_3535# Gnd 5.46fF
1667 C206 w_2222_3534# Gnd 5.46fF
1668 C207 w_1178_3479# Gnd 5.46fF
1669 C208 w_2524_3615# Gnd 5.46fF
1670 C209 w_2222_3614# Gnd 5.46fF
1671 C210 w_2222_3864# Gnd 5.46fF
1672 C211 w_346_3871# Gnd 5.46fF
1673 C212 w_266_3871# Gnd 5.46fF
1674 C213 w_266_3997# Gnd 5.46fF
1675 C214 w_595_4173# Gnd 5.46fF
1676 C215 w_345_4173# Gnd 5.46fF
1677 C216 w_265_4173# Gnd 5.46fF
1678 C217 w_15_4173# Gnd 5.46fF
1679 C218 a_67_n474# Gnd 3.23fF
1680 C219 clk Gnd 10.31fF
1681 C220 w_0_n480# Gnd 5.46fF
1682 C221 w_302_n229# Gnd 5.46fF
1683 C222 w_0_n230# Gnd 5.46fF
1684 C223 w_302_n149# Gnd 5.46fF
1685 C224 w_0_n150# Gnd 5.46fF
1686 C225 gnd Gnd 169.06fF
1687 C226 a_30_n141# Gnd 4.12fF
1688 C227 a_n7_n412# Gnd 5.47fF
1689 C228 w_0_0# Gnd 5.46fF
1690 C229 p1 Gnd 8.50fF
1691 C230 w_0_0# Gnd 5.46fF
1692 C231 gout Gnd 6.85fF
1693 C232 vdd Gnd 170.66fF
1694 C233 w_239_99# Gnd 5.46fF
1695 C234 w_0_0# Gnd 5.46fF
1696
1697
1698
1699 .tran 0.1n 130n
```

< SECTION 10 > Parameters of the post-layout CLA adder:

So in the section we saw how the post-layout CLA adder was giving the simulation results and compared that result with the pre-layout CLA adder. Now lets look at the worst and best delay of the CLA adder for the prelayout and post layout case in a tabular form :-

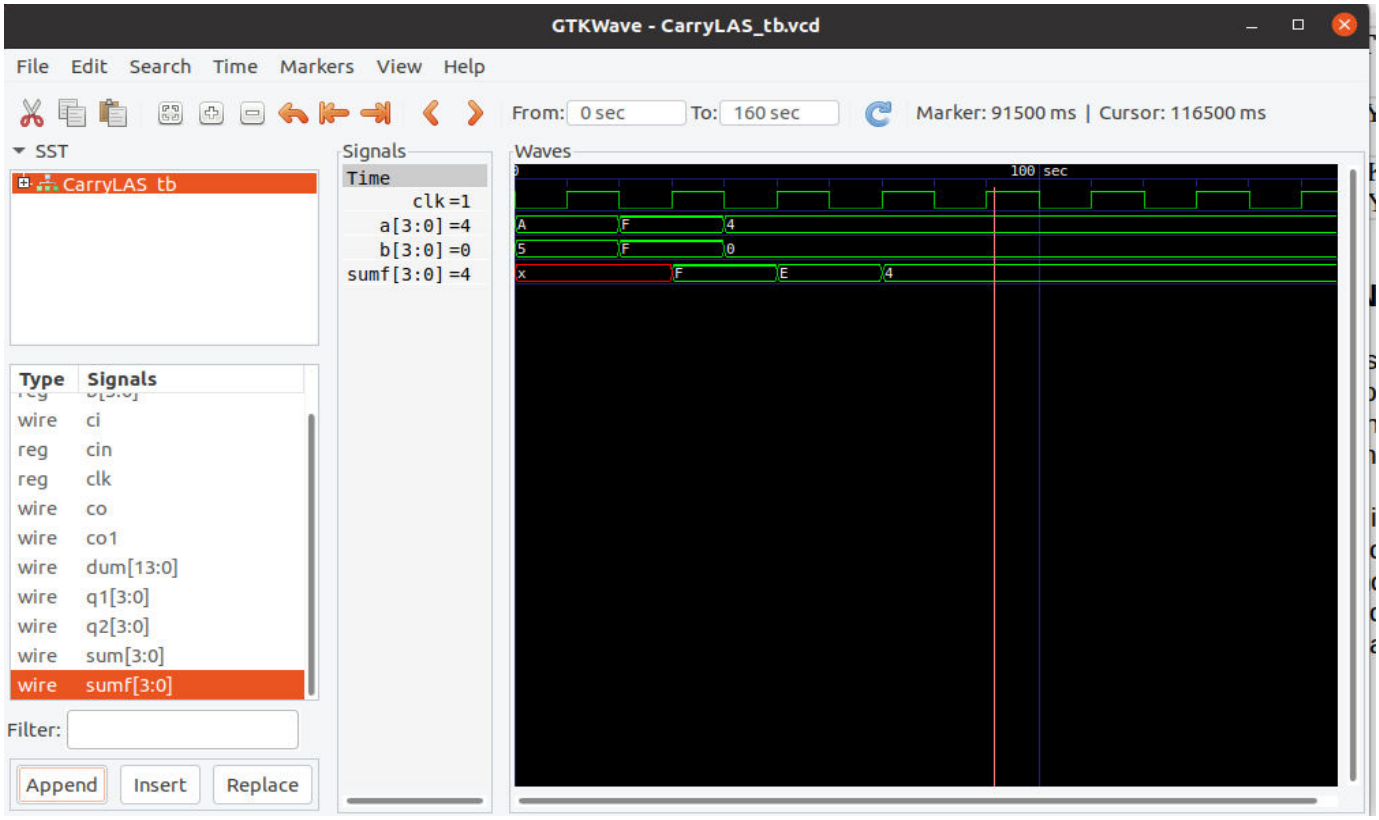
PARAMETERS	POST-LAYOUT	PRE-LAYOUT
MAX DELAY	5.5698 ns	4.009 ns
MAX CLOCK FREQUENCY	2.6 GHz	2.63 Ghz

<SECTION 11 > Verilog code for the CLA adder :-

Till now we saw how we saw the implementation of the CLA adder with the help of the NGSPICE and MAGIC implementation, now we will look at the CLA adder implementation with the help of the verilog coding. The corresponding simulation results are as follows:

The simulation results are for the values
A = 1010 and B = 0101
A = 1111 and B = 1111
A = 0100 and B = 0000
With initial carry cin = 0 for all cases.

Output for the above cases is given below:



So we can see that the results coming at the output is as expected and the sum is also appearing at the positive edge of the second cycle, as per the given question. The inputs are read at every positive edge which then give the sum output at the positive edge of the next cycle. Also on observing we will see that for the 2nd value i.e. when A = 1111 and B = 1111 the sum will come as 1E so the 1 will be reflected in the carry output.

For this verilog implementation, it was asked to use structural implementation. So the corresponding implementation is as follows:

D Flip Flop

```
1 `timescale 1ns / 1ps
2
3 module d_flipflop(D, clk, Q, Qn);
4 output Q;
5 output Qn;
6 input  clk;
7 input  D;
8 wire o1,o2,o3,o4 ;
9 nand ( o1, D, o2);
10 nand (o2, clk, o3,o1);
11 nand (o3, clk, o4);
12 nand (o4, o3, o1);
13 nand (Qn, o2, Q);
14 nand (Q, Qn, o3);
15
16 endmodule
```

CLA adder module

```
module CarryLA_4(a,b,ci,sum,co);

input [3:0] a,b;
input ci;

output [3:0] sum;
output co;

wire[3:0] g,p,cout;
wire G0,P0;
wire[9:0] w;

and a0(g[0],a[0],b[0]);
and a1(g[1],a[1],b[1]);
and a2(g[2],a[2],b[2]);
and a3(g[3],a[3],b[3]);

xor x0(p[0],a[0],b[0]);
xor x1(p[1],a[1],b[1]);
xor x2(p[2],a[2],b[2]);
xor x3(p[3],a[3],b[3]);

and and0(w[0],p[0],ci);
or or0(cout[0],g[0],w[0]);

and and1(w[1],p[1],p[0],ci);
and and2(w[2],p[1],g[0]);
or or1(cout[1],g[1],w[2],w[1]);

and and3(w[3],p[2],p[1],p[0],ci);
and and4(w[4],p[2],p[1],g[0]);
and and5(w[5],p[2],g[1]);
or or2(cout[2],g[2],w[5],w[4],w[3]);

and and6(w[6],p[3],p[2],p[1],g[0]);
and and7(w[7],p[3],p[2],g[1]);
and and8(w[8],p[3],p[2],p[1],p[0],ci);
and and9(w[9],p[3],g[2]);
or or3(cout[3],g[3],w[9],w[8],w[7],w[6]);

and and10(co,cout[3],1);

xor xor0(sum[0],p[0],ci);
xor xor1(sum[1],p[1],cout[0]);
xor xor2(sum[2],p[2],cout[1]);
xor xor3(sum[3],p[3],cout[2]);

endmodule
```

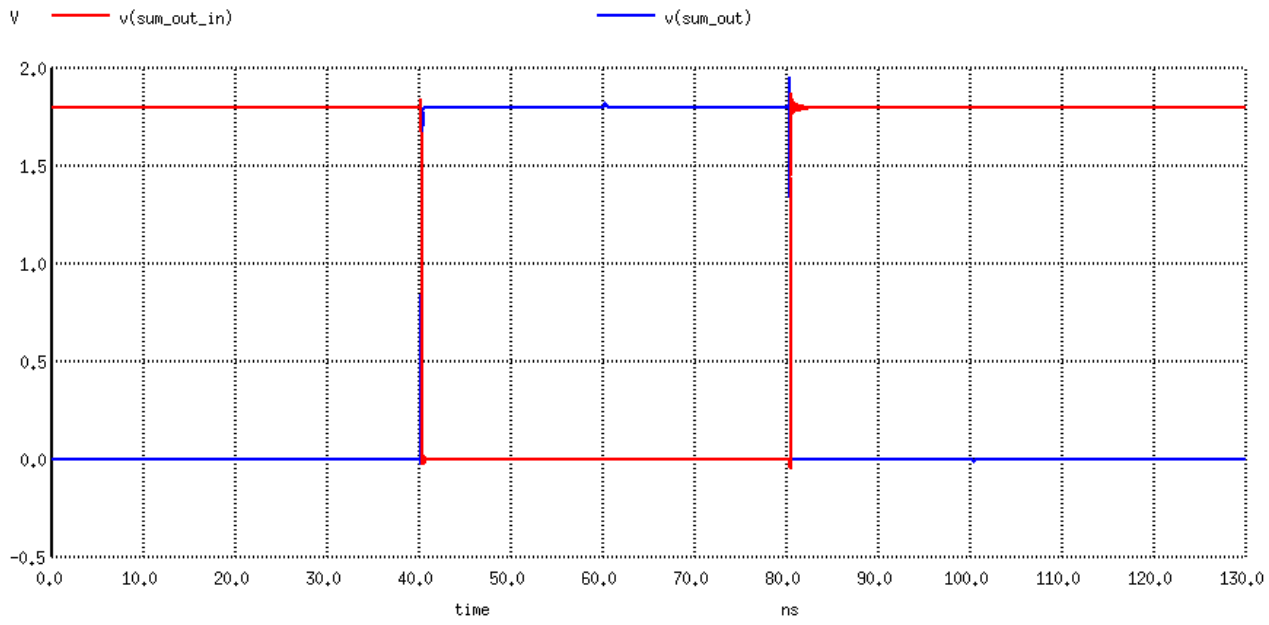
CLA adder test bench

```
module CarryLAS_tb;

reg [3:0] a;
reg [3:0] b;
reg cin;
reg clk;
wire [3:0] sum;
wire [3:0] sumf;
wire [13:0] dum;
wire of; //overflow
wire co;
wire [3:0]q1;
wire [3:0]q2;
integer i;


initial         begin
                $dumpfile("CarryLAS_tb.vcd");
                $dumpvars(0,CarryLAS_tb);
        end

d_flipflop dff1(a[0],clk,q1[0], dum[0]);
d_flipflop dff2(b[0],clk,q2[0], dum[1]);
d_flipflop dff3(a[1],clk,q1[1], dum[2]);
d_flipflop dff4(b[1],clk,q2[1], dum[3]);
d_flipflop dff5(a[2],clk,q1[2], dum[4]);
d_flipflop dff6(b[2],clk,q2[2], dum[5]);
d_flipflop dff7(a[3],clk,q1[3], dum[6]);
d_flipflop dff8(b[3],clk,q2[3], dum[7]);
d_flipflop dff13(cin,clk,ci, dum[12]);


CarryLA_4 CLA(q1,q2,ci,sum,co1);


d_flipflop dff9(sum[0],clk,sumf[0], dum[8]);
d_flipflop dff10(sum[1],clk,sumf[1], dum[9]);
d_flipflop dff11(sum[2],clk,sumf[2], dum[10]);
d_flipflop dff12(sum[3],clk,sumf[3], dum[11]);
d_flipflop dff14(co1,clk,co, dum[13]);

initial clk = 0;
always #10 clk = ~clk;


initial
begin
assign cin =0;
assign a=4'b1010;
assign b=4'b0101;


#20
assign a=4'b1111;
assign b=4'b1111;


#20
assign a=4'b0100;
assign b=4'b0000;
#120
$finish;
end


endmodule
```

So we can see that in case of the structural modeling we make use of the gates and try to make connections as per the schematic of the main circuit.

CONCLUSION :

In this project I was able to understand how circuits are implemented in real life and what all ways are there to implement the circuits. CLA adder was implemented with the help of NGSPICE, MAGIC tool and Verilog coding. This project gave an insight of how we use different component to make a fully functional logical circuit and how we should take care of hold time and setup time to avoid error in our circuits. Finally the output of my adder is high enough to run an inverter of size 20/10 and on passing the sum bit, we will get the inverted output. Below is the result of that:



So, the input sum bit is given by sum_out and output of inverter is given as sum_out_in.