Experiment No.6
Implement Carry Look Ahead Adder.
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Date of Performance:
Date of Submission:

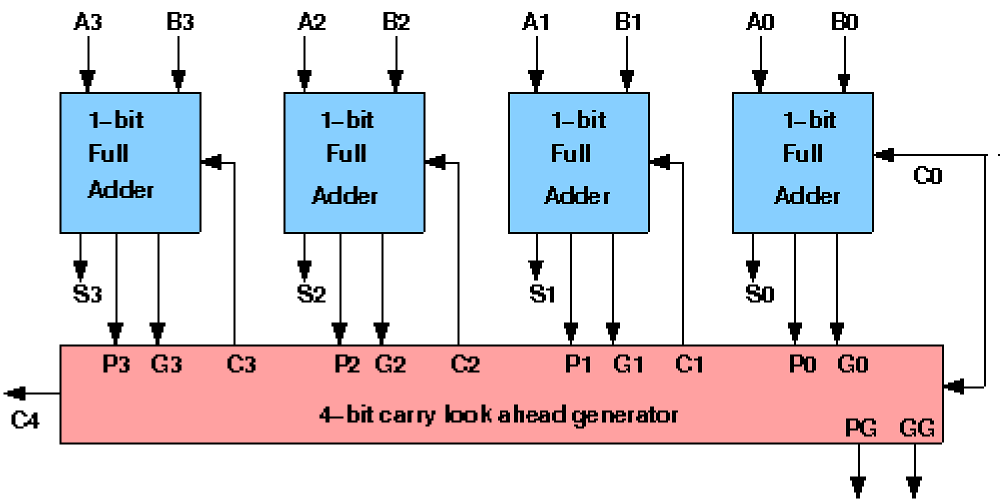
Aim: . To implement carry look ahead adder.

Objective:
It computes the carries parallely thus greatly speeding up the computation.

1. To understanding behaviour of carry lookahead adder from module designed by the student as part of the experiment
2. To understand the concept of reducing computation time with respect of ripple carry adder by using carry generate and propagate functions.
3. The adder will add two 4 bit numbers

Theory:

To reduce the computation time, there are faster ways to add two binary numbers by using carry lookahead adders. They work by creating two signals P and G known to be Carry Propagator and Carry Generator. The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry ,regardless of input carry. The block diagram of a 4-bit Carry Lookahead Adder is shown here below -



The number of gate levels for the carry propagation can be found from the circuit of full adder. The signal from input carry Cin to output carry Cout requires an AND gate and an OR gate, which constitutes two gate levels. So if there are four full adders in the parallel adder, the output carry C5 would have 2 X 4 = 8 gate levels from C1 to C5. For an n-bit parallel adder, there are 2n gate levels to propagate through.

Design Issues :

The corresponding boolean expressions are given here to construct a carry lookahead adder. In the carry-lookahead circuit we ned to generate the two signals carry propagator(P) and carry generator(G),

$$Pi = Ai \oplus Bi$$
$$Gi = Ai \cdot Bi$$

The output sum and carry can be expressed as

$$Sumi = Pi \oplus Ci$$
$$Ci+1 = Gi + (Pi \cdot Ci)$$

Having these we could design the circuit. We can now write the Boolean function for the carry output of each stage and substitute for each Ci its value from the previous equations:

$C1 = G0 + P0 \cdot C0$

$C2 = G1 + P1 \cdot C1 = G1 + P1 \cdot G0 + P1 \cdot P0 \cdot C0$

$C3 = G2 + P2 \cdot C2 = G2\ P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot C0$

$C4 = G3 + P3 \cdot C3 = G3\ P3 \cdot G2\ P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0 + P3 \cdot P2 \cdot P1 \cdot P0 \cdot C0$

Procedure:

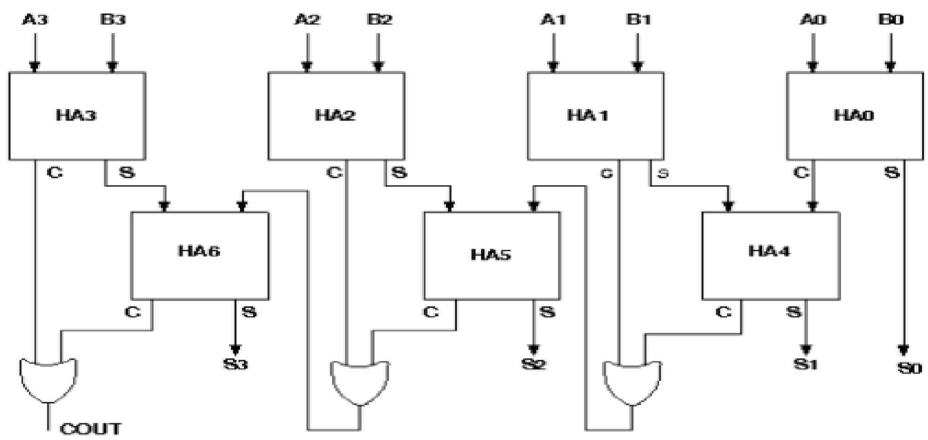
Procedure to perform the experiment: Design of Carry Look ahead Adders

1) Start the simulator as directed. This simulator supports 5-valued logic.
2) To design the circuit we need 7 half adder, 3 OR gate, 1 V+(to give 1 as input), 3 Digital display(2 for seeing input and 1 for seeing output sum), 1 Bit display(to see the carry output), wires.
3) The pin configurations of a component are shown whenever the mouse is hovered on any canned component of the palette or press the 'show pinconfig' button. Pin numbering starts from 1 and from the bottom left corner (indicating with the circle) and increases anticlockwise.
4) For half adder input is in pin-5,8 output sum is in pin-4 and carry is pin-1
5) Click on the half adder component(in the Adder drawer in the pallet) and then click on the position of the editor window where you want to add the component(no drag and drop, simple click will serve the purpose), likewise add 6 more full adders(from the Adder drawer in the pallet), 3 OR gates(from Logic Gates drawer in the pallet), 1 V+, 3 digital display and 1 bit Displays(from Display and Input drawer of the pallet, if it is not seen scroll down in the drawer)
6) To connect any two components select the Connection menu of Palette, and then click on the Source terminal and click on the target terminal. According to the circuit

diagram connect all the components; connect V+ to the upper input terminals of 2 digital displays according to you input. Connect the OR gates according to the diagram shown in the screenshot connect the pin-1 of the half adder which will give the final carry output. Connect the sum (pin-4) of those adders to the terminals of the third digital display which will give output sum. After the connection is over click the selection tool in the pallet.

7) See the output; in the screenshot diagram we have given the value 0011(3) and 0111(7) so get 10 as sum and 0 as carry. You can also use many bit switches instead of V+ to give input and by double clicking those bit switches can give different values and check the result.

Circuit diagram of Carry Look Ahead Adder:

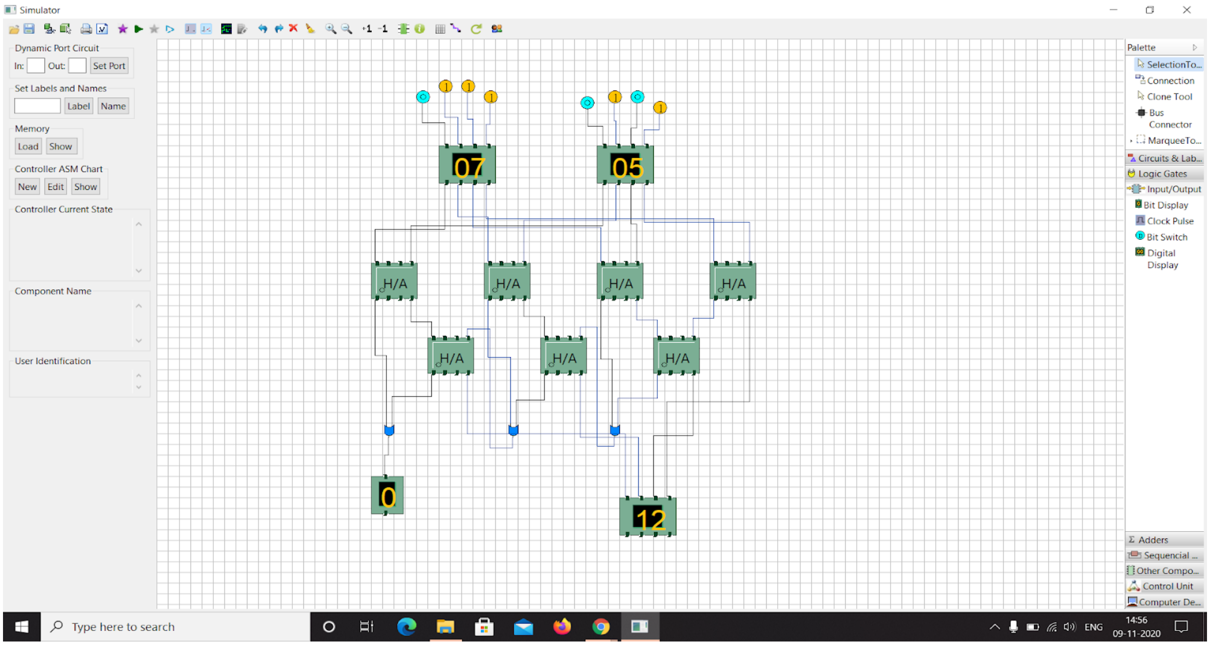


Components required:

The components needed to create 4 bit carry look ahead adder is listed here -

1. 7 half-adders: 4 to create the look adder circuit, and 3 to evaluate Si and Pi · Ci
2. 3 OR gates to generate the next level carry Ci+1
3. wires to connect
4. LED display to obtain the output

Screenshots of Carry Look Ahead Adder:



Conclusion:

The experiment carried out with the Carry Look-Ahead Adder in Logisim has furnished us with significant insights into the efficiency and operation of this advanced digital circuit. We've illustrated the remarkable speed at which the Carry Look-Ahead Adder can perform binary number addition, thanks to its ability to minimize carry propagation delays and reduce computation time. This attribute underscores its pivotal role in contemporary computer architecture and arithmetic circuits. Beyond that, this experiment reaffirms the significance of streamlined adder designs and demonstrates how complex digital circuits can be practically implemented within the realm of digital logic simulation.