CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Memory Organization

Lecture No.- 02

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Recap of Previous Lecture

Topic Memory Hierarchy ✓

Topic Memory Presentation

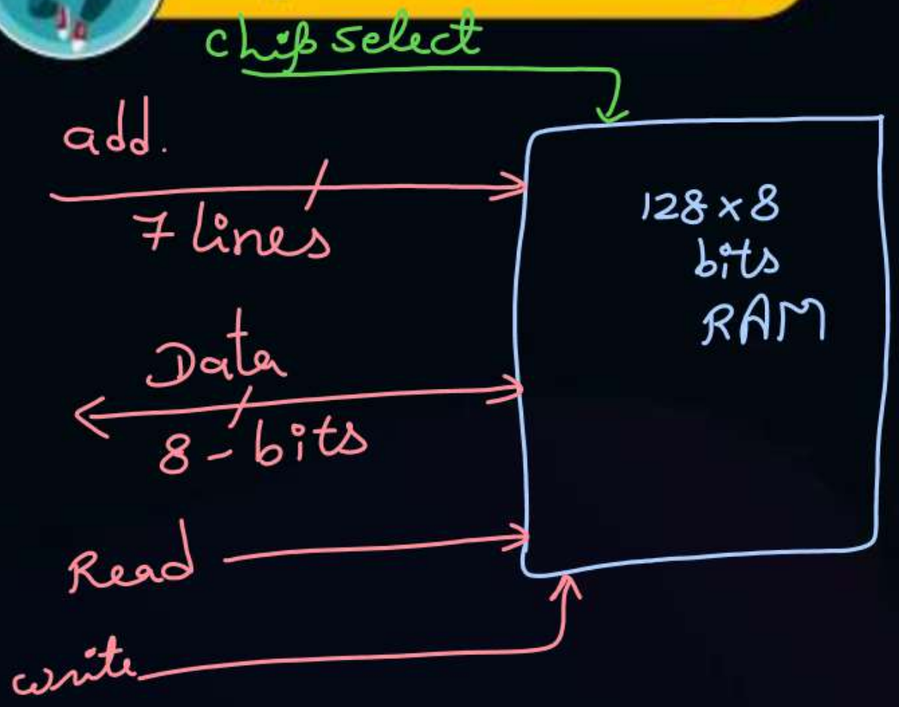
Topic Memory Address Decoder

Topic Main Memory

Topics to be Covered

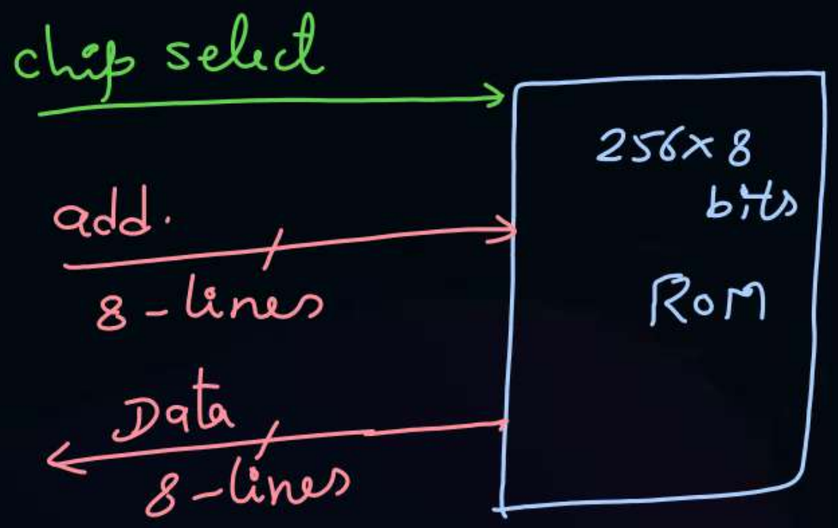
- Topic: RAM Chip
- Topic: ROM Chip
- Topic: Multiple Chips in Single Memory System
- Topic: DRAM Refresh

Topic : RAM Chip



chip select	Read	write	operation
0	x	x	No operation
1	0	1	write
1	0	0	No operation
1	1	x	Read

Topic : ROM Chip

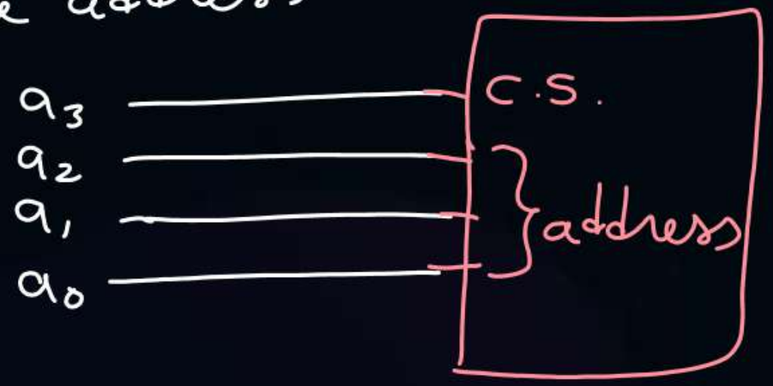


C.S.	operation
0	No operation
1	Read

Topic : Chip Select

ex:-

4-line address



a_3 must be always 1 to select chip.

$a_3\ a_2\ a_1\ a_0$

addresses ⇒

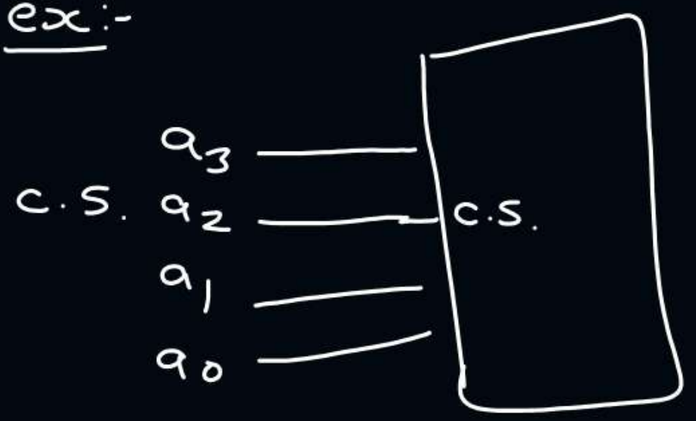
a_3	a_2	a_1	a_0
1	0	0	0
1	0	0	1
1	0	1	0
⋮			
1	1	1	1

$(8)_{10}$

Range

$(15)_{10}$

ex:-

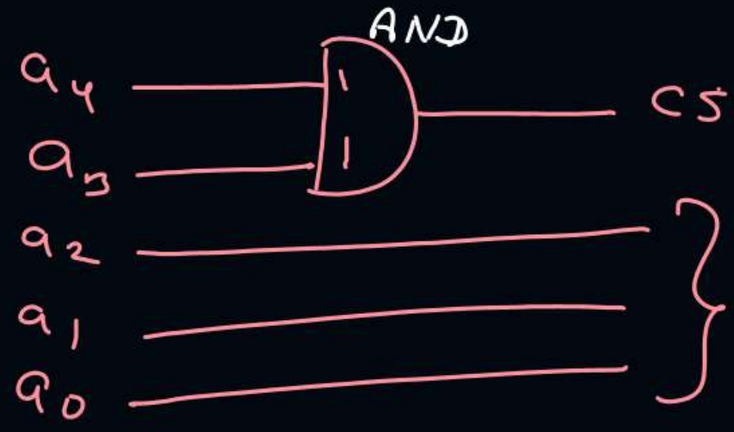


$a_3\ a_2\ a_1\ a_0$

add. ⇒ 0 1 0 0

⋮

1 1 1 1



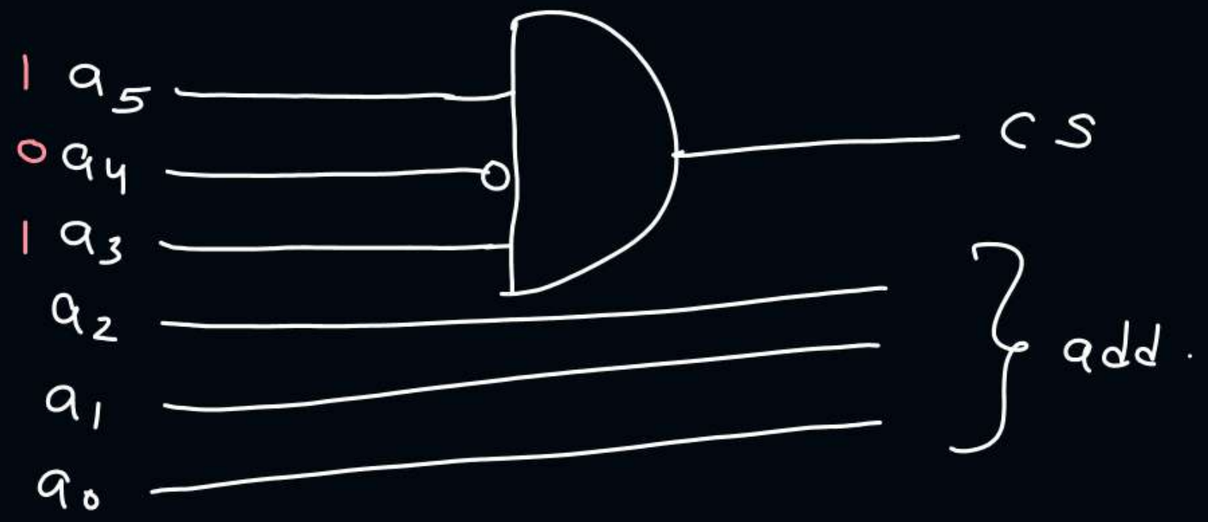
1 1 0 0 0

⋮

1 1 1 1 1

} add. range

ex:-



add. range :- 101 000

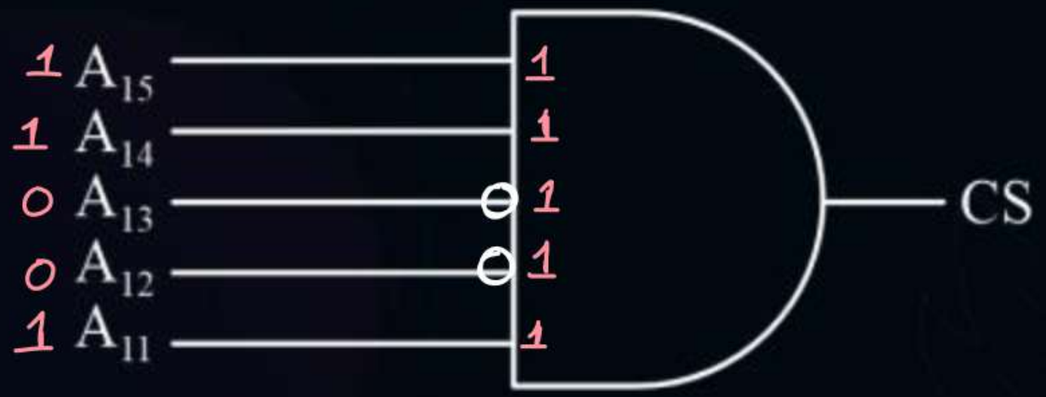
:

101 111

[MCQ]

GATE - 2019 PYQ

#Q. The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the memory system has 16 address lines denoted by A_{15} to A_0. What is the range of address (in hexadecimal) of the memory system that can get enabled by the chip select (CS) signal?

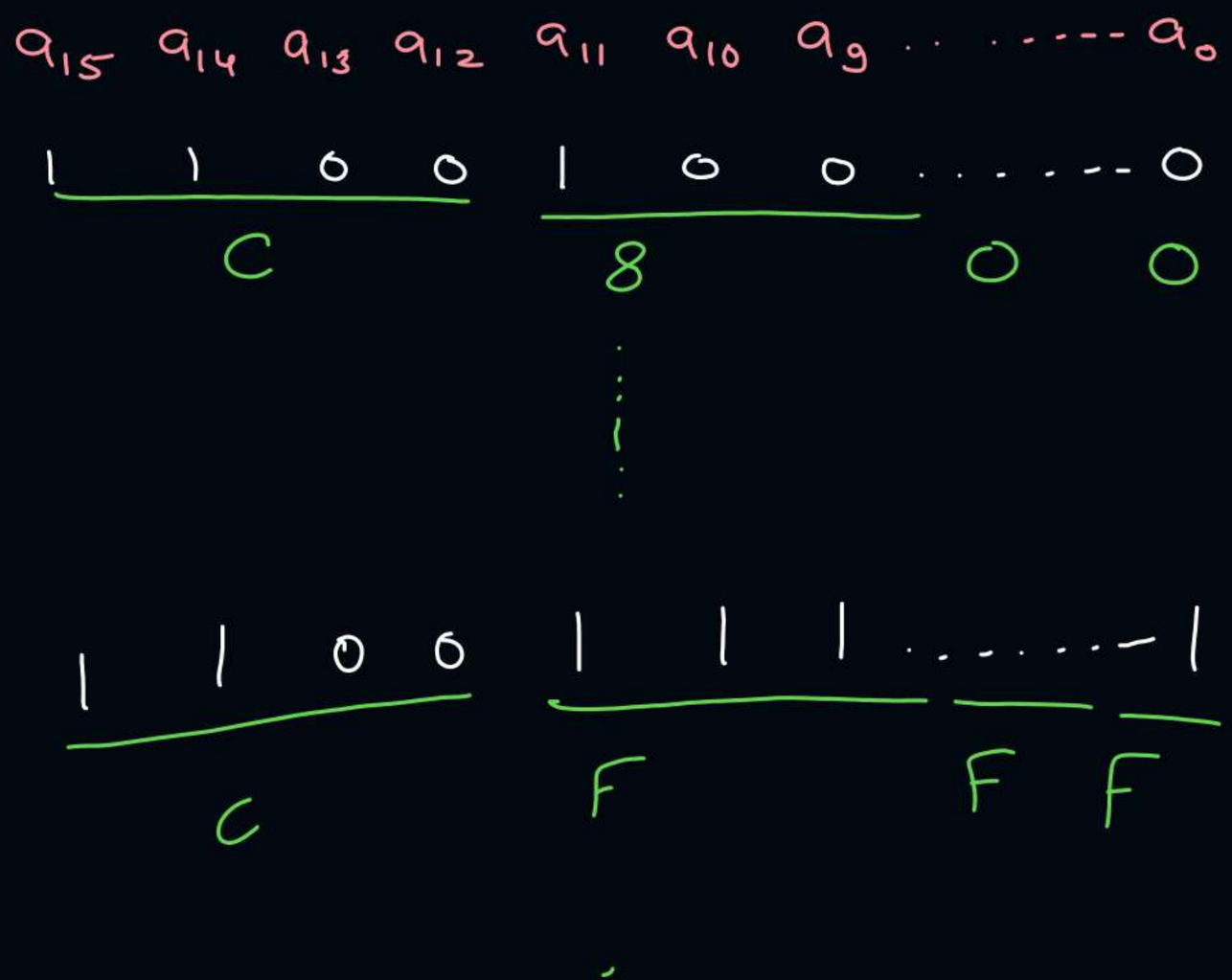


A ✓ C800 to CFFF

B CA00 to CAFF

C C800 to C8FF

D DA00 to DFFF


a_{15} a_{14} a_{13} a_{12} a_{11} a_{10} a_9 ..... a_0
1 1 0 0 1 0 0 0
C 8 0 0
1 1 0 0 1 1 1 1
C F F F

Topic : Multiple Chips in Single Memory System

Total capacity = no. of chips * 1 chip capacity

[NAT]

#Q. How many 64 bytes RAM chips are needed to provide a memory capacity of 1Kbytes?

$$= \frac{1\,k\,bytes}{64\,bytes}$$

$$= \frac{2^{10}}{2^{6}}$$

$$= 2^{4}$$

$$= 16 \quad \text{Ans.}$$

[NAT]

#Q. Total memory capacity is 8 Mbytes, if we use 16 chips of size 512Kbytes each?

$= 16 * 512$ k bytes

$= 2^4 * 2^9 * 2^{10}$ bytes

$= 2^{23}$ bytes

$= 8$ m bytes

Topic : Multiple Chips in Single Memory System

ex:-

add.

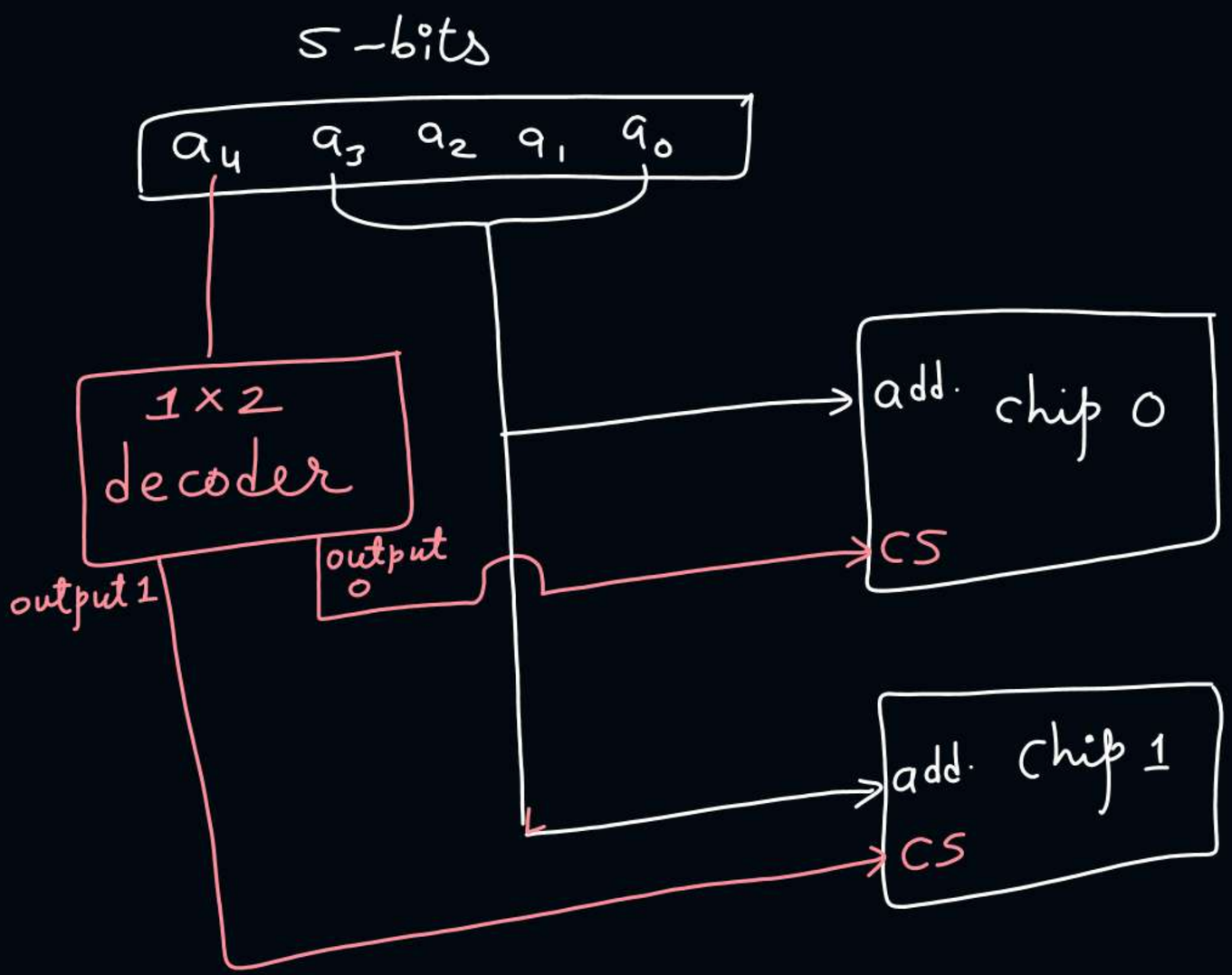
16×8 bits $\Rightarrow$ 4-bits

16×8 -bits $\Rightarrow$ 4-bits

32×8 bits $\Rightarrow$ 5-bits

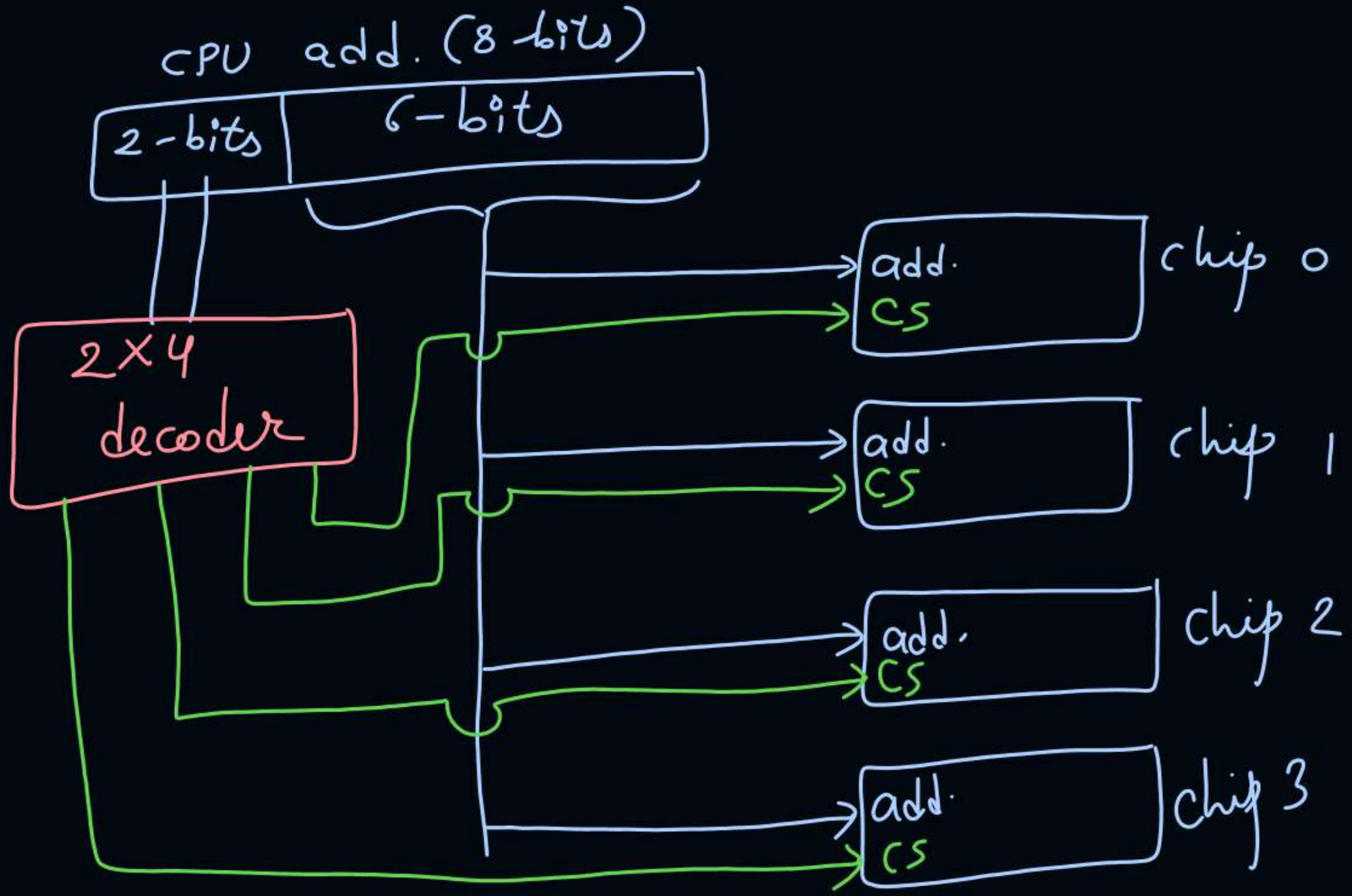
CPU generates 5-bits add.

$(0)_{10}$	0 0 0 0 0
$(15)_{10}$	0 1 1 1 1
$(16)_{10}$	1 0 0 0 0
$(31)_0$	1 1 1 1 1



vertical arrangement of chips

ex:- 4 chips of size 64 x 8 bits ⇒ 64 bytes | Total capacity = 4 * 64B = 256B



[NAT]

#Q. (a) How many 128×8 bits RAM chips are needed to provide a memory capacity of 2048 bytes? ⇒ 16

(b) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? 11, 7

(c) How many lines must be decoded for chip select? Specify the size of decoder? 4, 4×16

(a) no. of chips $= \frac{2048 \text{ bytes}}{128 \times 8 \text{ bits}} = \frac{2^{11}}{2^{7}} = 2^{4} = 16$

(b) mem. = 2048 bytes $= 2^{11}$ bytes ⇒ add. = 11 bits

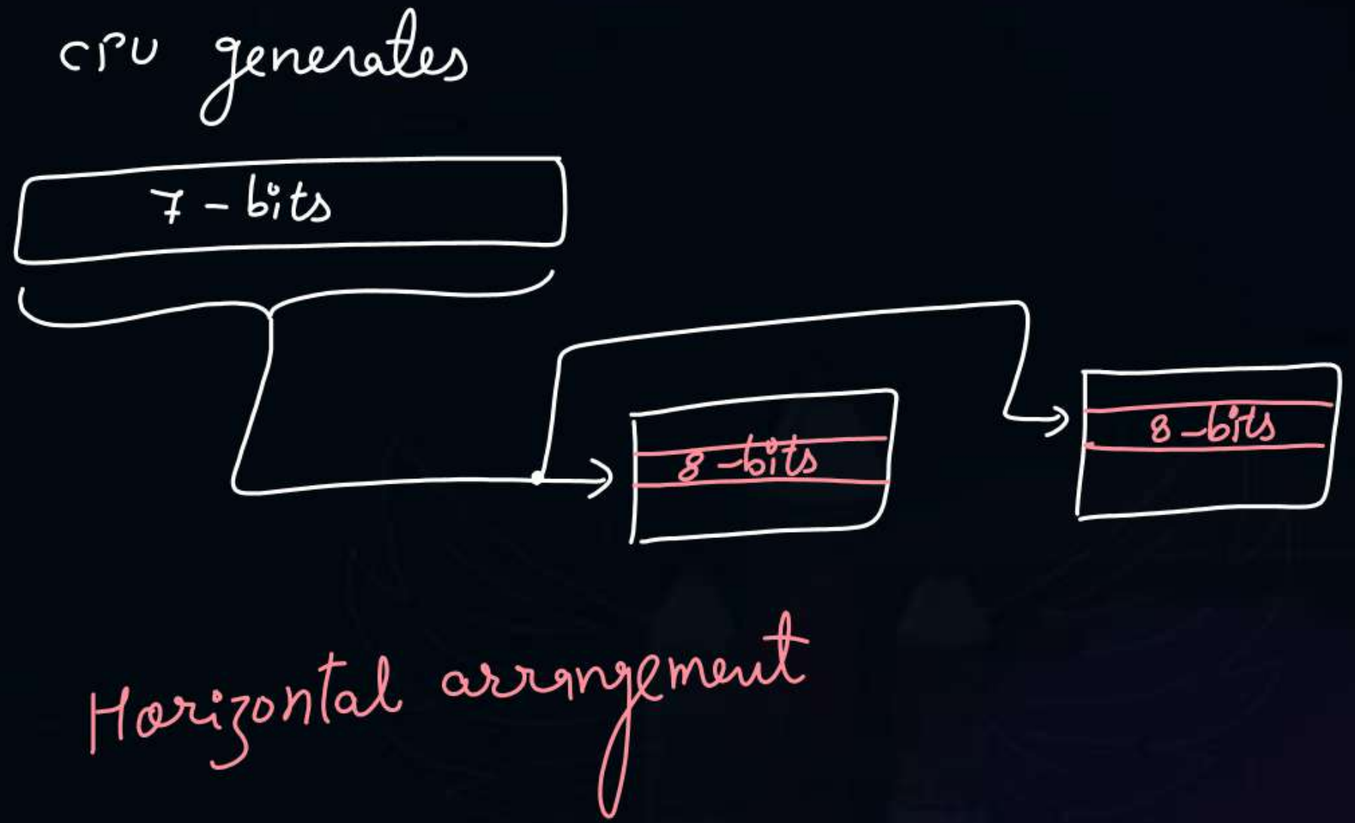
Common ⇒ 7 bits for 128×8 bits chips

[NAT]

#Q. How many 128×8 bits RAM chips are needed to provide a memory capacity of 128 ×16 bits?

$$= \frac{\cancel{128} \times \overset{2}{\cancel{16}} \text{ bits}}{\cancel{128} \times \cancel{8} \text{ bits}}$$

$$= 2$$



Topic : Solution

Horizontal arrangement ⇒ when data per address required more

Vertical —11— ⇒ when no. of address required more

[NAT]

#Q. How many 128×8 bits RAM chips are needed to provide a memory capacity of 256×16 bits?

$$= \frac{256 \times 16}{128 \times 8}$$

$$= 4 \text{ chips}$$

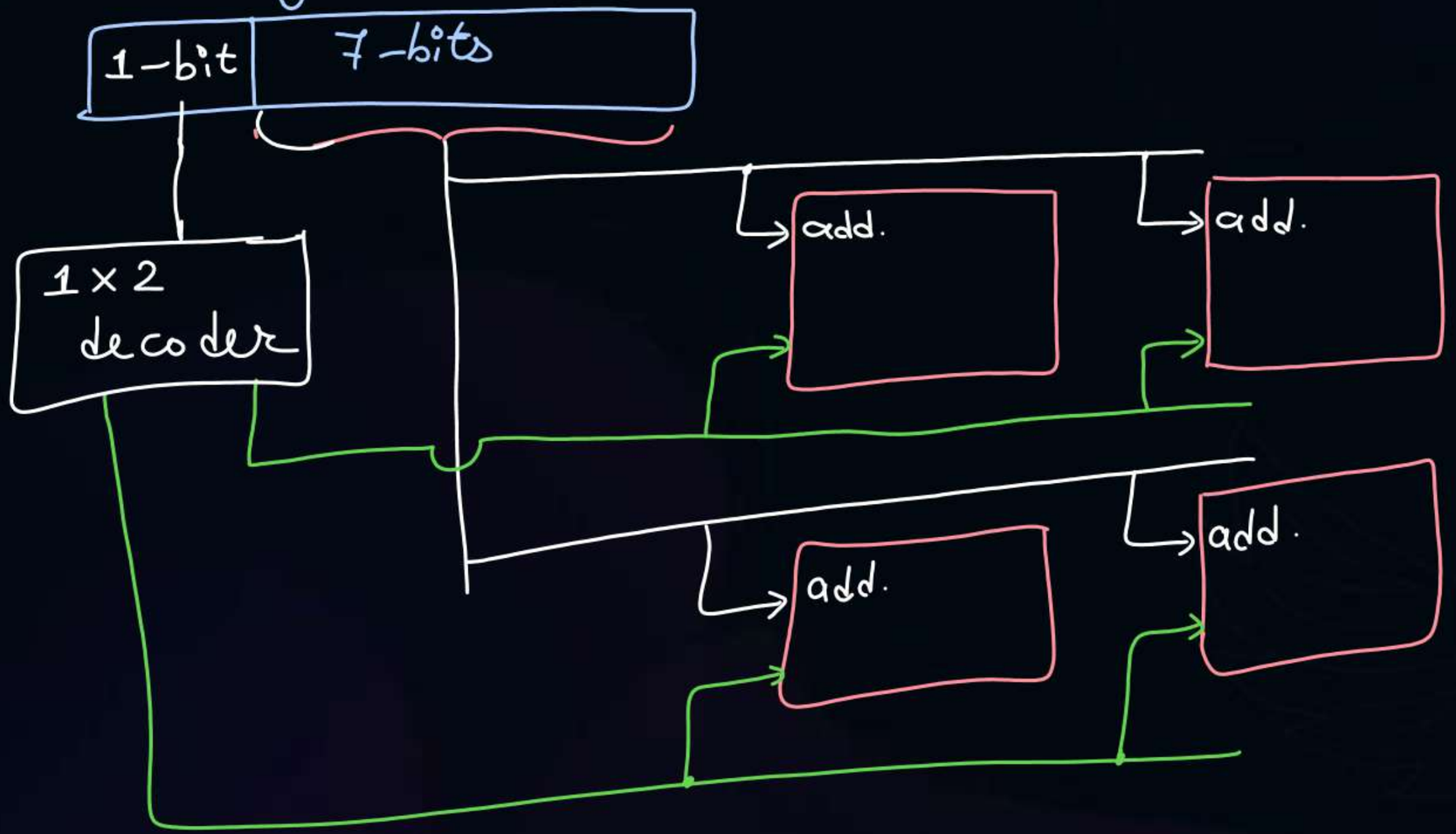
for 256 × 16 bits ⇒ CPU generates add = 8 bits

for 128 × 8 bits ⇒ chip can understand add. = 7 bits

Topic : Solution

Hybrid arrangement

CPU generates 8-bits add.



[MCQ] GATE – 2009

#Q. How many 32K × 1 RAM chips are needed to provide a memory capacity of 256K bytes?

A. 8

B. 32

C. ✓ 64

D. 128

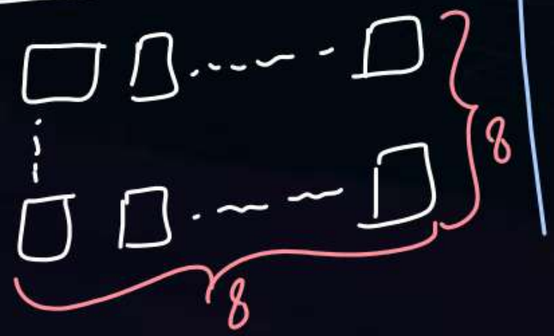
$$= \frac{256\text{K bytes}}{32\text{K} \times 1 \text{ bits}}$$

$$= \frac{^{8}\cancel{256}\text{K} \times \cancel{8}^{8} \text{ bits}}{\cancel{32}\text{K} \times \cancel{1} \text{ bits}}$$

$$= 64$$

default storage unit ⇒ bits

arrangement ⇒



#Q. Consider a 4 bytes wide mem. with capacity = 8GB.

Mem. add. length = 31 bits ?

Soln on each add. expected data = 4 bytes

$$\text{no. of addresses needed} = \frac{8GB}{4B} = 2G \Rightarrow 2^{31} \Rightarrow \text{add.} = 31 \text{ bits}$$

$$\text{Expected memory} = 2G \times 4 \text{ bytes}$$

#q. Consider a 32-bits wide memory with total capacity of 16 GB, is built using 256M x 8 bits RAM chips. How many chips are needed and how the chips are arranged?

Soln

word size = 32 bits = 4B

no. of addresses = $\frac{16\,GB}{4B} = 4G$

expected mem. = 4G x 32 bits

no. of chips = $\frac{4G \times 32 \text{ bits}}{256M \times 8 \text{ bits}}$

$= \frac{2^{32} \times 32}{2^{28} \times 8}$

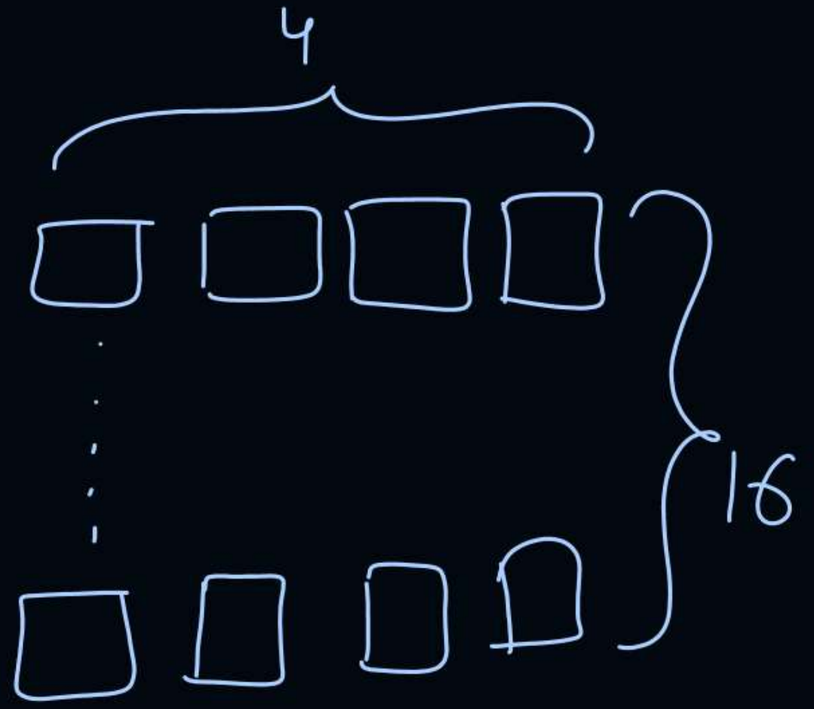
$= 2^4 \times 4$

$= 64$ chips

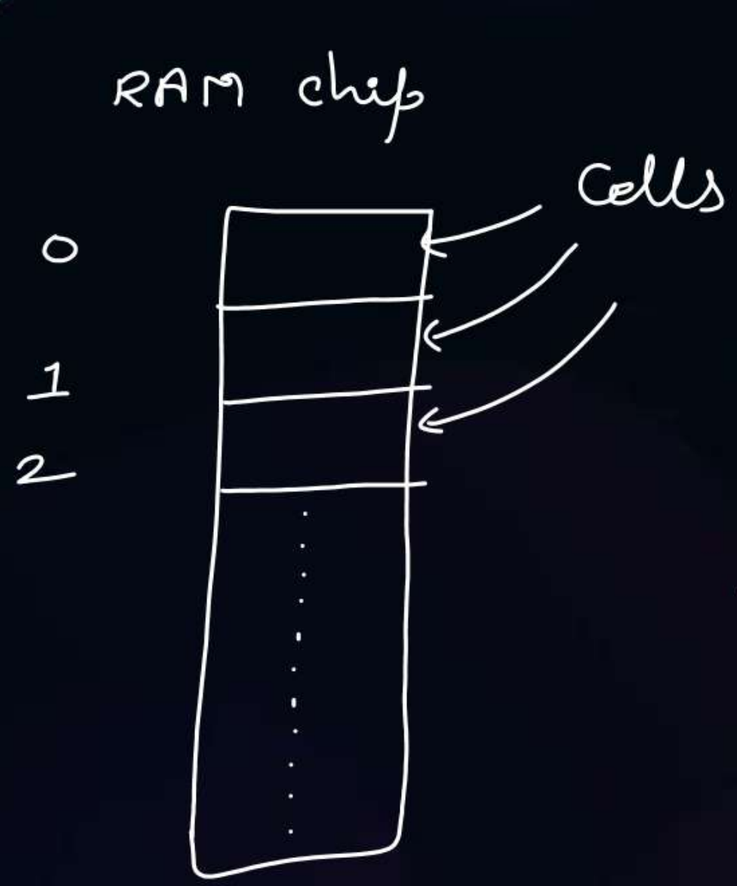
Ans:-

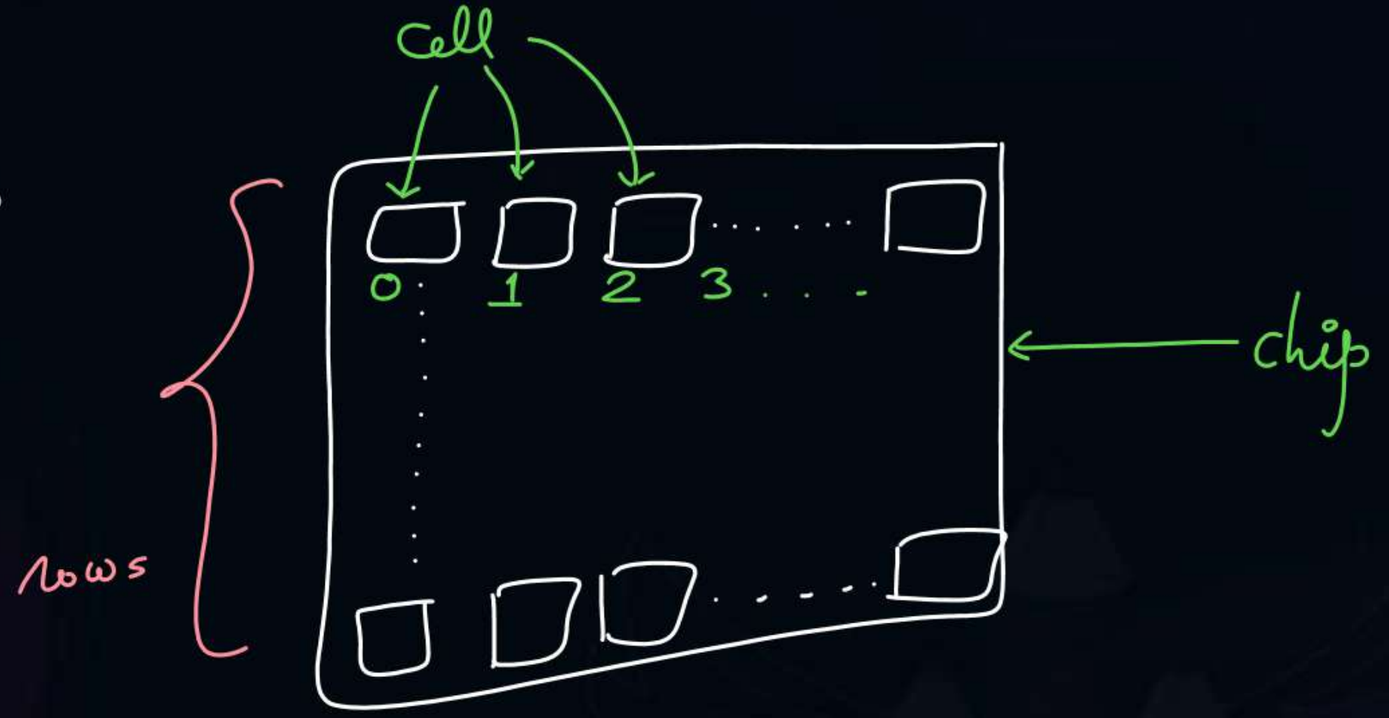
no. of chips = 64

arrangement ⇒ 16 × 4



Topic : DRAM Refresh

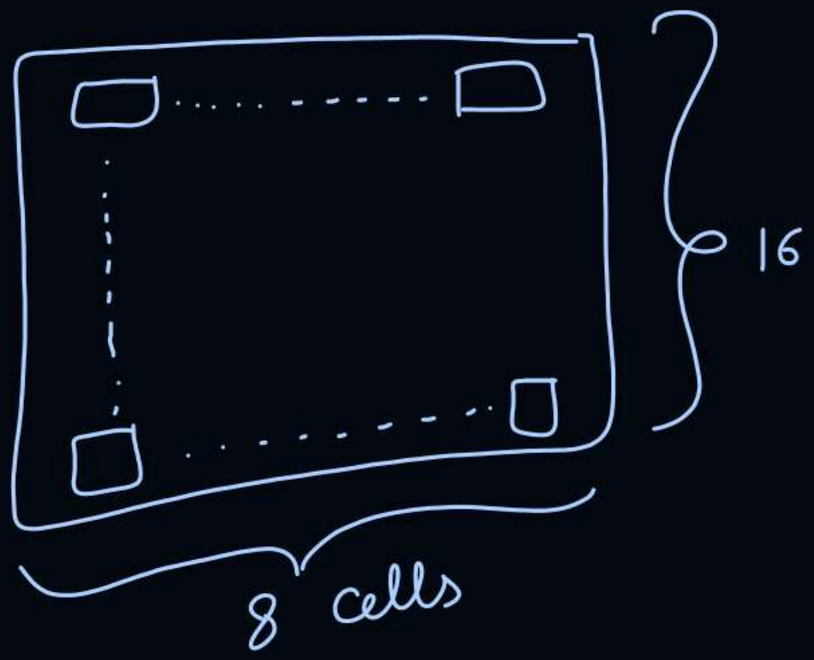




ex:-

chip (DRAM) $\Rightarrow$ 128 × 8 -bits

assume



16 rows of cells with
8 cells in each row

In one time, one row of cells can be refreshed.

1 chip refresh time = no. of rows of cells * 1 refresh time

n chips (of a memory system)
refresh time = 1 chip refresh time

Ques) Assume a mem. system which is built using 16 chips of size 128k x 16 bits. each chip has 512 rows of cells. one refresh operation takes 2 nsec, then entire mem. system refresh time = ?

Soln

1 chip refresh time = 512 * 2 nsec

= 1024 nsec ≅ 1 usec

[MCQ] GATE- 2009 PYQ

#Q. A main memory unit with a capacity of 4 megabytes is built using 1M × 1-bit DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is?

A 100 nanoseconds

B ✓ 100×2^{10} nanoseconds

C 100×2^{20} nanoseconds

D 3200×2^{20} nanoseconds

1 chip refresh time = 1k * 100 nsec

(n chip)

H.W.

no. of chip = ?

chips arrangement = ?

} from prev. Quest^{n}

2 mins Summary

Topic RAM Chip

Topic ROM Chip

Topic Multiple Chips in Single Memory System

Topic DRAM Refresh

Happy Learning

THANK - YOU