CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Instruction & Addressing Modes

Lecture No.- 01

By- Vishvadeep Gothi sir

Recap of Previous Lecture

Topic Micro Operation

Topic Memory Access

floor funct^n $\Rightarrow \lfloor 3.9 \rfloor = 3$

ceil " $\Rightarrow \lceil 3.2 \rceil = 4$

Topics to be Covered

Topic Instruction

Topic ISA

Topic Types of Instruction

[MCQ]

#Q. Consider the following program segment. Here R1, R2 and R3 are the general-purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1, (3000)	R1 ← M[3000]	2
LOOP:	MOV R2, (R3)	R2 ← M[R3]	1
	ADD R2,R1	R2 ← R1 + R2	1
	MOV (R3),R2	M [R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 – 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory reference for accessing the data in executing the program completely is

A 10

B 11

C 20

D 21

Solution

	Operation
LOOP:	R1 ← M[3000]
	R2 ← M[R3]
	R2 ← R1 + R2
	M [R3] ← R2
	R3 ← R3 + 1
	R1 ← R1 – 1
	Branch on not zero
	Stop

R1 = ~~10~~ ~~9~~ 8 0

R2 = ~~100~~ ~~110~~ ~~100~~ 109

R3 = ~~2000~~ ~~2001~~ 2002

Loop runs 10 times

Total memory references for data = 1 + 2*10

= 21

Memory

1000	Program
2000	~~100~~ 110
2001	~~100~~ 109
2002	~~100~~ 108
2003	~~100~~ 107
2004	~~100~~ 106
2005	~~100~~ 105
2006	~~100~~ 104
2007	~~100~~ 103
2008	~~100~~ 102
2009	~~100~~ 101
2010	100
3000	10

[MCQ]

#Q. Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1, (3000	R1 ← M[3000]	2
LOOP:	MOV R2, (R3)	R2 ← M[R3]	1
	ADD R2,R1	R2 ← R1 + R2	1
	MOV (R3),R2	M [R3] ← R2	1
	INC R3	R3 ← R3 + 1	1
	DEC R1	R1 ← R1 – 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:

A 100

B 101

C 102

D 110

[MCQ]

#Q. Consider the following program segment. Here R1, R2 and R3 are the addresses general-purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
1000	MOV R1, (3000)	R1 ← M[3000]	2
1008 LOOP:	MOV R2, (R3)	R2 ← M[R3]	1
1012	ADD R2,R1	R2 ← R2 + R1	1
1016	MOV (R3),R2	M [R3] ← R2	1
1020	INC R3	R3 ← R3 + 1	1
1024	DEC R1	R1 ← R1 – 1	1
1028	BNZ LOOP	Branch on not zero	2
1036	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction "INC R3", what return address will be pushed on the stack?

A 1005

B 1020

C 1024

D 1040

[NAT]

GATE - 2021

#Q. Consider the following instruction sequence where registers R1, R2 and R3 are general purpose and MEMORY [X] denotes the content at the memory location X.

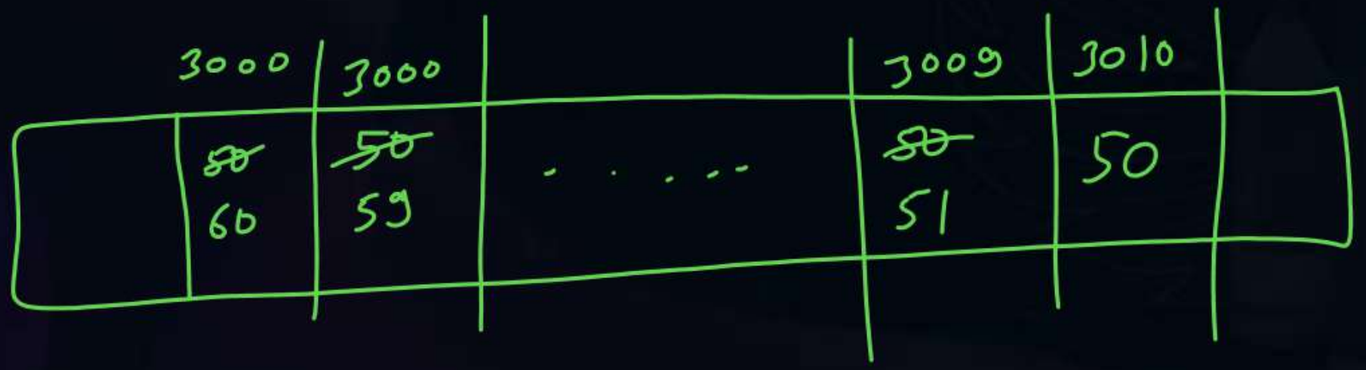
Instruction	Semantics	Instruction Size (bytes)
MOV R1, (5000)	R1 ← MEMORY[5000]	4
MOV R2, (R3)	R2 ← MEMORY[R3]	4
ADD R2, R1	R2 ← R1 + R2	2
MOV (R3), R2	MEMORY[R3] ← R2	4
INC R3	R3 ← R3 + 1	2
DEC R1	R1 ← R1 – 1	2
BNZ 1004	Branch if not zero to the given absolute address	2
HALT	Stop	1

1000

1004

Assume that the content of the memory location 5000 is 10, and the content of the register R3 is 3000. The content of each of the memory locations from 3000 to 3010 is 50. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable.

After the execution of the program, the content of memory location 3010 is 50.

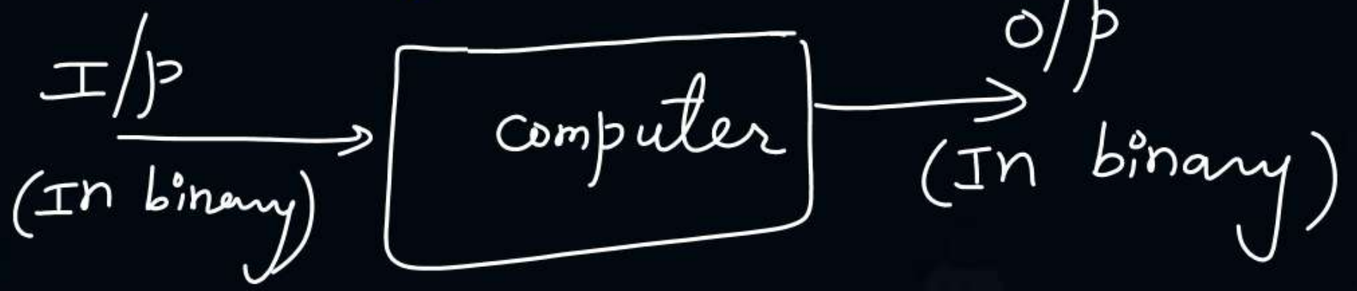


Topic : Instruction

```
#include<stdio.h>
void main()
{
int a, b, c;
printf("Enter 2 values: ");
scanf("%d %d", &a, &b);
c = a + b;
printf("Sum = %d", c);
}
```

Digital computer

(Instructns + data)



Topic : Instruction

High level lang. program

```
#include<stdio.h>
void main()
{
int a, b, c;
printf("Enter 2 values: ");
scanf("%d %d", &a, &b);
c = a + b;
printf("Sum = %d", c);
}
```

programming statements

Language Translation

(compiler)

Instructions

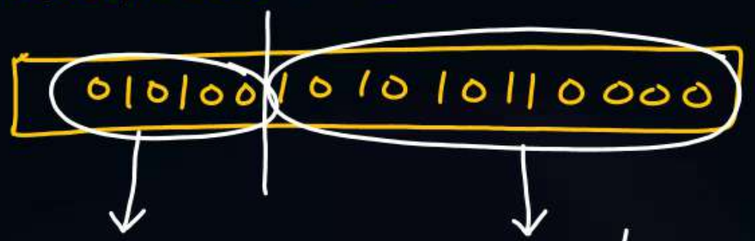
Low-level lang. prog. or Machine code or byte code or binary code or object code

```
10111000
10000001
11110010
01010101
11110110
01010101
10001111
10100011
00111101
```

Topic : Instruction

A group of bits which instructs computer to perform some operation

Assume instⁿ



denotes operation ⇓ operation code

denotes operands information

Instⁿ

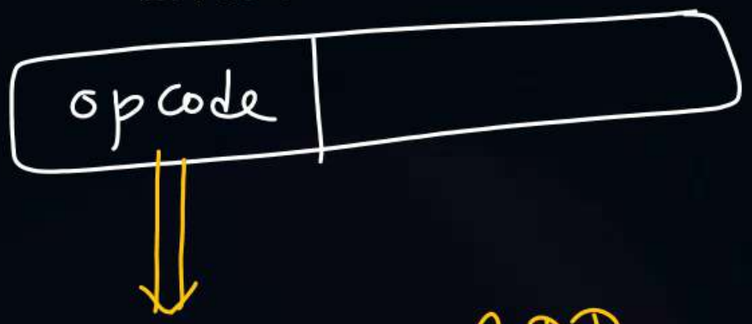
Topic : Instruction

Assume a CPU can perform 8 different operations ⇒ A CPU supports 8-distinct types of instructions

⇓

opcode of inst^n ⇒ 3-bits

Inst^n



000 — ADD

001 — SUB

010 — mem. to Reg.

011 — Reg. to mem.

⋮ ⋮

111 — complement

Topic : Instruction

ex:-

distinct no. of instns supported	opcode size
8	3 bits
16	4 bits
32	5 bits
24	5 bits
x	$\lceil \log_2 x \rceil$

Topic : ISA (Instruct set Architecture)

Collection of all inst^ns supported by a CPU.

Size of ISA ⇒ no. of inst^ns supported by a CPU

or

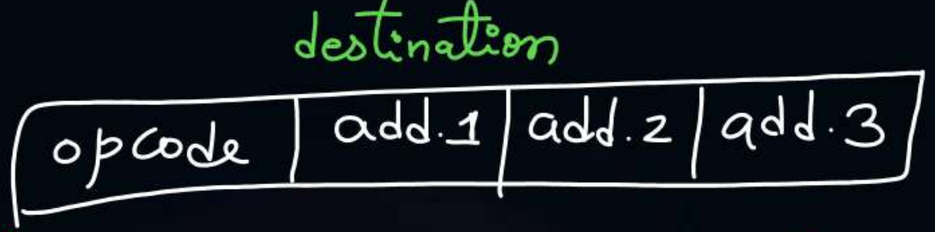
Size of inst^n set

Topic : Types of Instruction

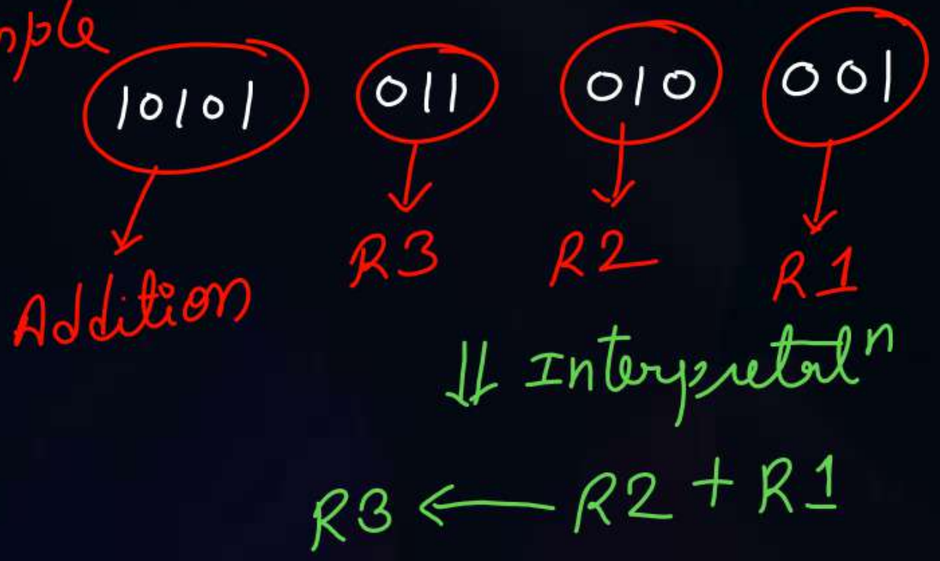
- 3-Address Instruction:
- 2-Address Instruction:
- 1-Address Instruction:
- 0-Address Instruction:

Topic : 3-Address Instruction

Max 3 addresses can be specified within an instruction for operands



example



// Interpretation

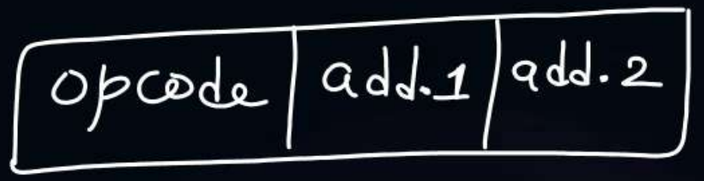
R3 ⟵ R2 + R1

one operand ⇒ destination

2 operands ⇒ source

Topic : 2-Address Instruction

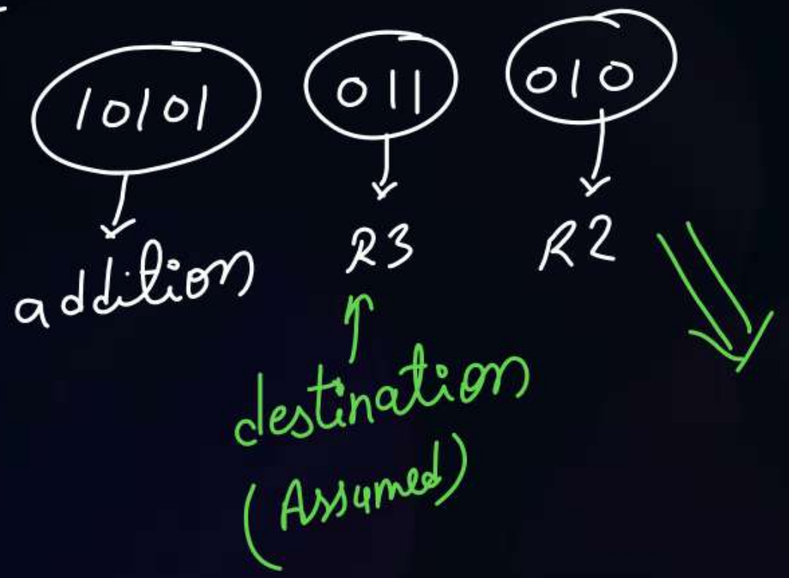
Max 2 addresses can be specified within an instruction



one operand ⇒ only source

" " ⇒ source, destination both

ex:-



$R3 \leftarrow R3 + R2$

Topic : 1-Address Instruction

Max 1 address can be specified within an instruction

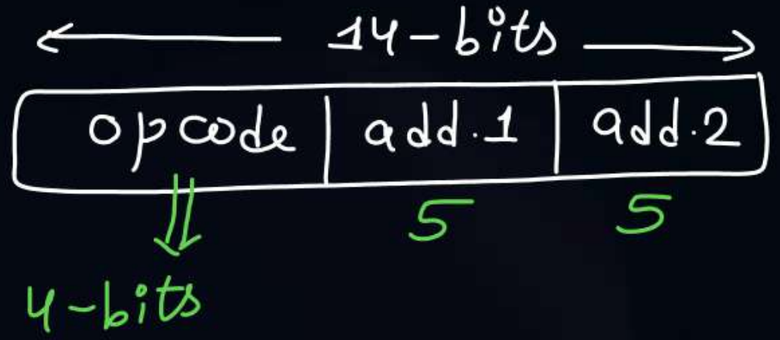
Topic : 0-Address Instruction

No any address can be specified within an instruction

[NAT]

#Q. Consider a digital computer which supports only 2-address instructions each with 14-bits. If address length is 5-bits then maximum and minimum how many instructions the system can support?

Soln



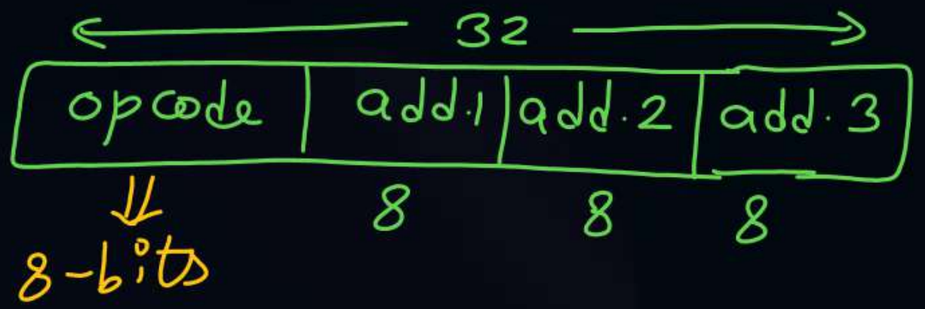
$max = 2^4 = 16$

$min = 1$

[NAT]

#Q. Consider a digital computer which supports only 3-address instructions each with 32-bits. If address length is 8-bits then maximum and minimum how many instructions the system can support?

Soln



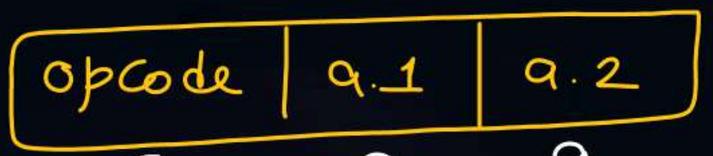
$max = 2^8 = 256$

$min = 1$

[NAT]

#Q. Consider a digital computer which supports 64 2-address instructions. If address length is 9-bits then the length of the instruction is _____ bits?

Soln



6+9+9 = 24 bits

no. of instns supported = 64 ⇒ opcode = 6 - bits

[NAT]

#Q. Consider a digital computer which supports 64 2-address instructions. If address length is 9-bits then the length of the instruction is _____ bits?

In above question: Each instruction must be stored in memory in a byte-aligned fashion. If a program has 200 instructions, then amount of memory required to store the program text is _____ bytes?

[NAT]

#Q. Consider a digital computer which supports 32 2-address instructions. Consider the address length is 8-bits. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 300 instructions, then amount of memory required to store the program text is _____ bytes?

[NAT]

#Q. A processor has 50 distinct instructions and 16 general purpose registers. Each instruction in system has one opcode field, 2 register operand field and a 10 bits memory address field. The length of the instruction is ____ bits?

[NAT]

#Q. A processor has 20 distinct instructions and 32 general purpose registers. A 24- bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____?

[NAT]

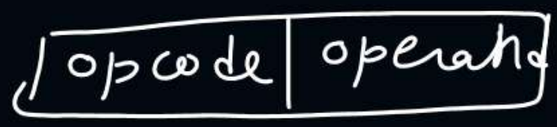
#Q. A processor has 20 distinct instructions and 32 general purpose registers. A 24- bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____?

In above question: Assume that immediate operand field is an unsigned number, What is its maximum and minimum value possible?

2 mins Summary

Topic Micro-operations

Topic Instructions



Topic Instruction Set Architecture

Topic Types of Instructions

Topic Opcode

Happy Learning

THANK - YOU