CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Cache Organization

Lecture No.- 03

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Recap of Previous Lecture

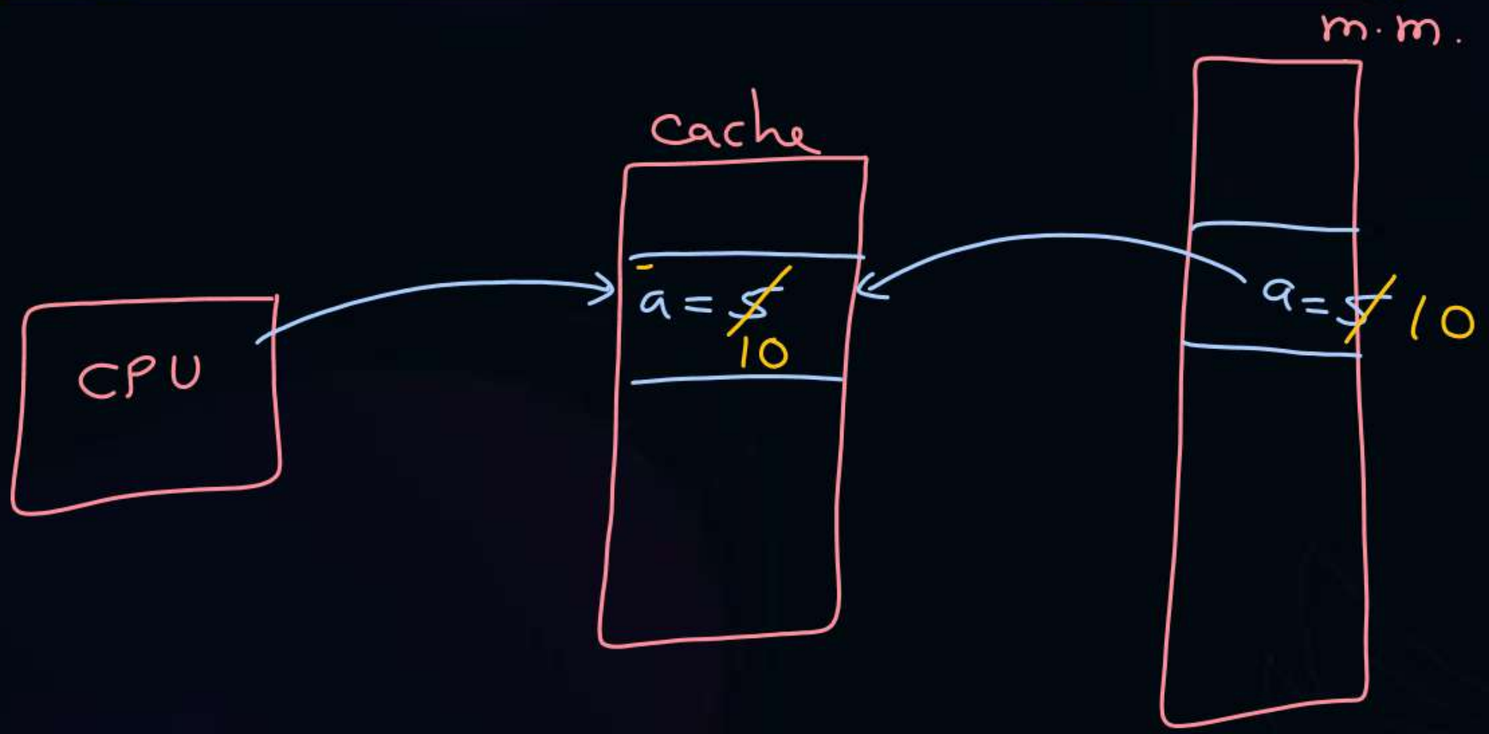
Topic Cache Memory

Topic Average Memory Access Time

Topics to be Covered

- Topic: Cache Write
- Topic: Write Through & Write Back
- Topic: Write Allocate
- Topic: Cache Mapping

Topic : Cache Write or Write Propagation



Topic : Cache Write or Write Propagation

1. Write Through
2. Write Back

Topic : Write Through

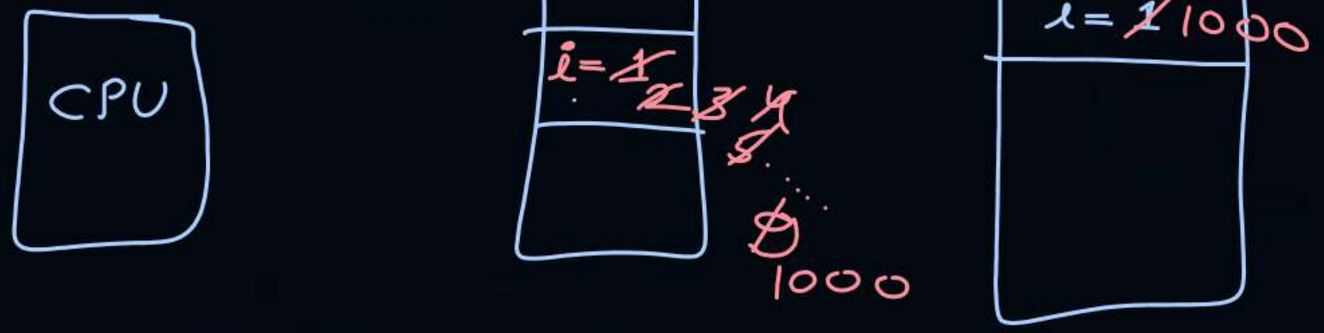
Advantage ☺ :- No any inconsistency of content b/w Cache & mm.

Disadv. ☹ :- Time consuming

↳ because write operatn is performed always in mm irrespective of hit or miss in cache.

If any block is replaced from cache at any point of time, then it is not written back in mm.

Topic : Write Back



for (i=1; i<=1000; i++)

Adv. :- Time saving as compared to write through

Disadv. :- Inconsistency of content b/w mm. & cache.

If any block is replaced from cache.

(dirty block / modified block)

CPU performed write in that block

⇓

perform write back for the block.

CPU did not perform write in that block ever

⇓

directly replace the block without write back

Topic : Write Allocate vs No Write Allocate

used with write back

Write Allocate:

from mm to cache

The block is loaded on a write miss.

No Write Allocate: → used with write through

The block is modified in the main memory and not loaded into the cache.

write through cache with no write allocate

Read

Hit

CPU reads required content from cache

Miss

CPU reads required content from mm.

CPU brings missed block from mm to cache by replacing a block in cache if needed.

(replaced block is overwritten)

write

Hit

Perform write in cache & main memory simultaneously

Miss

Perform write in mm & do not bring missed block from mm to cache

write back with write allocation

Read

Hit

CPU reads req. content from cache

Miss

CPU reads req. content from mm. CPU brings missed block from mm to cache.

If loading of block replaces a block from cache then write back if replaced block is dirty.

write

Hit

CPU performs write in cache

Miss

bring missed block from mm to cache, then perform the write operation in cache.

If loading of block replaces a block from cache then write back if replaced block is dirty.

Topic : T_{avg} in Write Through Cache

Sim. accessed cache

$$T_{read\ avg} = H * t_{cm} + (1-H)t_{mm}$$

$$T_{write\ avg} = Max(t_{cm}, t_{mm}) = t_{mm}$$

T_{avg} = % of read operations * $t_{avg\ read}$ + % of write operations * $t_{avg\ write}$

Effective hit rate = % of read * read hit rate

[MCQ]

$t_{cm} = 100ns$ $t_{mm} = 1000ns$

$H = 90\%$

#Q. A system has a write through cache with access time of 100ns and hit ratio of 90%. The main memory access time is 1000ns. The 70% of memory references are for read operations.

A 1) Average memory access time for read operations only

B 2) Average memory access time for write operations only

C 3) Average memory access time for read-write operations both

D 4) Effective Hit ratio

1.) $T_{avg\ read} = 0.9 * 100 + 0.1 * 1000 = 190\ ns$

2) $T_{avg\ write} = t_{mm} = 1000\ ns$

3) $T_{avg} = 0.7 * 190 + 0.3 * 1000$
$= 433\ nsec$

4) Eff. hit rate $= 0.7 * 0.9 = 0.63$

Topic : T_{avg} in Write Back Cache

assume ⇒ x = fraction of dirty blocks replaced

Sim. :-

$$T_{avg} = H * t_{cm} + (1-H)(t_{bt} + \text{write back time})$$

Hier.

$$T_{avg} = H * t_{cm} + (1-H)(t_{cm} + t_{bt} + \text{write back time})$$

write back time = x * block transfer time from cache to mem.

#Q. $t_{cm} = 10\,ns$

$H = 80\%$

% of dirty blocks to be replaced = 2 %

block transfer time b/w cache & mem. = 200 ns

write back policy (Hierarchical access)

$T_{avg} = ?$

Ans:-

Sol^n

$$T_{avg} = 0.8 * 10 + 0.2\,(10 + 200 + 0.02 * 200)$$

$$= 8 + 42.8$$

$$= 50.8\ ns$$

[NAT]

H.W.

#Q. The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations; 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is?

[NAT]

H.W.

#Q. Size of data sent to main memory from CPU:

1. For write hit, when a write through cache is used?
2. For write miss, when a write through cache is used?
3. For write hit, when a write back cache is used?
4. For write miss, when a write back cache is used?

[MCQ]

H.W.

#Q. Size of data sent from main memory to cache:

1. For write hit, when a write through cache is used?
2. For write miss, when a write through cache is used?
3. For write hit, when a write back cache is used?
4. For write miss, when a write back cache is used?

[NAT]

#Q. The memory access time is 2 nanosecond for a read operation with a hit in cache, 10 nanoseconds for a read operation with a miss in cache, 4 nanoseconds for a write operation with a hit in cache and 15 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 memory read operations and 60 memory write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is?

	Read	write
Hit	2	4
Miss	10	15

$t_{avg\ read} = 0.9 * 2 + 0.1 * 10 = 2.8$ nsec

$t_{avg\ write} = 0.9 * 4 + 0.1 * 15 = 5.1$ nsec

Total mem. references $= 100 + 60 = 160$

% of read $= \frac{100}{160}$

% of write $= \frac{60}{160}$

$T_{avg} = \frac{100}{160} * 2.8 + \frac{60}{160} * 5.1$

$= 1.75 + 1.9125$

$= 3.6625$ nsec

2 mins Summary

Topic Cache Memory

Topic Average Memory Access Time

Topic Cache Write

Happy Learning

THANK - YOU