CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

CPU & Control Unit

Lecture No.- 03

By- Vishvadeep Gothi sir

Recap of Previous Lecture

Topic CPU

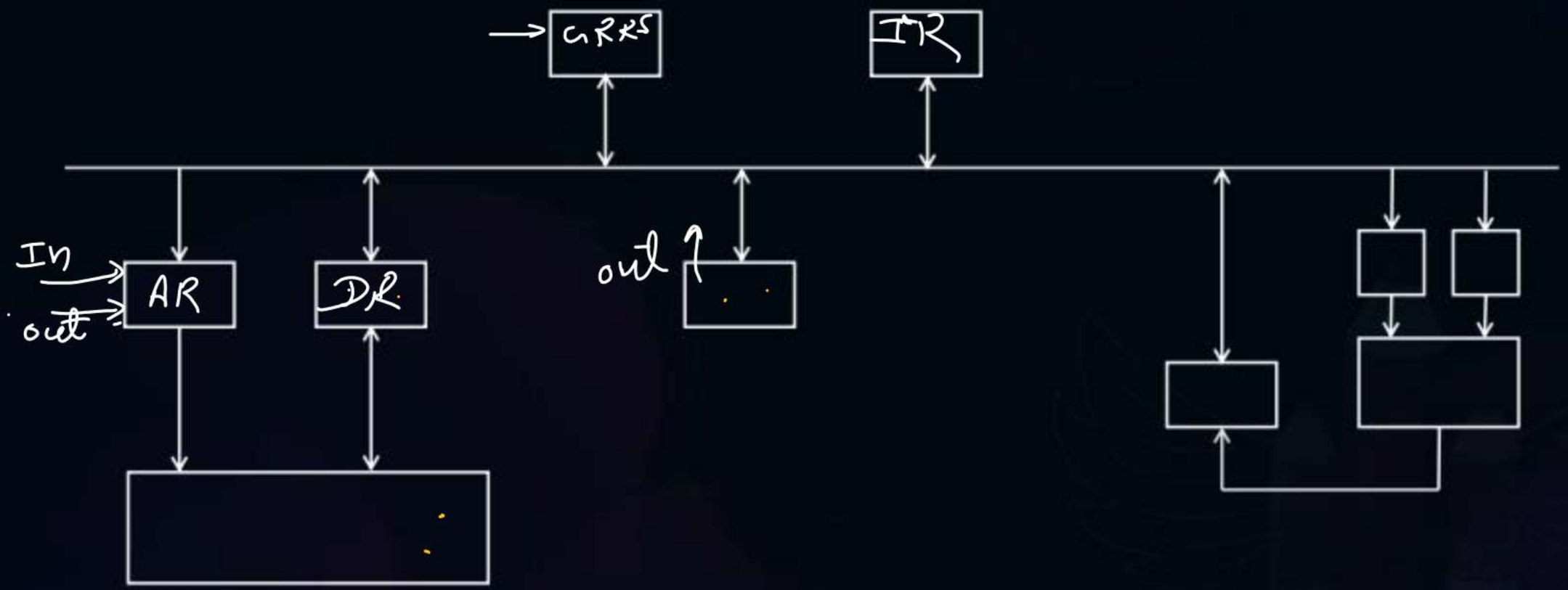
Topic MIPS

Topic Data Path

Topics to be Covered

- **Topic** Datapath
- **Topic** Control Unit Organization
- **Topic** Hardwired Control Unit
- **Topic** Micro-Programmed Control Unit
- **Topic** RISC vs CISC

Topic : Datapath



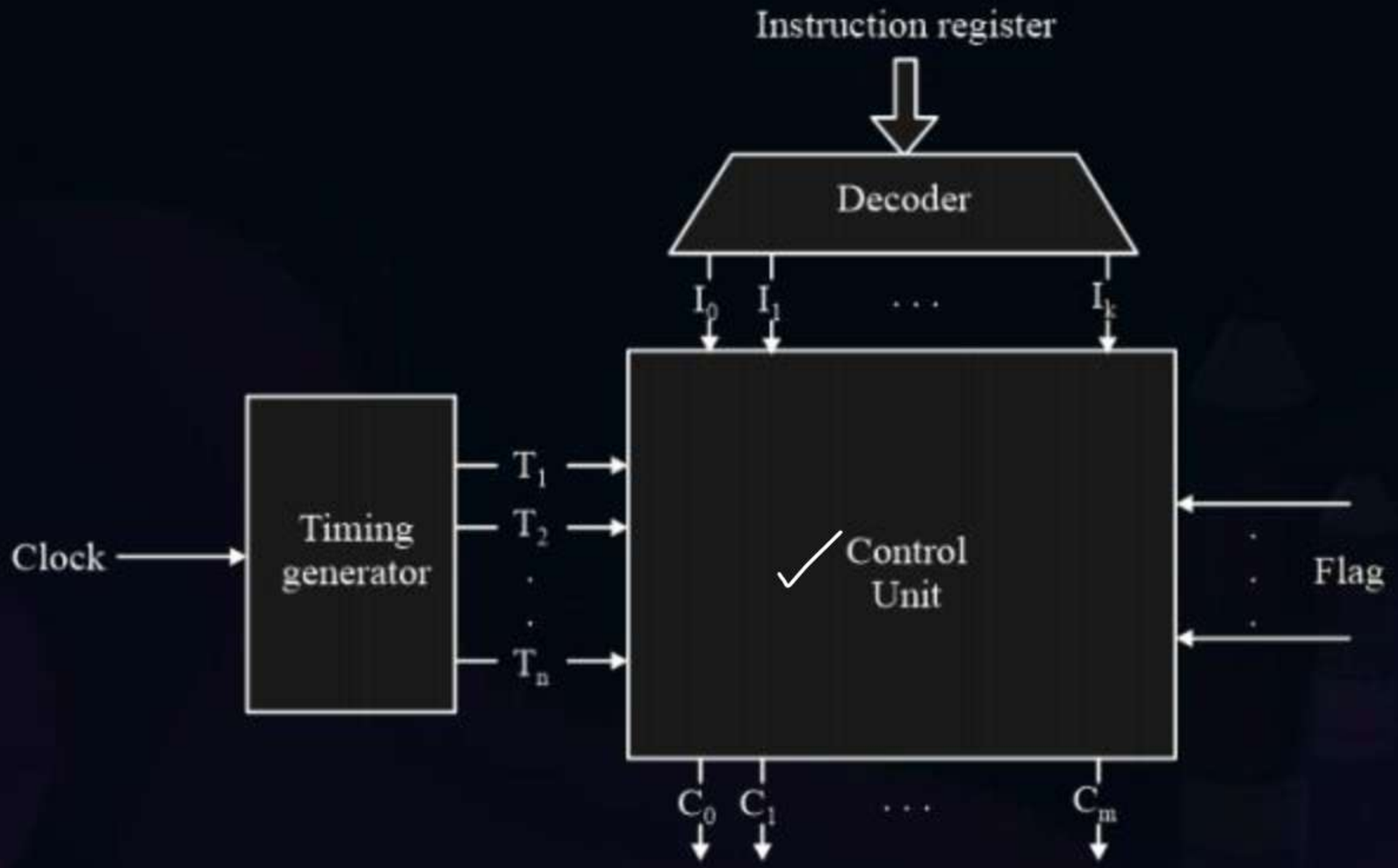
Topic : Hardwired Control Unit

Control logic is implemented with Gates, flip-flops, decoders and other digital circuits.

Advantage: Can be optimized to produce a faster mode of operation.

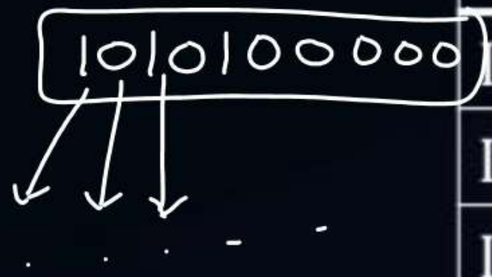
Disadvantage: Rearranging the wires among various components is difficult.

Topic : Hardwired Control Unit



[MCQ]

#Q. A hardwired CPU uses 10 control signals S1 to S10, in various time steps T1 to T5, to implement 4 instructions 11 to 14 as shown below:



	T1	T2	T3	T4	T5
I1	S1, S3, S5	S2, S4, S6	S1, S7	S10	S3, S8
I2	S1, S3, S5	S8, S9, S10	S5, S6, S7	S10	S1, S3
I3	S1, S3, S5	S7, S8, S10	S2, S6, S9	S10	S1, S3
I4	S1, S3, S5	S2, S6, S7	S5, S10	S6, S9	S10

Which of the following pairs of expressions represent the circuit for generating control signals S5 and S10 respectively?

A

$S5 = T1 + I2 \cdot T3$ and
$S10 = (I1 + I3) \cdot T4 + (I2 + I4) \cdot T5$

B

$S5 = T1 + (I2 \cdot I4) \cdot T3$ and
$S10 = (I1 + I3) \cdot T4 + (I2 + I4) \cdot T5$

C

$S5 = T1 + (I2 \cdot I4) \cdot T3$ and
$S10 = (I1 + I3 + I4) \cdot T2 + (I2 + I3) \cdot T4 + (I2 + I4) \cdot T5$

D

$S5 = T1 + (I2 \cdot I4) \cdot T3$ and
$S10 = (I2 + I3) \cdot T2 + I4 \cdot T3 + (I1 + I3) \cdot T4 + (I2 + I4) \cdot T5$

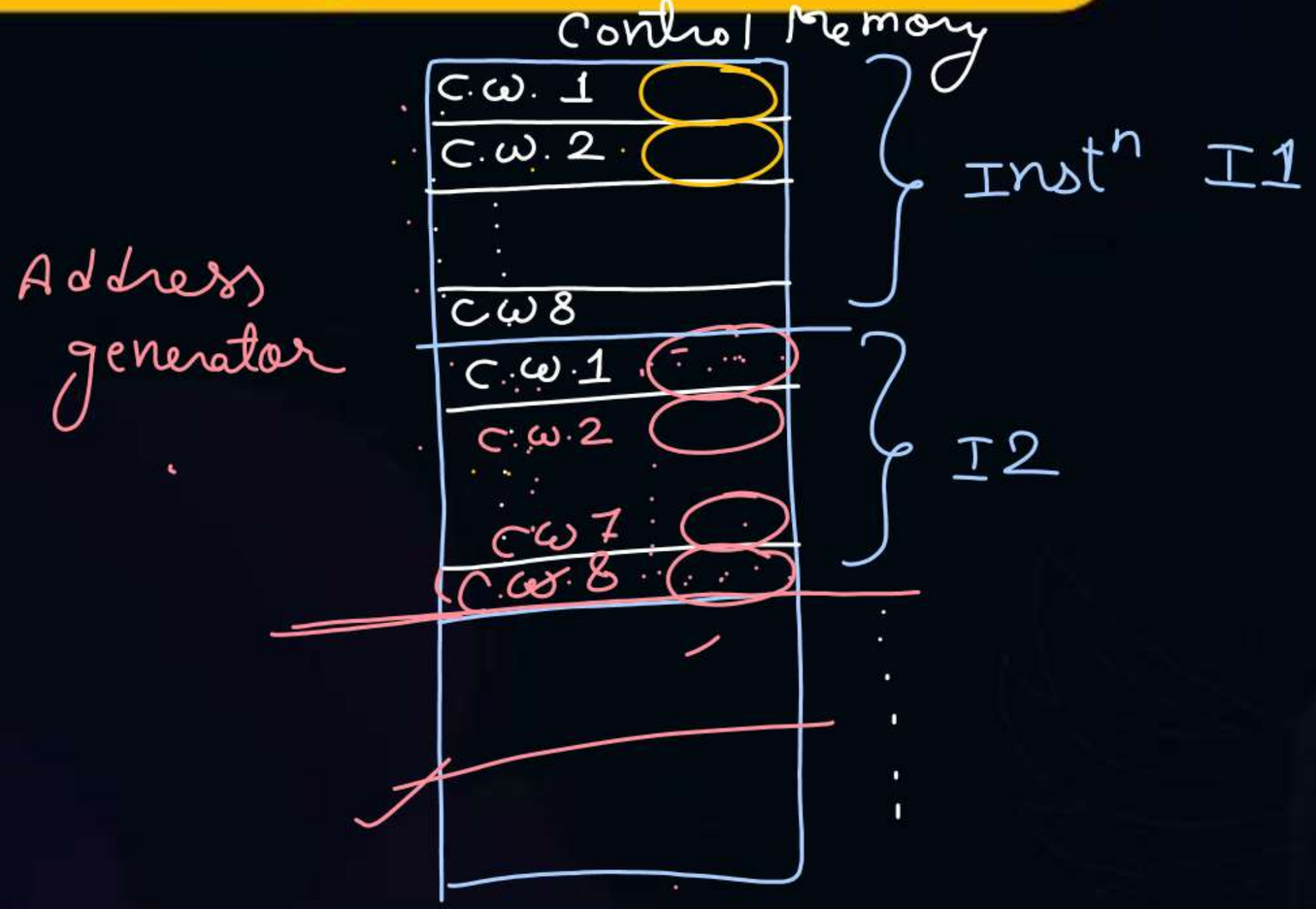
Topic : Micro-Programmed Control Unit

Control logic is implemented with micro-programs.

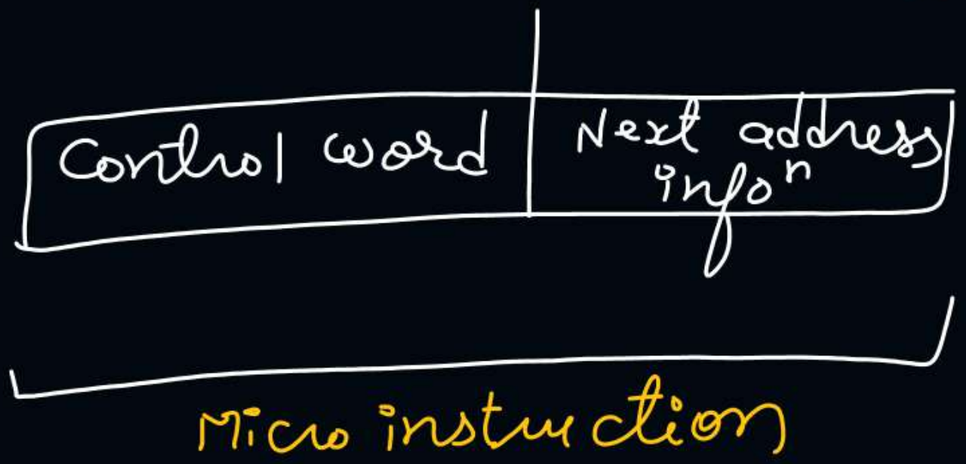
Advantage: Updating the control logic is easy.

Disadvantage: Slower than hardwired control unit.

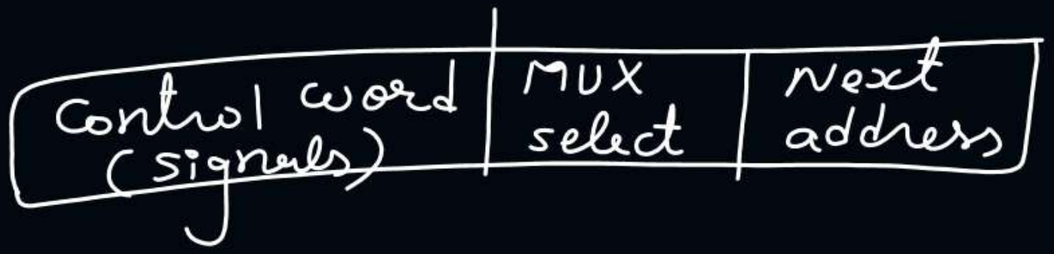
Topic : Micro-Programmed Control Unit

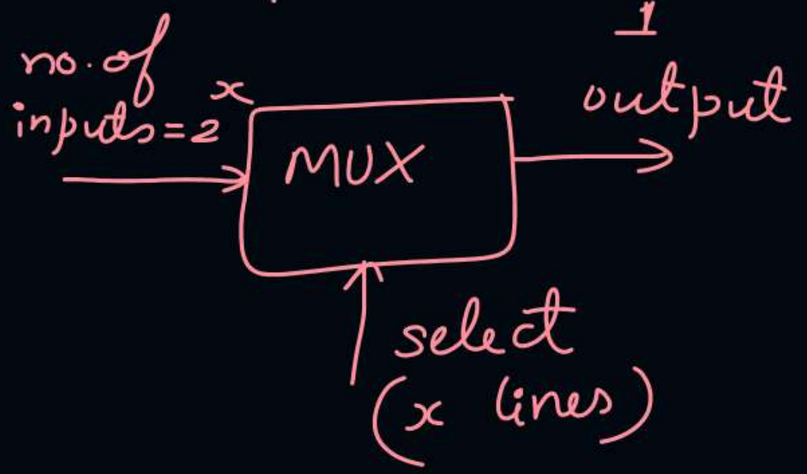


on one address in control memory the content stored

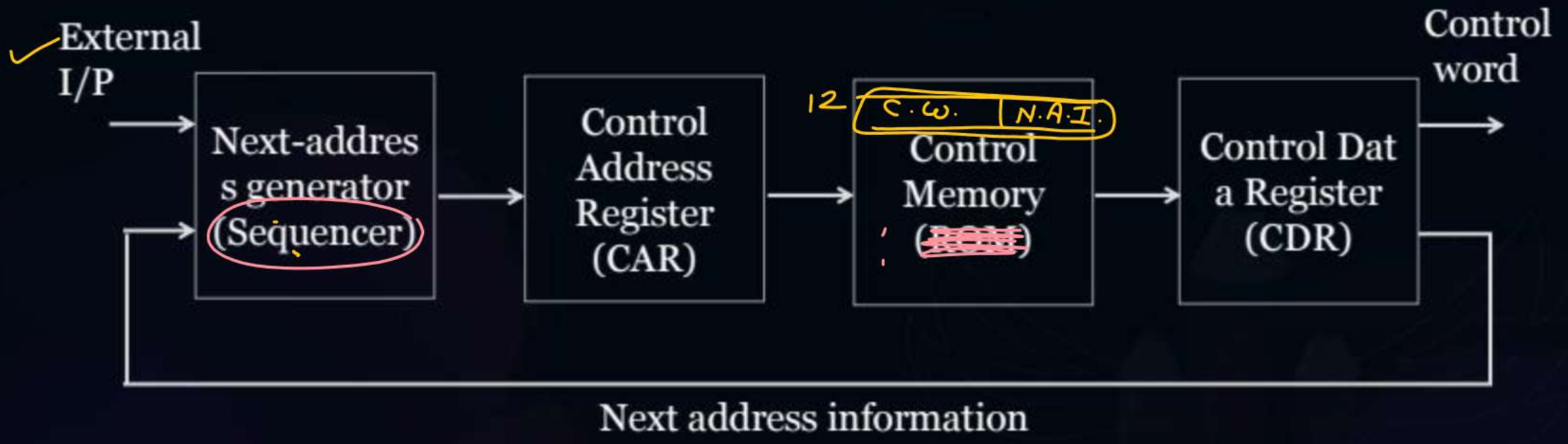


standard format of microinstⁿ





Topic : Control Word Sequencing



Topic : Control Word Sequencing

ex:-

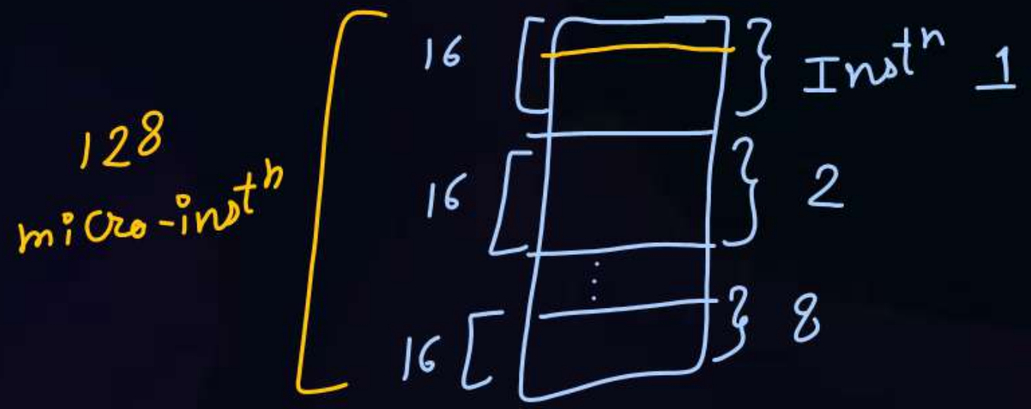
A CPU supports ⇒ 8 types of distinct inst^{ns}

To execute each inst^{n} ⇒ A sequence of 16 control words are needed

Total no. of micro-inst^{ns} stored in control memory.

⇓

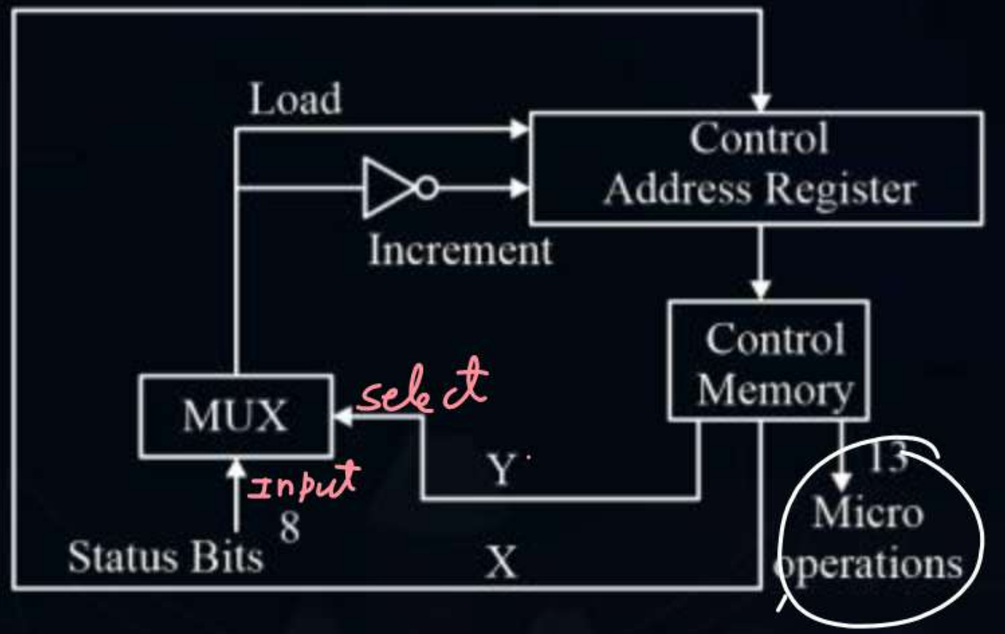
8 * 16 = 128 ⇒ 7-bit address needed



[MCQ]

#Q. The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX.

How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

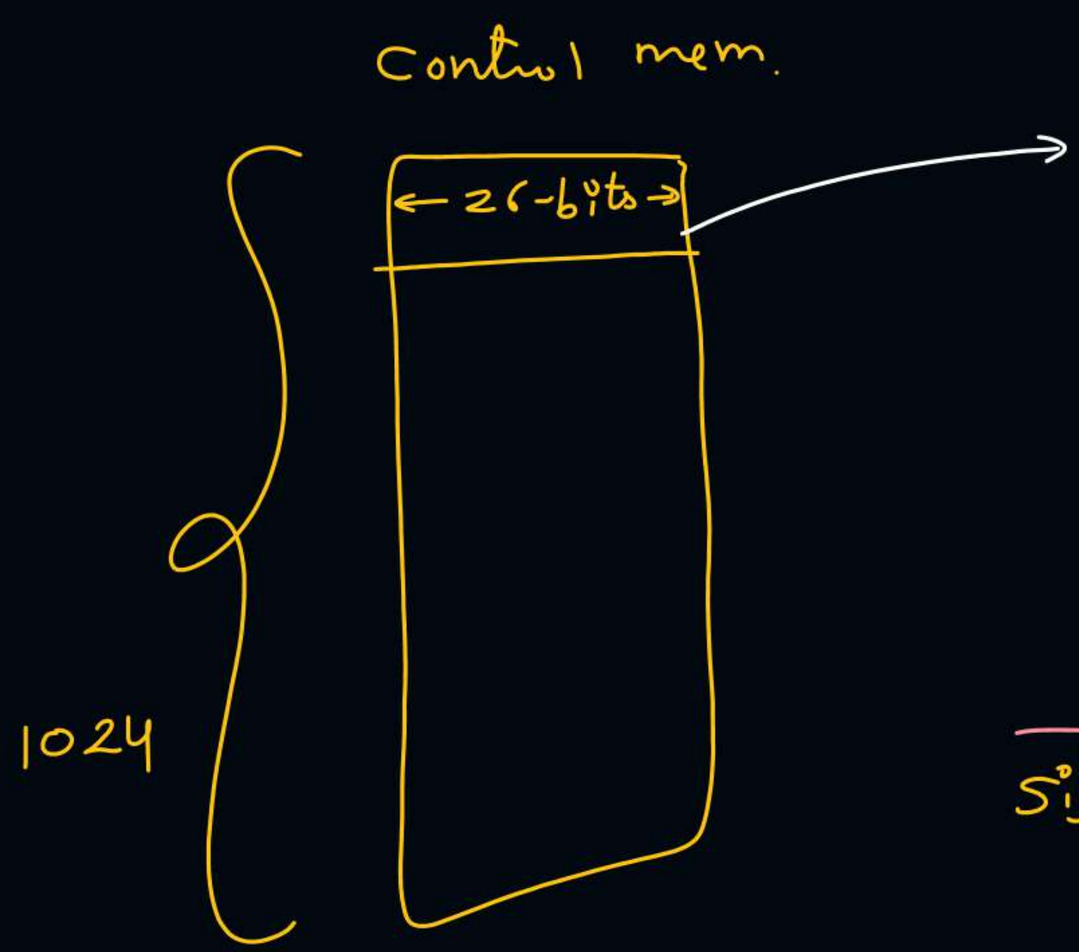


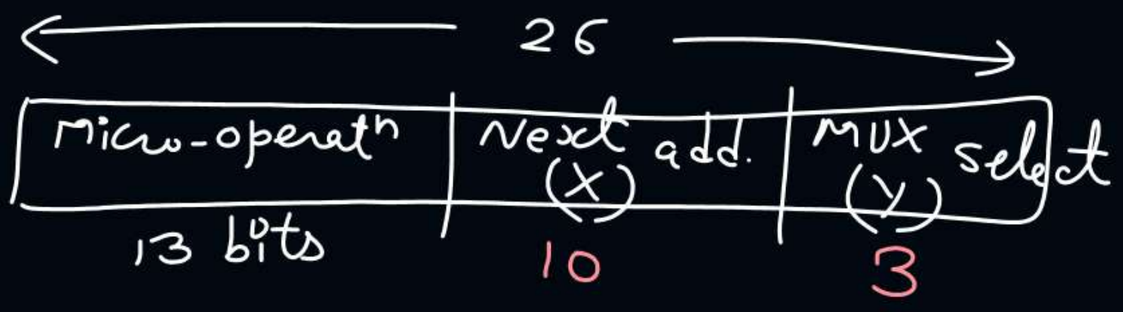
A 10, 3, 1024

B 8, 5, 256

C 5, 8, 2048

D 10, 3, 512





Total no. of micro-instns in memory = 2^{10} = 1024

Size of control memory = 1024 * 26 bits

Ques) CPU supports ⇒ 16 instns

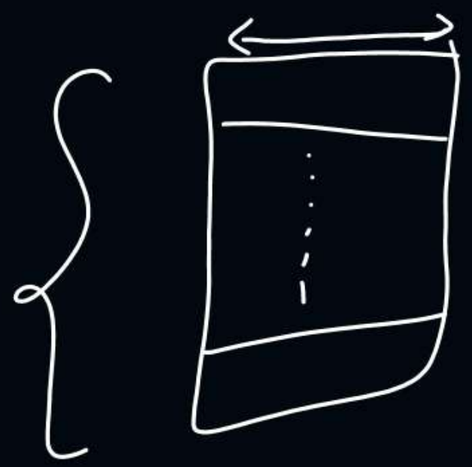
To execute each instn ⇒ A sequence of 64 micro operations needed

microinstn format ⇒

mux has 8 input lines ⇒ select = 3

control memory size = _____ k bits ?

Soln



Control mem. size = no. of microinstns * 1 micro-instn size

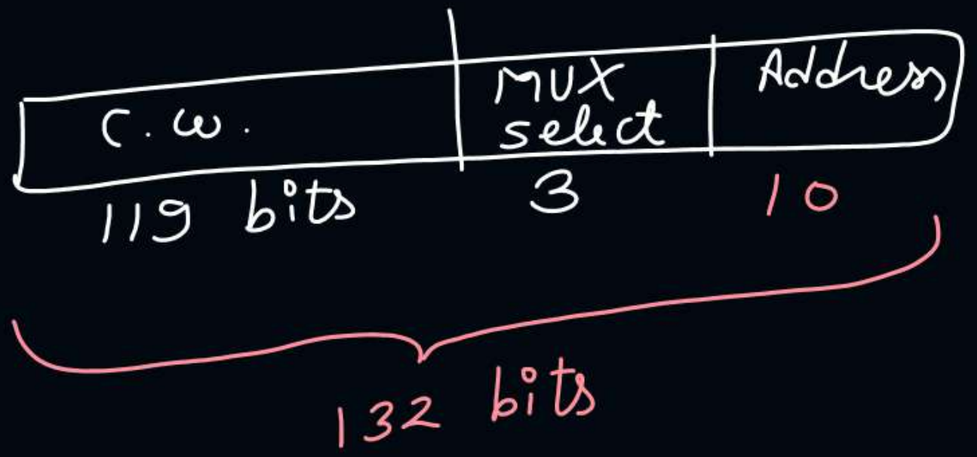
= 1024 * 132 bits

= 132 k bits

Ans.

no. of micro instns = 16 * 64

= 1024 ⇒ add. size = 10 bits



Ques) no. of instns = 128

for each instn ⇒ 64 micro-operations } ⇒ Total = 128 * 64

$= 2^7 * 2^6$

$= 2^{13}$

⇓

add. = 13 bits

Microinstn

Mux has 16 input lines. ⇒ select = 4

Control memory size = _____ k bits ?

Soln

Microinstn size = 125 + 4 + 13 = 142 bits

Control memory size $= 2^{13} * 142$ bits

$= 2^3 * 142$ k bits

$= 1136$ k bits $= 142$ k bytes

Topic : Types of Microprogrammed Control Unit

Horizontal

→ one bit per control signal

→ Larger control word

vertical

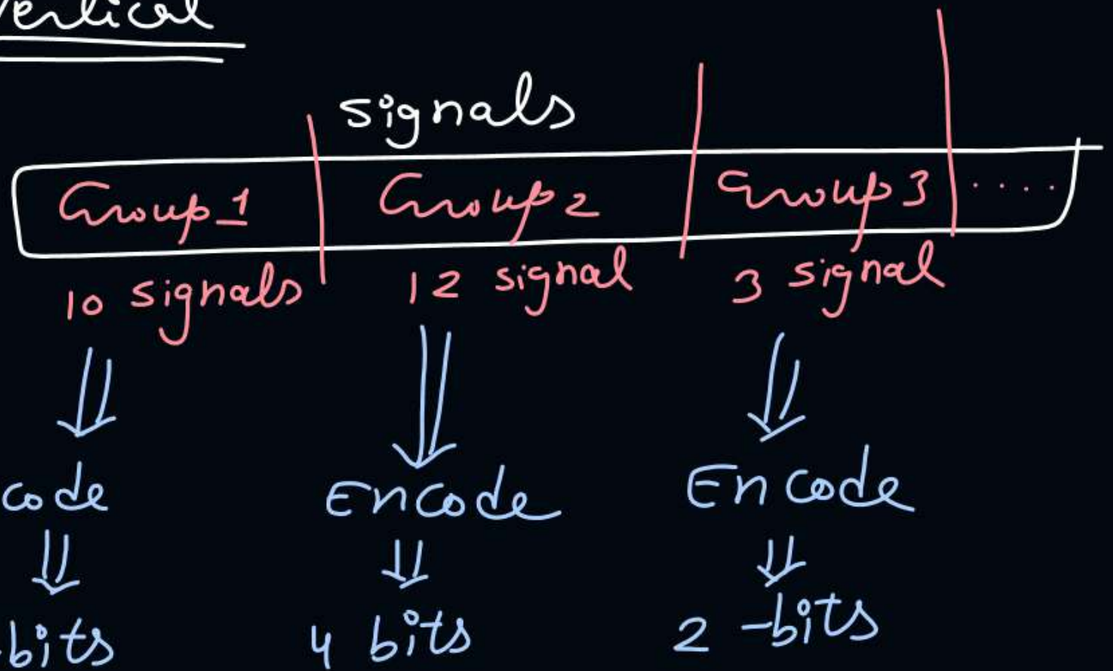
→ Divide all control signals into various groups, in such a way that at a time from one group only one signal will be active.

Each group infon is stored in encoded form to reduce the control word size.

→ To generate signals, decoder is needed.

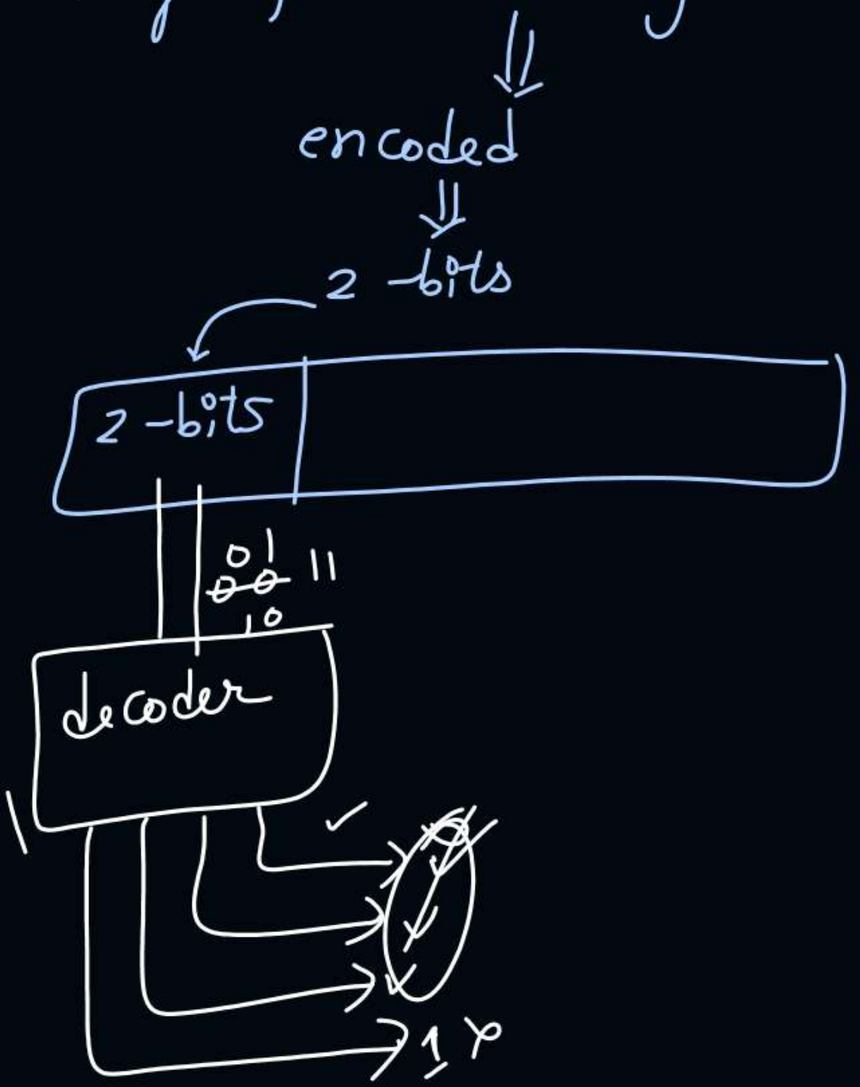
→ slower

Vertical



ex:-

A group has 3 signals



If some signals can not be the part of any of the groups then those are stored in horizontal manner.

Topic : Speed Comparison

fastest ⇒ Hardwired control unit

faster ⇒ Horizontal microprogrammed C.U.

slowest ⇒ vertical ——— 〃 ———

[NAT]

#Q. A control unit generates 120 control signals, which are divided into 6 groups of mutually exclusive signals as below:

Group1 = 30 ⇒ 5 bits
Group2 = 13 ⇒ 4 bits
Group3 = 12 ⇒ 4 bits
Group4 = 3 ⇒ 2 bits
Group5 = 27 ⇒ 5 bits
Group6 = 35 ⇒ 6 bits

5+4+4+2+5+6 = 26 bits

Horizontal = 120 bits
Vertical = 26 bits
Bits saved = 94 bits

How many bits can be saved by using vertical micro-programmed control unit as compared to horizontal one?

[NAT]

H.W.

#Q. A micro-programmed control unit is required to generate a total of 25 control signals. Assume that during any microinstruction at most 2 control signals are active. Minimum number of bits required in the control word to generate the required control signals will be?

Topic : RISC vs CISC

S. No.	RISC (Reduced Instruction-Set Computer)	CISC (Complex Instruction-Set Computer)
1.	Less Number of Instructions Supported	More Number of Instructions
2.	Fixed Length Instructions	Variable Length Instructions
3.	Simple Instructions	Complex Instructions
4.	Simple and less number of addressing Modes	Complex and More number of addressing Modes
5.	Easy to implement using hardwired control unit	Difficult to implement using hardwired control unit

Topic : RISC vs CISC

S. No.	RISC (Reduced Instruction-Set Computer)	CISC (Complex Instruction-Set Computer)
6.	One Cycle per instruction	More than one cycle per instruction
7.	Register-to-Register arithmetic operation only (Reg. - based arch.)	Register-to-Memory & Memory-to-Register arithmetic operations possible
8.	More Number of Registers	Less Number of Registers

[MCQ]

#Q. Consider the following processor design characteristics.

I. Register-to register arithmetic operations only

II. Fixed-length instruction format

III. Hardwired control unit

Which of the characteristics above are used in the design of a RISC processor?

A I and II only

B II and III only

C I and III only

D ✓ I, II and III

2 mins Summary

Topic Datapath

Topic Control Unit Organization

Topic Hardwired Control Unit

Topic Micro-Programmed Control Unit

Topic RISC vs CISC

Happy Learning

THANK - YOU