CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Cache Organization

Lecture No.- 04

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Recap of Previous Lecture

- Topic: Cache Write
- Topic: Write Through & Write Back
- Topic: Write Allocate
- Topic: Cache Mapping

Topics to be Covered

- Topic: Cache Mapping
- Topic: Direct Mapping
- Topic: Tag
- Topic: Tag Directory

⇒ when CPU accesses cache (on-chip) ⇒ system buses not used

⇒ —11— main mem. ⇒ —11— are used

[NAT]

GATE- PYQ 2014

#Q. The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations; 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is?

$T_{avg\ read} = 0.9 * 1 + 0.1 * 5 = 1.4 ns$

$T_{avg\ write} = 0.9 * 2 + 0.1 * 10 = 2.8 ns$

no. of mem. read operations = 100 + 60 = 160

— " — write — " — = 40

Total = 200

% of read = $\frac{160}{200} = 0.8$

% of write = $\frac{40}{200} = 0.2$

$T_{avg} = 0.8 * 1.4 + 0.2 * 2.8$

$= \underline{\underline{1.68 \text{ ns}}}$ Ans.

[NAT]

#Q. Size of data sent to main memory from CPU:

1. For write hit, when a write through cache is used? → 1 byte or 1 word (1 data item size)
2. For write miss, when a write through cache is used? ⇒ 1 data item size
3. For write hit, when a write back cache is used? ⇒ nothing
4. For write miss, when a write back cache is used? ⇒ nothing (write allocate)

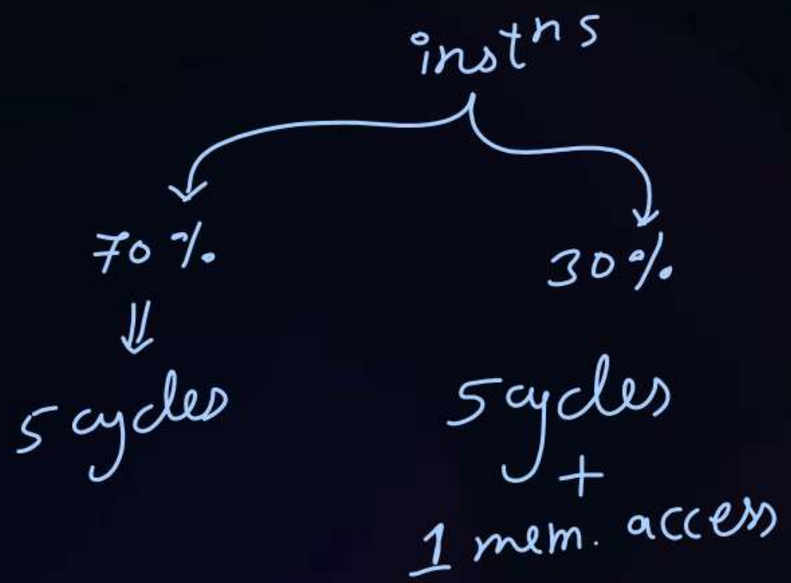
~~[MCQ]~~
NAT

#Q. Size of data sent from main memory to cache:

1. For write hit, when a write through cache is used? ⇒ nothing
2. For write miss, when a write through cache is used? ⇒ nothing
3. For write hit, when a write back cache is used? ⇒ nothing
4. For write miss, when a write back cache is used? ⇒ 1 block

[NAT]

#Q. Consider a system with average cycles per instruction (CPI) is 5 (without any operand access from memory). Consider the average memory access time is 8 cycles and 30% instructions only need 1 memory access for operand then the average CPI is _____ ?



$$CPI_{avg} = 0.7 * 5 + 0.3 * (5 + 8)$$
$$= 7.4$$

$$CPI_{avg} = 5 + 0.3 * 8$$
$$= 7.4$$

#Q. $CPI_{avg} = 6$ (w/o any mem. operand access)

1 Mem access = 3 cycles

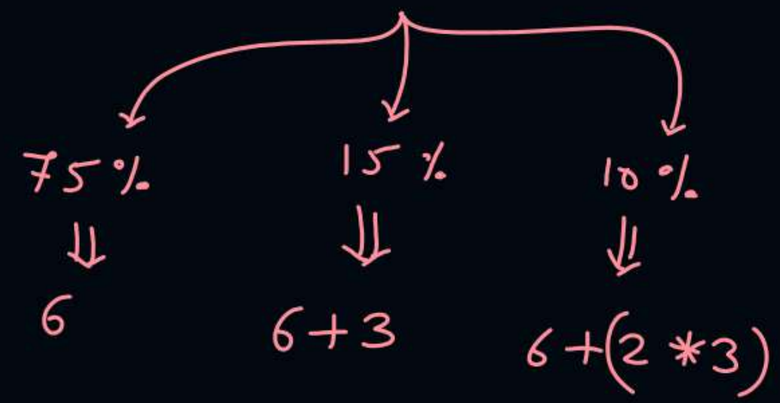
15% instns ⇒ 1 mem. access for operand

10% instns ⇒ 2 —— 11 ——

CPI_{avg} = ?

$CPI_{avg} = 6 + (0.15 * 3) + (0.1 * 2 * 3)$

$= \underline{\underline{7.05}}$ Ans.

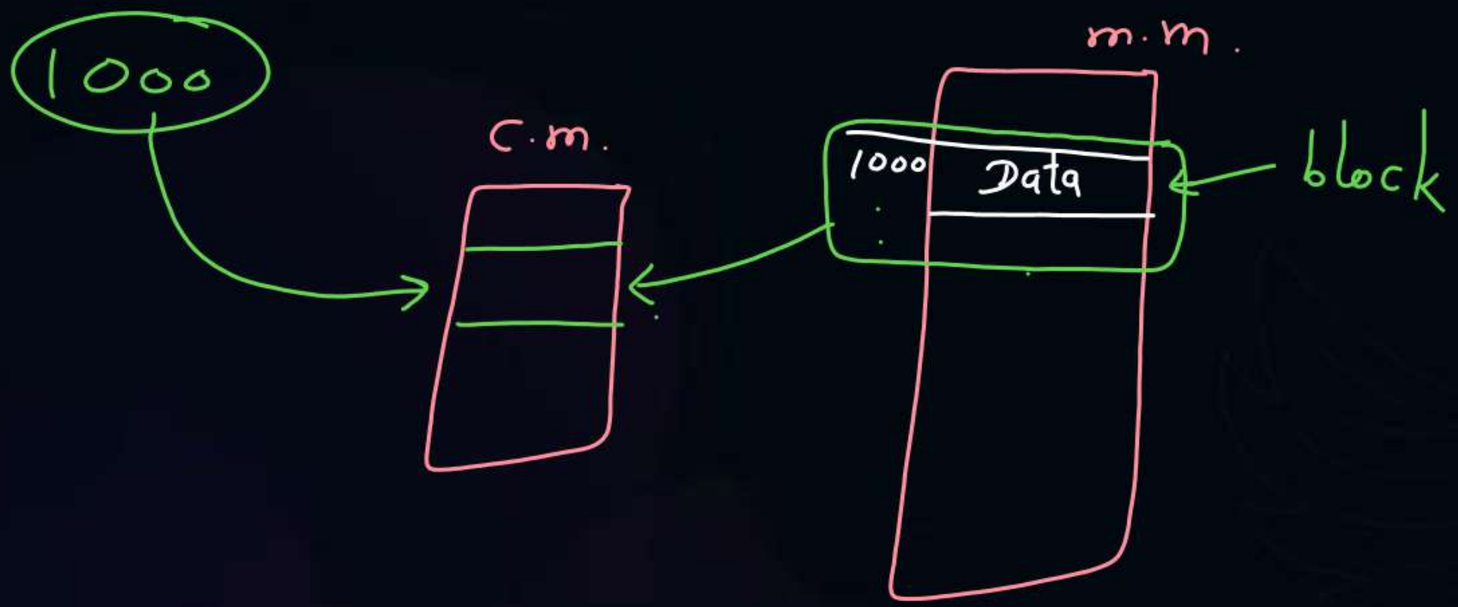


$= (0.75 * 6) + 0.15 * 9 + 0.1 * 12$

$= 7.05$

Topic : Cache Mapping

⇒ CPU always generates m.m. address.



⇒ when a block of mm is copied to cache then a pattern is used to copy this block on to a specific location in cache. so that while searching in cache using mm address, this pattern help to find that specific locatⁿ where this block can be present.

The pattern is called as cache mapping.

or

Transformatⁿ of mm data into cache is known as cache mapping.

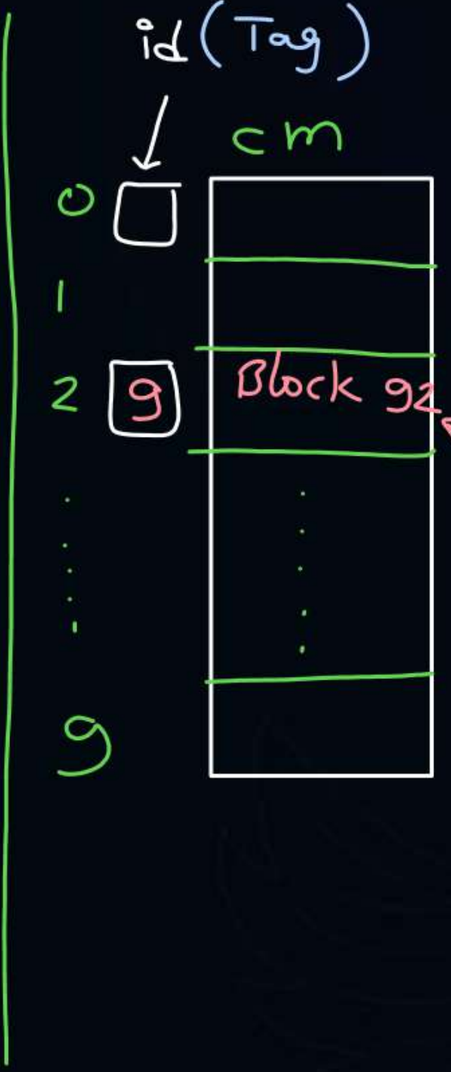
Topic : Cache Mapping

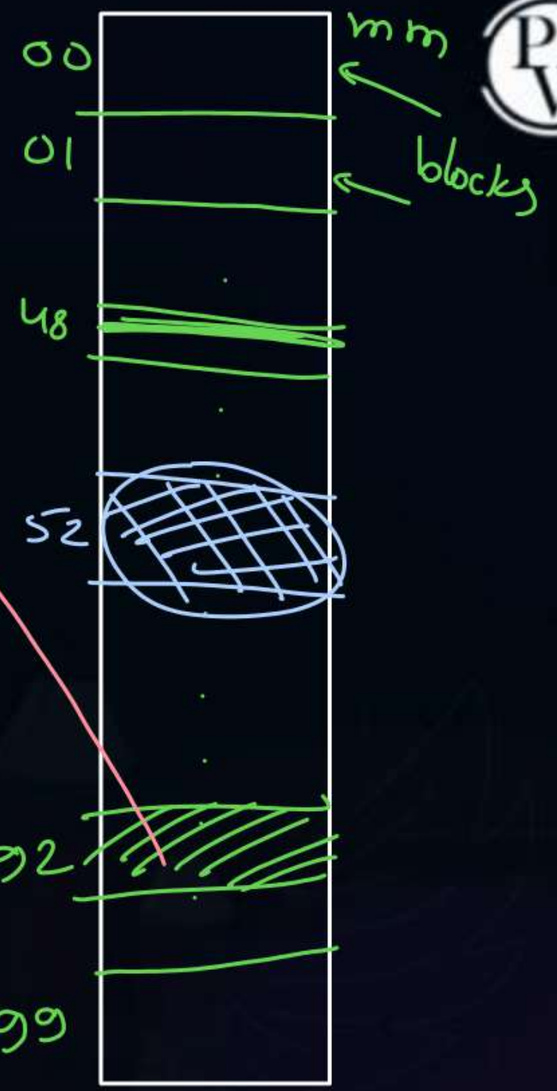
→ applied on blocks

- Direct Mapping
- Set Associative Mapping
- Fully Associative Mapping

Topic : Direct Mapping

- Blocks in cache = 10 (0-9)
- Blocks in Main memory = 100 (00-99)





Topic : Direct Mapping

Cache

0	1	2	3	4	5	6	7	8	9
		Block 52						Block no. 48	

92

Main Memory

00	01	02	03	04	05	06	07	08	09
10	11	12	13	14	15	16	17	18	19
20	21	22	23	24	25	26	27	28	29
30	31	32	33	34	35	36	37	38	39
:	:	52	:	:	:	:	:	:	:
90	91	92	93	94	95	96	97	98	99

← Competitors

Topic : Direct Mapping

cm block no. = (mm block no.) % (no. of blocks in cache)

exi-

mm block no.	cm block no.
34	34 % 10 = 4
62	62 % 10 = 2
95	95 % 10 = 5

Topic : Direct Mapping

CPU Request (MM block)	Mapping (CM block no.)	Hit /Miss	Comments
52	52 % 10 = 2 check block 2 in cache & no any block is present there.	Miss	Bring block no. 52 of mm into cache at block no. 2.
48	48 % 10 = 8 check block 8 in cache & no any block is present there.	Miss	Bring block no. 48 of mm into cache at block no. 48

Topic : Direct Mapping

CPU Request (MM block)	Mapping (CM block no.)	Hit /Miss	Comments
52 (again)	52 % 10 = 2 check block 2 in Cache and block 52 of mm is present there	Hit	CPU reads content from cache
92	92 % 10 = 2 check block 2 in cache; and block 52 of mm is present there not 92	Miss	Bring block 92 of mm into cache at block 2 of cm; by replacing mm block no. 52.

Topic : Direct Mapping

There is competitⁿ b/w 10 blocks here in our example to reside one cm block.

⇓

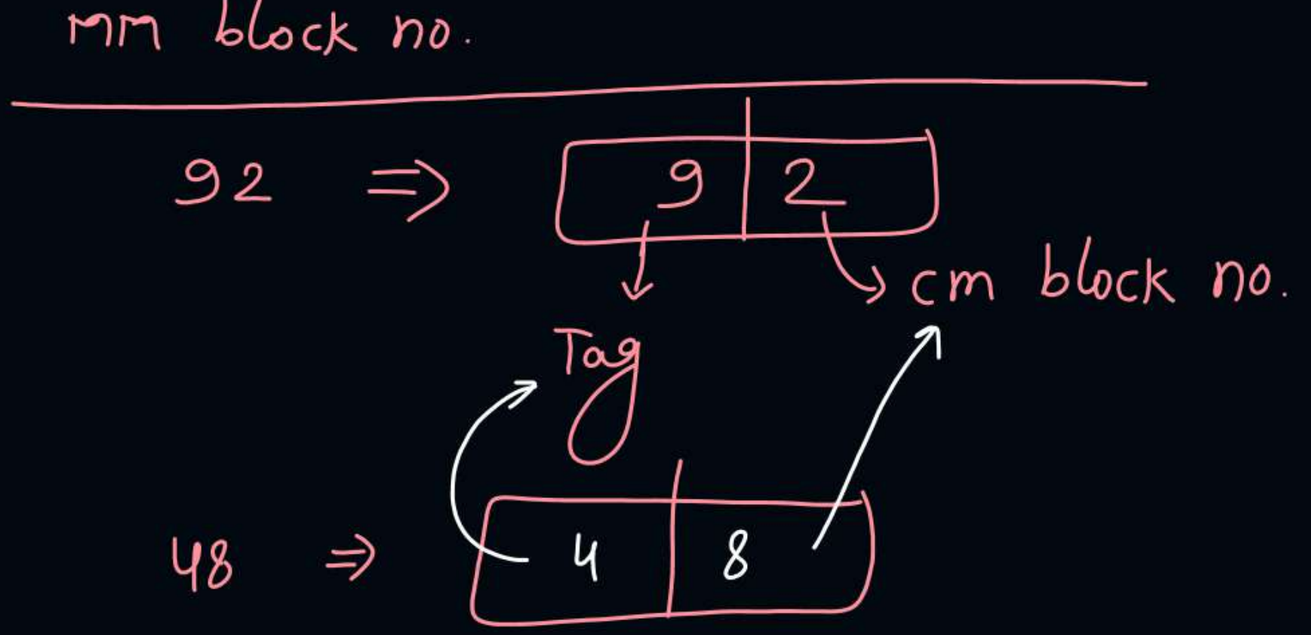
but which mm block among all competitors is present in Cache currently is identified using "Tag".

MM block no.

Tag	CM block no.

$$Tag = \left\lfloor \frac{\text{MM block no.}}{\text{no. of blocks in cache}} \right\rfloor$$

exc:-



2 mins Summary

Topic Cache Mapping

Topic Direct Mapping

Topic Tag

Topic Tag Directory

Happy Learning

THANK - YOU