Computer Organization & Architecture

IO Organization

DPP: 01

Q1 8-bit characters are transmitted using a synchronous mode of transmission with 1 start bit, 8 data bits and 1 stop bit. The efficiency of the transmission line is _____?

Q2 8-bit characters are transmitted using a parity synchronous mode of transmission with 1 start bit, 8 data bits, 2 stop bits and 1 parity bit. If the transfer rate of the line is 3000 bits per second, then effective transfer rate is _____ bytes per second?

Q3 Consider a CPU which takes 0.05 microseconds as interrupt overhead time when a device generates interrupt for CPU, and CPU accepts it. After that CPU takes 5 cycles to service the interrupt. If CPU runs on 10MHz clock rate then total time CPU spends for interrupt service is _____ microseconds (rounded upto 2 decimal places)?

Q4 Which of the following is connected to CPU directly?

(A) Keyboard (B) Hard-disk
(C) RAM (D) Camera

Q5 Which of the following is/are true?

(1) Data format used in IO devices may differ from CPUs format
(2) IO devices are slower than CPU
(3) IO devices are slower than main memory

(A) Only 1
(B) Only 1 & 2
(C) Only 1 & 3
(D) All 1, 2 & 3

Q6 Which of the following is true regarding IO mapped IO as compared to memory mapped IO?

1. ALU operation cannot be performed on IO data directly
2. IO devices have their own address space
3. Less number of Instructions to access IO
4. Less number of IO devices connected

(A) Only 2 & 3
(B) Only 2 & 4
(C) Only 2, 3 & 4
(D) All 1, 2, 3 & 4

Q7 Which of the following is true regarding memory mapped IO as compared to IO mapped IO?

1. ALU operation cannot be performed on IO data directly
2. IO devices do not have their own address space
3. Some memory wastage
4. More number of IO devices connected

(A) Only 2 & 3
(B) Only 2 & 4
(C) Only 2, 3 & 4
(D) All 1, 2, 3 & 4

Q8 Consider a device operating on 8 MBPS speed and transferring the data to memory using cycle stealing mode of DMA. If it takes 250 nanoseconds to transfer 16 bytes data to memory when it is ready/prepared. Then percentage of time CPU is blocked due to DMA is _____ % (rounded upto 1 decimal place)?

Q9 Consider a device operating on cycle stealing mode of DMA and transfer the data to memory in 20 nanoseconds when 8 bytes data is ready or prepared. If the DMA blocks 0.1 fraction of CPU time for this transfer, then the transfer rate of the device is _____ megabytes per second?

Answer Key

Q1	0.8~0.8
Q2	250~250
Q3	0.55~0.55
Q4	(C)
Q5	(C)
Q6	(D)
Q7	(C)
Q8	12.5~12.5
Q9	40~40

Hints & Solutions

Q1 Text Solution:

Total bits sent for one character = 1 start bit + 8 character bits + 1 stop bit = 1+8+1 = 10 bits

Efficiency of transmission line = (bits per character) / (bits transmitted per character)

=8/10 = 0.8

Q2 Text Solution:

Total bits sent for one character = 1 start bit + 8 character bits + 2 stop bits + 1 parity bit

= 1+8+2+1 = 12 bits

Efficiency of transmission line = (bits per character) / (bits transmitted per character)

= 8/12

= 2/3

Effective transfer rate = (2/3) * 3000 = 2000 bits per second

= 2000/ 8 bytes per second

= 250 bytes per second

Q3 Text Solution:

CPU cycle time = 1/10Mhz = 0.1 microseconds

Total interrupt service time = interrupt overhead time + interrupt service time

= 0.05 + 5* 0.1

= 0.55

Q4 Text Solution:

Only memory is the other component of computer among all given which is directly connected to CPU. Rest all other 3 are peripheral devices and are connected with CPU using IO interface.

Q5 Text Solution:

(1) Data format used in IO devices may differ from CPUs format; that's why IO interface helps in data format conversions during data transfer between CPU & IO.

(2) CPU is fastest among all components of computer.

(3) Memory is faster than IO devices and slower than CPU

Q6 Text Solution:

1. ALU operation cannot be performed on IO data directly, because IO access instructions and memory access instructions in IO mapped IO are different-different and IO data can not be given to ALU directly through one instruction.
2. IO devices have their own address spaces and memory addresses are separate.
3. Less number of Instructions to access IO than the memory access instructions.
4. Less number of IO devices connected than memory mapped IO.

Q7 Text Solution:

1. ALU operation can be performed on IO data directly, because IO access instructions and memory access instructions are same.
2. IO devices don not have their own address spaces and are mapped to memory addresses only.
3. Memory wastage because the addresses which are given to IO devices cannot be used.
4. More number of IO devices connected than IO mapped IO.

Q8 Text Solution:

8 MB data preparation time in IO = 1 second

1 byte data preparation time in IO = 1/8M

= 0.125 microseconds

= 125 nanoseconds

16 bytes data preparation time in IO = 16 * 125 = 2000 nanoseconds

The percentage of time CPU is blocked due to DMA is = (250 / 2000) * 100%

= 12.5%

Q9 Text Solution:

Fraction of time CPU is blocked due to DMA = (transfer to memory time / preparation time)

0.1= 20 / preparation time

preparation time = 200 nanoseconds

In 200 nanoseconds, device can prepare data = 8 bytes

In 1 nanoseconds, device can prepare data = 8 bytes /200nanoseconds

= 8000 bytes / 200microseconds

= 40 bytes / microseconds

In 1 second, device can prepare data = 40 bytes * 10^6/ second

= 40 Mbytes per second