CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Memory Organization

Lecture No.- 01

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Recap of Previous Lecture

Topic DMA

Topic Modes of DMA

Topic Cycle Stealing

Topics to be Covered

- Topic: Memory Hierarchy
- Topic: Memory Presentation
- Topic: Memory Address Decoder
- Topic: Main Memory

Topic : Memory Hierarchy

Memory hierarchy used when discussing performance issues.

Goal of Memory Hierarchy:

1. To maximize the Access Speed
2. To minimize the Per Bit Storage Cost

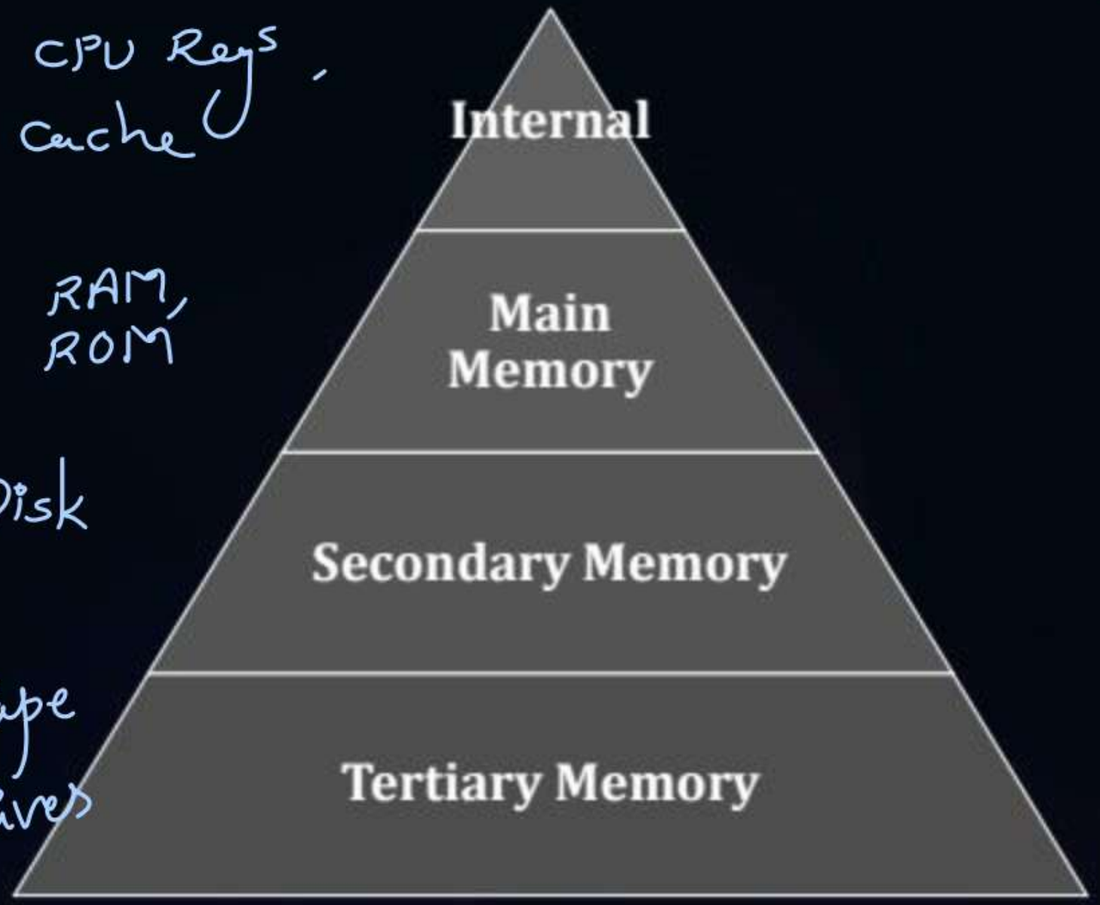
Topic : Memory Hierarchy

CPU Regs
Cache

RAM,
ROM

Disk

Tape
drives



Access speed

Size

per bit storage cost

frequency of access by CPU

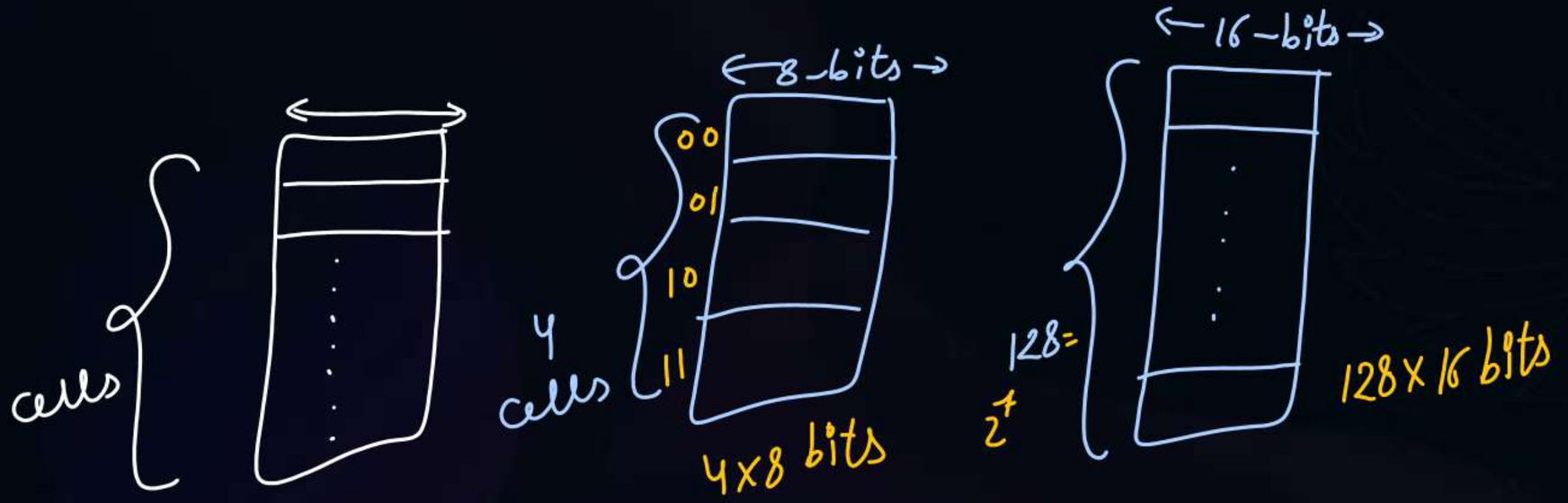
Access time

Topic : Memory Presentation

Memory is represented by :-

= no. of cells × 1 cell capacity

= no. of memory location × bits per location



Topic : Memory Presentation

no. of cells = 2^x	n
address size = x bits	$\lceil \log_2 n \rceil$ bits

ex:-

$128K \times 8$ bits $\Rightarrow$ $128K \times 1$ Byte $\Leftarrow$ byte addressable

$128K$: no. of cells

8 bits : cell capacity

$\Downarrow$

$128K$ bytes

Topic : Memory Presentation

mem. capacity => 256 GB $= 2^8 \cdot 2^{30}$ bytes $= 2^{38} \times 1\,B$

add. size = 38 bits

$\Downarrow$

add. $= \log_2 2^{38} = 38$

[MCQ]

#Q. Memory is represented as?

A. A×B where A = No. of memory locations, B = No. of bits in each location

B. $2^a \times B$ where a = No. of address bits, B = No. of bits in each location

C. B×A where, B = No. of bits in each location, A = No. of memory locations

D. (A) & (B) both

[MCQ]

#Q. A memory has 14-bits address bus. Then^how many memory locations are there?

max.

no. of locations $= 2^{14} = 16k = 16384$

A 16K

B 16384

C 2^{14}

D All

Memory cycle time :- (Mem. access time)

Time in which read or write operation is performed on one address of memory.

[MCQ]

#Q. The memory cycle time of a memory is 200nsec. The maximum rate with which the memory can be accessed?

Note: Consider memory as byte addressable.

A 500 Bytes / Sec

B 2000 Bytes / Sec

C ✓ 5 Mbytes / Sec

D 5 GBytes / Sec

In 200 ns, data accessed = 1B

In 1 ns, —"— = $\frac{1B}{200\,ns}$

In 1 sec, —"— = $\frac{1B}{200 * 10^{-9}\,sec}$

$= \frac{10^9\,B}{200\,sec}$

$= 5\,MB/sec$

Ques) If mem. access time = 50nsec (mem. byte addressable)

access rate = ____20____ MBPSec

Soln

In 50 nsec, data accessed = 1B

1 sec, —//— = $\frac{1B}{50 * 10^{-9} sec}$

= 20 MBPS

[NAT] GATE-PYQ Ans = 31

#Q. A processor can support a maximum memory of 4 GB, where the memory is word addressable (a word consists of two bytes). The size of the address bus of the processor is at least ____ bits?

$2G \times 2\text{bytes}$

$\Downarrow$

2^{31}

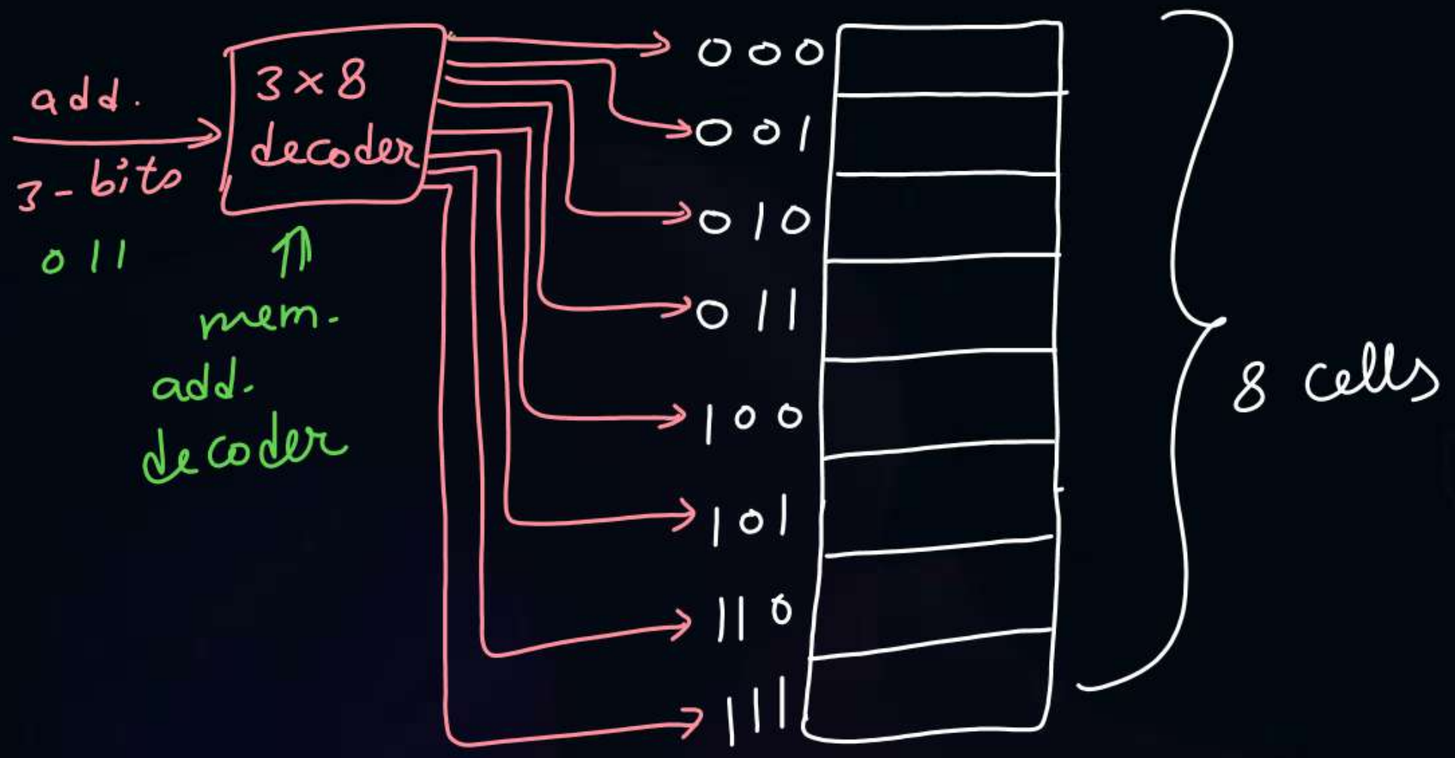
$\Downarrow$

$\text{add.} = \log_2 2^{31} = 31 \text{ bits}$

$\text{no. of words (cells)} = \frac{4GB}{2B} = 2G$

Topic : Memory Address Decoder

ex:- 8 × 16 bits memory



ex:-
mem:- 128 × 8 bits

add. size = 7 bits

mem. add. decoder = 7 × 128

---

ex:
mem:- 64M × 16 bits

no. of cells = 2^{26} ⇒ add. = 26 bits

mem. add. decoder = 26×2^{26}

or

$= 26 \times 64M$

[NAT]

#Q. Consider a memory of size 2K × 8-bits. What is the size of decoder needed to access the cells of the memory uniquely?

no. of cells = $2k = 2^{11}$ ⇒ add. size = 11 bits

decoder = 11×2^{11} or $11 \times 2k$

[NAT] GATE – PYQ

#Q. If there are m input lines n output lines for a decoder that is used to uniquely address a byte addressable 1 KB RAM, then the minimum value of m + n is _____?

1 KB

↓

1k x 1B

↓

cells = 1k = 2^{10} ⇒ add. = 10 bits

decoder size = 10×2^{10}

m = 10

n = 1024

m + n = 10 + 1024 = 1034

Ans.

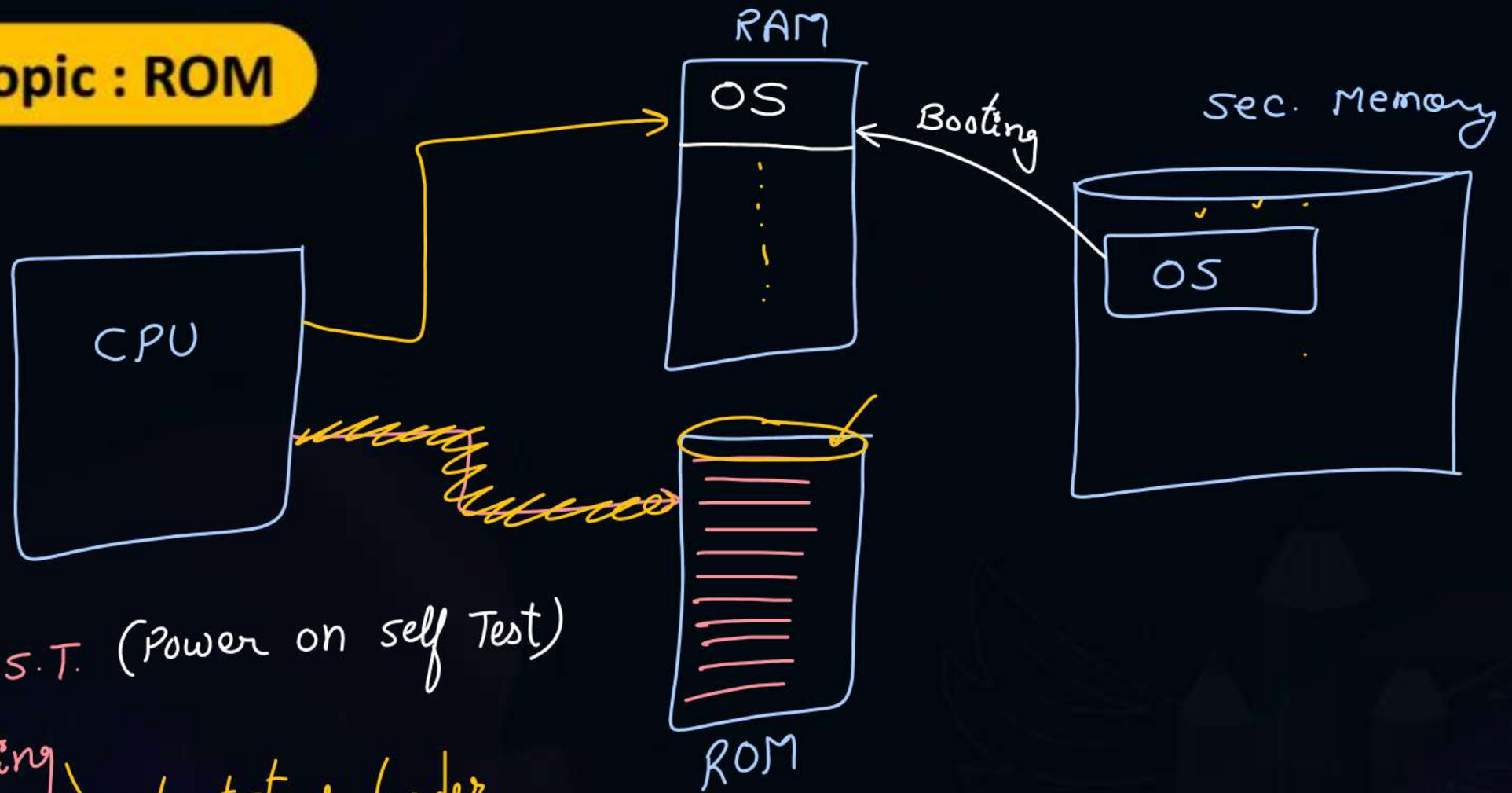
Topic : Main Memory

Used to store current running program (instructions) and their data.

Types :-

1. RAM (Random Access memory) ⇒ Volatile
2. ROM (Read Only memory) ⇒ Non-volatile

Topic : ROM



1. P.O.S.T. (Power on self Test)
2. Booting → bootstrap loader
   → responsible for booting

Topic : RAM

Used to store OS, ^ user programs and other running programs & their data.

Topic : Types of RAM

Static (S-RAM)	Dynamic (D-RAM)
1. Made up of flip-flops	1. Made up of capacitors
2. No any recharge needed	2. Periodic recharge/refresh is needed.
3. Faster read/write	3. slower read/write
4. Costlier	4. Less costlier
5. Used for cache implementation	5. Used mainly for main memory chips
6. Less idle power consumption	6. More idle power consumption
7. More operational power consumption	7. Less operational power consumption

[NAT]

#Q. Consider 2 4-bits unsigned values A and B. What will be the maximum size of result for:

1. Addition of A and B ⇒ 5-bits
2. Multiplication of A and B ⇒ 8-bits

| (n+1) bits
| 2n bits

| A | B
max value | $(1111)_2$ ⇓ $= (15)_{10}$ | $(1111)_2$ ⇓ $(15)_2$

| $A + B \Rightarrow (30)_{10} \Rightarrow$ 5-bits needed

| $A * B \Rightarrow (225)_{10} \Rightarrow$ 8-bits needed

[MCQ]

#Q. The amount of ROM needed to store the table for multiplication of two 4-bit unsigned integer is?

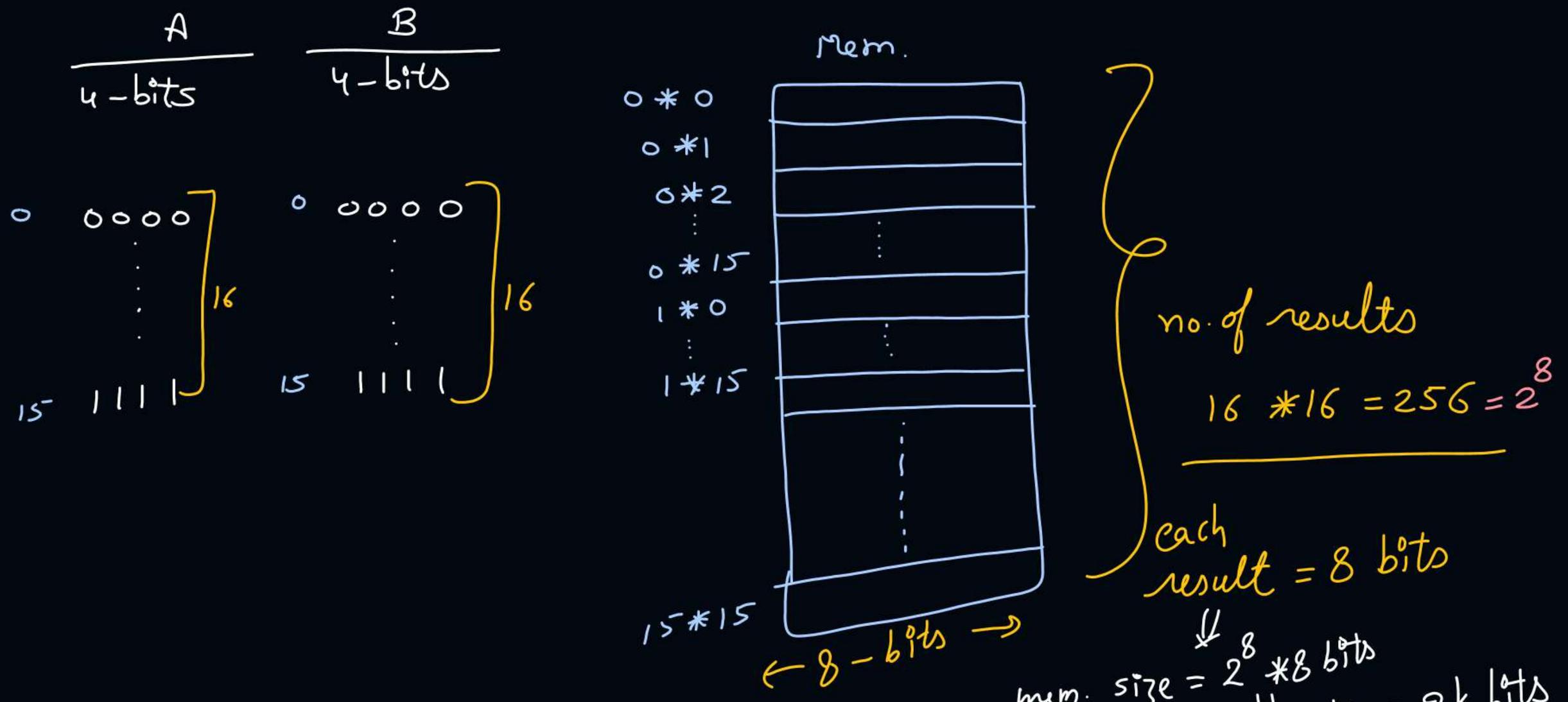
store result of multiplicat^{n} of each possible value of each int.

A 64 bits

B 128 bits

C 1K bits

D ✓ 2K bits


A
4-bits
B
4-bits
0
0000
15
1111
16
0
0000
15
1111
16
Mem.
0*0
0*1
0*2
0*15
1*0
1*15
15*15
←8-bits→
no. of results
16*16 = 256 = 2^8
each result = 8 bits
mem. size = 2^8 * 8 bits
= 2^11 bits = 2k bits

A	B	Multiplication table size	Addition table size
4-bits	4-bits	$2^8 \times 8$ bits	$2^8 \times 5$ bits
n-bits	n-bits	$2^{2n} \times 2n$ bits	$2^{2n} \times (n+1)$ bits

2 mins Summary

Topic Memory Hierarchy

Topic Memory Presentation

Topic Memory Address Decoder

Topic Main Memory

Happy Learning

THANK - YOU