CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

CPU & Control Unit

Lecture No.- 01

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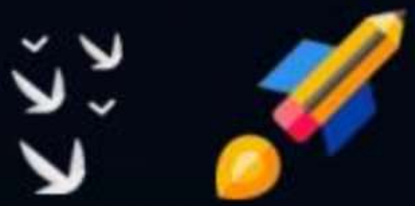
Recap of Previous Lecture

- **Topic** Addressing Modes
- **Topic** Types of Addressing Modes
- **Topic** CPU Cycle
- **Topic** CPI

Topics to be Covered

- Topic CPU
- Topic MIPS
- Topic Data Path
- Topic Control Unit
- Topic Control Unit Organization



Load ⇒ mem. to CPU data transfer

store ⇒ CPU to mem. data transfer

Topic : CPU

1. CPU Cycle
2. CPU Clock rate
3. CPI
4. Execution Time = CPI * cycle time

$\Rightarrow$ n * CPI * cycle time

	Add. or Bits or bytes	Time
K	2^{10}	10^{3}
M	2^{20}	10^{6}
G	2^{30}	10^{9}

Millisecond (ms) $\Rightarrow$ 10^{-3} sec.

Microsecond (μs) $\Rightarrow$ 10^{-6} sec

Nanosecond (ns) $\Rightarrow$ 10^{-9} sec

ex:- CPU clock rate 2 GHz

cycle time = ?

soln cycle time $= \frac{1}{2\,GHz}$

$= \frac{1 \text{ second}}{2 * 10^9}$

$= \frac{1}{2}$ nsec

$= 0.5$ nsec

$\frac{1}{GHz} = nsec \Rightarrow \frac{1}{nsec} = 1\,GHz$

$\frac{1}{mHz} = \mu sec \Rightarrow \frac{1}{\mu sec} = 1\,MHz$

$\frac{1}{kHz} = msec \Rightarrow \frac{1}{msec} = 1\,kHz$

ex:-

= 0.2 nsec

= 0.0002 μsec

ex: (2)

= 20 μsec

= 20000 nsec

ex:-

= 0.2 GHz

= 200 MHz

ex:-

= 20000 KHz

= 0.02 GHz

Topic : MIPS

Million Inst^{ns} Per second

⇓

no. of inst^{ns} executed by a CPU in one second (in million)

in t seconds no. of inst^{ns} executed = n

in 1 —— || —— $= \frac{n}{t}$

$$= \frac{n}{n * CPI * cycle\ time}$$

$$= \frac{1}{CPI * cycle\ time}$$

$$MIPS = \frac{1}{CPI * Cycle\ time * 10^6}$$

$$MIPS = \frac{clock\ rate}{CPI * 10^6}$$

Topic : Average CPI

Consider computing the overall CPI for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 200 MHz

Instruction Category	Number of Instructions	No. of cycles per Instruction	Total cycles
ALU	48	1	48 * 1 = 48
Load & Store	10	3	10 * 3 = 30
Branch	39	4	39 * 4 = 156
Other	3	5	3 * 5 = 15
	Total = 100		249

Avg. cycles per inst^n (CPI$_{avg}$) $= \dfrac{\text{Total cycles}}{\text{no. of inst}^{ns}}$

$= \dfrac{249}{100}$

$= 2.49$

$\text{MIPS} = \dfrac{200\ \text{MHz}}{2.49 * 10^6} = 80.32\ \text{MIPS}$

[NAT] GATE- 2014

Ans = 1.6

#Q. Consider two processors P1 and P2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P1. If the clock frequency of P1 is 1GHz, then the clock frequency of P2 (in GHz) is _____?

	P1	P2
execution time	t_1	$t_2 = 0.75\, t_1$
CPI	C_1	$C_2 = 1.2\, C_1$
freq. (clock rate)	$f_1 = 1GHz$	$f_2 = ?$
no. of insths	n_1	n_2

n no. of inst^{ns} execution time $= \dfrac{n * CPI}{\text{clock rate}}$

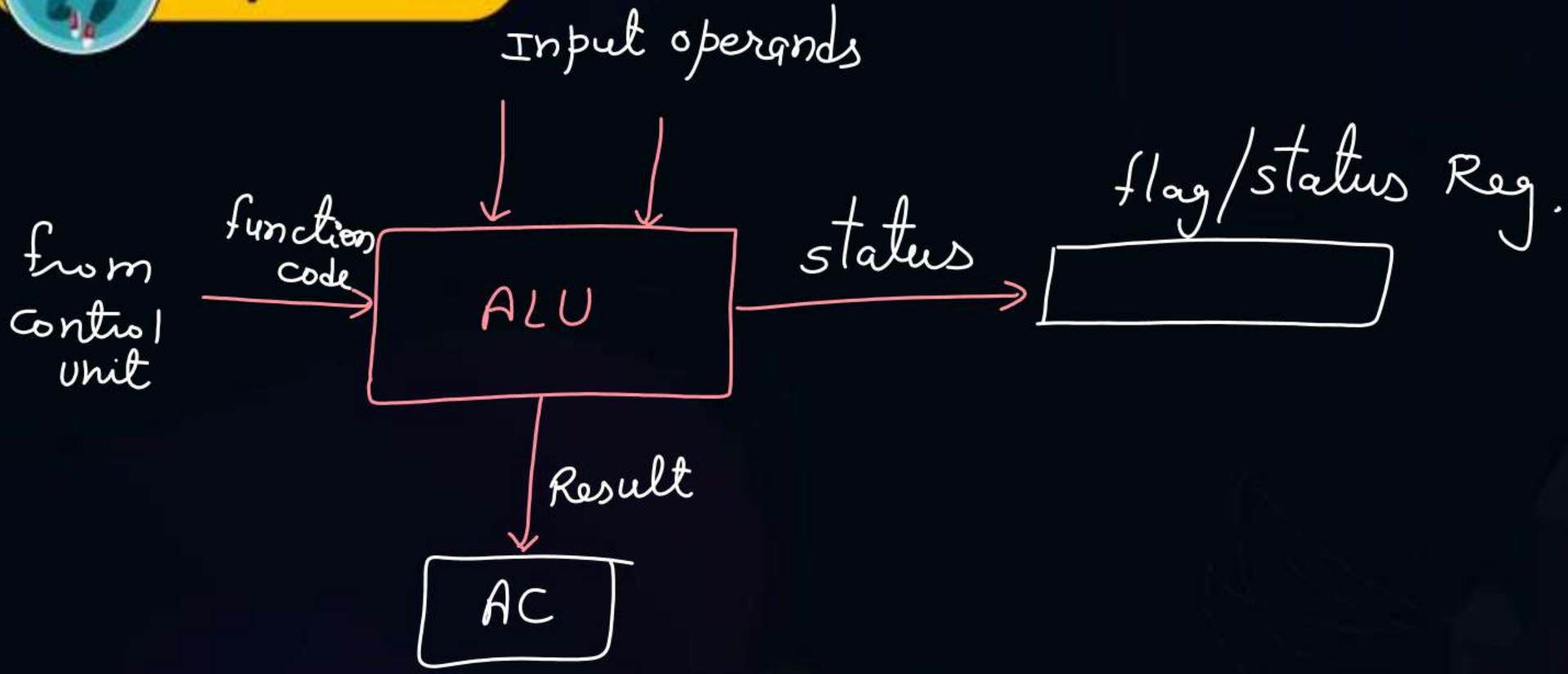
$$n_1 = n_2$$

$$\frac{t_1 * f_1}{CPI_1} = \frac{t_2 * f_2}{CPI_2}$$

$$\frac{t_1 * 1GHz}{C_1} = \frac{0.75\, t_1 * f_2}{1.2\, C_1}$$

$$f_2 = \frac{1.2}{0.75} * 1GHz = 1.6\,GHz$$

Topic : ALU


Input operands
function code
from control unit
ALU
status
flag/status Reg.
Result
AC

Topic : Datapath

Collection of functional units such as arithmetic logic units or ~~multipliers~~ multiplexers

to Perform data processing operations

Topic : Datapath

operation => $R1 \leftarrow R2 + R3$

$\Downarrow$

micro operations :-

$S \leftarrow R2$

$T \leftarrow R3$

$AC \leftarrow S + T$

$R1 \leftarrow AC$

operation :-

Instⁿ fetch

$AR \leftarrow PC$

$DR \leftarrow M[AR]$

$IR \leftarrow DR, \quad PC \leftarrow PC + 1$

ex:- Assume all mem. access (micro) operations take 4 CPU cycles and remaining all take 1 CPU cycle.

no. of CPU cycles for

$R1 \leftarrow R2 + R3$

$\Downarrow$

4 cycles

inst^n fetch

$\Downarrow$

1 + 4 + 1 = 6 cycles

Topic : Control Unit

It generates control signals and sends them to different-different components of computer.

The components perform their respective operations accordingly.

To perform microoperatⁿ :-

$S \leftarrow R2$ control signals $\Rightarrow$ $R2_{out}$, S_{IN}

$T \leftarrow R3$ —11— $\Rightarrow$ $R3_{out}$, T_{IN}

$AC \leftarrow S + T$ —11— $\Rightarrow$ S_{out}, T_{out}, $ALU_{addition}$, AC_{IN}

$R1 \leftarrow AC$ —11— $\Rightarrow$ AC_{out}, $R1_{IN}$

$AR \leftarrow PC \quad \Rightarrow \quad PC_{out}, AR_{In}$

$DR \leftarrow M[AR] \quad AR_{out}, Memory_{read}, DR_{In}$

$IR \leftarrow DR, PC \leftarrow PC+1 \quad DR_{out}, IR_{In}, PC_{Incr}$

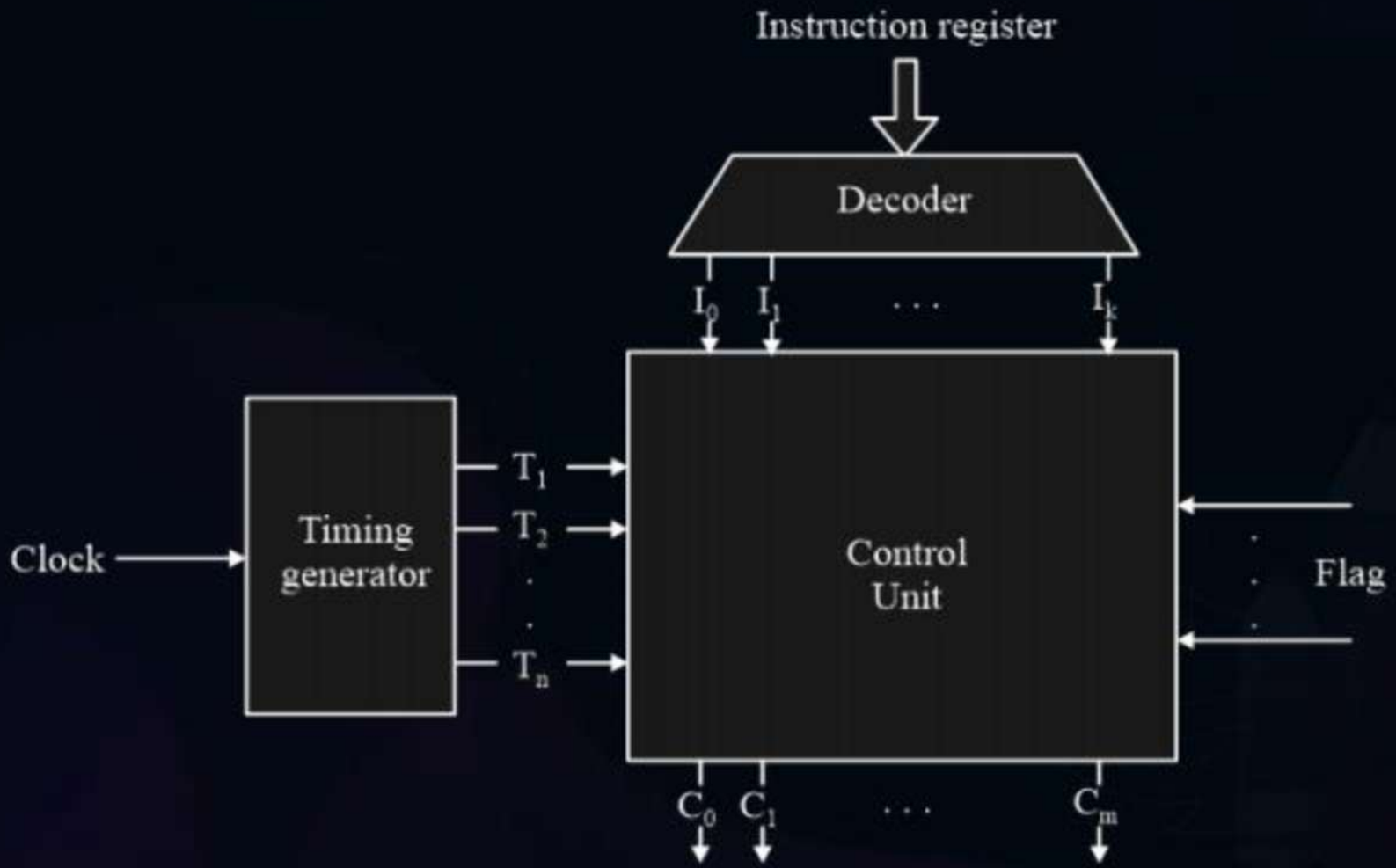
Topic : Hardwired Control Unit

Control logic is implemented with Gates, flip-flops, decoders and other digital circuits.

Advantage: Can be optimized to produce a faster mode of operation.

Disadvantage: Rearranging the wires among various components is difficult.

Topic : Hardwired Control Unit



[MCQ]

#Q. A hardwired CPU uses 10 control signals S1 to S10, in various time steps T1 to T5, to implement 4 instructions 11 to 14 as shown below:

	T1	T2	T3	T4	T5
I1	S1, S3, S5	S2, S4, S6	S1, S7	S10	S3, S8
I2	S1, S3, S5	S8, S9, S10	S5, S6, S7	S10	S1, S3
I3	S1, S3, S5	S7, S8, S10	S2, S6, S9	S10	S1, S3
I4	S1, S3, S5	S2, S6, S7	S5, S10	S6, S9	S10

Which of the following pairs of expressions represent the circuit for generating control signals S5 and S10 respectively?

A

$S5 = T1 + I2 \cdot T3$ and
$S10 = (I1 + I3) \cdot T4 + (I2 + I4) \cdot T5$

B

$S5 = T1 + (I2 \cdot I4) \cdot T3$ and
$S10 = (I1 + I3) \cdot T4 + (I2 + I4) \cdot T5$

C

$S5 = T1 + (I2 \cdot I4) \cdot T3$ and
$S10 = (I1 + I3 + I4) \cdot T2 + (I2 + I3) \cdot T4 + (I2 + I4) \cdot T5$

D

$S5 = T1 + (I2 \cdot I4) \cdot T3$ and
$S10 = (I2 + I3) \cdot T2 + I4 \cdot T3 + (I1 + I3) \cdot T4 + (I2 + I4) \cdot T5$

2 mins Summary

- **Topic** CPU
- **Topic** CPI & MIPS
- **Topic** Datapath
- **Topic** Control Unit
- **Topic** Hardwired Control Unit

Happy Learning

THANK - YOU