GATE

CS & IT

Computer Organization & Architecture

DPP: 01

Memory Organization

Q1 The memory cycle time of a memory is 500nsec. The maximum rate with which the memory can be accessed?
Note: Consider memory as byte addressable.
(A) 500 Bytes / Sec
(B) 2000 Bytes / Sec
(C) 2 Mbytes / Sec
(D) 2 GBytes / Sec

Q2 The address bus width of a memory of size 4096 × 8 bits is ____ bits?

Q3 Consider a byte addressable memory which has 0.2GBPS writing rate. The memory access time is ___ nanoseconds?

Q4 Consider a word addressable memory of total capacity of 4GB. The memory is accessed using a minimum of 29 bits address bus. The word size per address in this memory is ____ bytes?

Q5 Consider a memory with maximum size of X bytes. Memory is word addressable with word size of W bytes. The size of the address bus of the processor is at least _____ bits?
(A) $Log_2(X/W)$ (B) $2^{(X/W)}$
(C) X/W (D) $Log_2(X)$

Q6 A DRAM chip of 64M×16 bits has 128K rows of cells with y cells in each row. If DRAM takes x-ns for 1 refresh then total refresh time of the DRAM is _____ Microseconds, if $x = 2 \times \log_2 y$?
(A) 1200 (B) 2304
(C) 3202 (D) 5444

Q7 A 32-bits wide main memory unit with a capacity of 16GB is built using 8-bits RAM chips. If there are x-horizontal arrangements of chips are there, with y number of chips in each horizontal arrangement then the value of 10x + y is?

Answer Key

Q1	(C)
Q2	12~12
Q3	5~5
Q4	8~8
Q5	(A)
Q6	(B)
Q7	324~324

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Hints & Solutions

Q1 Text Solution:

Memory cycle time means memory take 500nanoseconds for read or write on one address.

Here memory is byte addressable hence on 1 address 1 byte content is stored.

In 500 nanoseconds, data accessed from memory = 1 byte

In 1 second, data accessed from memory = 1 byte / 500 nanoseconds

=

0.002 gigabytes per second

= 2

megabytes per second

Q2 Text Solution:

Number of cells in memory = 4096 = 2^{12}

Hence address size for memory = 12 bits

Q3 Text Solution:

For 0.2 GB data, time taken = 1 second

For 1 byte data, time taken = 1 second / 0.2 G

= 5 nanoseconds

Q4 Text Solution:

Address size = 29 bits, hence Number of cells in memory = 2^{29}

Number of cells in memory = total capacity / word size

4GB = 2^{29} / word size

Word size = 4GB / 2^{29}

= $2^{32}/2^{29}$ bytes

= 2^3 bytes

= 8 bytes

Q5 Text Solution:

Number of cells in memory = total capacity / word size

= X/W

Address size of memory = $\log_2(X/W)$

Q6 Text Solution:

: Number of cells in memory as given = 64M

128K × cells per row = 64M

Cells per row = 64M / 128K = 2^9

Hence y = 2^9

Hence x = 2 × $\log_2 y$ = 2 × $\log_2 2^9$ = 18 nanoseconds

DRAM refresh time = number of rows of cells × 1 refresh time

= 128K × 18 nanoseconds

= 2304 microseconds

Q7 Text Solution:

32-bits wide main memory means for each address, demanded data is 32 bites = 4 bytes

Number of words in memory = 16GB / 4bytes = 4 G

Hence memory can be represented as 4G × 4 bytes

1 chip capacity = 128M× 8-bits = 128M ×1 byte

Number of chips required = total capacity / 1 chip capacity

(4G × 4) / (1)

Here for such memory 32 vertically arranged, 4 chip horizontal arrangements are needed.

Hence x = 32 and y = 4

Value of 10x + y = 10 × 32 + 4 = 324