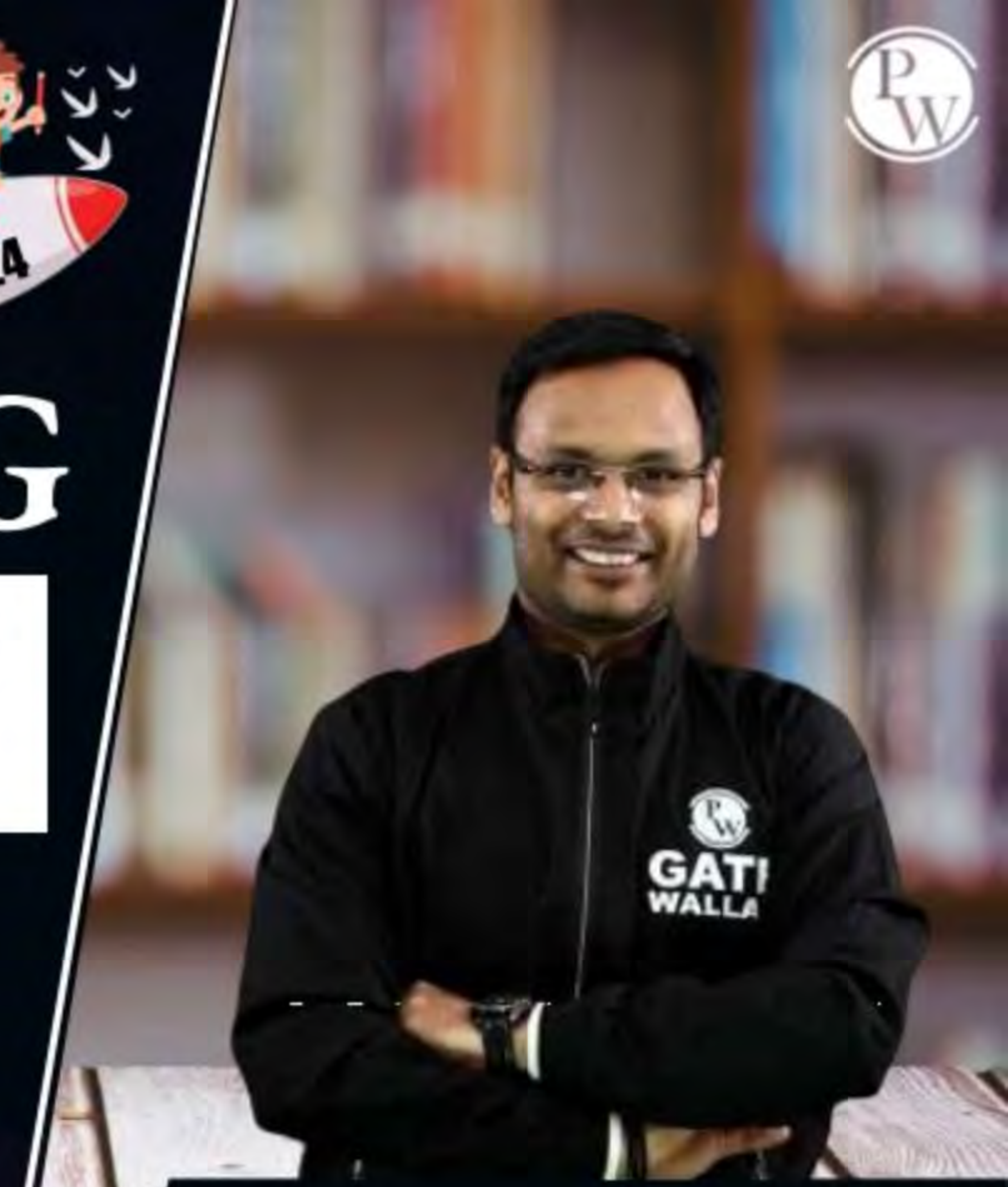
CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Pipeline Processing



Lecture No.- 02

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Recap of Previous Lecture

Topic Pipeline Processing

Topic Pipeline Cycle Time

Topic Speed Up

Topics to be Covered

$$\frac{n * t_n}{(k+n-1)\, t_p}$$

Topic Pipeline Throughput

Topic Latency

Topic Instruction Pipeline

[NAT]

#Q. The time delay of the four segments in pipeline are as shown follows:
$t_1 = 50$ ns, $t_2 = 30$ ns, $t_3 = 95$ ns, and $t_4 = 45$ ns.
The interface registers delay time $t_r = 5$ ns.
How long would it take to process 100 tasks in the pipeline?

$t_p = 95 + 5 = 100\text{ ns}$

$n = 100$

$k = 4$

$\text{time} = (4 + 100 - 1)\,100$

$= 10300\text{ ns}$

[NAT]

#Q. How can we reduce the total time about the one-half of the time calculated in above question?

seg 3 with delay is decomposed into 2 segments with delays 50ns, 45ns

$t_1 = 50ns$

$t_2 = 30ns$

$t_{31} = 50ns$

$t_{32} = 45ns$

$t_4 = 45ns$

$k = 5$

$t_p = 50 + 5 = 55ns$

$n = 100$

pipeline time

$= (5 + 100 - 1) 55$

$= 5720 ns$

Learning :-

If seg. delays are almost equal then pipeline performs better.

Questⁿ) There are 2 pipelines

old	new
5 segments with delay	S4 divided into 2 segments with delays 13 ns, 7 ns.
S1 ⇒ 5 ns	
S2 ⇒ 12 ns	
S3 ⇒ 9 ns	
S4 ⇒ 20 ns	
S5 ⇒ 8 ns	

1. speed up of new pipeline as compared to old, for 50 inputs
2. ——— " ——— " ——— in ideal condition

old	new
$k = 5$	$k = 6$
$t_p = 20$ ns	$t_p = 13$ ns
$n = 50$	$n = 50$
time $= (5+50-1)20$ $= 1080$ ns	time $= (6+50-1)13$ $= 715$ ns

1. speed up $= \frac{1080}{715} = 1.51$

2. $S = \frac{(k+n-1)\,t_{p_{old}}}{(k+n-1)\,t_{p_{new}}}$

$= \frac{20}{13}$

$= 1.54$

[NAT]

#Q. Consider a non-pipelined processor with a clock rate of 4 gigahertz and average cycles per instruction of 5. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to ~~5~~ 3 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is ________.

Non-pipeline

cycle time $= \frac{1}{4GHz} = 0.25\,ns$

$t_n = 5 * 0.25\,ns = 1.25\,ns$

Pipeline

$k = 5$

pipeline cycle time $(t_p) = \frac{1}{3GHz} = 0.33\,ns$

$$S = \frac{t_n}{t_p} = \frac{1.25}{0.33} = 3.75$$

How to calculate t_p :-

1. Given in Questn
2. Max of seg. delays
3. Max of seg. delays + Reg./Buffe delay
4. $\frac{1}{\text{clock rate}}$

How to calculate t_n :-

1. Given in Questn
2. Sum of all segment delays
3. CPI * $\frac{1}{\text{clock rate}}$

Topic : Latency and Throughput

pipeline = t_p

non-pipeline = t_n

Latency :-

After how much time a new input is given to system

→ no. of operations performed per unit time

in time $(k+n-1)t_p$, no. of operations = n

in time 1 —— " —— $= \boxed{\dfrac{n}{(k+n-1)t_p}}$

Throughput

$$\boxed{\text{Throughput}_{(\text{ideal})} = \frac{1}{t_p}}$$

[NAT]

$t_p = 126 + 5 = 131\,ns$ | $t_n = 120 + 126 + 121 + 110 + 118 + 120 = 715\,ns$

#Q. Consider 6 segment pipeline with segment delay of segments as 120ns, 126ns, 121ns, 110ns, 118ns and 120ns respectively. The intermediate buffer delay is 5ns.

Consider that the system is used for performing 100 tasks.

1. What is the latency of non-pipeline system $= 715\,ns$
2. What is the latency of pipeline system $= 131\,ns$
3. What is the throughput of pipeline system $= \frac{100}{(6+100-1)\,131\,ns} = \frac{100}{105 * 131 * 10^{-9}\,s} \simeq 7 * 10^{6}/sec$
4. What is the throughput of pipeline system in ideal case

$\hookrightarrow = \frac{1}{131 * 10^{-9}\,sec} = 7.63 * 10^{6}$ per sec

[NAT]

Ans = 33.33%

#Q. The stage delays in a ~~5~~ 4-stage pipeline are 60ns, 50ns, 55ns and 80ns. The last stage (with delay 80ns) is replaced with a functionally equivalent design involving two stages with respective delays 60ns and 35ns. The throughput increase of the pipeline is ______ percent?

$k = 4$

60, 50, 55, 80

$t_p = 80$

$\text{throughput} = \frac{1}{80}$

$k = 5$

60, 50, 55, 60, 35

$t_p = 60$

$\text{throughput} = \frac{1}{60}$

% of throughput increase

$$= \frac{\frac{1}{60} - \frac{1}{80}}{\frac{1}{80}} * 100\%$$

$$= 33.33\%$$

[NAT]

#Q. Consider a 6-stage pipeline with delays 2, 4, 3, 5, 3 and 4 ~~cycles~~ ns. This pipeline is upgraded to a new 8-segment pipeline in which each segment delay is 2 ~~cycle~~ ns.

1. How much time is saves using new pipeline over old one for 100 tasks?
2. What is the speed up of new pipeline as compared to old pipeline for 100 tasks? 3. Ideal speed up

old	new
$k = 6$	$k = 8$
$t_p = \max(2,4,3,5,3,4) = 5\,ns$	$t_p = \max(2,2,2,2,2,2,2,2) = 2\,ns$
$n = 100$	$n = 100$

old	new
$\text{time} = (6 + 100 - 1)\, 5\, ns$	$\text{time} = (8 + 100 - 1)\, 2$
$= 525\ ns$	$= 214\ ns$

1. Time saved $= 525 - 214 = 311\ ns$

2. $\text{speed up} = \dfrac{525}{214} = 2.45$

3. $S_{ideal} = \dfrac{5}{2} = 2.5$

ex:-

Assume a 5 stage pipeline

delays:-

5 ns

4 ns

6 ns

5 ns

4 ns

$$\Rightarrow t_p = \max(5, 4, 6, 5, 4) + 1 = 7\,ns$$

$$t_n = 5+4+6+5+4$$

$$= 24\,ns$$

Buffer ⇒ 1 ns

for 1 operat^n pipeline time $= (k+1-1)t_p = k * t_p$

$$= 5 * 7$$

$$= 35\,ns$$

Note :-

$$k * t_p \geq t_n$$

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when all segments take equal delay and there is no any buffer or register delay then

$$\boxed{t_n = k * t_p}$$

all segments are perfectly balanced

If pipeline processing is implemented on Instruction Cycle

Topic : Instruction Pipeline

Example :-

IF:	Instruction Fetch
ID:	Instruction Decode & Address Calculation
OF:	Operand Fetch
EX:	Execution
WB:	Write Back

2 mins Summary

Topic Pipeline Throughput

Topic Latency

Topic Instruction Pipeline

Happy Learning

THANK - YOU