CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Instruction & Addressing Modes

Lecture No.- 06

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Recap of Previous Lecture

- Topic: Effective Address
- Topic: Branch Instruction
- Topic: Instruction Cycle
- Topic: Fetch Cycle & Execution Cycle
- Topic: Addressing Modes

Topics to be Covered

- **Topic** Addressing Modes
- **Topic** Types of Addressing Modes
- **Topic** CPU Cycle
- **Topic** CPI

Topic : Implied Mode

The opcode definition itself defines the operand

Opcode	Mode	Address

Topic : Immediate Mode

The address field of instruction specifies the operand value

Opcode	Mode	Address

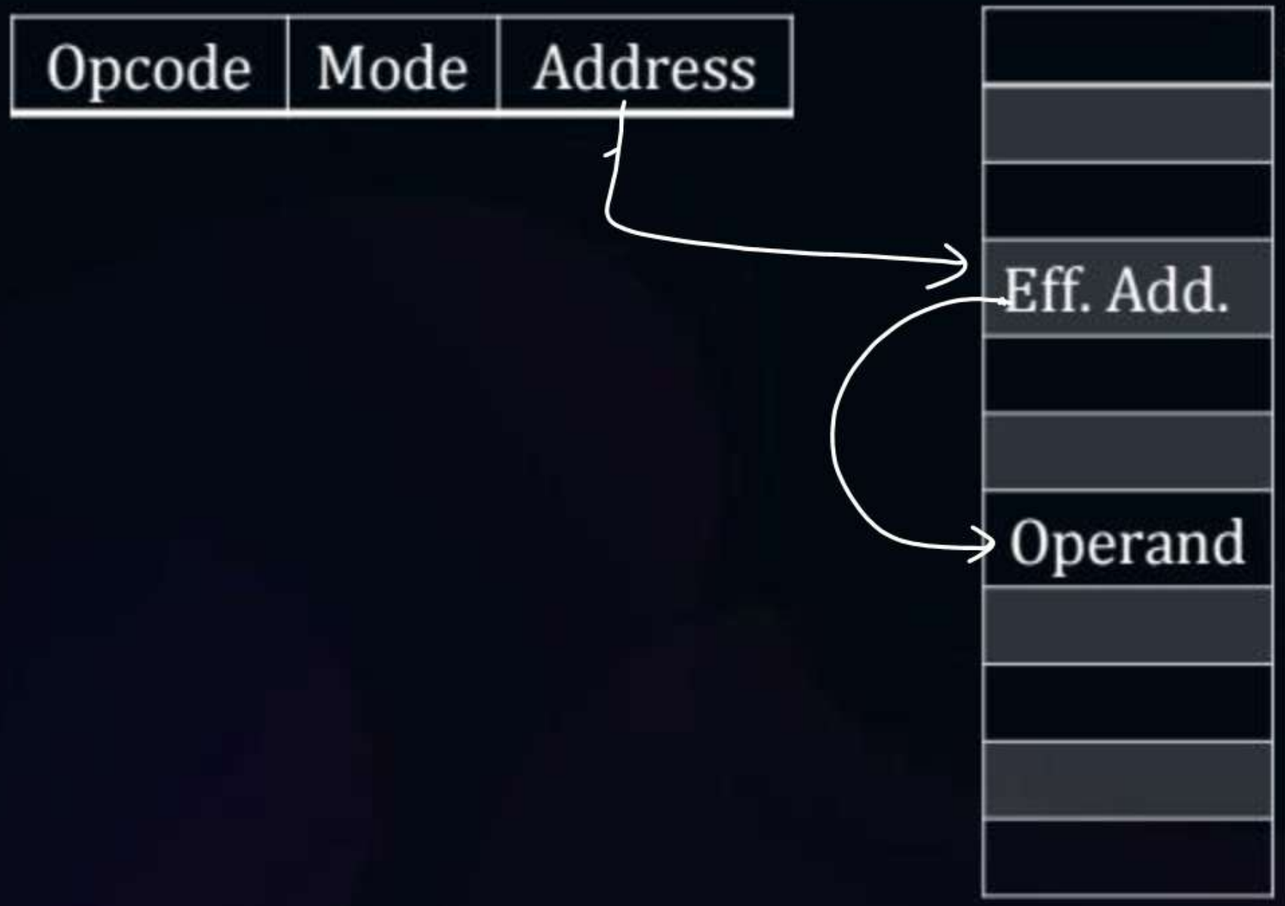
Topic : Direct Mode

The address field of instruction specifies the effective address

Opcode	Mode	Address

Topic : Indirect Mode

The address field of instruction specifies the effective address

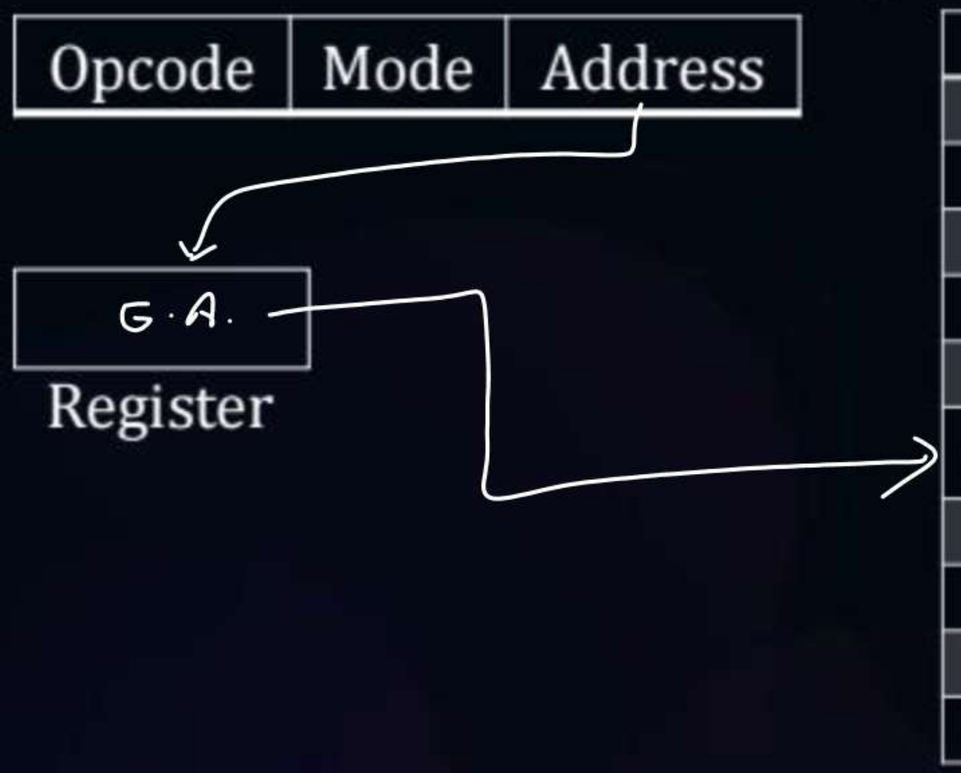


Topic : Register Mode

The address field of instruction specifies a register which holds operand

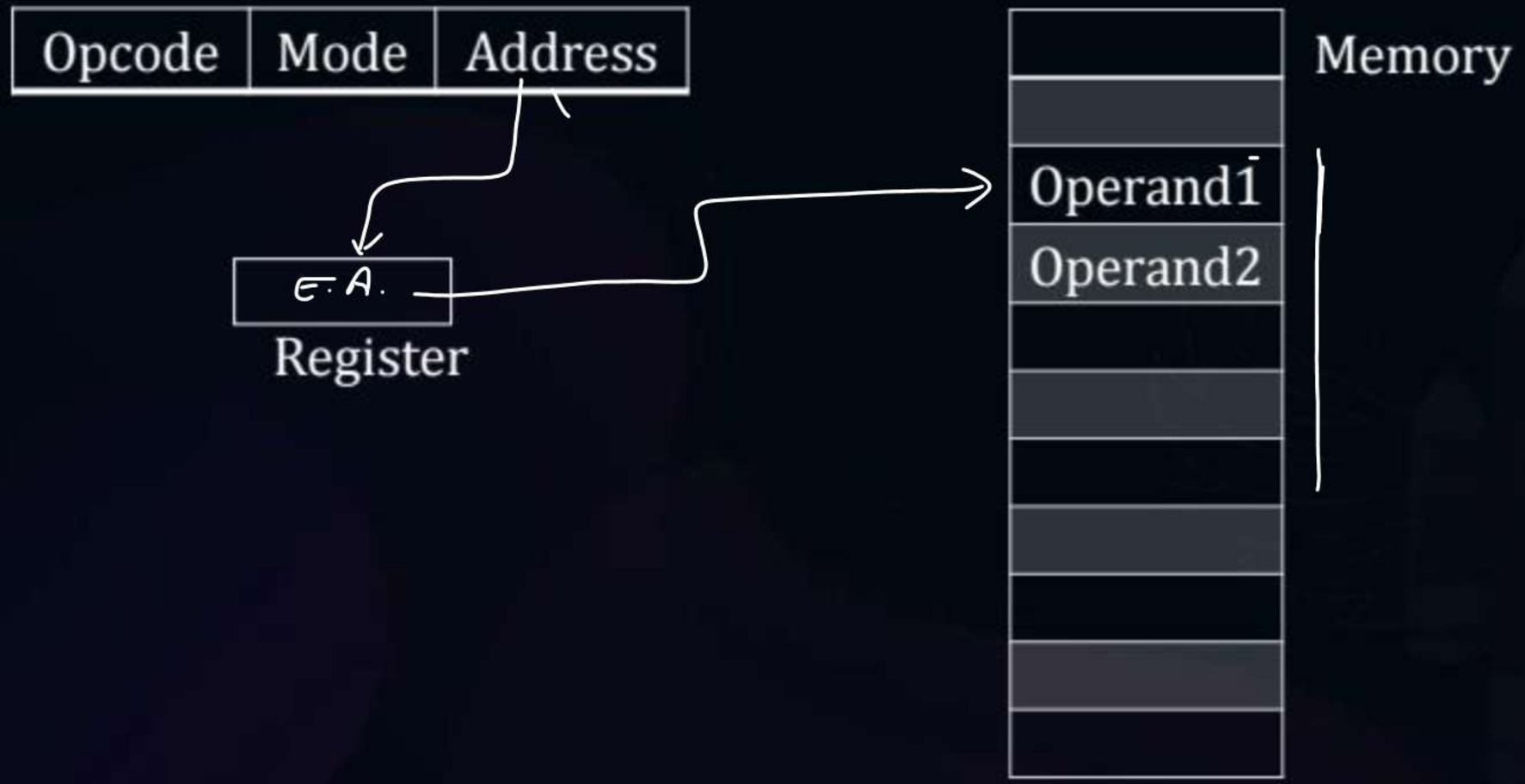
Topic : Register Indirect Mode

The address field of instruction specifies a register which holds operand



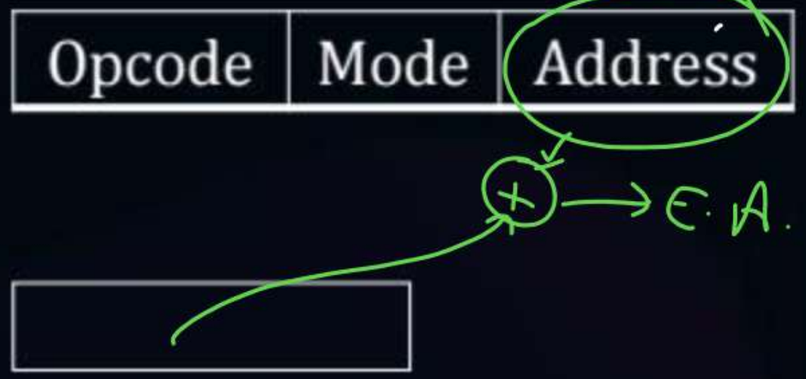
Topic : Autoincrement/Autodecrement Mode

Variant of register indirect mode, in which content of register is automatically incremented or decremented to access a table of content sequentially.



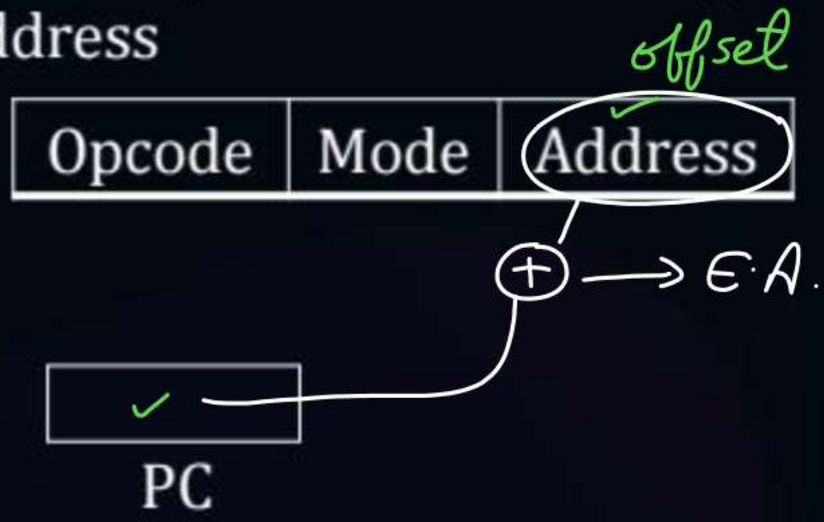
Topic : Indexed Mode

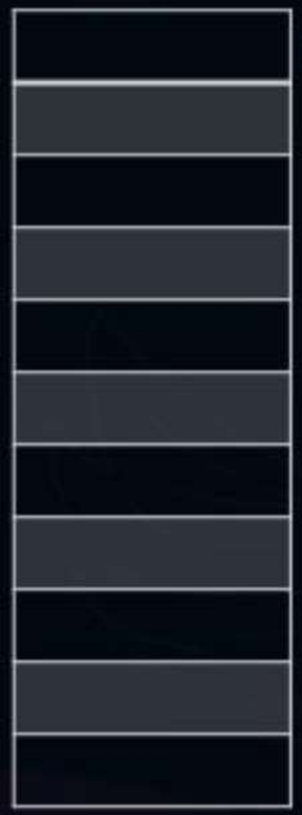
Address part of instruction (base address) is added to index register value to get the effective address



Topic : PC-Relative Mode

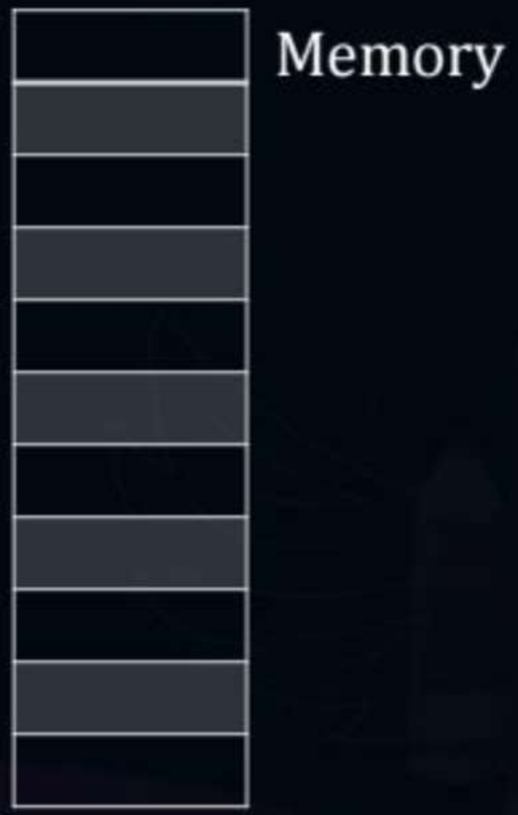
Address part of instruction (offset) is added to PC register value to get the effective address





Topic : Base Register Mode

Address part of instruction (offset) is added to Base register value to get the effective address



Addressing modes

Computable

Computation is needed to calculate E.A.

- Auto inc./dec.
- Indexed
- PC - Relative
- Base Reg. mode

Non-computable

- Implied
- Immediate
- Direct
- Indirect
- Reg. mode
- Reg. indirect

PC-Relative
Base Reg. Mode
} ⇒ used for branch instns &
E.A. ⇒ Target add. of branch

All other modes
except above two
} ⇒ used for computation type instns
they either provide E.A. or operand

Topic : Example

inst^n | opcode | mode | add. = 500 |

add. of memory

	Memory
200	*Opcode* | Mode
201	Address = 500
202	Next Instruction
399	450
400	700
500	800
600	900
702	----------
800	300

Registers

PC = ~~200~~ 202

R500 = ~~400~~ 399

Index Reg.

XR = 100

AC

Mode	Effective Address	Operand
1. Immediate Mode	201	500
2. Direct Mode	500	800
3. Indirect Mode	800	300
4. Register Mode	—	400
5. Register Indirect Mode	400	700
6. Autodecrement Mode (Pre dec)	399	450
7. Indexed Mode	500 + 100 = 600	900
8. PC- Relative Mode	202 + 500 = 702	—

#Q. An instruction is stored at Location 300 with its address field at location 301. The address field has the value 400. A processor register contains the number 150. Evaluate the effective address, if addressing mode is:

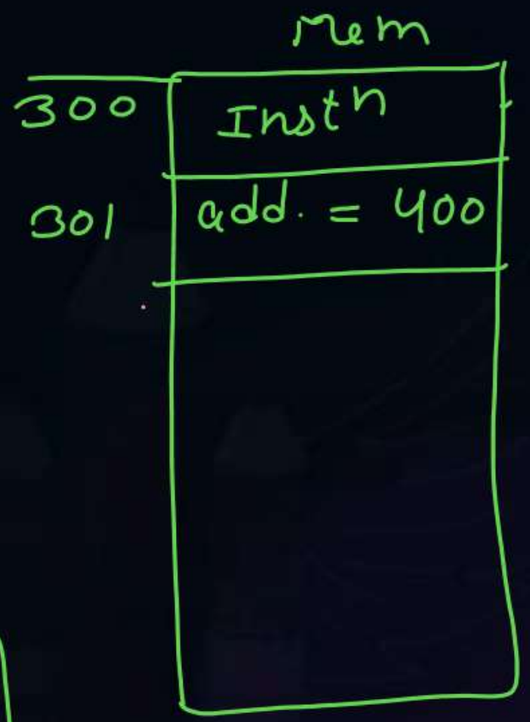
PC = 302

1. Direct ⇒ 400

2. PC-Relative
⇓
302 + 400 = 702

3. Immediate ⇒ 301

4. Register Indirect ⇒ 150



[MCQ]

#Q. In case the code is position independent, the most suitable addressing mode is

A Direct mode

B Indirect mode

C Relative mode

D Indexed mode

[MSQ]

#Q. The addressing mode that permits relocation, without any change whatsoever in the code, is

A Indirect addressing

B Base register addressing

C Indexed addressing

D PC relative addressing

[~~MCQ~~]

#Q. A relative branch mode type instruction is stored in memory at address 300. The branch is made to an address 450.

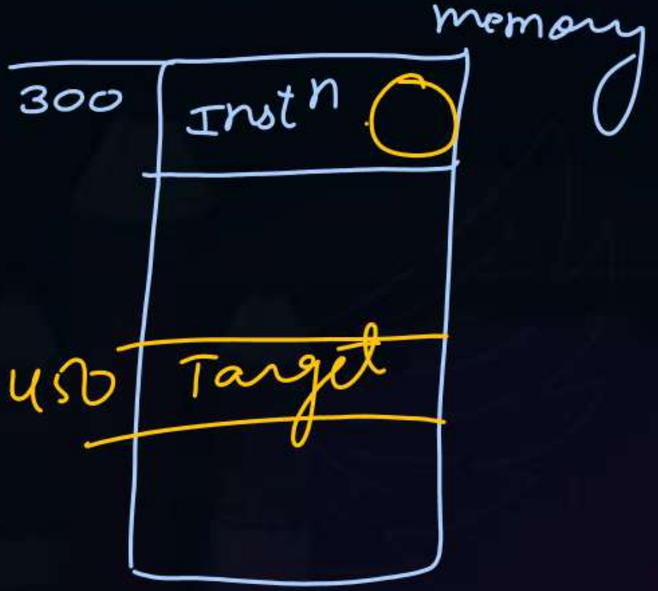
1. What should be the value of relative address field of the instruction? → offset
2. Determine the value of PC before instruction fetch, after the fetch and after execution phase?

Target add. = 450

E.A. = PC + offset

450 = 301 + offset

offset = 149



	PC
Before instⁿ fetch	300
After —11—	301
After execution phase	450

[MCQ]

LW R1, 20(R2);

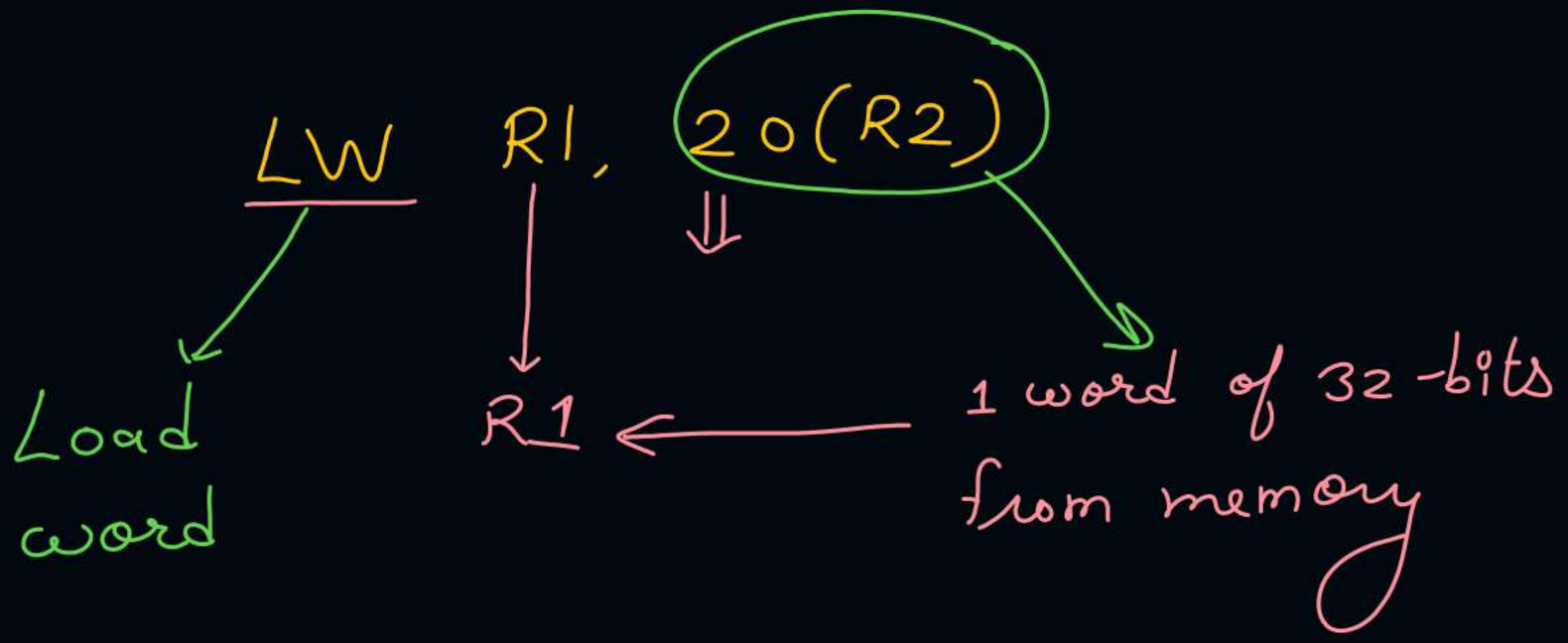
#Q. Consider a hypothetical processor with an instruction of type LW R1, 20(R2); which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for operand in memory?

A ✗ Immediate Addressing

B ✗ Register Addressing

C ✗ Register indirect and scaled addressing

D ✓ Base indexed addressing



E.A. = 20 + R2

20 → base add.

R2 → index Reg.

[NAT]

Ans = 4

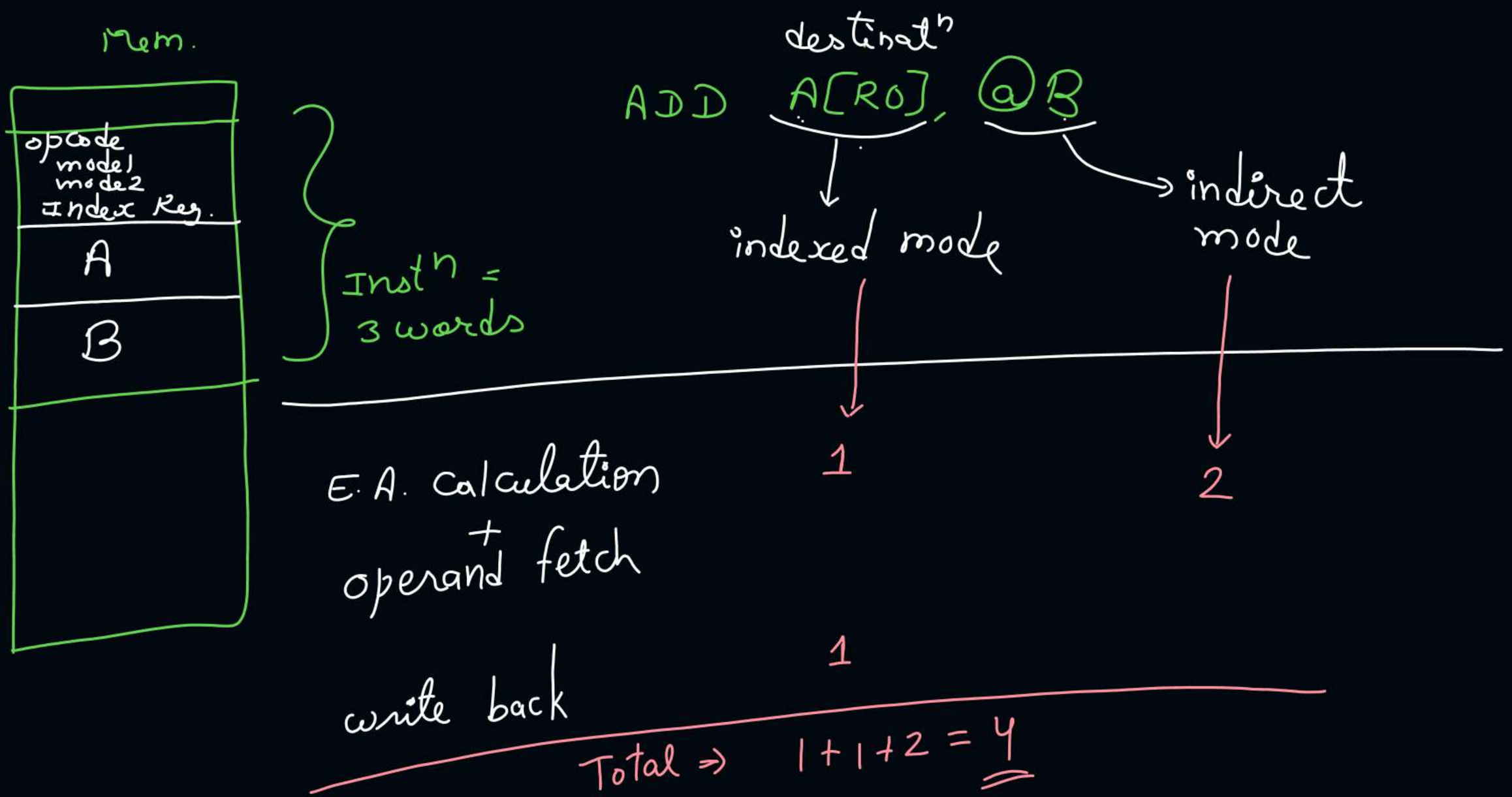
#Q. Consider a three word machine instruction

ADD A[R0], @B

The first operand (destination) "A[R0]" uses indexed addressing mode with R0 as the index register. The second operand (Source) "@B" uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is_____.

↳ no. of memory references


Mem.
opcode
mode1
mode2
Index Reg.
A
B
Instⁿ = 3 words
destinatⁿ
ADD A[R0], @B
indexed mode
indirect mode
1
2
E.A. calculation
+
operand fetch
1
write back
Total ⇒ 1+1+2 = 4

[NAT]

#Q. Consider a 6-words instruction, which is of the following type:

Opcode	Mode1	Mode2	Address1	Address2

The first operand (destination) uses register indirect mode and second operand uses indirect mode. Assume each operand is of size 2 words, each address is of 2 words and main memory takes 50ns for 1 byte access. Further assume that the opcode denotes addition operation which copies result of addition of 2 operands. One word size is 4 bytes. Total time required in:

1. Fetch cycle of instruction
2. Execution cycle of instruction
3. Instruction cycle of instruction

Topic : CPU

micro-operation

1. CPU Cycle ⇒ Time required to perform one smallest operation in CPU
2. CPU Clock rate ⇒ no. of CPU cycles per unit of time | clock rate = $\frac{1}{\text{cycle time}}$
3. CPI (Cycle Per Inst^{n}) ⇒ No. of CPU cycles to execute one inst^{n}.
4. Execution Time

1 inst^{n} execution time = CPI * 1 cycle time

or

Avg Inst^{n} execution time = CPI * $\frac{1}{\text{clock rate}}$

or

n inst^{ns} execution time $= n * CPI * 1$ cycle time

or

$= n * CPI * \frac{1}{\text{clock rate}}$

Topic : MIPS

1. CPU Cycle
2. CPU Clock rate
3. CPI
4. Execution Time

Topic : Average CPI

Consider computing the overall CPI for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 200 MHz

Instruction Category	Number of Instructions	No. of cycles per Instruction
ALU	48	1
Load & Store	10	3
Branch	39	4
Other	3	5

[NAT]

#Q. Consider two processors P1 and P2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P1. If the clock frequency of P1 is 1GHz, then the clock frequency of P2 (in GHz) is _____?

2 mins Summary

Topic Addressing Modes

Topic Types of Addressing Modes

Topic CPU, CPI, MIPS

Data path

Happy Learning

THANK - YOU