CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Pipeline Processing

Lecture No.- 04

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Recap of Previous Lecture

Topic Instruction Pipeline

Topic Stall Cycles

Topic Pipeline Hazard

Topics to be Covered

- Topic: Instruction Pipeline
- Topic: Pipeline Hazard
- Topic: Operand Forwarding
- Topic: Branch Prediction

Topic : Instruction Pipeline

IF: Instruction Fetch
ID: Instruction Decode & Address Calculation
OF: Operand Fetch
EX: Execution
WB: Write Back

Topic : Instruction Pipeline

Clock Cycles

Instructions	1	2	3	4	5	6	7	8	9	10	11	12	13	14
I1														
I2														
I3														
I4														
I5														
I6														
I7														
I8														
I9														

Topic : Pipeline Hazards

Situations that prevent the next instruction from being executing during its designated clock cycle

Topic : Pipeline Hazards

1. Structural Hazard / Resource Conflict
2. Data Hazard / Data Dependency
3. Control Hazard / Branch Difficulty

Topic : Structural Hazard

2 different segments try to use same resource at same time.

Topic : Data Hazard or Data Dependency

Result of an instruction is used as input in next

Soln

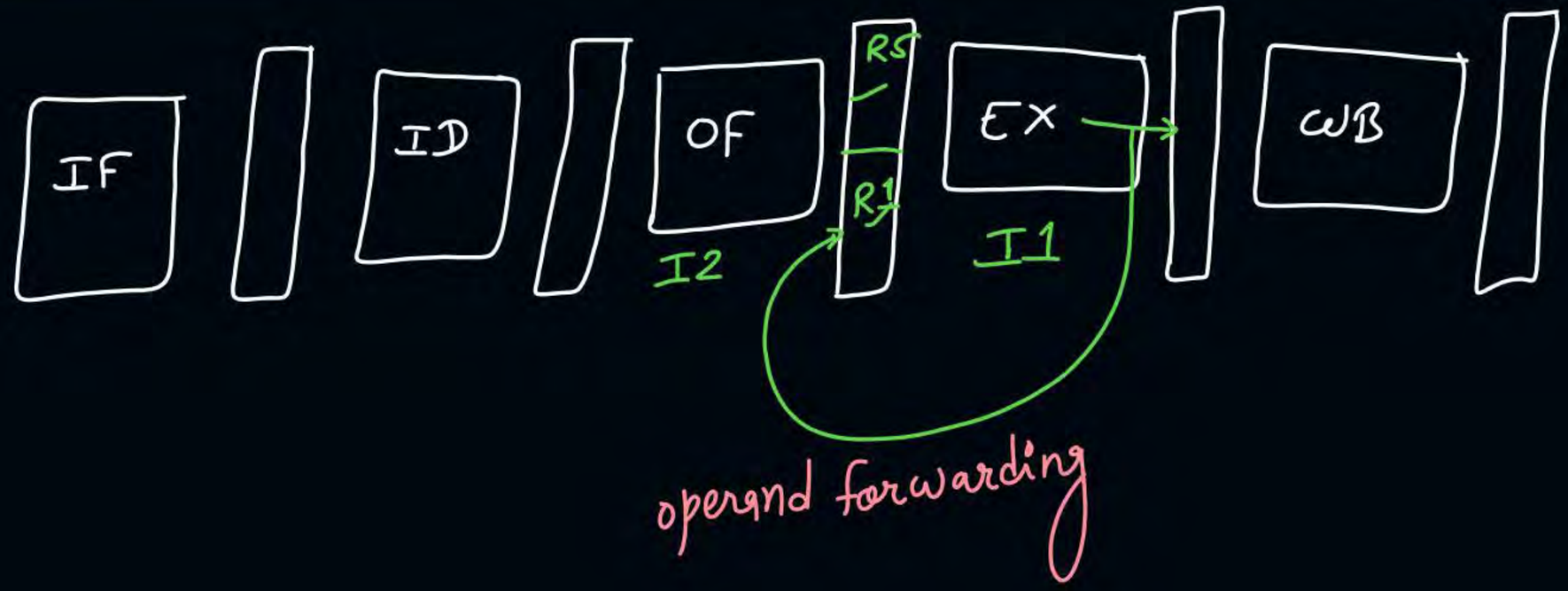
- S/w
  - delayed load
- H/w
  - → H/w interlock
  - → operand forwarding (bypassing)

operand forwarding :-

I1 :- R1 ← R2 + R3

I2 :- R4 ← R1 * R5

1	2	3	4		
IF	ID	OF	EX →	WB	
	IF	ID	OF →	EX	WB



Data dependency :-

1. ALU to ALU $\Rightarrow$ no stalls

2. memory to ALU

$R3 \leftarrow M[add.]$ Load inst^n

$R4 \leftarrow R3 * R2$

3. ALU to Memory

$R4 \leftarrow R6 * R5$

$M[add.] \leftarrow R4$ store inst^n

stalls

Topic : Control Hazard or Branch Difficulty

Hazards because of branch instructions

Soln

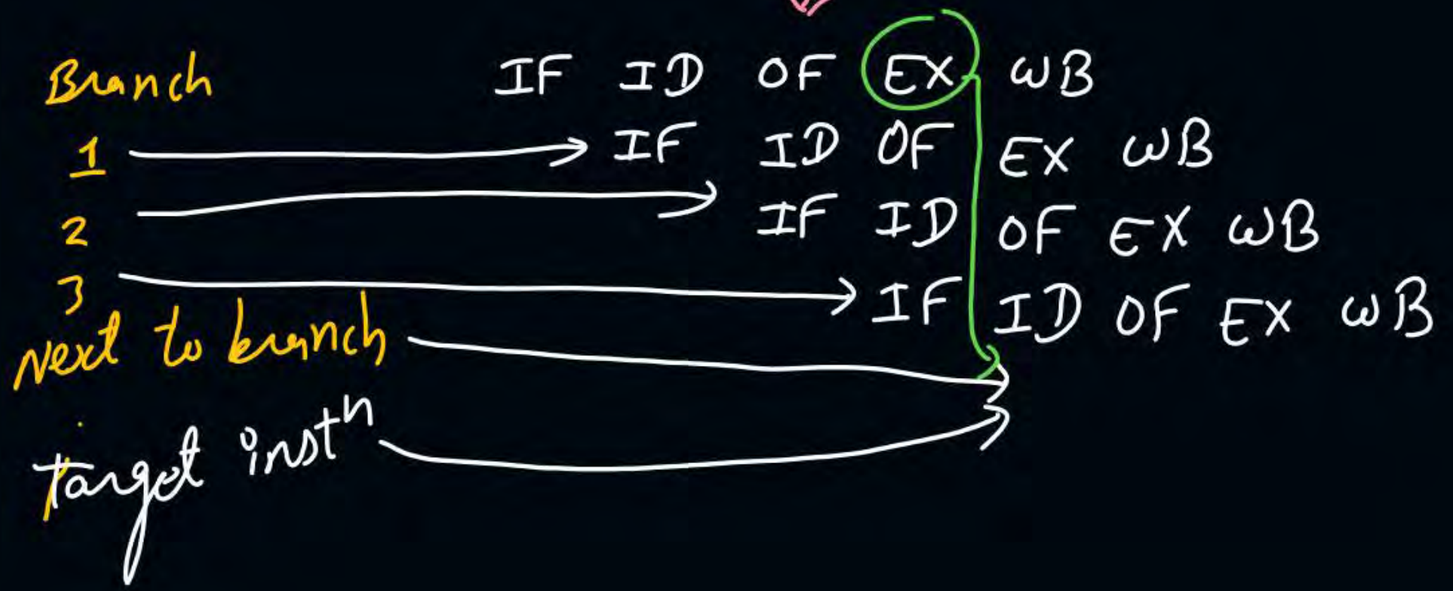
- Software solution
  - delayed branch (by compiler)
    - Insert no-operation or independent instns after branch instn.
- Hardware solution
  - Branch prediction

Delayed branch:-

I1 :- Branch inst^n
I2 :- next to branch inst^n
:
!

delayed branch →

Branch inst^n
inst^n 1
2
3
Next to branch inst^n



[NAT]

Ans = 8

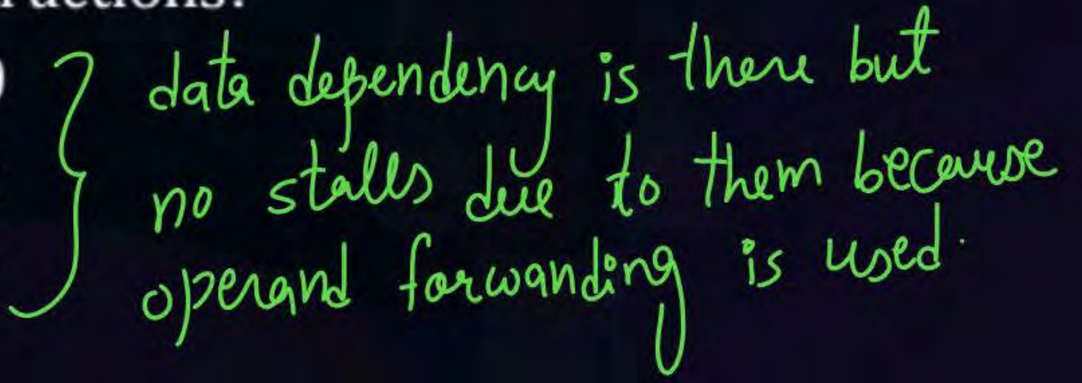
#Q. Consider a pipelined processor with the following four stages:

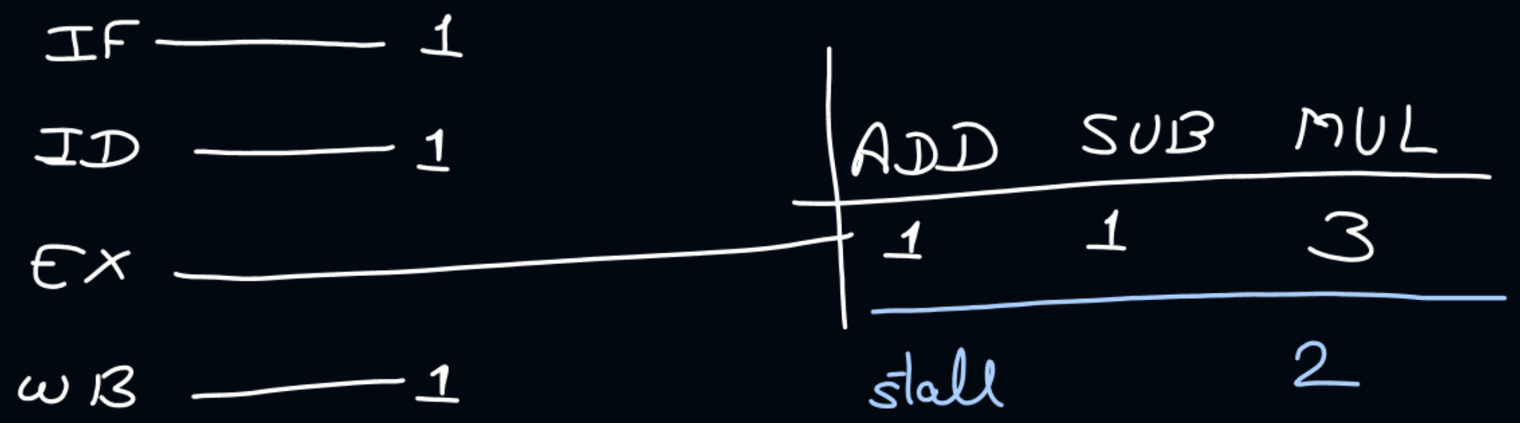
IF: Instruction Fetch ID: Instruction Decode and Operand Fetch

EX: Execute WB: Write Back

The IF, ID, and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycle in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD R2, R1, R0	R2←R1+R0
MUL R4, R3, R2	R4←R3*R2
SUB R6, R5, R4	R6←R5-R4





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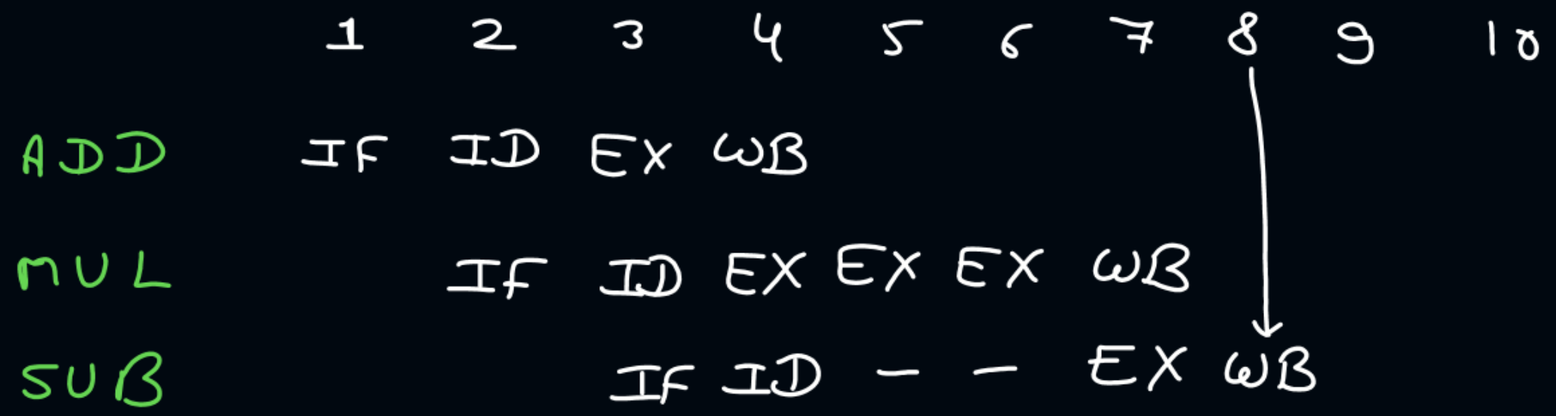
no. of cycles without any hazard = $k+n-1 = 4+3-1 = 6$

stalls due to structural hazard for 1 MUL instⁿ = 2

Total = 8



Ans = 8

#2) In prev. Quest^{n}, prog. has following inst^{n}

ADD
MUL
MUL
ADD
MUL
SUB
MUL

no. of cycles = —— ?

$n = 7$
$k = 4$

w/o hazard = $4 + 7 - 1 = 10$

stalls for MUL inst^{ns} = $4 * 2 = 8$

Total = $\underline{\underline{18}}$ Ans.

#Q)

no any data or branch hazard

IF — 1

ID — 1

OF — 1

EX — 1

WB — 1

	ADD	SUB	MUL	DIV
	1	2	3	5
stall		1	2	4

no. of instns		stalls
ADD type	= 4	0
SUB —11—	= 5	5*1=5
MUL —11—	= 2	2*2=4
DIV —11—	= 3	3*4=12
Total	= 14	

w/o hazard, no. of cycles = 5+14−1 = 18

stalls for structural hazard = 5+4+12 = 21

39

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Ans = 219

GATE – 2018

#Q. The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards.

The number of clock cycles required for completion of execution of the sequence of instruction is _____?

IF — 1

ID — 1

OF — 1

PO — 3

WB — 1

	40	35	25
	3	2	1
stalls	40*2=80	35*1=35	0

Total = 115

w/o hazard = 5 + 100 − 1 = 104

stalls = 115

219

[NAT] GATE-PYQ

Ans = 23

#Q. Consider a 4-stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below:

	S_1	S_2	S_3	S_4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?

For (i = 1 to 2) (I1; I2; I3; I4)

	1	2	3	4	5	6	7	8	9	10	11	12
I1	S1	S1	S2	S3	S4							
I2			S1	S2	S2	S2	S3	S3	S4	S4		
I3				S1	S1	-	S2	-	S3	-	S4	S4 S4
I4						S1	-	S2	S2	S3	S3	- - S4 S4
I1							S1	S1	-			

[NAT]

	S1	S2	S3	S4
I1	2	3	4	5
I2	3	6	8	10
I3	5	7	9	13
I4	6	9	11	15
I1	8	10	12	16
I2	9	13	14	18
I3	11	14	15	21
I4	12	16	18	23

	S_1	S_2	S_3	S_4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

2 mins Summary

Topic Instruction Pipeline

Topic Pipeline Hazard

Topic Operand Forwarding

Topic Branch Prediction

Happy Learning

THANK - YOU