CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Instruction & Addressing Modes

Lecture No.- 02

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Recap of Previous Lecture

Topic Instruction

Topic ISA

Topic Types of Instruction

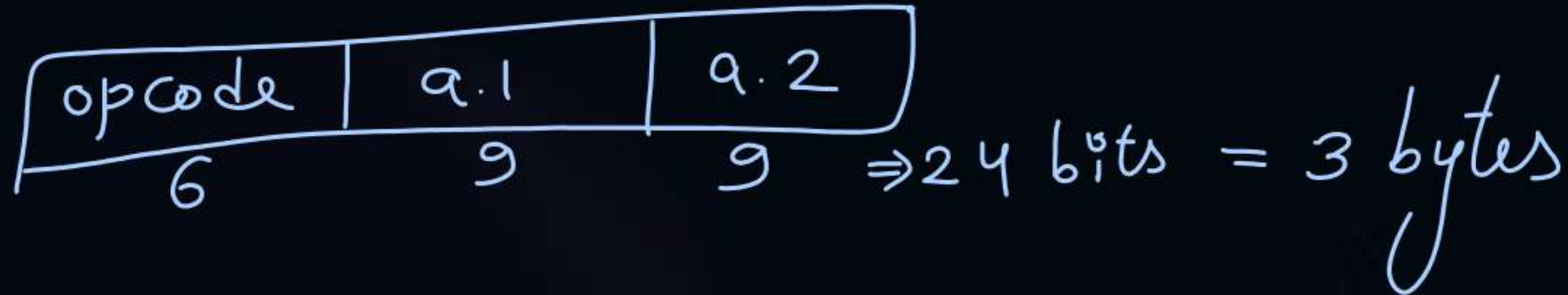# Topics to be Covered

Topic Instruction

Topic Multiple Instruction Support

#Q. Consider a digital computer which supports $\boxed{64}$ 2-address instructions. If address length is 9-bits then the length of the instruction is _____ bits?

opcode	a.1	a.2
6	9	9

$\Rightarrow 24$ bits $= 3$ bytes

#Q. Consider a digital computer which supports (64) 2-address instructions. If address length is 9-bits then the length of the instruction is _____ bits?

In above question: Each instruction must be stored in memory in a byte-aligned fashion. If a program has 200 instructions, then amount of memory required to store the program text is _____ bytes?

memory

8-bits
8-bits
8-bits

1 $inst^n = 3$ bytes

for 200 $inst^{ns} = 200 * 3 = 600$ Bytes
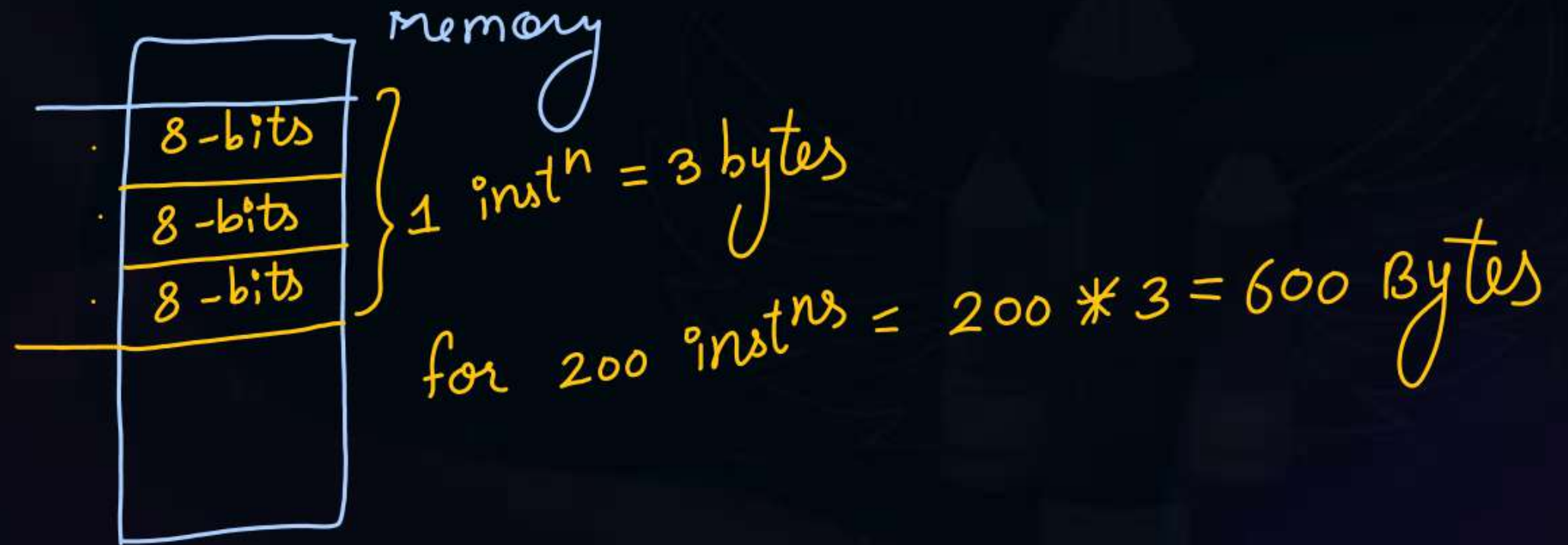
If insts must be stored in byte aligned fashion

& $Inst^n$ size = 12 bits

S0 0	8-bits
S0 1	4-bits
S02	Next instn

} 2 bytes space needed to store 1 instn

$\rightarrow opcode = 5-bits$

#Q. Consider a digital computer which supports ㉜ 2-address instructions. Consider the address length is 8-bits. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 300 instructions, then amount of memory required to store the program text is ____ bytes?
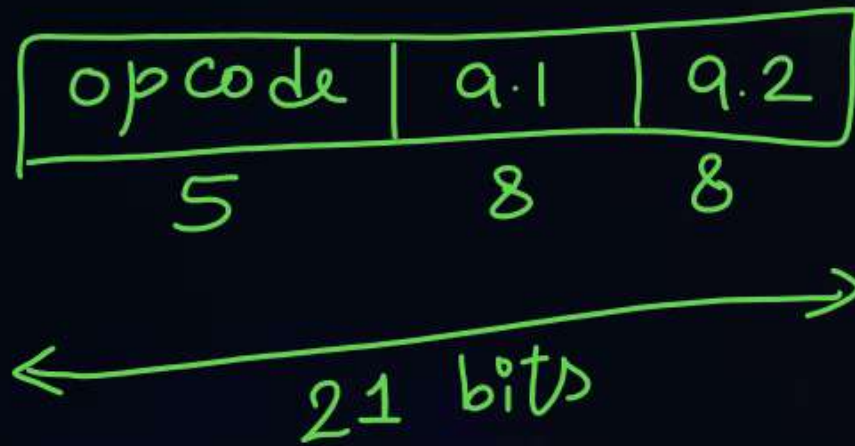
opcode	a.1	a.2
5	8	8

$\xleftarrow{\hspace{3cm}}$
21 bits

spaces required to store 1 instⁿ $= \left\lceil \dfrac{21}{8} \right\rceil$

$= 3$

8-bits
8-bits
5--bits
} 3 bytes
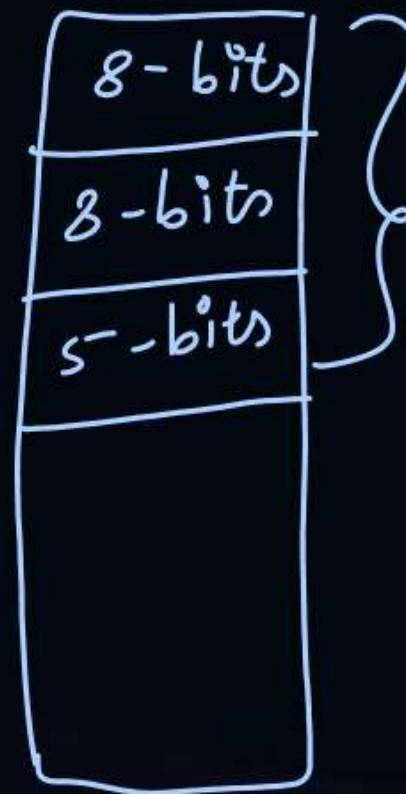
for 300 instⁿˢ $= 300 * 3$
$= 900$ bytes

$\rightarrow$ opcode $= 6$-bits   Ans $= \underline{\underline{24}}$

#Q.   A processor has ⑤⓪ distinct instructions and ⑯ general purpose registers. Each instruction in system has one opcode field, ② register operand field and a 10 bits memory address field. The length of the instruction is ___ bits?

opcode	Reg operand 1	Reg. operand 2	Memory address
6	4	4	10
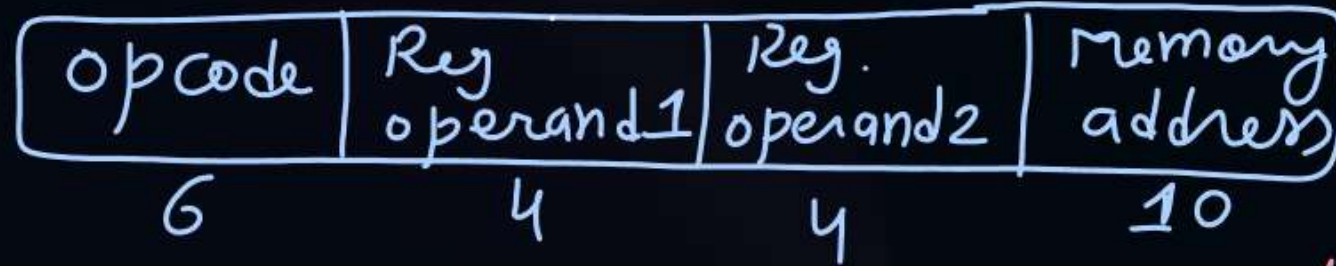
24 bits

R0

□ □
0000   0001

No. of $GPR^s = 16$
⇓
Numbers $\Rightarrow 0000$ to 1111
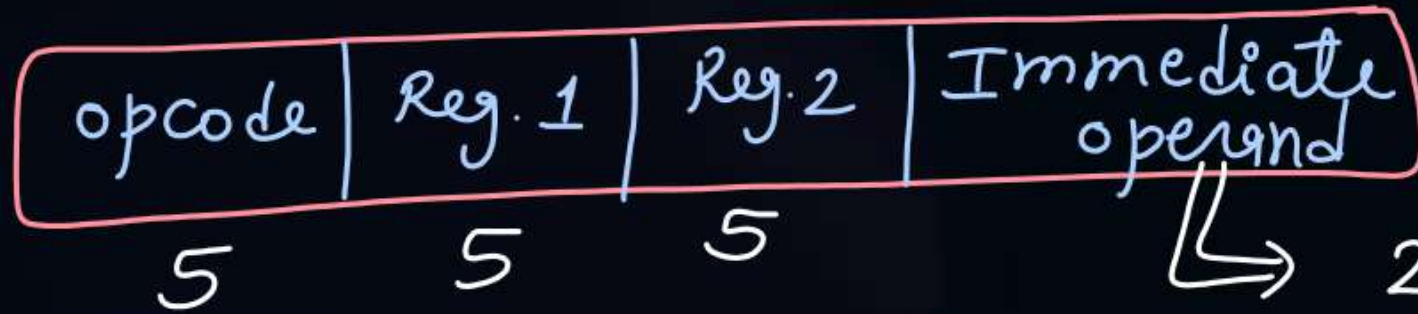
Reg. operand bits $= \lceil \log_2 16 \rceil$

$= 4$ bits

$opcode = 5-bits$

$Reg. \Rightarrow 5-bits$

#Q. A processor has 20 distinct instructions and 32 general purpose registers. A 24- bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ___?

24-bits

opcode	Reg. 1	Reg. 2	Immediate operand
5	5	5	

$24-(5+5+5)$

$= 9 \text{ bits}$

Ans $\Rightarrow$ 0, 511

#Q. A processor has 20 distinct instructions and 32 general purpose registers. A 24- bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ___?

In above question: Assume that immediate operand field is an unsigned number, What is its maximum and minimum value possible?

	Min value	Max value
for unsigned numbers of n-bits	0	$2^n - 1$
___ || ___ 9 bits	0	$2^9 - 1 = 511$

Signed number (n-bits)	Min	Max
sign- magnitude	$-(2^{n-1} - 1)$	$+(2^{n-1} - 1)$
1^s Complement	$-(2^{n-1} - 1)$	$+(2^{n-1} - 1)$
2^s complement	-2^{n-1}	$+(2^{n-1} - 1)$

(P W)

#Q. Consider a system which support only 3 address instructions only, and supports 256B memory. If the instruction size is 40-bits then maximum & minimum number of instruction supported by the system are?

$$\xleftarrow{\hspace{3cm} 40 \hspace{3cm}}$$

Opcode	Add1	Add2	Add3
	8	8	8
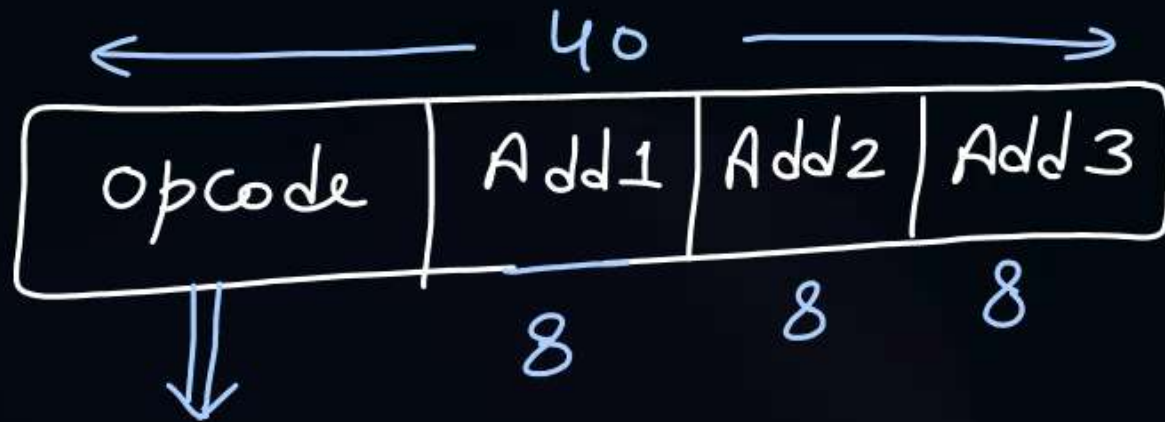
16 bits

$$Max = 2^{16} = 65536$$

$$Min = 1$$

Memory size $= 256B$

No. of cells in memory $= \dfrac{256B}{1B}$

$$= 256 = 2^8$$

Memory add. $= 8$ bits

(P W)

$$Ans = 4$$

#Q. Consider a computer which supports only 2-address and 1-address instructions. Each instruction is of 6-bits and each address is of 2-bits. If there are 3 2-address instructions supported by the system then maximum number of 1-address instructions supported by system is?

2-add. insth

$\longleftarrow \quad 6 \quad \longrightarrow$

opcode	a.1	a.2
2	2	2

1-add. insth

$\longleftarrow \quad 6 \quad \longrightarrow$

opcode	a.1
4	2

$\longleftarrow 2 \longrightarrow \longleftarrow 2 \longrightarrow$
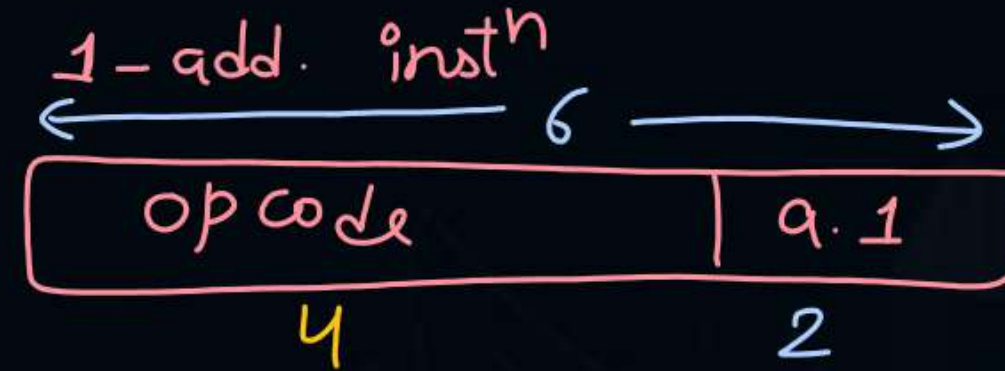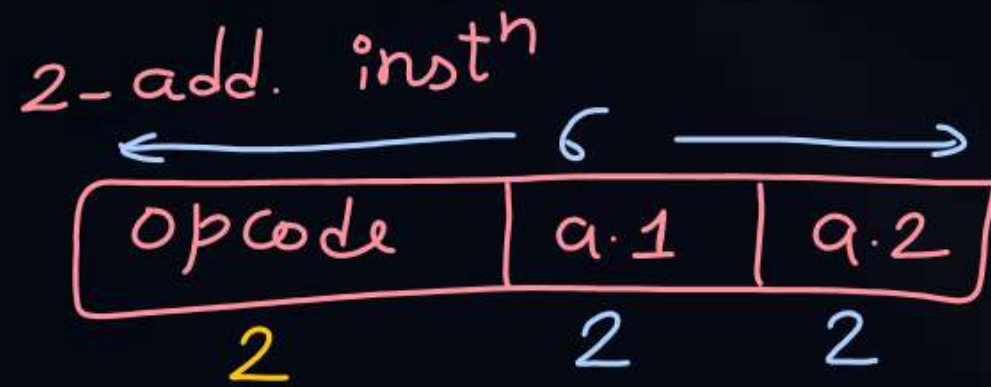
max opcodes $= 2^2 = 4 \ (00, 01, 10, 11)$

used opcodes $= \quad 3 \ (\underline{ex:- \ 00, 01, 10})$

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unused opcodes $= \quad 1 \quad (remaining :- 11)$

$$\Downarrow \quad \swarrow$$

11 00

11 01

11 10

11 11

max 1 add. inst^{ns}

An inst^n comes to CPU for execution

101011

Interpretation
for CPU

as 2-add. inst^n

10	10	11
opcode	add.1	add.2

as 1-add. inst^n

1010	11
opcode	add.1

Inst^n	type
000101	2-add. inst^n
001111	___ '' ___
01 1010	2 add. inst^n
10 1110	2 add. inst^n
11 0001	1-add. inst^n

How to solve Question :-

2-add. inst^n

$$\xleftarrow{\hspace{3cm}} 6 \xrightarrow{\hspace{2cm}}$$

opcode	a.1	a.2
2	2	2
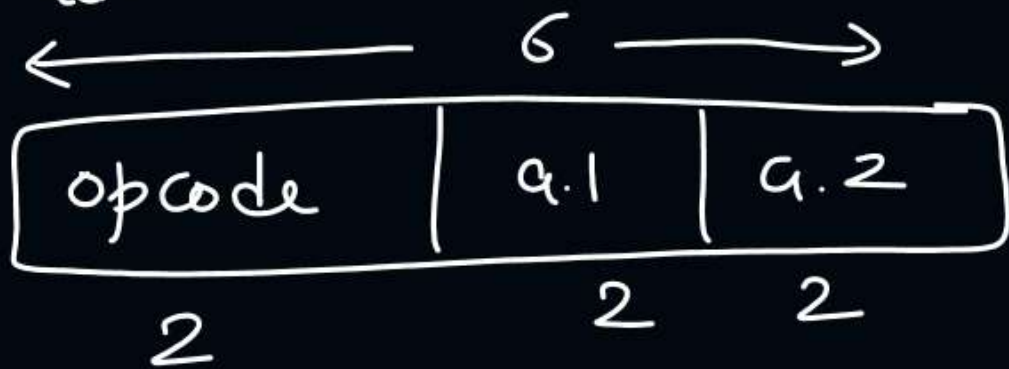
max opcodes $= 2^2 = 4$

used opcodes $= \qquad 3$

unused opcode $= \quad 1$

1-add. inst^n

$$\xleftarrow{\hspace{4cm}} 6 \xrightarrow{\hspace{1cm}}$$

opcode	a.1
4	2

$$\xleftrightarrow{2} \quad \xleftrightarrow{2}$$
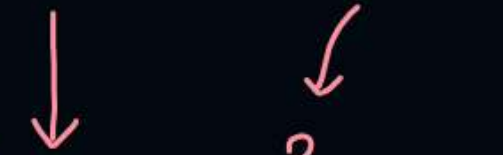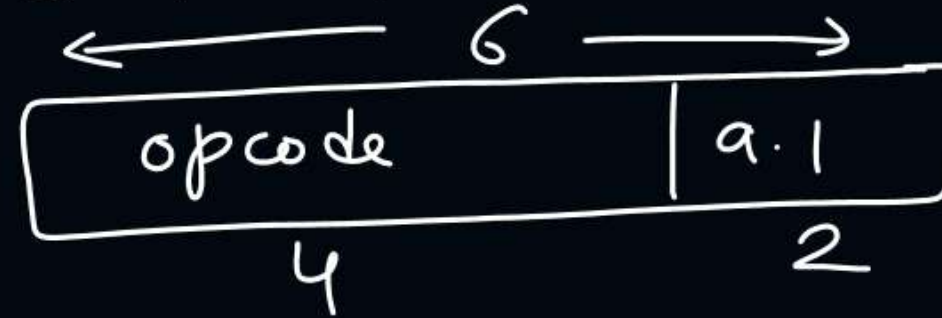
max $= \underline{1} * 2^2 = 4$

1-add. insth^{n}s

used 2-add. inst^{ns}	unused opcode	Max 1-add. inst^{ns}
4	$4-4 = 0$	$0 * 2^2 = 0$ ← only 2-add. inst^{ns} supported
3	$4-3 = 1$	$1 * 2^2 = 4$
2	$4-2 = 2$	$2 * 2^2 = 8$
1	$4-1 = 3$	$3 * 2^2 = 12$
0	$4-0 = 4$	$4 * 2^2 = 16$ → only 1-add. inst^{ns} supported

#Q. Consider a computer which supports only 2-address and 1-address instructions. Each instruction is of 6-bits and each address is of 2-bits. If there are 3 2-address instructions supported by the system then maximum number of 1-address instructions supported by system is?
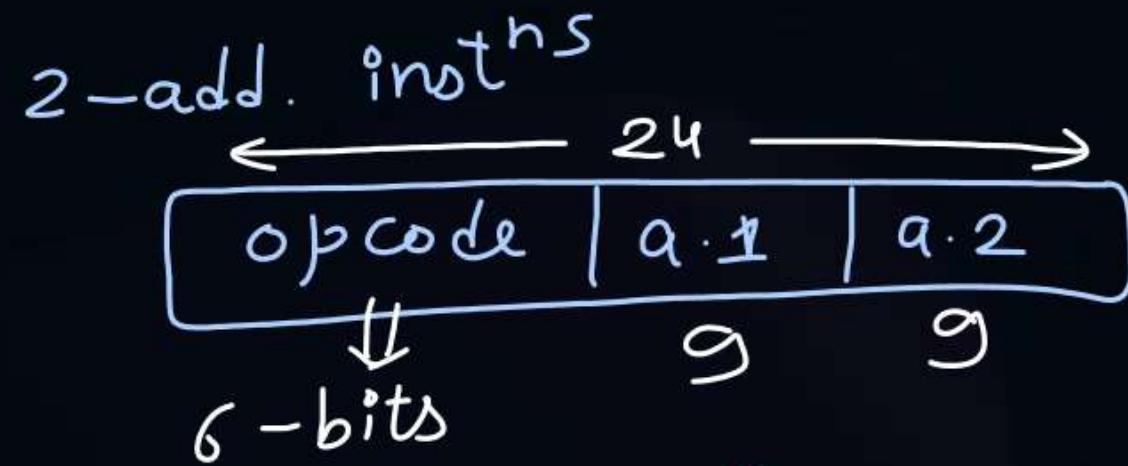
In above instruction what is the range of number of 1-address instructions ~~supported~~?
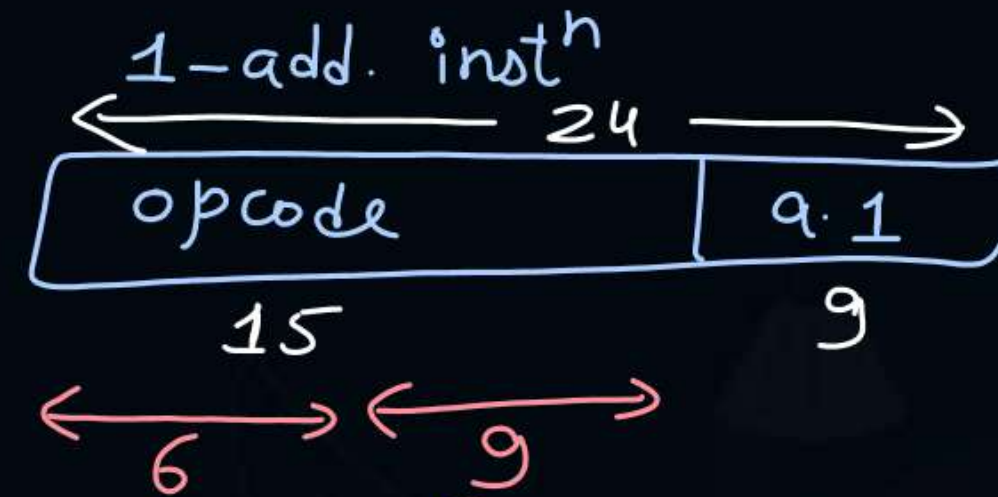   used?

$$\min \Rightarrow 1$$
$$\max \Rightarrow 4$$

$$\text{Range} \Rightarrow 1 \text{ to } 4$$

#Q. Consider a system with 24-bit instructions and 9-bit addresses. If there are 57 2-address instructions then maximum how many 1-address instructions can be formulated in the system?
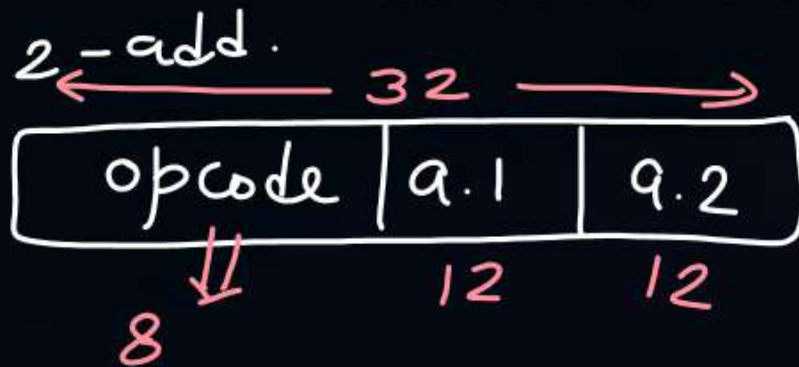
2-add. $inst^{ns}$

$\xleftarrow{\hspace{2cm}} 24 \xrightarrow{\hspace{2cm}}$

| opcode | a.1 | a.2 |

6-bits   9   9

1-add. $inst^{h}$

$\xleftarrow{\hspace{3cm}} 24 \xrightarrow{}$

| opcode | a.1 |

        15   9

$\xleftarrow{} 6 \xrightarrow{} \xleftarrow{} 9 \xrightarrow{}$

Max opcodes $= 2^{6} = 64$

used opcodes $= \quad 57$
_____
unused opcodes $= \quad 7$
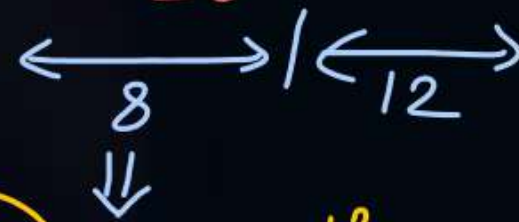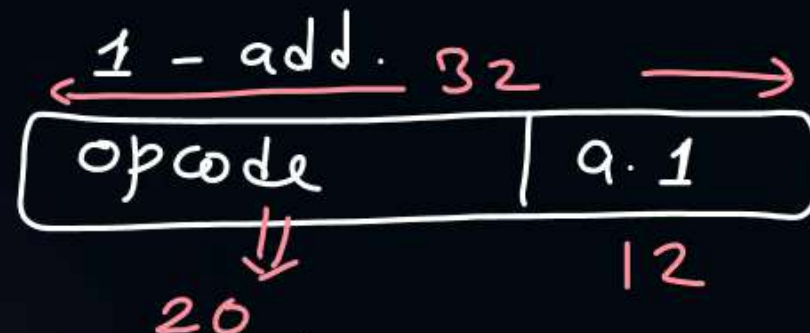
Max 1-add. $= 7 * 2^{9} = 3584$
$inst^{ns}$

#Q. Consider a system with 32-bit instructions and 12-bit addresses. If there are 254 2-address instructions then maximum how many 1-address instructions can be formulated in the system?
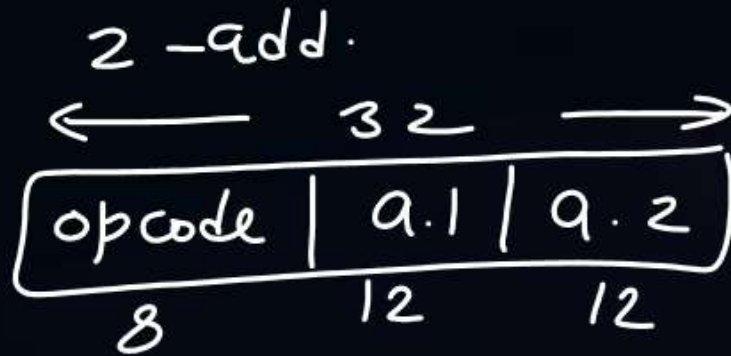
2-add.

$\xleftarrow{\hspace{1cm}} 32 \xrightarrow{\hspace{1cm}}$

opcode	a.1	a.2

8 ⇊   12   12

$\max = 2^8 = 256$

used $= 254$

$\dfrac{\text{used}}{\text{unused}} = 2$

1 - add. $\xleftarrow{\hspace{0.5cm}} 32 \xrightarrow{\hspace{0.5cm}}$

opcode	a.1

20 ⇊   12

$\xleftarrow{\hspace{0.3cm}} 8 \xrightarrow{\hspace{0.3cm}} / \xleftarrow{\hspace{0.3cm}} 12 \xrightarrow{\hspace{0.3cm}}$

⇊

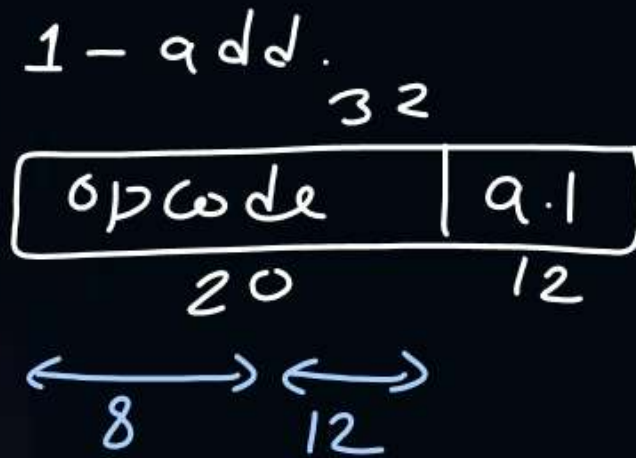$2 * 2^{12} = 2^{13} = \underline{8192}$ Ans.

#Q. Consider a system with 32-bit instructions and 12-bit addresses. If there are 254 2-address instructions and 8000 1-address instructions then maximum how many 0-address instructions can be formulated?

2 - add.

$\longleftarrow$ 32 $\longrightarrow$

| opcode | a.1 | a.2 |

8   12   12

$$max = 2^8 = 256$$
$$\frac{used \quad\quad = 254}{unused \quad = 2}$$

1 - add.

32

| opcode | a.1 |

20   12

$\longleftrightarrow$ $\longleftrightarrow$
8   12

$$max = 2 * 2^{12} = 8192$$
$$\frac{used \quad\quad\quad = 8000}{unused \quad = 192}$$

0 - add.

32

| opcode |

32

$\longleftrightarrow$ $\longleftrightarrow$
20   12
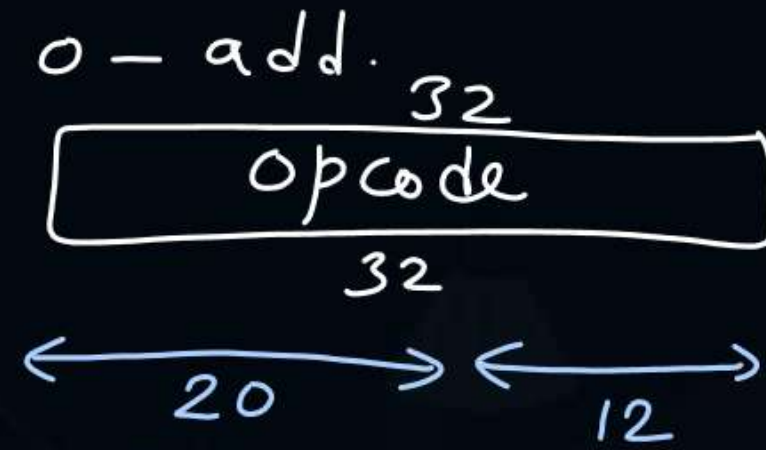
$$max = 192 * 2^{12} = 786432 \quad Ans.$$

#Q.   Consider a system which supports 3-address and 2-address instructions both. It has 30-bit instructions with 8-bit addresses. If there are 'x' 3-address instructions then maximum how many 2-address instructions can be formulated?

#Q. Consider a system which supports 2-address and 1-address instructions both. It has 24-bit instructions with 10-bit addresses. If there are 4096 1-address instructions then maximum how many 2-address instructions can be formulated?

#Q. Consider a system with 16-bits instructions and 64 CPU registers. The System supported 2 types of instructions: Type-A and Type-B.

Type-A instructions have an opcode, one register operand and one immediate operand of 3-bits

Type-B instructions have an opcode, and 2 register operands.

If there are 10 Type-B instructions supported by the system then maximum how many Type-A Instructions supported by the system?

#Q. Consider there are 3 types of instructions in system:
1. Register Operand instructions: One opcode and 2 registers
2. Memory Operand instructions: One opcode, 1 register and 1 memory address
3. Immediate Operand Instructions: One opcode, 1 register and 1 immediate operand

Number of registers = 64

Number of bits in immediate operand = 10-bits

Memory size = 512Mbytes (byte addressable)

Total Instructions:

1. Reg Operand type: 10

2. Memory Operand type : 12

3. immediate Operand type : 4

Maximum and Minimum instruction length are?

Topic Instructions

Topic Multiple Instruction Support