CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

CPU & Control Unit

Lecture No.-02

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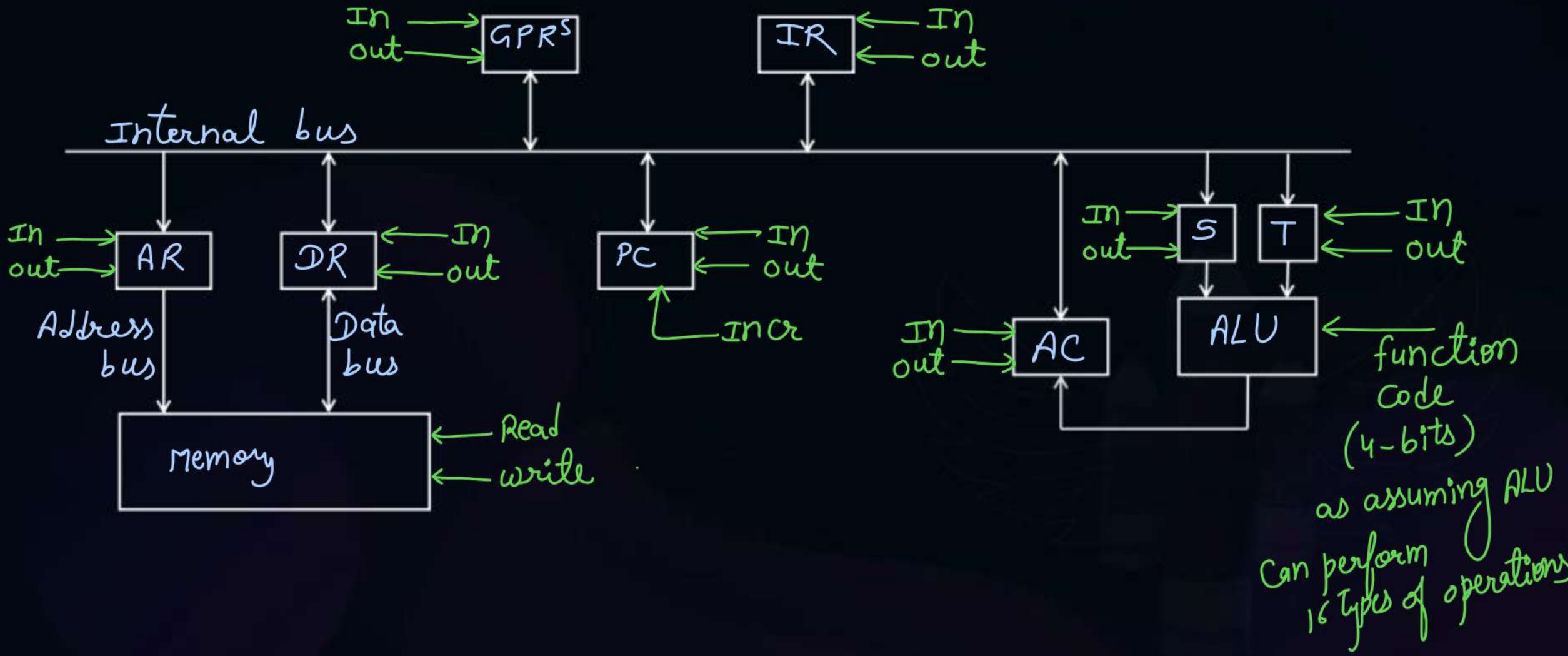
Recap of Previous Lecture

- **Topic** CPU
- **Topic** MIPS
- **Topic** Data Path

Topics to be Covered

- Topic: Datapath
- Topic: Control Unit Organization
- Topic: Hardwired Control Unit
- Topic: Micro-Programmed Control Unit
- Topic: RISC vs CISC

Topic : Datapath



Topic : Control Unit

Instⁿ fetch :-

$AR \leftarrow PC$ — PC_{out}, AR_{IN}

$DR \leftarrow M[AR]$ — $AR_{out}, Mem_{read}, DR_{IN}$

$IR \leftarrow DR, PC \leftarrow PC + 1$ — $DR_{out}, IR_{IN}, PC_{INCR}$

Control Variable:- Name of control signal or line.

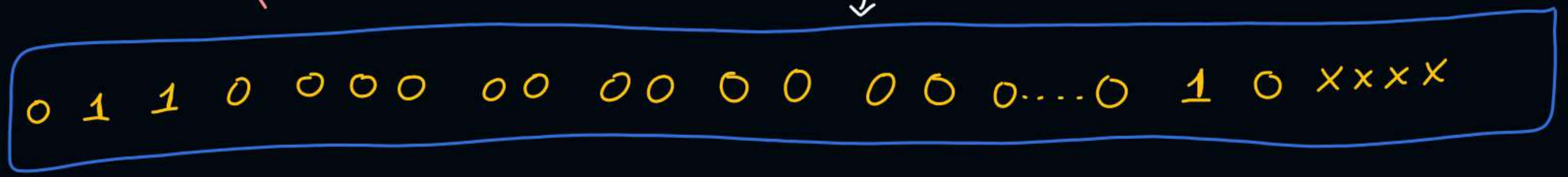
Control word:- collection of all control signals generated by control unit at a time.

AR		DR		PC			IR		S		T		AC		GPRs	Mem.		ALU
In	out	In	out	In	out	Incr	In	out	In	out	In	out	In	out	.....	R	W	function code (4-bits)

for micro-operation: AR ← PC

Control word

DR ← M[AR]



Topic : Control Unit Organization

How control unit generates control word.

2 types :-

1. Hardwired Control unit
2. Micro-programmed control unit

Topic : Hardwired Control Unit

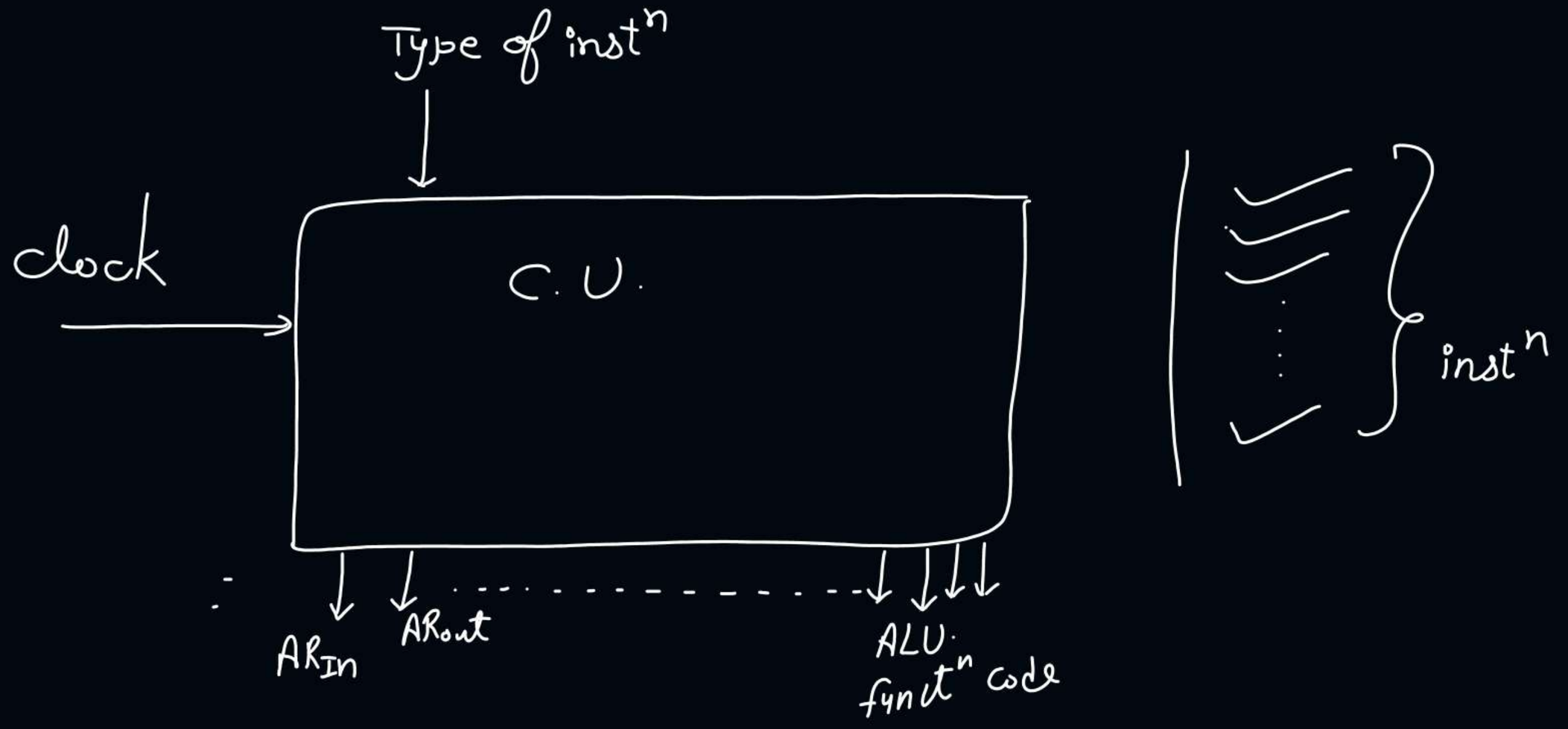
How Control signals are generated

Control logic is implemented with Gates, flip-flops, decoders and other digital circuits.

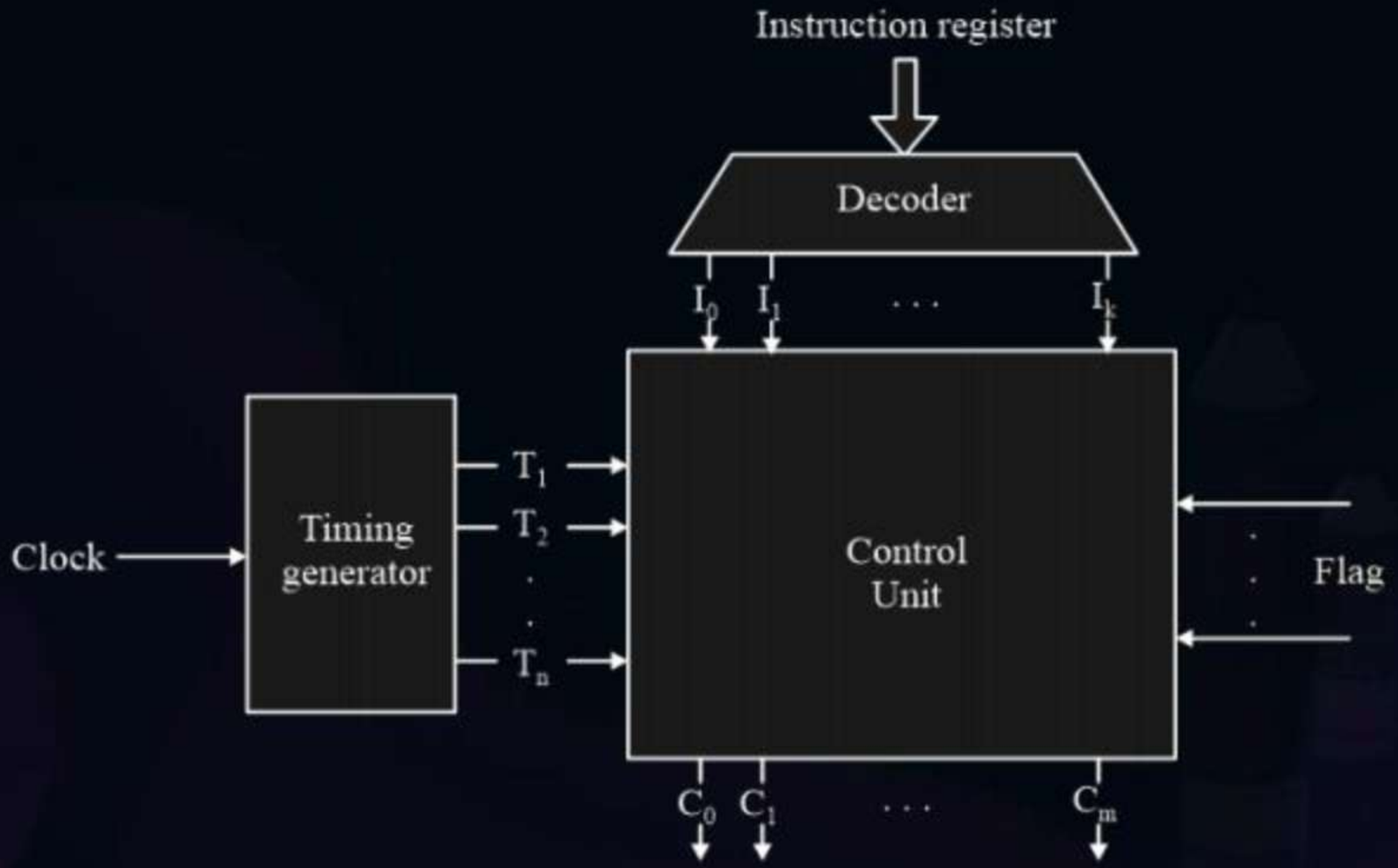
Advantage: Can be optimized to produce a faster mode of operation.

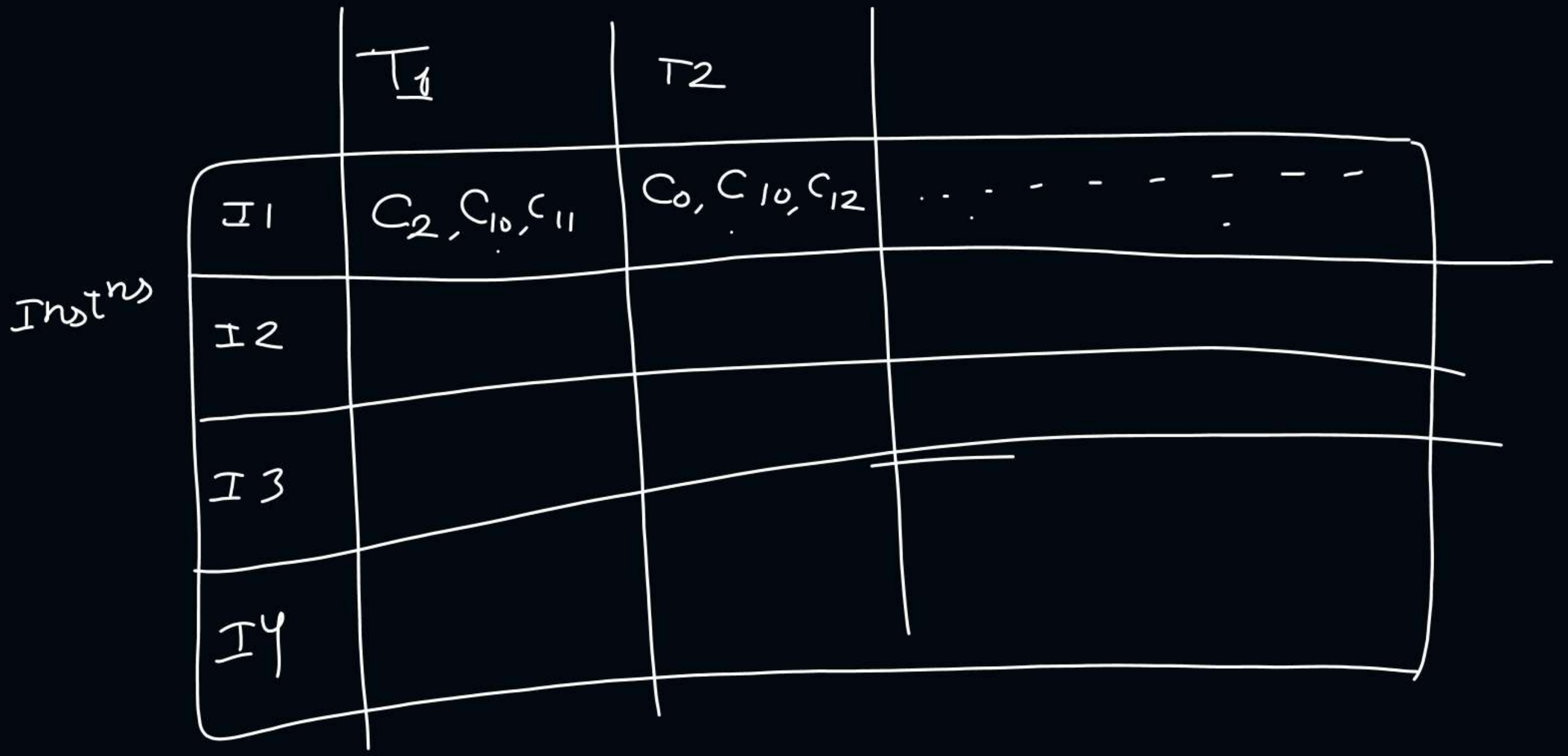
Disadvantage: 1. Rearranging the wires among various components is difficult.
(updation in control logic is difficult)

2. It is used for simple CPU designs.
(Difficult to implement hardwired control unit for complex CPU)


Type of inst^n
clock
C.U.
AR_In
AR_out
ALU funct^n code
inst^n

Topic : Hardwired Control Unit




T1
T2
Instns
I1
C2, C10, C11
C0, C10, C12
I2
I3
I4

[MCQ]

$S_{10} = T_2(I_2 + I_3) + T_3 I_4 + T_4(I_1 + I_3) + T_5 (I_2 + I_4)$

#Q. A hardwired CPU uses 10 control signals S1 to S10, in various time steps T1 to T5, to implement 4 instructions I1 to 14 as shown below:

	T1	T2	T3	T4	T5
I1	S1, S3, S5	S2, S4, S6	S1, S7	S10	S3, S8
I2	S1, S3, S5	S8, S9, S10	S5, S6, S7	S6	S1, S3, S10
I3	S1, S3, S5	S7, S8, S10	S2, S6, S9	S10	S1, S3
I4	S1, S3, S5	S2, S6, S7	S5, S10	S6, S9	S10

Which of the following pairs of expressions represent the circuit for generating control signals S5 and S10 respectively?

$I_1 T_1 + I2\,T1 + I3\,T_1 + I_4 T_1 + I2\,T_3 + I_4 T_3$

$T_1 (I_1 + I_2 + I_3 + I_4) + (I_2 + I_4) T_3 \Rightarrow T_1 + (I_2 + I_4) T_3$

A

$S5 = T1+I2\cdot T3$ and
$S10 = (I1 + I3)\cdot T4 + (I2 + I4)\cdot T5$

B

$S5 = T1+(I2+I4)\cdot T3$ and
$S10 = (I1 + I3)\cdot T4 + (I2 + I4)\cdot T5$

C

$S5 = T1+(I2+I4)\cdot T3$ and
$S10 = (I1 + I3 + I4)\cdot T2 + (I2 + I3)\cdot T4+(I2+I4)\cdot T5$

D

$S5 = T1+(I2+I4)\cdot T3$ and
$S10 = (I2 + I3)\cdot T2+I4\cdot T3+(I1 + I3)\cdot T4+(I2+I4)\cdot T5$

Topic : Micro-Programmed Control Unit

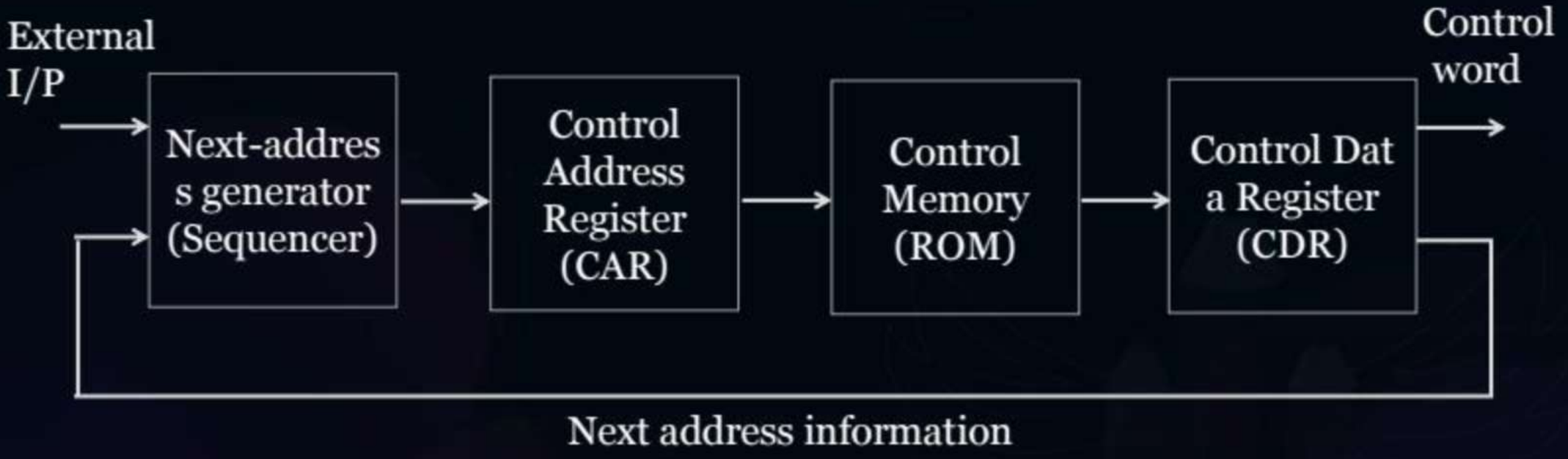
Control logic is implemented with micro-programs.

Advantage: 1. Updating the control logic is easy.
2. Easier to implement for complex CPUs

Disadvantage: Slower than hardwired control unit.

All required control words are stored in a memory inside C.U.. whenever whichever control word is to be required, that is read from mem. & is sent to components to perform micro-operation.

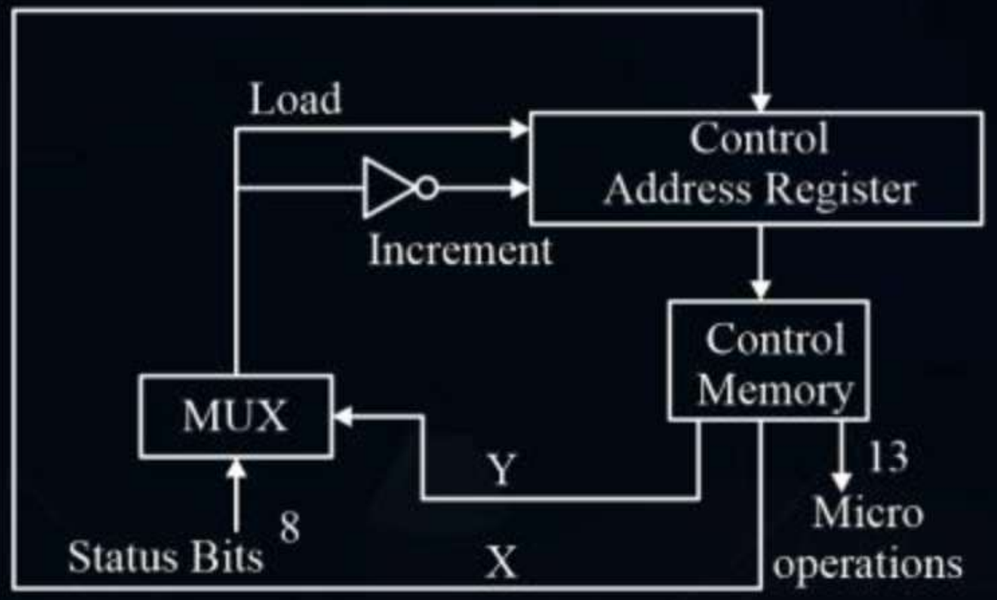
Topic : Control Word Sequencing



[MCQ]

#Q. The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX.

How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?



A 10, 3, 1024

B 8, 5, 256

C 5, 8, 2048

D 10, 3, 512

[NAT]

#Q. A control unit generates 120 control signals, which are divided into 6 groups of mutually exclusive signals as below:

Group1 = 30

Group2 = 13

Group3 = 12

Group4 = 3

Group5 = 27

Group6 = 35

How many bits can be saved by using vertical micro-programmed control unit as compared to horizontal one?

[NAT]

#Q. A micro-programmed control unit is required to generate a total of 25 control signals. Assume that during any microinstruction at most 2 control signals are active. Minimum number of bits required in the control word to generate the required control signals will be?

Topic : RISC vs CISC

S. No.	RISC (Reduced Instruction-Set Computer)	CISC (Complex Instruction-Set Computer)
1.	Less Number of Instructions Supported	More Number of Instructions
2.	Fixed Length Instructions	Variable Length Instructions
3.	Simple Instructions	Complex Instructions
4.	Simple and less number of addressing Modes	Complex and More number of addressing Modes
5.	Easy to implement using hardwired control unit	Difficult to implement using hardwired control unit

Topic : RISC vs CISC

S. No.	RISC (Reduced Instruction-Set Computer)	CISC (Complex Instruction-Set Computer)
6.	One Cycle per instruction	More than one cycle per instruction
7.	Register-to-Register arithmetic operation only	Register-to-Memory & Memory-to-Register arithmetic operations possible
8.	More Number of Registers	Less Number of Registers

[MCQ]

#Q. Consider the following processor design characteristics.

I. Register-to register arithmetic operations only

II. Fixed-length instruction format

III. Hardwired control unit

Which of the characteristics above are used in the design of a RISC processor?

A. I and II only

B. II and III only

C. I and III only

D. I, II and III

2 mins Summary

Topic Datapath

Topic Control Unit Organization

Topic Hardwired Control Unit

Topic Micro-Programmed Control Unit

Topic RISC vs CISC

Happy Learning

THANK - YOU