Computer Organization & Architecture

Pipeline Processing

DPP: 1

Q1 Consider a non-pipelined system which takes 100ns to perform a task. The same task can be performed using a 6-segment pipeline with cycle time of 20ns. The speed up of pipeline (rounded up to 2 decimal place) for 1000 tasks is _____?

Q2 Consider 6 segment pipeline with segment delay of segments as 140 picoseconds, 109 picoseconds, 160 picoseconds, 154 picoseconds, 125 picoseconds and 170 picoseconds respectively. Pipeline uses an intermediate buffer after every segment with a delay of 10 picoseconds. Speed up of pipeline (rounded up to 2 decimal place) for processing of 1000 tasks is _____ ?

Q3 Consider a non-pipelined processor with a clock rate of 5GHz and an average cycle of 4 per instruction. The same processor is upgraded to a pipelined processor with 6 stages and the clock speed of 4GHz. Assume that there are no stalls in the pipeline. MIPS count of the pipeline processor in ideal condition and MIPS count of non-pipeline processor respectively are?

(A) 4000, 5000 (B) 4000, 1250

(C) 1250, 4000 (D) 5000, 1250

Q4 The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 nanoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionally equivalent design involving two stages with respective delays 450 and 350 nanoseconds. The throughput increase of the pipeline is _____ %?

Q5 Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delay for FI, DI, FO, EI and WO are 9 ns, 8 ns, 12 ns, 10 ns and 11 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 20 instructions I1, I2, I3, ...,I20 is executed in this pipelined processor. Instruction I7 is only the branch instruction, and its branch target is I17. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is _____?

Q6 Consider a program which contains 500 instructions I1, I2 , I3 .. I500. Further consider a 5-stage pipeline with stages as: Instruction Fetch, Decode, Operand Fetch, Execution and Write-Back. The program contains 3 branch instructions, information of those given in a table below. The number of cycles required to execute this program in the given pipeline is _____?

Branch Instruction	Target Instruction	Branch Taken or Not
I9	I49	Taken
I234	I381	Not Taken
I412	I497	Taken

Q7 Consider a non-pipelined processor with a clock rate of 5GHz and an average cycle of 5 per instruction. The same processor is upgraded to a pipelined processor with 6 stages and the clock speed of 4GHz. Assume that there are no stalls in the pipeline. The speed up (rounded up to 2 decimal place) achieved in the pipeline for 1000 instructions is _____?

Answer Key

Q1	4.98~4.98
Q2	4.74~4.74
Q3	(B)
Q4	60~60
Q5	234~234
Q6	390~390
Q7	3.98~3.98

Hints & Solutions

Q1 Text Solution:

Speed up = (1000 × 100) / [(6 + 1000 – 1) × 20]

= 4.975

= 4.98

Q2 Text Solution:

Pipeline cycle time Tp = max(segment delays) + register delay

= max (140, 109, 160, 154, 125, 170) + 10

= 180 picoseconds

One task execution time in non-pipeline system = Sum of all segment delays

= 140 + 109 + 160 + 154 + 125 + 170

= 858 picoseconds

Speed up = (858 × 1000) / [(6 + 1000 – 1) × 180]

= 4.74

Q3 Text Solution:

MIPS = $\frac{\text{Clock rate}}{\text{CPI} \times 10^6}$

CPI in pipeline in ideal conditions = 1.

MIPS of Pipeline = $\frac{4\ \text{GHz}}{1 \times 10^6}$ = 4000

MIPS of non-pipeline = $\frac{5\ \text{GHz}}{4 \times 10^6}$ = 1250

Q4 Text Solution:

For old pipeline the 4 stages are having delays: 800, 500, 400 and 300 nanoseconds.

Old pipeline cycle time = max (800, 500, 400, 300) = 800 nanoseconds

Old pipeline throughput = 1/800

New pipeline has 5 stages with delays: 450, 350, 500, 400 and 300 nanoseconds.

New pipeline cycle time = max (450, 350, 500, 400, 300) = 500 450, 350, 500, 400 and 300

Old pipeline throughput = 1/500

% of increase in throughput = (1/500 – 1/800) / (1/800) * 100%

= 60%

Q5 Text Solution:

Pipeline cycle time Tp= max (9,8,12,10,11) + 1 = 13ns

Number of instructions executed (From I1 to I7 and I17 to I20) = n = 7 + 4 =11

Number of pipeline cycles without stalls due to branch = k + n – 1 = 5 + 11 – 1 = 15

Number of stalls due to branch = 4 – 1 = 3

Total cycles = 15 + 3 = 18

Total execution time = 18 * 13 = 234 ns

Q6 Text Solution:

Instruction I234 is not taking branch hence there is no any jump, hence all instructions are executed.

Number of instructions executed from I1 to I9 = 9

Number of instructions executed from I49 to I412 = 412 – 49 + 1 = 364

Number of instructions executed from I497 to I500 = 500 – 497 + 1 = 4

Total = 9 + 364 + 4 = 377

Number of cycles needed to execute 377 instructions without any stalls = 5 + 377 – 1 = 381

Number of stall cycles needed due to 3 branch instructions = 3 × (4 – 1) = 9

Total cycles needed = 381 + 9 = 390

Q7 Text Solution:

Non pipeline cycle time = 1/5GHz = 0.2nanoseconds

1 operation execution time in non-pipeline = 5 * 0.2 = 1 nanoseconds

Pipeline cycle time = 1/4GHz = 0.25 nanoseconds

Speed up = $\frac{1\times1000}{(6+1000-1)\times0.25}$

= 3.98