# CS & IT

## ENGINERING

# COMPUTER ORGANIZATION AND ARCHITECTURE

Basics of COA



Lecture No.- 02

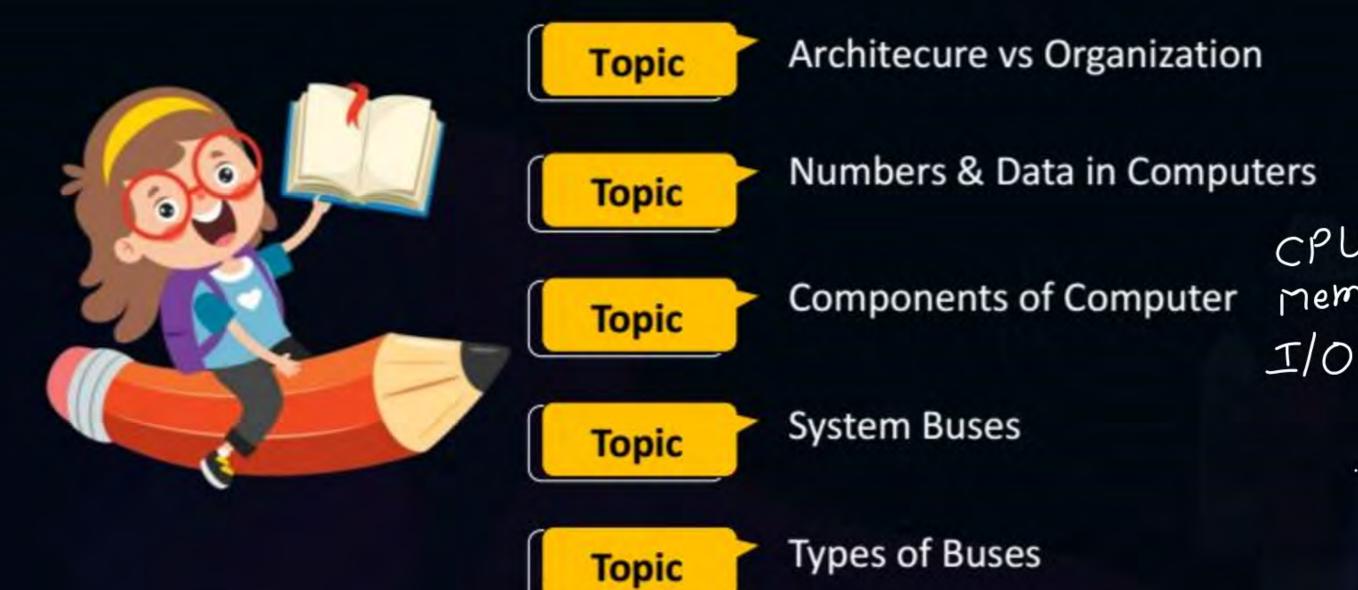
### **Recap of Previous Lecture**



CPU

mem.





## **Topics to be Covered**









#### **Topic: CPU Registers**



small memories inside CPU to carry out

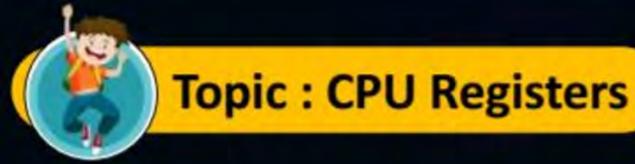
processing

CPU

RAM

Regam

values





#### **CPU Register**

- General Purpose Registers (GPRs) ⇒ Used for any
- Special Purpose Registers

Used for specific purpose

work.

(denoted by

RO, R1, R2,....)



#### **Topic: CPU Registers**



#### **CPU Register**

- General Purpose Registers (GPRs)
- Special Purpose Registers
- Accumulator (AC)
- Program Counter (PC)
  - Instruction Register (IR)
  - Stack Pointer (SP)
  - 5. Flag Register / Program Status Word (PSW) / 5 Talus Register
  - Address Register (AR) / Memory Address Register (MAR)
  - 7. Data Register (DR) / Memory Data Register (MDR) / MBR (Memory Buffer Reg.)

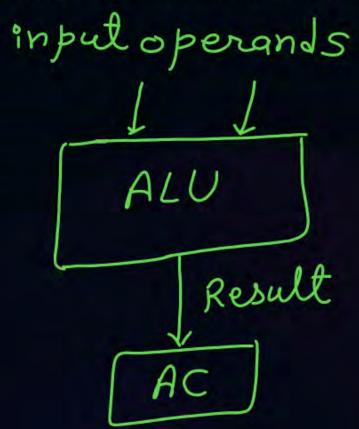


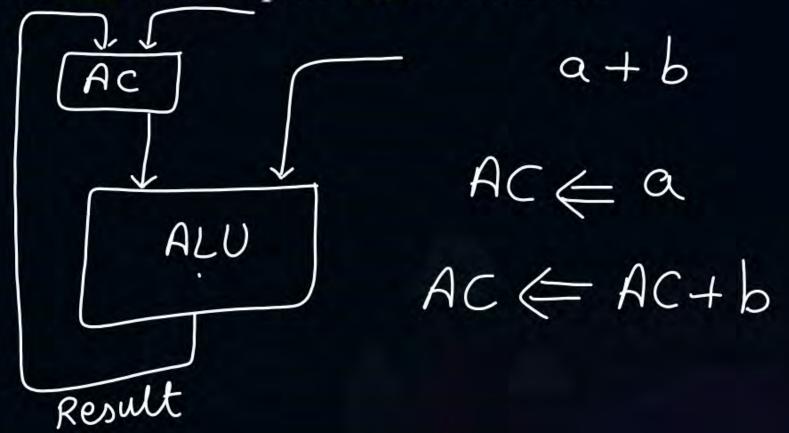
#### Topic: Accumulator



one

Used to store result of ALU and sometimes on of the operand₅for ALU too.







#### **Topic: Types of Architecture**

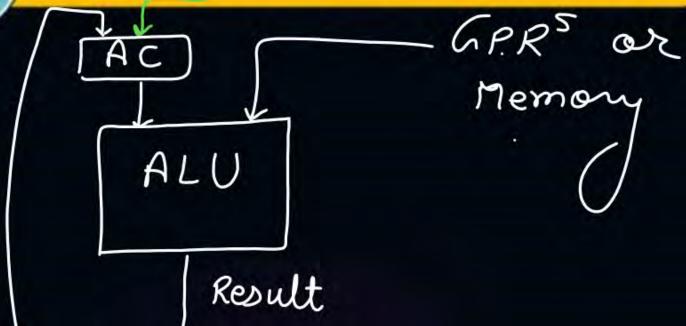


#### **Based on ALU input:**

- AC-Based Architecture (single Ac based architecture)
- Register Based Architecture
- Register-Memory Based Architecture
- Complex System Architecture
- Stack Based Architecture



#### **Topic: AC-Based Architecture**



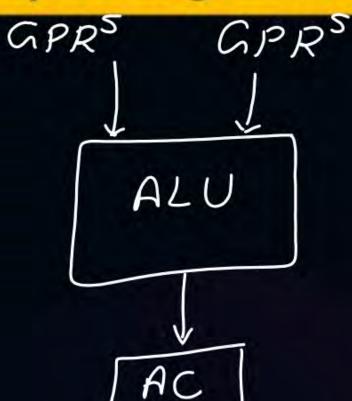
a, b, c, d are in memory

$$AC \Leftarrow AC + b$$
 $AC \Leftarrow AC + d$ 
 $AC \Leftarrow AC \leftarrow AC + d$ 
 $AC \Leftarrow AC \Leftarrow AC * R^1$ 



#### **Topic: Register-Based Architecture**





$$\frac{(a+b) * (c+d)}{R1}$$

$$R1 \leftarrow a$$
 $R2 \leftarrow b$ 

a, b, c, d

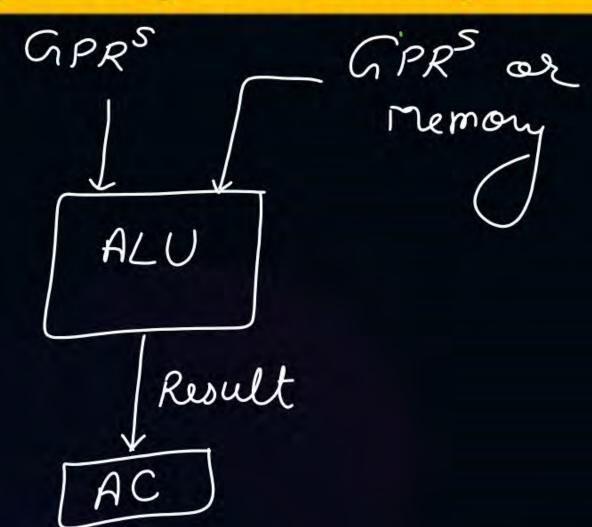
are in memory



#### **Topic: Register-Memory Based Architecture**



in memory



$$(a+b) * (c+d)$$

$$a,b,c,d \text{ are in memory }$$

$$R1 \Leftarrow a$$

$$AC \Leftarrow R1 + b$$

$$R1 \Leftarrow AC$$

$$R2 \Leftarrow C$$

$$Ac \Leftarrow R2 + d$$

$$R2 \Leftarrow AC$$

$$R2 \Leftarrow R1 + R2 + d$$

$$R2 \Leftarrow R1 + R2$$





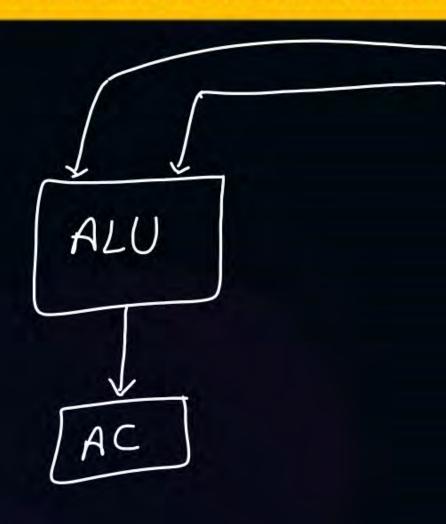
$$AC \Leftarrow a+b$$
 $R1 \Leftarrow AC$ 
 $AC \Leftarrow C+d$ 
 $R2 \Leftarrow AC$ 
 $AC \Leftarrow R1 * R2$ 
 $AC \Leftarrow R1 * R2$ 



## Topic : Stack-Based Architecture

(not used now a days)





From stack (In memory)



#### **Topic: Program Counter**



Stores address of next instruction to be executed



address 500 501 502 I3 If instruction I2 is in execution in CPU, then PC stores => address of I3 502



#### **Topic: Instruction Register**



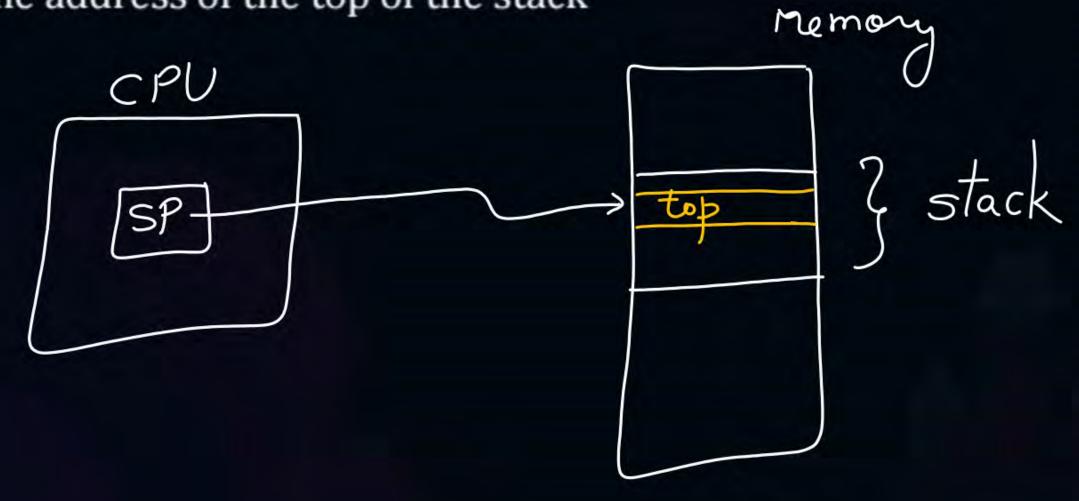
Stores the current instruction to be executed



#### **Topic: Stack Pointer**



Stores the address of the top of the stack

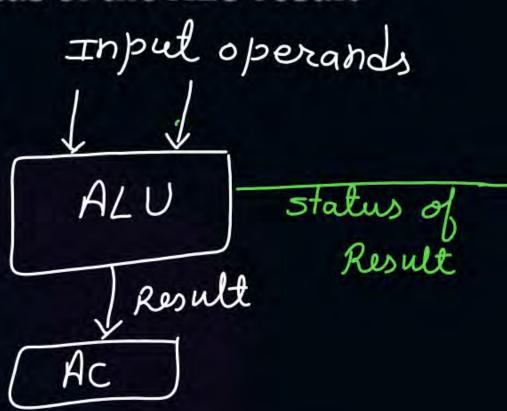


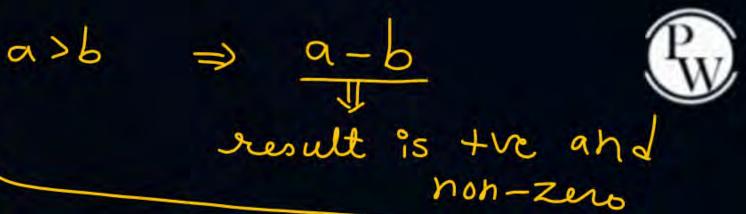


#### **Topic: Flag or Status Register**

Stores the status of the ALU result

it is used for conditions checking







#### **Topic: Address Register or MAR**



Used to send address to memory



#### **Topic: Data Register or MDR**



- Used to send data to memory
- And to receive data from memory

#### [NAT]



- #Q. A CPU has 4 bytes instructions. A program (Instructions  $I_1$  to  $I_{200}$ ) starts at address 200 (in decimal). Find the address of following instructions:
  - 1. I<sub>1</sub>
  - 2. I<sub>5</sub>
  - 3. I<sub>120</sub>





#Q. A CPU has 4 bytes instructions. A program (Instructions  $I_1$  to  $I_{200}$ ) starts at address 500 (in decimal). What should be the PC value when instruction  $I_6$  will be executing in CPU?





#Q. A CPU has 4 bytes instructions. A program (Instructions  $I_1$  to  $I_{200}$ ) starts at address 500 (in decimal). What should be the PC value when instruction i will be executing in CPU?



#### 2 mins Summary

Topic CPU Registers

Topic Types of Architecture

Topic Program Counter

Topic Instruction Register

Topic Stack Pointer

Tomarrow



AR, C DR

Memory, address, pc,





# Happy Learning THANK - YOU