GATE Computer Science & IT

BASIC COMPUTER ORGANIZATION AND ARCHITECTURE

Practice Questions Booklet

ANALYSIS OF CSO IN GATE PAPER

Years	Marks
2015	5
2016	8
2017	12
2018	10
2019	9
2020	10
2021 Set -1	8
2021 Set -2	9

CSO GATE SYLLABUS

- **Number System:** Octal, Hexadecimal and Decimal Representation, Complements, l's Complement, 2's Complement, Fixed-Point Representation, Floating-Point Representation, Binary Codes *etc.*
- **Cache Memory:** Associative Mapping, Direct Mapping, Set-Associative Mapping and Writing into Cache *etc.*
- **Instruction Sets:** Addressing Modes and Formats: Three-Address Instructions, Two - Address Instructions, One-Address Instructions and Zero-Address Instructions, Data Transfer and Manipulation Instruction *etc.*
- **Assembly Language**: Rules of the Language, Translation to Binary *etc.*
- **Instruction Pipelining**: Ideal Instruction Pipeline, Data Dependency, Handling of Branch Instructions *etc.*
- **External Memory**: Disk Structure and Disk Data transfer.
- **Input-Output Organization:** Input-Output Interface, Memory-Mapped I/O, Modes of Transfer, Programmed Interrupt-Initiated I/O, Priority Interrupt, Direct Memory Access (DMA), DMA Controller and DA Transfer *etc.*
- **ALU, Data-Path and Control Unit**.

CSO GATE REFERENCE BOOKS

- Computer Organization by Carl Hamature
- Computer System and Architecture by M. Morris Mano
- Computer Organization and Architecture by William Stallings
- Computer Organization and Design by David A. Patterson and John L. Hennessy

TABLE OF CONTENTS

UNITS AND ABBREVIATIONS

- **Units of File size** (how big a file is on your computer) is usually measured in units of "**kilobytes**", "**megabytes**", and "**gigabytes**." In this computing (binary, but not data transfer) usage, '**K'** (uppercase) represents a multiplier of 1,024, '**B'**(uppercase) represent bytes and '**b**'(lowercase) represent bits. Other abbreviations use this same base of 1,024:
  - **1 KB** (one KiloByte) = 1,024 Bytes (approximately 1 thousand Bytes)
  - **1 MB** (one MegaByte) = 1,024 KB (approximately 1 million Bytes)
  - **1 GB** (one GigaByte) = 1,024 MB (approximately 1 billion Bytes)
  - **1 TB** (one TeraByte) = 1,024 GB (approximately 1 trillion Bytes)

- **Units of Data transfer** on the other hand is expressed in **bits**. In this computing (data transfer) usage '**k'** (lowercase) represents a multiplier of 1,000. In bit rates the abbreviations are as follows:
  - 1 **kbps** = 1,000 bits per second
  - 1 **Mbps** = 1,000,000 bits per second.
  - 1 **Gbps** = 1,000,000,000 bits per second.

  Where:-
  kbps (kilobits/sec) means ***thousands of bits per second*** **(**where "thousand"= 10^3)
  mbps or Mbps (megabits/sec) means ***millions of bits per second*** (where "millions"= 10^6)
  gbps or Gbps (gigabits/sec) means ***billions of bits per second*** (where "billion"= 10^9)
  tbps (terabits/sec) means ***trillions of bits per second*** (where "trillions"= 10^{12})
  pbps (petabits/sec) means ***quadrillions of bits per second*** (where "trillions"= 10^{15})

- **Units of Time**
  - 1 second = 10^3 milliseconds (ms)
  - 1 second = 10^6 microseconds (μs)
  - 1 second = 10^9 nanoseconds (ns)
  - 1 second = 10^{12} picoseconds (ps)
  - 1 second = 10^{15} femtoseconds (fs)
  - 1 milliseconds (ms) = 10^{-3} seconds
  - 1 microseconds (μs) = 10^{-6} seconds
  - 1 nanoseconds (ns) = 10^{-9} seconds
  - 1 picoseconds (ps) = 10^{-12} seconds
  - 1 femtoseconds (fs) = 10^{-15}second

NUMBER SYSTEM

Q1. The binary representation of the hexadecimal number 3B7F is

(a) 0100 1001 1110 1101 (b) 0011 1011 0111 1111

(c) 0010 0100 0000 1010 (d) 0110 0011 1011 1100

Q2. The decimal representation of the binary number $(10011010010)_2$ is _____

Q3. The binary representation of the decimal number $(54321)_{10}$ is

(a) 11000001111000001 (b) 1101 0100 0011 0001

(c) 11000000111000001 (d) 10011100000011001

Q4. The binary representation of the decimal number $(654321.015625)_{10}$ is

(a) 10010001001000010.100100 (b) 000000100100011111.100001

(c) 10010001001000000.000001 (d) 1001 1111 1011 1111 0001. 000001

Q5. The hexadecimal representation of the decimal number $(54321)_{10}$ is

(a)1011 (b) D431

(c) 3023 (d) 3039

Q6. The hexadecimal representation of the decimal number $(654321.015625)_{10}$ is

(a)1C140.00 (b) 9 FBF1.04

(c) 0E240.01 (d) 9 FBF1.01

Q7. The octal representation of the hexadecimal number $(A7C8)_{16}$ is

(a) $(123456)_8$ (b) $(123614)_8$

(c) $(123710)_8$ (d) $(1010011111001000)_2$

Q8. The octal representation of the decimal number $(668)_{10}$ is

(a) $(1234)_8$ (b) $(2341)_8$

(c) $(3412)_8$ (d) $(4123)_8$

Q9. The octal representation of the decimal number $(52345)_{10}$ is

(a) 12345 (b) 146 171

(c) 30071 (d) 17003

Q10. The octal representation of the decimal number $(561234.015625)_{10}$ is

(a) 123456.11 (b) 2 110 122.10

(c) 113600.11 (d) 2 110 122.01

Q11.	The octal representation of the hexadecimal number $(ABCDE)_{16}$ is (a) 2777565 (b) 2777650 (c) 6435210 (d) 2536336
Q12.	The octal representation of the hexadecimal number $(FEDCBA.AB)_{16}$ is (a) 77556272.516 (b) 12345670.116 (c) 23451671.116 (d) 77556272.526
Q13.	The following numbers are represented in hexadecimal, octal, binary, and decimal, respectively. Which answer specifies four unique integer numbers? (a) 0x050, 062, 0z000101000, 50 (b) 0x050, 070, 0z001010000, 62 (c) 0x032, 062, 0z001100010, 62 (d) 0x062, 062, 0z010000010, 62
Q14.	Which of the following representation(s) is/are equivalent to 0z010101010101? (a) $(555)_8$ (b) $(1365)_{10}$ (c) 0x555 (d) $(1031)_{11}$
Q15.	How many different values can be represented using four digits in the hexadecimal system? _____
Q16.	The octal representation of the hexadecimal number (ABC.DEF)16 is_____ (Round off to two decimal places)
Q17.	The base–3 representation of the base–81 number $(74)(34)(3)_{(81)}$ is_____
Q18.	What is decimal equivalent of $(5477211)_7$?_____
Q19.	The base–27 representation of the base–3 number $(12211022)_3$ is_____
Q20.	Find a digit d such that $d111_6 = 1d46_7$._____
Q21.	Solve the equation $1xx6_9 = 1x010_5$ for the missing digit. Then x=_____
Q22.	If $(x876)_{16} = (114166)_8$ Then x = _____

Q23.	If $(7654)_x + (3210)_x = (13064)_x$, where x > 0, then positive x is (a) 5 (b) 6 (c) 8 (d) 9
Q24.	If $(555)_{10} = (x)_5$, then x = _____
Q25.	If $(33332222)_4 = (1x8702)_9$,then x = _____
Q26.	What can be the possible value of x, if $(33)_x + (11)_x = (110)_x$?_____
Q27.	If $(753)_x$ (in base-x number system) is equal to $(384)_y$ (in base-y number system), the possible values of x and y are (a) 7, 12 (b) 13, 9 (c) 8, 11 (d) 9, 13
Q28.	Consider the equation $(43)_x = (y3)_8$ where x and y are unknown. The number of possible solutions is_____
Q29.	Let X = $(1100)_7$ and Y = $(453)_7$ then what is the value of $(X-Y)_7$ is?_____
Q30.	The roots of the quadratic equation "$x^2 - 11x + 22 = 0$" are given by x = 3 and x = 6. What is the base of the numbers? _____
Q31.	The roots of the cubic equation $x^3 – 23x^2 + 142x – 120= 0$ are given by x = 1, x = 10 and x =12. What is the base of the numbers? _____
Q32.	For what value of b the equation is satisfied $(1234)_b + (5432)_b = (6666)_b$ (a) 6 (b) 7 (c) 10 (d) Any value > 6
Q33.	Convert the fractional decimal number 194.03125 to binary with a maximum of six places to the right of the binary point. (a) 01000010.00001 (b) 01000010.00001 (c) 11000011.10001 (d) 11000010.00001

Q34.	What is the smallest unsigned number that can be represented using a sequence of 23 bits? (a) 0 (b) $-(2^{22}-1)$ (c) $-2^{23}-1$ (d) $2^{23}-1$
Q35.	What is the largest unsigned number that can be represented using a sequence of 32 bits? (a) -2^{31} (b) $2^{31}-1$ (c) $-(2^{32}-1)$ (d) $2^{32}-1$
Q36.	What is the smallest signed number (most negative) using a sequence of 32-bits that can be represented in signed magnitude? (a) -2^{31} (b) $-(2^{31}-1)$ (c) $2^{32}-1$ (d) $2^{31}-1$
Q37.	What is the largest signed number (most positive) using a sequence of 32 bits that can be represented in signed magnitude? (a) -2^{31} (b) $-(2^{31}-1)$ (c) $2^{32}-1$ (d) $2^{31}-1$
Q38.	What is the smallest signed number (most negative) using a sequence of 32 bits that can be represented in one's complement? (a) -2^{31} (b) $-(2^{31}-1)$ (c) $2^{32}-1$ (d) $2^{31}-1$
Q39.	What is the largest signed number (most positive) using a sequence of 32 bits that can be represented in one's complement? (a) -2^{31} (b) $-(2^{31}-1)$ (c) $2^{32}-1$ (d) $2^{31}-1$
Q40.	What is the smallest signed number (most negative) using a sequence of 32 bits that can be represented in two's complement? (a) -2^{31} (b) $-(2^{31}-1)$ (c) $2^{32}-1$ (d) $2^{31}-1$

Q41. What is the largest signed number (most positive) using a sequence of 32 bits that can be represented in two's complement?

(a) -2^{31} (b) $-(2^{31}-1)$

(c) $2^{32}-1$ (d) $2^{31}-1$

Q42. Which one of the following is the 8-bit two's complement representation of the sign magnitude number $(010010001)_{sm}$.

(a) $(011101111)_{2's}$ (b) $(000010001)_{2's}$

(c) $(011101110)_{2's}$ (d) $(010010001)_{2's}$

Q43. Match the following 6-bit representations of -25 with the names of these representations:

6-bit representations	names of representations
1. 100111	i) one's complement
2. 111001	ii) biased with $B=2^5$
3. 110101	iii) signed magnitude
4. 100110	iv) two's complement
5. 000111	v) unknown

(a)1-iv, 2-iii,3-v,4-i,5-ii (b) 1-iv, 2-ii,3-v,4-i,5-iii

(c) 1-v, 2-ii,3-iv,4-i,5-iii (d)None of these

Q44. Which of the following numbers is NOT -1 in the specified representation?

(a) 1111 1110 in 8-bit 1's complement

(b) 1000 0001 in 8-bit biased representation with a bias of 128

(c) 1 01111111 00000000000000000000000 in 32-bit IEEE floating point format

(d) 1111 1111 in 8-bit 2's complement

Q45. Which of the following number is the 8-bit two's complement representation for $(-89)_{10}$?

(a) $(10111101)_{2s}$

(b) $(10111110)_{2s}$

(c) 01000010_{2s}

(d) none of the above

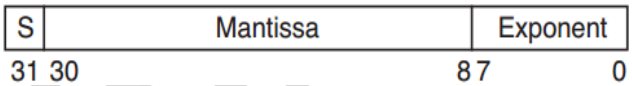
Q46.	What will be the correct result when two 8-bit 2's complement numbers 11001111 and 10001111 are added? (a) 0101 1110 carry = 1, overflow = 0 (b) 0101 1110 carry = 0, overflow = 1 (c) 0101 1110 carry = 1, overflow = 1 (d) 0101 1110 carry = 0, overflow = 0
Q47.	Which of the following number is the 3-digit 6's complement representation for $(48)_{10}$? (a) 4406s (b) 4346s (c) 4356s (d) 4366s
Q48.	What is the value represented by the 8-bit 2's complement fixed point number 1101.1010_{2s}? (a) 13.225_{10} (b) -2.3125_{10} (c) -2.375_{10} (d) -3.3125_{10}
Q49.	Which of the following statements about 8-bit two's complement is/are correct? (a) The most significant bit has a weight of −26 (b) The representable range is −128 to +127 (c) The representable range is −127 to +128 (d) To calculate −x from x, we flip all the bits and add 1
Q50.	When do we need to use sign extension? (a) When we convert an n-bit 2's complement value to the 1's complement version. (b) When we convert an n-bit 1's complement value to the 2's complement version. (c) When we have an n-bit 2's complement value and we want to use it as the same value with fewer bits. (d) When we have an n-bit 2's complement value and we want to use it as the same value with more bits.

Q51.	Consider the results of adding the following pairs of six-bit (i.e. one sign bit and five data bits) two's complement number. Which of the operation is/are cause overflow? (a) 0 1 0 1 1 0 + 0 0 1 0 0 1 (b) 1 0 1 0 1 1 + 1 0 0 1 0 1 (c) 1 1 1 1 1 0 + 0 0 0 1 1 1 (d) None of the above
Q52.	Consider the results of subtracting the following pair of six-bit (i.e. one sign bit and five data bits) two's complement number. Which of the operation is/are cause overflow? (a) 0 1 0 1 1 0 − 0 0 1 1 1 1 (b) 1 1 1 1 1 0 − 1 1 0 1 0 1 (c) 1 0 0 0 0 1 − 0 1 1 1 0 1 (d) None of the above
Q53.	The following two values A = 11111111111111111111111010101 and B= 11111111111111001001111010101 are representations of 2's complement integers. Which one of the following is true? (a) A is larger (b) B is larger (c) A and B are equal (d) Can't say anything, data insufficient

Q54.	X is an 8-bit two's complement number with value 10100010. What is the result of operation X >> 2? (a) 11101000 (b) 00101000 (c) 11010110 (d) 10101000
Q55.	**[MSQ]** Assume that (i) A, B and C are 8-bit two's complement numbers, (ii) A = 11100001, (iii) B = 01001001, and, (iv) C = 00010010. Which one of the following operations cannot causes an overflow? (a) A >> 2 (b) A + B (c) B << 1 (d) A + C
Q56.	For the number -74 which option has the correct 8-bit binary values for all three representations: 1's complement, 2's complement and signed magnitude respectively? (a) 1011 0110, 1011 0101, 1100 1010 (b) 1011 0101, 1011 0110, 1100 1010 (c) 1011 0101, 1011 0100, 1100 1010 (d) 1100 1010, 1011 0110, 1011 0101
Q57.	**[MSQ]** Which of the following statements about 8-bit two's complement are correct? (a) The largest positive number is $127 = 2^7 - 1$. (b) The least negative number is $-127 = -(2^7 - 1)$. (c) Adding 11111110 and 00000010 produces an overflow. (d) Adding 01111110 and 00000010 produces an overflow.
Q58.	In which of the following coding schemes that 0111 represents the smallest value? (a) The standard 4-bit Gray code (b) The BCD code (c) The 84-2-1 code (d) The 2421 code
Q59.	We have number 11001 in gray code then it's decimal equivalent is:_____

Q60.	How many of following statement is/are correct? S1: To convert a decimal integer to base 4 form, repeated multiplication by 4 is used. S2: In the Gray code sequence, two consecutive code values differ by one bit. (a) only s1 (b) only s2 (c) both s1 & s2 (d) none of them
Q61.	Which of the following weighted decimal codes is not self-complementing? (a) 2421 code (b) 3132 code (c) 5211 code (d) 4421 code
Q62.	Which of the following is/are self-complementary code? (a) 2421 (b) 4. Data Link Layer Medium Access Control Question & solution Excess-3 (c) 5211 (d) 84-21
Q63.	If we add the following two decimal digits, 7+6, in excess-3 code what will be the sum. (a) 0001 0000 (b) 0001 0011 (c) 0000 1011 (d) 0100 0110
Q64.	Which of the following statements is/are true? (a) The sign-and-magnitude scheme has two representations for zero. (b) The BCD is a self-complementing code. (c) To convert a decimal integer to base 4 forms, repeated multiplication by 4 is used. (d) In the Gray code sequence, two consecutive code values differ by one bit.
Q65.	Given the space of N bits, if the absolute magnitudes of the largest positive and negative values that the space can represent are the same, the number system being used can be: (a) 1's complement only (b) 2's complement only (c) sign-and-magnitude only (d) Both (a) and (c)

Q66.	What is the IEEE-754 32-bit floating point format representation of 16? (a) 0 10000101 10000000000000000000000 (b) 0 00000100 00000000000000000000000 (c) 0 10000011 10000000000000000000000 (d) 0 10000011 00000000000000000000000
Q67.	Given the following hexadecimal form in the IEEE 754 single-precision floating-point number representation: 0xC4EFC000. What decimal value does it represent? _____ (rounded off to three decimal places)
Q68.	Given the following hexadecimal value in the IEEE 754 single-precision floating point number representation: 0xC4127000. What decimal value does it represent? _____ (Round off to two decimal places)
Q69.	Given the following hexadecimal representation in IEEE 754 single-precision floating-point number system: 0x42CE8000. What decimal value does it represent? _____ (Round off to two decimal places)
Q70.	Given the following binary value in the IEEE 754 single-precision floating-point number representation: 0 10000111 11110100000000000000000. What decimal value does it represent? _____ (Round off to two decimal places)
Q71.	Given the following binary value in the IEEE 754 single-precision floating-point number representation: 1 10000011 01100010000000000000000. What decimal value does it represent? _____(Round off to two decimal places)
Q72.	What is the hexadecimal representation of a decimal number -3.5 in IEEE-754 single-precision floating-point system? (a) 0xC0E00000 (b) 0xC0700000 (c) 0xC0600000 (d) 0xC0F00000

Q73.	What is the hexadecimal representation of a decimal number -75.35 in IEEE-754 single-precision floating-point system? (a) 0xC20F0000 (b) 0xC20E0000 (c) 0xC296B333 (d) 0xC10E0000
Q74.	What is the hexadecimal representation of a decimal number 52.21875 in IEEE-754 single-precision floating-point system? (a) 0x40200000 (b) 0x41200000 (c) 0x42E87000 (d) 0x4250E000
Q75.	Assuming IEEE single-precision floating point numbers (with an 8-bit exponent), Which of the following has the greatest value? (a) 0x00000000 (b) 0x00000001 (c) 0x50000000 (d) 0xC0000000
Q76.	Given the following hexadecimal representation in IEEE 754 single-precision floating-point number system: 0x4305C000. What decimal value does it represent? (a) 5.75 (b) 66.875 (c) 133.75 (d) 267.5
Q77.	Computer A uses the following 32-bit floating-point representation of real numbers:  Computer B uses the following floating point representation scheme:  Which of the following statements is true with regard to Computer B's method of representing floating-point numbers over Computer A's method? (a) both the range and precision are increased (b) the range is increased but the precision is decreased (c) the range is decreased but the precision is increased (d) both the range and precision are decreased

Q78.	For a 7-bit normalized floating-point format: $(-1)^S \times (.FFFF) \times (2^{EE})$ where FFFF is unsigned and EE is two's complement, what is the smallest positive value you an represent just after 0? (a) 0.5 (b) 0.25 (c) 0.125 (d) 0.28125
For next three questions consider a floating-point representation with a sign bit in the leftmost position, followed by a three-bit base 4 exponent and represented as 1's complement, followed by a normalized six-bit fraction. Zero is represented by the bit pattern 0 000 000000	
Q79.	What decimal number is represented by the bit pattern: 1 110 010000? _____
Q80.	What is the bit pattern (in decimal) for the smallest non-zero positive representable number? _____
Q81.	What is the bit pattern for the largest positive representable number? _____
Q82.	Consider a hypothetical 10-bit similar to IEEE floating point representation including all special cases. There is a sign bit in the most significant bit. The next five bits are the two's complement exponent. The last 4 bits is the normalized fraction. What is the floating-point representation for 0.125? (a) 0x130 (b) 0x230 (c)0x1D0 (d)0x103
Q83.	Express the floating-point number 1.63 in binary notation using 1-bit sign, 3-bit exponent in excess-4 notation (100 stands for 0), and 4-bit un normalized mantissa in the same order. (a) 0x5D (b) 0x6B (c) 0x55 (d) 0x2A
For next four question, suppose a designer create a variant similar to an IEEE floating point number that uses 1 bit for sign, 7 bits for biased exponent and 8 bits for mantissa. It has all the properties of IEEE 754 (e.g., ±0, ±∞, NAN, Denormalized number) just with different ranges, precision & representations	
Q84.	What is the biasing value in this representation? _____
Q85.	What is the largest number smaller than +∞ (in decimal)? ___ _____
Q86.	What is the smallest positive normalized number (closest to 0 in HEX)?_____

Q87. **[MSQ]**

Which of the following is not the floating point representation of decimal number -0.1325 using the design above in hexadecimal is?

(a) BC80 (b) CC40

(c) BB31 (d) None of these

For the next five questions, Consider the following 16-bit floating point representation similar to IEEE floating point format. There is a sign bit in the most significant bit to represent sign of the number. The next five bits are the exponent. The exponent stored in Excess – 15 notations. The last ten bits are the mantissa. The mantissa stored in sign-magnitude representation. The rules are like those in the IEEE standard (normalized, denormalized, representation of 0, infinity, and NAN)

Q88. What is the smallest positive normal number greater than zero in decimal?

(a) $2^{-14} \times (1 + \frac{0}{1024})$ (b) $2^{-14} \times (0 + \frac{1023}{1024})$

(c) $2^{-14} \times (0 + \frac{1}{1024})$ (d) $2^{15} \times (1 + \frac{1023}{1024})$

Q89. What is the largest positive normal number greater than zero in decimal?

(a) $2^{-14} \times (1 + \frac{0}{1024})$ (b) $2^{-14} \times (0 + \frac{1023}{1024})$

(c) $2^{-14} \times (0 + \frac{1}{1024})$ (d) $2^{15} \times (1 + \frac{1023}{1024})$

Q90. What is the smallest positive subnormal number greater than zero in decimal?

(a) $2^{-14} \times (1 + \frac{0}{1024})$ (b) $2^{-14} \times (0 + \frac{1023}{1024})$

(c) $2^{-14} \times (0 + \frac{1}{1024})$ (d) $2^{15} \times (1 + \frac{1023}{1024})$

Q91. What is the largest positive subnormal number greater than zero in decimal?

(a) $2^{-14} \times (1 + \frac{0}{1024})$ (b) $2^{-14} \times (0 + \frac{1023}{1024})$

(c) $2^{-14} \times (0 + \frac{1}{1024})$ (d) $2^{15} \times (1 + \frac{1023}{1024})$

Q92. What is the largest positive normal number less than one in above floating-point representation?

(a) 0x3BFF (b) 0x3C00

(c) 0x3C01 (d) 0x3555

CACHE ORANIZATION

For next two questions consider a direct mapped cache having 8 cache lines. Each cache line consists of 2 words, and each word is one byte. The address bus consists of 7 bits.

Q 1. Which one of the following statements is correct?

(a) The index field consists of 2 bits.

(b) The index field consists of 1 bit.

(c) The tag field of the cache consists of 3 bits.

(d) The tag field of the cache consists of 2 bits.

Q 2. Which one of the following statements is correct?

(a) The total number of bytes for storing data in the cache is 16 bytes.

(b) The total number of bytes for storing data in the cache is 32 bytes.

(c) The total number of bytes for storing data in the cache is 8 bytes.

(d) The total number of bytes for storing data in the cache is 8K bytes

Q 3. Assume a 2-way set-associative word addressable cache is being used in a system with a 24-bit address using an 8-word block size. How many sets are there if the cache has 1024 lines, i.e., 8K words? _____

For the next three questions, consider 32-bit byte addressable physical memory and 2 MB cache with blocks of size 8KB each:

Q 4. How many bits in the tag, index and offset fields of the cache address respectively if the cache is direct mapped?

(a) 19, 6, 13 (b) 19, 0, 13

(c) 11, 8, 13 (d) 11,8,12

Q 5. How many bits in the tag, index and offset fields of the cache address respectively if the cache is 4 -way set-associative?

(a) 13, 6, 13 (b) 19, 0, 13

(c) 11, 8, 13 (d) 11,8,12

Q 6. How many bits in the tag, index and offset fields of the cache address respectively if the cache is full associative?

(a) 13, 6, 13 (b) 19, 0, 13

	(c) 11, 8, 13	(d) 11,8,12

For next two questions, consider a 2-way set-associative cache with following specification:

- word size: 32 bits
- cache block size: 2048 bits
- physical address size: 32 bits
- Number of blocks in cache: 2048
- memory is word addressable

Q 7.	How many bits are used for tag, index and offset if memory is word addressable?	
	(a) 13, 11, 8	(b) 14, 10, 6
	(c) 16, 10 and 6	(d) 10, 11, 11
Q 8.	How many bits are used for tag, index and offset if memory is byte addressable?	
	(a) 13, 11, 8	(b) 14, 10, 8
	(c) 16, 10 and 6	(d) 10, 11, 11

For next two questions consider two different cache configurations for an 8-bit processor. Both caches have two 16-byte blocks (for a total capacity of 32 bytes), but one is direct-mapped and the other is two-way set associative.

Q 9.	For the direct-mapped cache, how many bits are in the tag, index, and offset respectively?	
	(a) 5,1,1	(b) 3,1,4
	(c) 2,2,4	(d) 4,1,2
Q 10.	For the two-way set associative cache, how many bits are in the tag, index, and offset?	
	(a) 3,1,4	(b) 4,0,4
	(c) 5,0,3	(d) 2,2,4

For next two questions consider a direct-mapped cache design with a 32-bit address and byte-addressable memory, the following bits of the address are used to access the cache (Assume word size is 32 bit)

Tag	Index	Offset
31-10	9-5	4-0

Q 11.	What is the size of cache line in words?_____

Q 12.	How many lines does the cache have?_____

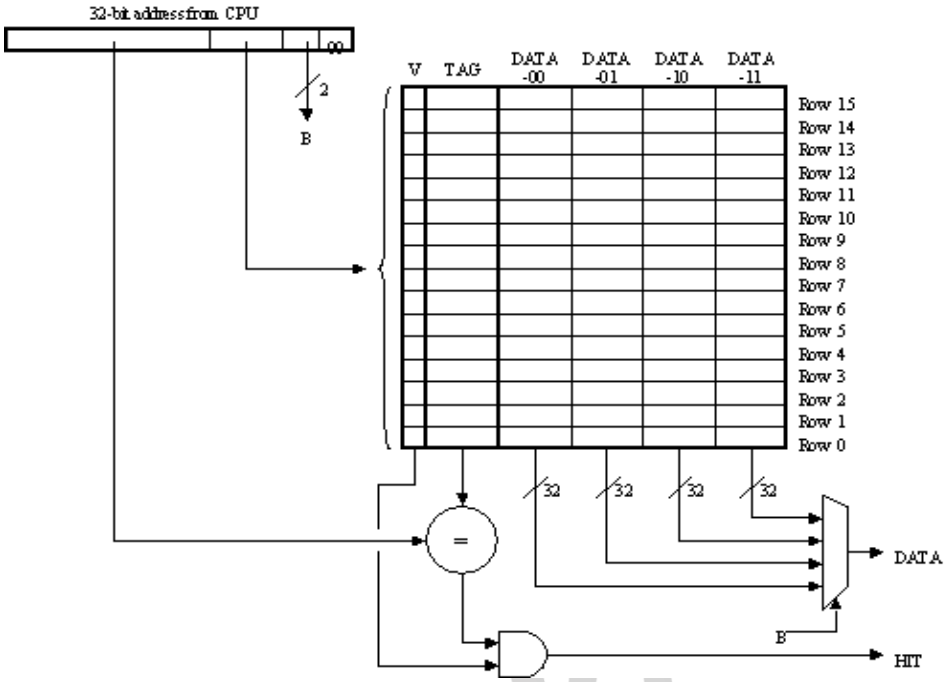
For next two questions, consider the 16 Kbyte cache with following specification:

- Each block will hold 32 bytes of data (not including tag, valid bit, etc.)
- The cache would be 2-way set associative
- Physical addresses are 32 bits
- Data is addressed to the word and words are 32 bits long

Q 13.	How many blocks would be in this cache?_____
Q 14.	How many bits of tag are stored with each block entry?_____
Q 15.	Consider a byte-addressable 4-way set associative cache with a full data capacity of 8192 bytes. Each cache block consists of 4 words, and each word is 4 bytes long. The number of bits in the set-index field and the number of bits in the offset field of the memory address is (a) Set-index = 4 bits; Offset = 2 bits (b)Set-index = 6 bits; Offset = 2 bits (c)Set-index = 6 bits; Offset = 4 bits (d)Set-index = 7 bits; Offset = 4 bits
Q 16.	Consider a cache with a size of 256 bytes and a block size of 16 bytes. In which cache index (in decimal) the memory address $28E7_{16}$ is mapped if cache is direct mapped cache and if cache is a 2-way set-associative cache respectively? (a) 7 and 15 (b) 15 and 7 (c) 14 and 6 (d) 14 and 7
Q 17.	Assume a 2-way set-associative word addressable cache with 1024 lines is being used in a system with a 24-bit address using an 8-word block size. If a block containing the address $(7BE453)_{16}$ is stored in the cache, what would the tag be? (a) 0x7BE (b) 0x3DF (c) 0x7BE4 (d) data insufficient
Q 18.	Given a 16-KB two-way associative cache with 32-byte cache lines and a 64-bit address space there will be x bits used for the index. If that same cache were fully-associative

	you'd need y bits to be used for the index. Then x* y =_____
Q 19.	Consider the processors have a 256kB 16-way set associative L2 cache with a 64-byte cache line size. How many cache lines will be there? (a) 2048 (b) 512 (c) 256 (d) 4096
Q 20.	Consider system: • A processor has a direct mapped cache • Data words are 8 bits long (i.e. 1 byte) • Data addresses are to the word • A physical address is 20 bits long • The tag is 11 bits • Each block holds 16 bytes of data How many blocks are in this cache?_____
Q 21.	Assume you have a 2-way set associative cache. • Words are 4 bytes • ***Addresses are to the byte*** • Each block holds 512 bytes • There are 1024 blocks in the cache If you reference a 32-bit physical address – and the cache is initially empty – how many data words are brought into the cache with this reference?_____
Q 22.	Consider a cache with 32-bit addresses, 768 blocks, and a block size of 128 bytes. Tags are 17 bits. How many sets are there, and what is the associatively of the cache? (a) 128 sets, 6-way set associatively. (b) 256 sets, 3-way set associatively. (c) 128 sets, 8-way set associatively. (d) Data inadequate
Q 23.	An 8-way set-associative cache memory allows a maximum of 256 different MM blocks to map to the same cache set. A block is 8-byte long. The MM is 16 MB. What are the sizes (in bits) of the tag, set and byte fields, respectively? (a) 9, 13, and 2. (b) 17, 3, and 3.

	(c) 18, 3, and 3		(d) 8, 13, and 3	
Q 24.	Which of the following accurately computes the set index for a cache with 8-byte blocks and 32 sets?(Assume I being physical address) (a) INDEX = (I /8) % 32; (c) INDEX = (I & 0XF8) / 8;		(b) INDEX = (I » 3) & 31; (d) All of the above	
For the next seven questions, consider the direct mapped cache organization of a computer shown below. Computer uses 32-bit data words and 32-bit word addresses.				
Q 25.	What are the maximum number words of data from main memory that can be stored in the cache at any one time? (a) 4	(b)8	(c) 16	(d)32
Q 26.	How many bits of the address are used to select which line of the cache is accessed? (a) 4	(b)8	(c) 16	(d)32
Q 27.	How many bits wide is the tag field? (a) 24	(b) 28	(c) 26	(d) 25
Q 28.	Assume that memory location 0x0002045C was present in the cache. Using the row and column labels from the figure, in what cache line could we find the data from that memory location?			



	(a) 4	(b) 5	(c) 6	(d) 7
Q 29.	What would the value of the tag field have to be for the cache row in which the above data appears?			
	(a) 0x000204	(b) 0x00020	(c) 0x0002045	(d) 0x00204
Q 30.	When an access causes a cache miss, how many bytes need to be fetched from memory to fill the appropriate cache location(s) and satisfy the request?			
	(a) 4	(b)8	(c) 16	(d)32
For next four questions consider a 64 KB, 2-way set-associative cache with 32-Bytes blocks in a 32-bit byte addressable system, in which a byte address is of the form b31, b30, … , b1, b0				
Q 31.	What is the total number of cache blocks in the cache			
	(a) 2 K blocks	(b) 4 K blocks	(c) 512 blocks	(d) 1 K blocks
Q 32.	Identify the address bits that are used for indexing a block in the cache (a) b15, b14, … , b6, b5 (11 bits) (b) b13, b12, … , b5, b4 (10 bits) (c) b14, b13, … , b5, b4 (11 bits) (d) b14, b13, … , b6, b5 (10 bits)			
Q 33.	Identify the address bits that are used as a tag for a block in the cache (a) b31, b30, … , b17, b16 (16 bits) (b) b31, b30, … , b15, b14 (18 bits) (c) b31, b30, … , b16, b15 (17 bits) (d) b30, b29, … , b16, b15 (16 bits)			
Q 34.	What is the total number of bits used as tags for all the blocks in the cache?			
	(a) 136 K bits		(b) 68 K bits	
	(c) 17 K bits		(d) 34 K bits	
Q 35.	How many possible locations are there for storing the address 0x45E4 in a 64KB 4 -way set-associative write back cache with 32 byte cache lines?			
	(a) 1		(b) 4	

	(c) 16 (d) 2048
Q 36.	Consider a 256 byte, direct mapped cache that uses 13 bits for tag and 2 bits for block offset. Given that memory is byte addressable, what is the maximum number of megabytes that memory can hold?_____
Q 37.	Suppose you have a word-addressed memory hierarchy system with the following parameters: • Block size = 16 words • Main memory size = 64 blocks • Cache size = 8 blocks Suppose your cache is set-associative with 4 sets (i.e., 2 cache blocks per set). The tag values in the cache are:

TAG	Cache Block Number	Set Number
0000	0	0
0100	1	0
1000	2	1
1001	3	1
1100	4	2
1000	5	2
0110	6	3
1101	7	3

Accessing which of the following memory addresses:

(1) 0x37A and

(2) 0x22C results in cache hit?

(a) Only (1) will result in cache hit

(b) Only (2) will result in cache hit

(c) Both will result in cache hit

(d) Both will result in cache miss

Q 38.	A byte-addressable machine with 32-bit memory addresses has a cache with the following properties: • 16byte cache blocks • 8KB of data in the cache • Direct mapped • Write through • 1 valid bit/block

	How many bits of metadata are required for each cache entry?___
Q 39.	Consider a direct mapped cache with a 32-bit address divided as follows: bits 0 - 3 = offset bits 4 - 14 = index bits 15 - 31 = tag How much space is required to store the tags for the cache?(in KB)_____
Q 40.	Consider a 4-way set associative write-back cache of size 64KB. Each cache block holds 8 words of 4 bytes each. Physical addresses are 32 bits long. Assuming that the 64KB of cache refers purely to "usable cache" – i.e. cache that is used only to store data or instructions, and not overheads like tag bits, what is the actual overall cache size including the overheads? _____KB

The following next four questions ask you to evaluate alternative cache designs using patterns of memory references taken from running programs. **Each of the caches under consideration has a total capacity of 8 (4-byte) words, with one word stored in each cache line. The cache designs under consideration are:**

DM: a direct-mapped cache.

S2: a 2-way set-associative cache with a least-recently-used replacement policy.

FA: a fully-associative cache with a least-recently-used replacement policy.

The questions below present a sequence of addresses for memory reads. **You should assume the sequences repeat from the start whenever you see "...".** Keep in mind that byte addressing is used; addresses of consecutive words in memory differ by 4. Each question asks which cache(s) give the best hit rate for the sequence. Answer by considering the steady-state hit rate, i.e., the percentage of memory references that hit in the cache after the sequence has been repeated many times.

Q 41.	Which cache(s) have the best hit rate for the sequence 0, 16, 4, 36, ... (a) DM (b) S2 (c) FA (d) Both B and C
Q 42.	Which cache(s) have the best hit rate for the sequence 0, 4, 8, 12, 16, 20, 24, 28, 32, ... (a)DM (b) S2

	(c) FA (d) All give same
Q 43.	Which cache(s) have the best hit rate for the sequence 0, 4, 8, 12, 16, 20, 24, 28, 32, 28, 24, 20, 16, 12, 8, 4, ... (a) DM (b) S2 (c) FA (d) All have same performance
Q 44.	Which cache(s) have the best hit rate for the sequence 0, 4, 8, 12, 32, 36, 40, 44, 16, .. (a) DM (b) S2 (c) FA (d) All have same performance
For the next three questions, consider the following sequence of memory references given as word addresses: 22, 10, 27, 21, 23, 30, 4, 22, 7, 35, 5, 31, 10, 27, and 21. Assume the cache is initially empty.	
Q 45.	How many of the above references a cache hit is if 64 bytes direct mapped cache with block size of 8 bytes and a word size of 4 bytes is used? _____
Q 46.	How many of the above references a cache hit is if a 64 bytes 2-way set associative cache, with block size of 8 bytes, a word size of 4 bytes, and LRU replacement policy is used?_____
Q 47.	How many of the above references a cache hit is if a 64 byte Fully associative cache, with block size of 8 bytes, a word size of 4 bytes, and LRU replacement policy is used?_____
Q 48.	Consider a direct mapped cache memory with total 16 cache blocks (0-15) and a main memory with 256 blocks (0-255). Assuming that initially the cache did not have any memory block. Consider the following sequence of memory block references: 3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, and 253. Which memory blocks will be present in the cache after the above sequence of memory block references? (a) 2, 3, 180, 181, 88, 186, 43, 44, 253, 14, 191 (b) 3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253 (c) 3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186

	(d) 3, 180, 43, 2, 191, 190, 88, 14, 181, 44, 186
Q 49.	Consider a 2-way set associative cache memory with 8 sets (0-7) and total 16 cache blocks (0-15) and a main memory with 256 blocks (0-255). Assuming that initially the cache did not have any memory block. Consider the following sequence of memory block references: 3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253. Which memory blocks will be present in the cache after the following sequence of memory block references if LRU policy is used for cache block replacement? (a) 3,180,43,2,191,14,181 (b) 2, 191, 88, 190, 14, 181 (c) 14, 181, 44, 186, 253 (d) 88,2,186,3,43,180,44,181,253,190,14,191
Q 50.	A designer makes a mistake and builds a cache that has a MRU (most recently used) replacement policy instead of an LRU replacement policy. What is left in a 4-entry, fully associative, MRU cache with 1 byte lines after the following address accesses: 1, 2, 3, 4, 5,3, 5, 1, 5, 2 (a) 1,2,3,5 (b)2, 5, 1, 3 (c) 4,2, 5, 3 (d)both a and b
Q 51.	Consider a 64-byte cache with 8 byte blocks, an associativity of 2 and LRU block replacement. Virtual addresses are 16 bits. The cache is physically tagged. The processor has 16KB of physical memory. What is the total number of tag bits in cache?_____
Q 52.	What data will be in a 4-entry, fully-associative, LRU cache with one word per line after the following memory accesses word address: 0, 1, 2, 3, 4, 5, 3, 2, 1? (a) 1, 2, 3, 4 (b) 1, 2, 3, 5 (c) 1, 3, 4, 5 (d) 1, 2, 4, 5
Q 53.	Assume you have a fully associative cache with 4 entries. For the following memory block address sequence, which entry becomes at the end? Assume that LRU police is used for replacement. 8 9 5 2 6 5 9 10 3 (a) 3, 9, 5, 10 (b) 9,5,2,10

	(c) 8,9,5,10 (d) 9,5,2,3
Q 54.	Assume you have a 2-way set-associative LRU cache with 4 entries and a cache line size of 1 bytes. What will the hit (H) miss (M) pattern be for the following access pattern: 0 1 2 3 7 0 3 8 1? (a) M MMMMM H M M (b)MMMMM H M M H (c) M MMMM H H M M (d) M MMMM H H M H
For next two questions consider the access pattern A, B, C, B, A where each letter corresponds to a unique cache block. You are to assume there were no accesses to any block before this, and that all conflict is random.	
Q 55.	The probability of the second access to "A" being a hit on a direct-mapped cache with 4 lines is closest to: _____
Q 56.	For a fully-associative cache with 2 lines the probability of a hit is closest to____
For next four questions Assume the cache with 8 blocks. If following memory block address access in the given sequence 0, 0, 8, 8, 16, 16, 24, 32, 40, 44, 0, 8, 16, 24, 1, 2, 3, 4, 1, 2, 3, 4 What is cache hit(in %) rate in following four cases?	
Q 57.	Cache is direct mapped_____
Q 58.	Cache is 2-way set associative assume LRU Replacement_____
Q 59.	Cache is 4-way set associative assume LRU replacement_____
Q 60.	Cache is fully associative assume LRU replacement_____
Q 61.	Consider a fully associative cache with 8 cache blocks (numbered 0-7) and the following sequence of memory block requests: 4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7 If LRU replacement policy is used, which cache block will have memory block 7?_
Q 62.	If you have a 32-bit address space (addresses are 32 bits) and you have a 4-way associative cache that uses 5 bits as the set index and 4 bits as the byte offset, how large

	is the data portion of the cache (in bytes)?_____
For the next three questions, Consider a direct mapped of 8 words, with block 2 word per block. The following sequence of accesses to memory block 0, 5, 2, 7, 4, 0 and 4 is repeated 10 times.	
Q 63.	The number of compulsory misses_____
Q 64.	The number of conflict misses_____
Q 65.	The number of capacity misses____
Q 66.	Consider a 2-way set associative cache with 256 blocks and uses LRU replacement, initially the cache is empty. Conflict misses are those misses which occur due the contention of multiple blocks for the same cache set. Compulsory misses occur due to first time access to the block. The following sequence of accesses to memory blocks (0,128,256,128,0,128,256,128,1,129,257,129,1,129,257,129) is repeated 10 times. The number of conflict misses experienced by the cache is _____.
Q 67.	Which one of the following statements is/are correct? (a) Compulsory misses cannot be reduced by increasing the size of the cache. (b) Increasing the associativity of the cache can increase conflict misses. (c) Capacity misses can be reduced by increasing the associativity of the cache. (d) Compulsory misses can be reduced by increasing the associativity of the cache.
Q 68.	Which one of the following statements is/are correct? (a) Accessing a set-associative cache is faster than accessing a direct mapped cache. (b) Compulsory misses cannot be totally avoided. (c) A capacity miss occurs when a replaced cache line needs to be accessed again. (d) Compared with a direct mapped cache, a fully associative cache has a larger tag field.

Q 69. Match the column for each of the following suggested changes in set associative cache with a reason why the change might make things worse, assuming that the total size of the cache (i.e., the total amount of data it can store) must remain the same

1. Increase the block size	i. Decreases cache's ability to capture spatial locality
2. Decrease the block size	ii. Decreases cache's ability to capture temporal locality, because the cache stores fewer total blocks.
3. Decrease the set associativity	iii. Slows cache-hit time.
4. Increase the set associativity	iv. Increases potential for conflict misses

(a) 1-ii, 2-iii, 3-i, 4-iv

(b)1-iii,2-i,3-iv,4-ii

(c) 1-iv, 2-i, 3-ii, 4-iii

(d)1-ii,2-i,3-iv,4-iii

Q 70. Which of the following statement(s) is/are true?

(a) It is possible for Conflict Misses in Set-Associative Cache Mapping.

(b) Cache block search time in Direct Mapped Caches is larger than that of other Cache Organization.

(c) Increasing Cache Line size helps decreasing the Cache Miss Ratio for programs having Spatial Locality.

(d) Decreasing Cache Line sizes could decrease Conflict Misses.

Q 71. Which one of the following statements is/are correct?

(a) Temporal locality means a recently accessed data item is likely to be accessed again in the near future.

(b) Spatial locality means variables should be stored close to each other.

(c) Temporal locality means a temporary variable is more frequently used than a global variable.

	(d) Spatial locality means a branch instruction should not branch to an instruction that is too far away.
Q 72.	Which is the fastest cache mapping function? (a) Direct mapping (b) Set associative mapping (c) Fully associative mapping (d) Cannot say anything
Q 73.	Which is the slowest cache mapping function? (a) Direct mapping (b) Set associative mapping (c) Fully associative mapping (d) Cannot say anything
Q 74.	Which cache mapping function is most likely to thrash, i.e., two blocks contending with each other to be stored in the same line? (a) Direct mapping (b) Set associative mapping (c) Fully associative mapping (d) Cannot say anything
Q 75.	The problem with a cache that uses a *write through* policy is/are that: (a) It runs the risk of leaving main memory invalid for a long period of time. (b) It cannot be used with multiple CPUs even if the CPUs are watching main memory for an update. (c) It slows down the write process. (d) It requires additional overhead in the cache to keep track of which blocks have been modified.
Q 76.	Which of the following statements is/are not true about caches? (a)Caches do not have to be as big as the data the program needs to access (b) It takes longer to access a cache if it is full (c) Cache memories are faster than memories used for DRAM

	(d) Caches only help if the application reuses its data
Q 77.	Which one of the following is/are correct statement? (a) In a set associative cache, blocks in memory that map to the same set are stored contiguously in memory. (b) All other things equal, direct mapped caches have a lower tag overhead than fully associative caches. (c) Bigger cache blocks always lead to a higher hit rate. (d) On every store instruction, a write back cache will write to main memory
Q 78.	A cache has a 95% hit ratio, an access time of 100ns on a cache hit, and an access time of 800ns on a cache miss. What is the effective access time?_ _____ns
Q 79.	Assume a memory access to main memory on a cache "miss" takes 40 ns and a memory access to the cache on a cache "hit" takes 10 ns. If 75% of the processor's memory requests result in a cache "hit", what is the average memory access time? (a) 17.5 ns (b) 32.5 ns (c) 40.0 ns (d) 7.5 ns
Q 80.	Consider a cache with following specification • Hit rate: 92% • Hit latency: 2 cycle • Memory access time: 124 cycles What is the average memory access latency? (in cycle)_____
Q 81.	Your machine has a write-back cache. The cache read and writes times are both 2 nanoseconds. The memory read and writes times are both 50 nanoseconds. The proportion of writes is 15%, and the hit ratio is 90%. What is the average effective memory access time? (a) 6.1 nanoseconds (b) 7 nanoseconds (c) 13.45 nanoseconds (d) 3.4 nanoseconds
Q 82.	Consider a memory system with a single L1 cache that has an average access time of 100ns without L1, and 30ns with L1. L1 has an access time of 10ns. What is the hit ratio of L1 required to have an average access time of 30ns?

	(a) 90%	(b) 70%
	(c) 80%	(d) 81.8%
Q 83.	A direct mapped cache consists of eight blocks. Byte-addressable main memory contains 4K block of eight bytes each. Access time for cache is 22 ns and the time required to fill a cache slot from main memory is 300ns. (This time allows us to determine the block is missing and bring it into cache.) Assume a request is always started in parallel to both cache and to main memory. If a block is missing from cache, the entire block is brought into cache and the access is restarted. Initially, the cache is empty and cache hit rate is 80%. What is the effective access time for this program in nanoseconds? _____	
Q 84.	Consider the following memory system: • Level 1 cache: 91% hit rate, 1-cycle access time. • Level 2 cache: 98% hit rate, 15-cycle access time. • Memory: 140-cycle access time. What is the average memory access time in cycles for the above memory system?____ (Round off to two decimal places)	
Q 85.	Assume that the local hit rate for our L1 cache is 40% and the local hit rate for our L2 cache is also 40%. The hit time for the L1 cache is 5 cycles, the hit time for the L2 cache is 25 cycles, and access time for main memory is 100 cycles. The average memory access time in cycles is_____	
Q 86.	Your machine has a write-through cache. The cache read and writes times are both 2 nanoseconds. The memory read and writes times are both 50 nanoseconds. The proportion of writes is 15%, and the hit ratio is 90%. What is the average effective memory access time?	
	(a) 6.1 nanoseconds	(b) 5.9 nanoseconds
	(c) 7 nanoseconds	(d) 13.45nanoseconds
Q 87.	Consider the following cache system: • L1 has a hit time of 2 cycles, and hits 90% of the time. • L2 has a hit time of 15 cycles, and hits 95% of the time. • L3 has a hit time of 25 cycles, and hits 99% of the time. • Main Memory has an access time of 100 cycles.	

	The Average Memory Access Time (in terms of cycles) of cache is _____ (Rounded off to two decimal places)
For next three questions, consider a system with CPI of 1.2 cycles assuming memory access always results in cache hit. Processor run at 2 GHz. Consider a program running on this system has 30% Load and store instructions. The processor has an I-cache with miss rate of 2% and a D-cache with miss rate of 5%. The hit time is 1 clock cycle. The miss penalty for both the cache is 50 ns.	
Q 88.	What is the average memory access time for instruction access in clock cycles? _____
Q 89.	What is the average memory access time for data access in clock cycles? _____
Q 90.	What is the overall CPI including both instruction and data access?_____
Q 91.	A machine has a base CPI of 2 clock cycles. Assume that instruction miss rate is 12% and the data miss rate is 6%, and on average, 30% of all instructions contain one data reference. The miss penalty for the instruction and data cache is 10 cycles. What is the average CPI?_____
Q 92.	Compute the average memory access time for a 4-way set-associative, unified L2 cache with 64B blocks and a 95% hit rate. The access time for this 1MB cache is 8 cycles, and it take 80 cycles to move a 64B block from memory to the cache. _____Cycles
Q 93.	Suppose we have a cache that has an access time of 5ns, and a main memory with an access time of 80ns. If 10,000 accesses take a total of 70 microseconds. What is the miss rate of your cache?____
Q 94.	Suppose that in 1000 memory reference there are 40 misses in the first level cache and 20 misses in the second level cache. Assume miss penalty from the L2 cache to memory is 100 cycles the hit time of the L2 cache is 10 clock cycles. The hit time of the L1 cache is 1 clock cycle. If there are 1.5 memory references per instruction. What is the average stall cycle per instruction? (a) 3.4 cycles (b) 3.5 cycles

	(c) 3.2 cycles (d) 3.6 cycles
Q 95.	Consider a two-level cache hierarchy with L1 and L2 caches. An application incurs 2.8 memory accesses per instruction on average. For this application, the miss rate of L1 cache is 10%; the L2 cache experiences, on average, 10 misses per 1000 instructions. The miss rate of L2 expressed correct to two decimal places is _____.

For the next two questions, consider three machines with different cache configurations:

- Cache 1: Direct-mapped with one-word blocks
- Cache 2: Direct-mapped with four-word blocks
- Cache 3: Two-way set associative with four-word blocks

The following miss rate measurements have been made:

- Cache 1: Instruction miss rate is 4%; data miss rate is 8%.
- Cache 2: Instruction miss rate is 2%; data miss rate is 5%.
- Cache 3: Instruction miss rate is 2%; data miss rate is 4%.

For these machines, one-half of the instructions contain a data reference. Assume that the cache miss penalty is 6 + Block size in words. The ideal CPI for this workload is 2.0.

Q 96.	Which cache spends the most cycles on cache misses? (a) Cache 1 (b) Cache 2 (c) Cache 3 (d) Both a and b
Q 97.	Which cache has the best performance? (a) Cache 1 (b) Cache 2 (c) Cache 3 (d) Both b and c

INSTRUCTION SET ARCHITECTURE

Q 1. Match the following instruction to its appropriate addressing mode:

Instructions		**Addressing Mode**	
1.	MOV AL, 35H	i.	Direct Mode
2.	MOV AX,CX	ii.	Base addressing
3.	MOV AX, [BX]	iii.	Register mode
4.	ADD AL,[0301]	iv.	Register Indirect mode
5.	MOV AL,[BX+05]	v.	Immediate mode
6.	MOVL 12(R5),R3	vi.	Displacement mode

(a) 1-v, 2-iii,3-iv,4-i,5-ii, 6-vi
(b) 1-iii, 2-v,3-iv,4-i,5-ii, 6-vi
(c) 1-v, 2-iii,3-iv,4-i,5-vi, 6-ii
(d) 1-v, 2-iii,3-i,4-iv,5-ii, 6-vi

Q 2. Match List I with List II and select the correct answer. Assume that A and B are memory addresses.

List I	List II
A. Immediate addressing	1. LD A
B. Implied addressing	2. MOV R1, R2
C. Register addressing	3. SUB A, #20
D. Direct addressing	4. PUSH

(a) A – 3, B – 4, C – 2, D – 1
(b) A – 2, B – 1, C – 3, D – 4
(c) A – 3, B – 4, C – 1, D – 2
(d) A – 2, B – 4, C – 3, D – 1

Q 3. Match List-I with the List-II and select the correct answer.

List I	List II
S1: ADD R1, R2, 100(R3)[R3]	I. Displacement addressing
S2: Add R4,100(R1)	II. Scaled addressing
S3:Add R3,(R1+R2)	III. Index/base addressing
S4:Add R1,(R2)+	IV. Auto increment addressing

(a) S1 – I, S2 – II, S3 – III, S4 – IV
(b) S1 – II, S2 – I, S3 – III, S4 – IV

	(c) S1 – II, S2 – II, S3 – IV, S4 – III (d) S1 – I, S2 – III, S3 – II, S4 – IV

For the next four questions, suppose we have the instruction Load 1000. Given memory and register R1 contain the values below:

Memory

1000	1400
…	
1100	400
…	
1200	1000
…	
1300	1100
…	
1400	1300

R1: 200

Assuming R1 is implied in the indexed addressing mode; determine the actual value loaded into the accumulator using the following addressing modes:

Q 4.	In Immediate addressing the actual value loaded into the accumulator is_____
Q 5.	In Direct addressing the actual value loaded into the accumulator is _____
Q 6.	In Indirect addressing the actual value loaded into the accumulator is_____
Q 7.	In Indexed addressing the actual value loaded into the accumulator _____
Q 8.	What is the SOURCE ADDRESSING MODE for the instruction: ADD AX,[1000] //AX←MEM[1000] (a) Register Direct (b) Immediate (c) Memory Direct (d) Register Indirect
Q 9.	What is the DESTINATION ADDRESSING MODE for the instruction? ADD AX, [1000] //AX←MEM[1000] (a) Register Direct (b) Immediate

	(c) Memory Direct (d) Register Indirect
For next two questions, refer to a processor with an accumulator and two registers, R1 and R2. At some point in the execution of a program, R1 contains 40, R2 contains 50, Memory location 40 contains 50, location 50 contains 60, and location 60 contains 70.	
Q 10.	What will be the value in the accumulator A after the processor executes the following instruction? Load A, m(R1) // A ← Mem[R1] (a) 40 (b) 50 (c) 60 (d) can't be determined
Q 11.	What will be the value in the accumulator A after the processor executes the following instruction? Load A, m[R1] // A ←Mem[R2] (a) 40 (b) 50 (c) 60 (d) can't be determined
Q 12.	What will be the value in the accumulator A after the processor executes the following instruction? Loadi A, #40 // A ← 40 (a) 40 (b) 50 (c) 60 (d) can't be determined
Q 13.	Consider an 8-bit register that has the initial data 10010101. If we apply the following operations sequentially on given register: 1. Arithmetic Shift-right by one bit 2. Logical Shift-left by one bit 3. Logical Shift-right by one bit 4. Circular Shift-left by one bit 5. Circular Shift-right by one bit 6. Arithmetic Shift-left by one bit The content of 8-bit register at the end of the six operations (in binary) is____

Q 14.	What is the content of AL (in binary) after executing the following code? Assume that all register can store 8-bit data and the 2's complement number representation is used for the negative data.(Consider initial value of AL is 01010101) MOV BL, AL // BL ← AL MOV CL, 3 // CL ← 3 SHL AL, CL // left shift the contain of AL register MOV CL, 2 // CL ← 2 SHL BL, CL // left shift the contain of BL register ADD AL, BL // AL ←AL + BL (a)11111100 (b)00000100 (c) 11111000 (d) 10101010

Q 15.	A certain processor executes the following set of machine instructions sequentially.
	MOV R_0, # 0 // $R_0 \leftarrow 0$
	MOV R_1, 100(R_0) // $R_1 \leftarrow$Mem[R_0 + 100]
	ADD R_1, 200(R_0) // $R_1 \leftarrow R_1$+Mem[R_0 + 200]
	MOV 100(R_0), R_1 // [100+R0]←R1
	Assuming that memory location 100 contains the value 35 (Hex), and the memory location 200 contains the value A4 (Hex), what could be said about the final result?
	(a) Memory location 100 contains value A4
	(b) Memory location 100 contains value DA
	(c) Memory location 100 contains value D9
	(d) Given data is insufficient to decide

Q 16.	A stack-based processor executes the following set of machine instructions sequentially. 1. PUSH A 2. PUSH B 3. SUB 4. PUSH C 5. ADD 6. PUSH D 7. PUSH E 8. ADD 9. DIV 10. POP Y Initially A, B, C, D and E contain the values 20, 6, -4, 6 and 4 respectively, what is the result in Y after execution the given program? _____
Q 17.	A stack-based processor executes the following set of machine instructions sequentially. 1. PUSH 100 2. PUSH 200 3. ADD 4. POP 300 Assuming that (I) Memory location 100 contains the value 53 (Hex) and memory location 200 contains the value 4C (Hex). (II) The stack is byte organized and the stack pointer is at 00FF, and that (III) All PUSH and POP instructions have a memory operand. Which of the following could the final result be? (a) Memory location 300 contains the value 9F (b) Memory location 00FD contains the value 9F (c) Memory location 00FF contains a value 100 (d) Memory location 00FE contains a value 200

For next four questions, consider the following code fragment:

1. **loop**: SUBI R3, R1, #3 // R3 = R1 - 3
2. BEQZ R3, label1 // if R3 equals to zero jump to label1
3. ADDI R4, R4, #2 // R4 = R4 + 2
4. **label1**: ADDI R1, R1, #1 // R1 = R1 + 1
5. BNE R1, R2, loop // if R1 is not equals to R2 then jump to loop

Assume that the initial values of R1, R2 and R4 are 3, 6 and 10 respectively. After completion of the above code fragments...

Q 18.	What is the final contents of register R1?____
Q 19.	How many times instruction I_3 is executed ?_____
Q 20.	How many times instruction I_5 is executed ?_____
Q 21.	What is the final contents of register R4?_____
Q 22.	Given the 32-bits register values in two's complement representation s1 = 0X00000005 s2 = 0X00000003 s3 = 0XFFFFFFFC What will be the value of registers s1 through s4 after executing the following instructions? 1. SLT s1, s1, s2 // Set on less than (signed)if s1 < s2 then s1 = 1,otherwise s1=0 2. SLT s2, s1, s3 //Set on less than (signed)if s1 < s3 then s2 = 1,otherwise s2=0 3. SLTU s3, s1, s2 // Set on less than unsigned if s1 < s2 then s3 = 1 otherwise s3=0 4. SLTU s4, s1, s3 (a) s1=0, s2=0, s3=0 and s4=1 (b)s1=0, s2=0, s3=0 and s4=0 (c) s1=0, s2=0, s3=1 and s4=0 (d) s1=0, s2=1, s3=1 and s4=1

Q 23.	Consider the following MIPS assembly code: 1. SLT t0, t1, t2 // set t0 if t1< t2, otherwise set t0=0 2. BEQ t0, 0, X // if t0 is equal to zero then jump to label 3. BNE t3, 0, X // if t3 is not equal to zero then jump to label 4. ADDI t4, 0, 1 // t4 = 0 + 1 5. **X**: HALT // Stop execution Assume that the variables a, b, c, d, 1 and x are assigned to registers t1, t2, t3, t4, s0 and s1 respectively. Which high-level language code fragment does the above assembly code closely correspond? (a) if ((a<b) && (c==0)) d = 1; (b) if ((a<b) || (c==0)) d = 1; (c) if (a<b) d = 1; (d) none of the above
Q 24.	When a particular high-level language code fragment is compiled, it produces the following set of machine instructions. 1. MOV R_1, #j // $R_1 \leftarrow$ j 2. BEQZ R_1, label // if R_1 is equal to zero then jump to label 3. MOV R_2, #0 // $R_2 \leftarrow$ 0 4. JMP exit // unconditional jump to exit 5. label :MOV R_2, R_3 // $R_2 \leftarrow R_3$ 6. exit: HALT // Stop Assuming that values p and q are stored in registers R2 and R3 respectively, to which high-level language code fragment does the above machine code closely correspond? (a) if (j ≥ 0) p = q; else p = 0; (b) if (j ==0) q = p; else q = 0; (c) if (j ==0) p = q; else p = 0; (d) if (j == 0) p = 0; else p = q;

For the next four questions, consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

```
1.  MOV R1, (1000)          // R1 ←M[1000]
2.  MOV R2, (R3)            // R2 ←M[R3]
3.  LOOP:  ADD R2, R1       // R2 ← R1 + R2
4.  MOV (R3), R2            // M[R3] ← R2
5.  INC R3                  // R3 ← R3 +1
6.  DEC R1                  // R1 ← R1 - 1
7.  BNZ LOOP                // Branch on not zero
8.  HALT                    // Stop
```

Assume that memory location 1000 contains 100 and the base address of array is store in register R3 and the base address of array is 500. All the number is in decimal.

Memory Location	500	501	502	503	…	599	600
Contain	100	100	100	100	…	100	100

Q 25. After the completion of this program, the content of memory location 599 is: _____

Q 26. The content of memory location 600 is: _____

Q 27. How many times the instruction of program is executed:_____

Q 28. The number of memory references for accessing the data in executing the program completely is:_____

Q 29. Consider the following assembly code.

```
1. Loop: STLI t0, s0, 10   //Set on less than immediate if s0 < 10 then t0 = 1;
2. BEQ t0, zero, exit      // if t0 is equal to zero then jump to exit
3. SLL t1, s0, 2           // shift logically left s0 by 2 and store in t1
4. ADD t1, t1, s2          // t1 = t1+ s2
5. ADD t2, s1, s0          // t2 =  s1 + s0
6. SW t2, 0(t1)            // Mem[t1+ 0] = t2
7. ADDI s0, s0, 1          // s0 = s0 + 1
8. JMP Loop                // jump to loop
9. exit:                   // stop
```

Assume that the variables a and b are assigned to registers s0 and s1 respectively and

	the base address of the array D is in register s2. The initial value of variable a and b is 0 and 10 respectively. what is the value of s0 register after the execution of given code? _____

For the next two questions, consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

Instructions	Meaning
1. LOAD R_1, (R_0)	$R_1 \leftarrow M[[r_0]]$
2. ADD R_1, R_2	$R_1 \leftarrow R_1+R_2$
3. AND R_3, R_2	$R_3 \leftarrow R_3 \&\& R_2$
4. ADD R_3, R_4	$R_3 \leftarrow R_3+R_4$
5. LOAD (R_0), R_3	$M[[R_0]] \leftarrow R_3$
6. SUB R_1, R_3	$R_1 \leftarrow R_1-R_3$
7. HALT	HALT
8. OR R_2, R_1	$R_2 \leftarrow R_2 \mid\mid R_1$
9. ADD R_2, R_1	$R_2 \leftarrow R_2+R_1$

Suppose this processor has 32-bits Load/Store instruction, 16-bits ALU, BRANCH and HALT instructions. Program has been loaded in the memory with a starting address of 1000 (in decimal). Assuming the memory is word addressable and word size is 16 - bits.

Q 30.	If an interrupt occurs during the execution of the instruction "HALT", what return address will be pushed on to the stack? _____
Q 31.	Let the clock cycles required for various operations be as follows:

Instruction Type	Clock Cycles
Register to/from memory transfer	3
ADD/SUB with both operands in register	2
AND/OR with both operands in register	1
Instruction fetch and decode	2

What will be the total number of clock cycles required to execute the program___

For the next two questions, Consider the following program segment. Here R1, R2 and R3 are the general-purpose registers.

	Instruction	Operation	Instruction size (no. of words)
	MOV R1, (3000)	R1 ← m[3000]	2
LOOP:	MOV R2, (R3)	R2 ← M[R3]	1
	ADD R2, R1	R2 ← R1 + R2	1
	MOV (R3), R2	M[R3] ← R2	1
	INC R3	R3 ← R3 +1	1
	DEC R1	R1 ← R1 - 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal. Assume that the memory is word addressable.

Q 32.	The number of memory references for accessing the data in executing the program completely is_____
Q 33.	Assume that the memory is word addressable. After the execution of above program, the content of memory location 2010 is_____
Q 34.	A processor has 40 distinct instruction and 24 general purpose registers. A 32-bit instruction word has an opcode, two registers operands and an immediate operand. The number of bits available for the immediate operand field is (if fixed size instruction format is used) _____.
Q 35.	There are 50 registers and total 55 instructions available in a general-purpose computer.

	The computer allows only 2-address instructions, where one operand is a register and another is a memory location. The memory is byte addressable with 64KB in size. The minimum number of bits to encode the instruction will be _____.

For next three questions consider the system that has a memory unit with 16 bits per word. The instruction set consists of 200 different operations. All instructions have an operation code part (opcode) and an address part (allowing for only one address). Each instruction is stored in one word of memory.

Q 36.	How many bits are needed for the opcode? _____
Q 37.	How many bits are left for the address part of the instruction? _____
Q 38.	If the memory is byte addressable then the maximum allowable size for memory (in bytes) is _____

For next two questions, suppose a 32-bit instruction uses register addressing mode with the following format:

OPCODE	DEST	SRC1	SRC2

Assume that there are 242 opcodes in the instructions set and 64 registers in register set

Q 39.	The minimum number of bits required to represent the opcodes is_____
Q 40.	Let the minimum number of bits required to represent the SRC1, SRC2 and DEST registers are x, y and z respectively, then the value of x+y+z is _____
Q 41.	Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is _____.

Q 42.	A computer uses extensible opcode technique. It has 16-bit instructions which have 6-bits address field. It supports one address, two address instructions only. If there are eight two address instructions, then the maximum numbers of one address instructions are_____

For the next four questions, in a computer instruction format, the instruction length is 11 bits and the size of an address field is 4 bits. The computer support:

- 2-address instructions
- 1-address instructions
- 0-address instructions

All three type of instruction must be exist in the computer (i.e. there is at least one instruction from each type)

Q 43.	What is the maximum number of instruction with 0-address?_____
Q 44.	What is the maximum number of instruction with 1-address?_____
Q 45.	What is the maximum number of instruction with 2-address?_____
Q 46.	How many maximum number of instruction supported by this computer?_____
Q 47.	Consider a machine with x bits long instruction and 8 registers. We need to use 3 bits to specify a unique register. Suppose machine encode the following class of instructions: Class A: 4 instructions with 2 registers Class B: 255 instructions with 1 register Class C: 16 instructions with 0 registers The minimum value of x in the extensible opcode technique to encode the above class of instruction is_____

For next two questions, consider the machine in which instructions are 12 bits in length and addresses are 4 bits in length. There are 3 classes of instructions:

Class A: 2 addresses
Class B: 1 address
Class C: 0 addresses

All three type of instruction must be exist in the computer (i.e. there is at least one instruction from each type)

Q 48.	What is the maximum total number of instruction possible in machine?_____
Q 49.	What is the minimum total number of instruction possible in machine?_____
Q 50.	Consider a machine where each instruction is 4 bytes long. Conditional and unconditional branch instructions use PC-relative addressing mode with Offset specified in bytes to the target location of the branch instruction. Also, the Offset is always with respect to the address of the next instruction in the program sequence.

	Consider the following instruction sequence: Instruction i: DD R2,R3,R4 Instruction i+1: SUB R5,R6,R7 Instruction i+2: SEQ R1,R9,R10 Instruction i+3: ADD R1, R2, R3 Instruction i+4: BEQZ R1, Offset If the target of the branch instruction is i, the decimal value of Offset will be_____

INSTRUCTION PIPELINE

For next six questions, suppose we have the following functional units with the given latencies in a processor:

IF	2 ns
ID	2 ns
EX	3 ns
MEM	6 ns
WB	2 ns

Q 1. If we use these units to build a single-cycle implementation (non-pipeline), what is the cycle time (in ns) of pipeline processor?_____

Q 2. How long (in ns) does it take to execute a single instruction in non-pipeline processor?_____

Q 3. If we use these units to build our usual 5-stage pipeline processor, what is the cycle time of pipeline processor?_____

Q 4. How long (in ns) does it take to execute a single instruction in pipeline processor?_____

Q 5. How long does it take to execute N instructions using this pipeline, where N is some arbitrary large number?

(a) (6N) ns

(b) (6 × 5+(N – 1) × 6) ns

(c)6 × (4+N) ns

(d)Both(b)&(c)

Q 6.	What is the speedup of this pipelined processor over the non-pipeline processor?_
Q 7.	What is the cycle time for non-pipelined processor and what is the latency of an instruction? (a) 550ps, 2750ps (b) 570ps, 2850ps (c) 1700ps, 1700ps (d) 1800ps, 1800p
Q 8.	What is the cycle time for pipelined processor and what is the latency of an instruction? (a) 550ps, 2750ps (b) 570ps, 2850ps (c) 550ps, 2850ps (d) 1800ps, 1800ps
Q 9.	What is the throughput (in MIPS) of the non-pipelined and pipelined respectively? (a) 588.24, 1754.39 (b) 555.56, 1754.39 (c) 555.56, 1818.18 (d) 588.24, 1818.18
Q 10.	Comparing the time T1 taken for a single instruction on a pipelined CPU with time T2 taken on a non-pipelined but identical CPU, we can say that (a) T1 ≥ T2 (b) T1 ≤ T2 (c) T1 < T2 (d) T1 is T2 plus the time taken for one instruction fetch cycle
Q 11.	A non pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 1nsec, 1.5nsec, 4nsec, 3nsec, and 0.5nsec, respectively. The speedup of the pipeline processor for a large number of instructions is_____
Q 12.	A non pipelined single cycle processor operating at 100 MHz is converted into a synchro-nous pipelined processor with five stages requiring 2.5nsec, 1.5nsec, 2nsec, 1.5nsec and 2.5nsec, respectively. The delay of the latches is 0.5nsec. The speedup of the pipeline processor for a large number of instructions is (a) 4.5 (b) 4.0 (c) 3.33 (d) 3.0

Q 13.	Consider a 5-stage single cycle machine (non-pipeline), and a 5-stage pipeline machine. The cycle time of the non-pipeline is five times that of pipeline. Assume that there are no stalls in the pipeline. What is the speedup achieved over non-pipeline if pipeline phase time is 2 ns? _____
Q 14.	A pipeline P operating at 1 GHz has a speedup factor of 5 and operating at 60% efficiency. How many stages are there in the pipeline?_____
Q 15.	Consider two different machines; the first has a single cycle data path i.e., a single non pipelined machine with a cycle time of 4 ns. The second is a pipelined machine with four pipeline stages and a cycle time of 1 ns. What is the speedup of the pipeline machine versus the single cycle machine for the very large number of instructions?_____
Q 16.	In a 5-stage pipelined system, assume that stages 1 and 4 take 2ns each, stages 2 and 5 take 3ns each, and stage 3 takes 1ns. What is the speed-up attained for the pipelined system as compared to the non-pipelined system, if 50 instructions are executed? (a)2.500 (b)3.333 (c)3.395 (d)3.667
Q 17.	Suppose the four stages in a 4-stage pipeline take the following timing: 2ns, 3ns, 4ns, and 2ns. Given 1000 instructions, what is the speedup of the pipelined processor compared to the non-pipelined single-cycle processor?_____
Q 18.	The five stages of a certain pipeline take 2 ns, 3 ns, 4 ns, 5 ns, and 2 ns. If there are 20 instructions, what is the maximum speed up in the execution time of a pipeline implementation compared to a single-cycle implementation? (a) 2.50 (b) 2.67 (c) 5.00 (d)3.20
Q 19.	Consider the 5 stages of the processor have the following latencies:

Fetch	Decode	Execute	Memory	Write back
300ps	400ps	350ps	500ps	100ps

Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages. If you could split one of the pipeline stages into 2 equal halves, which one would you choose?

(a) Write back (b) Fetch

(c) Decode (d) Memory

Q 20. The stage delays in a 5-stage pipeline process are 800nsec, 400nsec, 900nsec, 400nsec and 300nsec, respectively. The third stage is replaced with a functionality equivalent design involving three stages with respective delays 550nsec, 350nsec and 350nsec. What will be change in the throughput of the pipeline processor?

(a) It is increases by 12.5%

(b) It is decreases by 12.5%

(c) It is increases by 12.25% increase

(d) It is decreases by 12.25%

Q 21. The stage delays in a 4 stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput increase of the pipeline is _____%.

For the next two questions, Consider a system in which it takes 8 cycles to complete execution of instruction and clock period is 0.5 ns.

Q 22. What is the Clock frequency of the machine? _____GHz

Q 23. What is the total number of instructions per second executed by system (in million)? ___

Q 24. If a non-pipelined processor had a maximum clock rate of 500 MHz and was converted to a perfectly balanced 10-stage pipeline, what would the pipelined processor's maximum clock rate be?

(a) 0.5 GHz (b) 500 GHz (c) 5 GHz (d) 50 GHz

Q 25. A single-cycle processor design with a 1 GHz clock is converted to a ten-stage, perfectly

	balanced, pipelined design. What will be the clock period of the new design? (a) 0.1 GHz (b) 10 GHz (c) 1000 GHz (d) 100 GHz
Q 26.	Consider a non-pipelined processor with a clock rate of 2.5 GHz and average cycles per instruction of 5. The same processor is upgraded to a pipelined processor with five stages but due to the internal pipeline delay, the clock speed is reduced to 2 GHz. Assume there are no stalls in the pipeline. The speed up achieved in this pipelined processor is_____
Q 27.	A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Instruction Execution (IE), Memory Access (MA) and Write Back (WB) stages. All stages take 1 clock cycle each for any instruction. Consider the following code fragment: Instruction Meaning of instruction Load R1, [1000] // R1 = M[1000] Load R3, 5(R2) // R3 = M[R2 + 5] MUL R4, R1, R6 // R4 = R1 x R6 DIV R5, R1, R6 // R5 = R1 / R6 SUB R6, R2, R7 // R6 = R2 – R7 What is the number of clock cycles needed to execute the above sequence of instructions on 5-stage pipeline processer? _____
Q 28.	A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Instruction Execution (IE), Memory Access (MA) and Write Back (WB) stages. All stages take 1 clock cycle each for any instruction. Consider the following code fragment: Instruction Meaning of instruction Load R1, [1000] // R1 = MEM[1000] Load R3, 5(R2) // R3 = MEM[R2 + 5] MUL R4, R1, R3 // R4 = R1 x R3 DIV R5, R1, R4 // R5 = R1 / R4 SUB R6, R4, R5 // R6 = R4 – R5 What is the number of clock cycles needed to execute the above sequence of instructions on 5-stage pipeline processer? _____
Q 29.	A 5-stage classical pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Instruction Execution (IE), Memory Access (MA) and Write Back (WB) stages. All stages take 1 clock cycle each for any instruction. Consider the following code fragment:

	Instruction Meaning of instruction
	MOV R3, R7 // R3←R7
	LD R8, (R3) // R8 = MEM[R3]
	ADD R3, R3, 4 // R3 = R3 + 4
	LOAD R9, (R3) // R9 = MEM[R3]
	What is the number of clock cycles needed to execute the above sequence of instructions on 5-stage pipeline processer? _____

Q 30.	A 5-stage classical pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), and Instruction Execute (EX), Memory Access (MA) and Write Back (WB) stages. The IF, ID, MA and WB stages take 1 clock cycle each for any instruction. The EX stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Consider the following sequence of instructions: Instruction Meaning of instruction I_0:MUL R_2 ,R_0 ,R_1 $R_2 \leftarrow R_0 * R_1$ I_1:DIV R_5 ,R_3 ,R_4 $R_5 \leftarrow R_3 / R_4$ I_2: ADD R_2 ,R_5 ,R_2 $R_2 \leftarrow R_5 + R_2$ I_3:SUB R_5 ,R_2 ,R_6 $R_5 \leftarrow R_2 - R_6$ What is the number of clock cycles needed to execute the above sequence of instructions? _____
Q 31.	Consider a pipelined processor with the following four stages: Instruction Fetch (IF), Instruction Decode and Operand Fetch (ID), Instruction Execute (EX), and Write Back (WB). The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle, the MUL instruction needs 3 clock cycles and the DIV instruction needs 5 clock cycles in the EX stage respectively. Consider the following sequence of instructions: Instruction Meaning of instruction I0: MUL R2 ,R0 ,R1 R2 ← R0 * R1 I1: DIV R5 ,R3 ,R4 R5 ← R3 / R4 I2: ADD R2 ,R5 ,R2 R2 ← R5 + R2 I3: SUB R5 ,R2 ,R6 R5 ← R2 - R6 What is the number of clock cycles taken to complete the following sequence of instructions?_____
Q 32.	The instruction pipeline of a RISC processor has the following stages: Instruction

	Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB). The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 30 instructions take 3 clock cycles each, 30 instructions take 2 clock cycles each, and the remaining 40 instructions take 1 clock cycle each. Assume that there are no stalls in the pipeline. The number of clock cycles required for completion of execution of the sequence of instructions is _____.

Q 33.	A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Instruction Execution (IE), Memory Access (MA) and Write Back (WB) stages. All stages take 1 clock cycle each for any instruction. Consider the following code fragment:
	Instruction Meaning of instruction
	I1: LOAD R2, 0(R1) // R2 = MEM[R1+0]
	I2: LOAD R1, 40(R3) // R1 = MEM[R3 + 40]
	I3: SUB R3, R1, R2 // R3 = R1 - R2
	I4: ADD R3, R2, R2 // R3 = R2 + R2
	I5: OR R4, R3, 0 // R4 = R3 || 0
	I6: STORE R3, 50(R1) // MEM[R1+50] = R3
	What is the number of clock cycles needed to execute the above sequence of instructions on 5-stage pipeline processer with operand forwarding? _____

Q 34.	A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Instruction Execution (IE), Memory Access (MA) and Write Back (WB) stages. All stages take 1 clock cycle each for any instruction. Consider the following code fragment:
	Instruction Meaning of instruction
	I1: LOAD R2, 0(R1) // R2 = MEM[R1+0]
	I2: LOAD R1, 40(R3) // R1 = MEM[R3 + 40]
	I3: SUB R3, R1, R2 // R3 = R1 - R2
	I4: ADD R3, R2, R2 // R3 = R2 + R2
	I5: OR R4, R3, 0 // R4 = R3 || 0
	I6: STORE R3, 50(R1) // MEM[R1+50] = R3
	What is the number of clock cycles needed to execute the above sequence of instructions on 5-stage pipeline processer without operand forwarding but the register file can be

	read and written in the same cycle. The write takes place during the first half of the cycle and the read takes place during the second half of the cycle? _____
Q 35.	A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation(PO)and Write Operand(WO)stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 2 clock cycles for ADD and SUB instructions, 5 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Assume no operand forwarding but a split-cycle register file (i.e. the register file can be read and written in the same cycle.) is in used. Instruction Meaning of instruction I0: MUL R2, R0, R1 //R2 ← R0 *R1 I1: DIV R5, R3, R4 //R5 ← R3/R4 I2: ADD R2, R5, R2 //R2 ← R5+R2 I3: SUB R5, R2, R6 //R5 ←R2-R6 What is the number of clock cycles needed to execute the following sequence of instructions?_____

Q 36.	Consider a 2GHz pipelined processor with the following four stages: Instruction Fetch (IF), Instruction Decode and Operand Fetch (ID), Execute (EX) and Write Back (WB). The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 2 clock cycle and the MUL instruction needs 5 clock cycles in the EX stage.
	Instruction Meaning of instruction
	ADD R2, R1, R0; //R2+Rl→R0
	MUL R0, R3, R4; //R0*R3→R4
	SUB R4, R5, R6; // R4 – R5 → R6
	Operand forwarding is not used in the pipelined processor. What is the time (in

	ns) to complete the above instruction? _____

Q 37.	Consider the ideal five stage in-order pipelining processor and the following sequence of instructions is executed on the processor: Instruction Meaning of instruction ADD R1, R2, R3 // R1 ← R2 + R3 SUB R4, R5, R6 // R4 ← R5 – R6 SUB R7, R8, R9 // R7 ← R8 + R9 ADD R10, R11, R12 // R10 ← R11 + R12 ADD R13, R14, R15 // R13 ← R14 + R15 During the fifth cycle of execution, which registers (in the register file) are being read and which register will be written? (a) Written: R1; Read: R12, R11 (b) Written: R1, R12; Read: R11 (c) Written: R11; Read: R12 (d) Written: None; Read: R12, R11

Q 38.	Consider the ideal five stage in-order pipelining and the following sequence of instructions is executed on the processor:
	Instruction Meaning of instruction
	LW R1, 0(R0); // R1 = MEM[0 + R0]
	LW R2, 4(R0; // R2 = MEM[4 + R0]
	ADD R3, R1, R2; // R3= R1 + R2
	SW R3, 8(R0); // MEM[8+R0] = R3
	LW R4, 12(R0); // R4 = MEM[12 + R0]
	ADD R5, R3, R4; // R5 = R3 + R4
	SW R5, 16(R0); // MEM[16+R0] = R5

	The number of RAW, WAR and WAW data dependencies exist in this code respectively is (a) 5, 1, 2 (b) 6, 0, 2 (c) 4, 1, 1 (d) 6, 0, 0
Q 39.	Consider the ideal five stage in-order pipelining processor and the following sequence of instructions is executed on the processor: Instruction Meaning of instruction ADD R1, R2, R3 // R1 ← R2 + R3 ADD R4, R2, R1 // R4 ← R2 + R1 LW R5, 0(R4) // R5 ← MEM[200 + R4] ADD R4, R5, R4 // R4 ← R5 + R2 If the operand forwarding is not used then how many data dependencies can create hazards? _____

Q 40.	Consider the ideal five stage in-order pipelining processor and the following sequence of instructions is executed on the processor:
	Instruction Meaning of instruction
	LW R1, 40(R2) // R1 ← MEM[40 + R2]
	ADD R2, R3, R0 // R2 ← R3 + R0
	ADD R1, R1, R2 // R1 ← R1 + R2
	SW R1, 20(R2) // MEM[20 + R2] = R1
	How many ANTI, TRUE and OUTPUT dependencies respectively are there in the above code?
	(a) 1, 3, 1 (b) 1, 4, 1
	(c) 1, 3, 2 (d) 1, 4, 2

Q 41.	Consider the ideal five stage in-order pipelining and the following sequence of instructions is executed on the processor: Instruction Meaning of instruction ADD R4, R2, R3 // R4 ← R2 + R3 SW R2, 100(R6) // MEM[100 + R6] = R2

	LW R5, 200(R4) // R5 ← MEM[200 + R4] SUB R5, R8, R6 // R5 ← R8 – R6 The number of RAW, WAR and WAW data dependencies exist in this code respectively is (a) 2,1,1 (b) 1,0,1 (c) 1,1,1 (d) 1,1,0
Q 42.	Consider the ideal five stage in-order pipelining processor and the following sequence of instructions is executed on the processor: Instruction Meaning of instruction ADDi R7, R7, 1 // R7 ← R7 + 1 SLL R8, R7, 2 // Shift R7 logical left by 2 bit ADD R8, R8, R14 // R8 ← R8 + R14 LW R8, 0(R8) // R8 ← MEM[0 + R8] LW R8, 0(R8) // R8 ← MEM[0 + R8] BNE R7, R22, TARGET // if R7 ≠ R22 then jump to target Let the number of RAW, WAR and WAW dependencies exists in the code is x, y and z respectively, then the value of x + y + z is_____
Q 43.	Consider a machine that has ideal five stage in-order pipelining processor. The machine uses delay slots to handle control dependences. The Jump targets, branch targets and destinations are resolved in the execute stage. What is the number of delay slots needed to ensure correct operation of pipeline processor?_____
Q 44.	Consider a machine that has ideal five stage in-order pipelining processor. Instruction Meaning of instruction I1. ADD R5, R4, R3 // R5 ← R4 + R3 I2. OR R3, R1, R2 // R3 ← R1 || R2 I3. SUB R7, R5, R6 // R7 ← R5 – R6 I4. Jump X // Jump to lable X I5. LW R10, (R7) // R10 ←MEM[R7] I6. ADD R6, R1, R2 // R6 ← R1 + R2

	I7. X: HALT Which instruction(s) in the assembly sequences above would you place in the delay slot(s)? Assume that the number of available delay slots is 2. (a)1st and 2nd instruction (b) 2nd and 3rd instruction (c) 2ndinstruction (c)Delay slot cannot be filled.
Q 45.	Consider a machine that has ideal five stage in-order pipelining processor. Instruction Meaning of instruction I1. ADD R5, R4, R3 // R5 ← R4 + R3 I2. OR R3, R1, R2 // R3 ← R1 || R2 I3. SUB R7, R5, R6 // R7 ← R5 – R6 I4. BEQ R5, R7, X // if R5 == R7 then jump to x I5. LW R10, (R7) // R10 ←MEM[R7] I6. ADD R6, R1, R2 // R6 ← R1 + R2 I7. X: HALT Which instruction(s) in the assembly sequences above would you place in the delay slot(s)? Assume that the number of available delay slots is 2. (a)1st and 2nd instruction (b) 2nd and 3rd instruction (c) 2nd only (d) Delay slot cannot be filled.
Q 46.	Consider a machine that has ideal five stage in-order pipelining processor. Instruction Meaning of instruction I1. ADD R2, R4, R3 // R2 ← R4 + R3 I2. OR R5, R1, R2 // R5 ← R1 || R2 I3. SUB R7, R5, R6 // R7 ← R5 – R6 I4. BEQ R5, R7, X // if R5 == R7 then jump to x I5. LW R10, (R7) // R10 ←MEM[R7] I6. ADD R6, R1, R2 // R6 ← R1 + R2 I7. X: HALT

	Which instruction(s) in the assembly sequences above would you place in the delay slot(s)? Assume that the number of available delay slots is 2. (a)1st and 2nd instruction (b) 2nd and 3rd instruction (c) 1st Only (d) Delay slot cannot be filled.

Q 47.	Consider a machine that has ideal five stage in-order pipelining processor.
	Instruction — Meaning of instruction
	I1. L1: LOAD R1, 8(R2) // R1 ←MEM[8 + R2]
	I2. ADD R3, R1, R8 // R3 ← R1 + R8
	I3. SUB R2, R1, R4 // R2 ← R1 – R4
	I4. STORE R7, 12(R2) // MEM[12 + R2] = R7
	I5. ADD R6, R2, R5 // R6 ← R2 + R5
	I6. BEQ R6, R7, L1 // if R6 == R7 then jump to L1
	Which instruction(s) in the assembly sequences above would you place in the delay slot(s)? Assume that the number of available delay slots is 2.
	(a) I_2 and I_4 instruction
	(b) I_3 and I_4instruction
	(c) I_2 and I_3instruction
	(d)Delay slot cannot be filled.

Q 48.	Register renaming solves the problem of: (a) Name Dependence (b) Output Dependence (c) Anti-Dependence (d) All of the above
Q 49.	**[MSQ]** Which of the following statements about pipelining is/are incorrect? (a) Pipelining reduces the latency of a single instruction. (b) Pipelining is invisible to the programmer. (c) Stalling the pipeline is the only method to handle structural hazards.

	(d)In pipeline memory reference may cause data hazards. (e)Bypassing and forwarding eliminates all data hazards.
Q 50.	Consider a classical 5 stage pipelined processor executes a program that consists of 50,000 instructions. Because of hazards 10% of instructions are stalled by one cycle, 15% by 2 cycles and 10% by 3 cycles. How many cycles take execution of this program? _____
Q 51.	Consider a 8-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 8-stage pipeline, the speedup achieved with respect to non-pipelined execution if 30% of the instructions incur 2 pipeline stall cycles is_____
Q 52.	Consider a processor with following specifications Clock Rate: 0.5 GHz CPI for ALU instructions: 1 CPI for Control instructions: 2 CPI for Memory instructions: 2.7 The average instruction execution time (in ns) for a program with 70% ALU instructions, 1% control instructions and 29% memory instructions is_____ (Rounded off to three decimal places)
Q 53.	A program's execution time is 100 seconds. Suppose FP instructions account for 30% of the execution time of the program and multiply instructions account for 10% of the execution time. How much faster would the program execute if we speed up FP instructions by a factor of 3 and multiply instructions by a factor of 5? _____ (Rounded off to three decimal places)
Q 54.	Adding a faster floating-point unit to a machine will give a speedup of 5 on FP instructions. The FP instructions make up 10% of the dynamic instruction count on the original machine and the average CPI for FP instructions on the original machine is 9 cycles and the average CPI for all other instructions on the original machine is 1 cycle. What is the overall speedup of the machine due to this modification?_____ (Rounded off to three decimal places)

For next three questions, consider a program has 10^9 instructions and 50% of these instructions are memory instructions. This program is executed on a processor that runs on a 2-GHz clock, executes the memory instructions in an average 4.0 CPI, and executes the other instructions in an average 1.0 CPI.	
Q 55.	What is the overall average CPI of program? _____
Q 56.	What is the time needed to execute this program? _____nsec
Q 57.	What is the speedup when the memory instructions are improved by a factor of 4? ____
Q 58.	Consider a non-pipelined processor with a clock rate of 5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2.5 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is _____.
Q 59.	Consider a program running on a 5-stage pipeline processor; assume that 25% instructions of program cause a single-cycle stall. If forwarding can eliminate 60% of the stalls, but increases the clock cycle by 20%, what is the speedup obtained by using forwarding? _____
Q 60.	What is the average CPI of a processor with base CPI as 1, if it has 2 branch delay slots, 20% of the instructions are branches, and the branch delay slots can be filled only 50% of the time?_____

Q 61.	Consider the following code consisting of 100 load instructions in which each instruction is dependent on the instruction immediately preceding
	LW R2, 0(R1)
	LW R3, 0(R2)
	LW R4, 0(R3)
	...
	What would the average CPI be for this code in the 5-stage pipelined processor without forwarding? _____

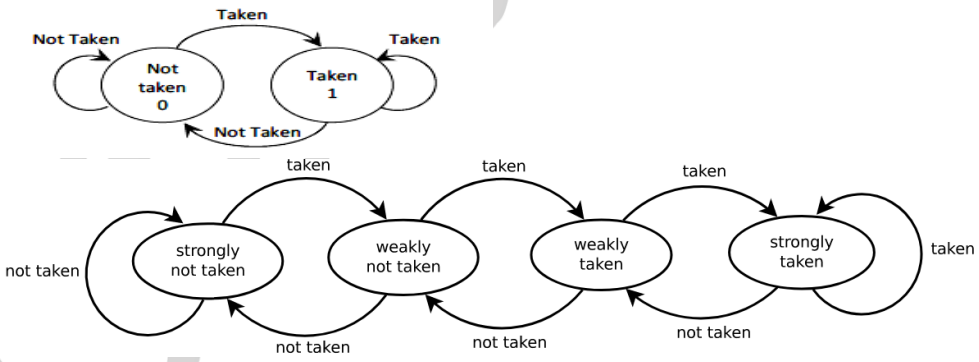
Q 62.	Consider the following code consisting of 100 load instructions in which each

	instruction is dependent on the instruction immediately preceding
	LW R2, 0(R1)
	LW R3, 0(R2)
	LW R4, 0(R3)
	...
	What would the average CPI be for this code in the 5-stage pipelined processor with forwarding? _____

Q 63.	Assume a processor with instruction frequencies and costs • Integer ALU: 50%, 1 cycle • Load: 20%, 5 cycles • Store: 10%, 1 cycles • Branch: 20%, 2 cycles Which change would improve performance more of the processor? **i.** Branch prediction to reduce branch cost to 1 cycle. **ii.** Faster data memory to reduce load cost to 3 cycles. (a) (i) will improve performance (b) (ii) will improve more performance (c) Both improve same performance (d) Nothing improved performance
Q 64.	Consider two machines M1 and M2. For both machines, all instructions except for mispredicted branches take one cycle. Mispredicted branches take one cycle plus an additional misprediction penalty. • Machine A has a clock rate of 1.0 GHz and a misprediction penalty of 5 cycles. • Machine B has a clock rate of 2.0 GHz and a misprediction penalty of 20 cycles. Branches are 25% of all instructions and 80% of branches are predicted correctly. Which of the following statement is correct? (a) Machine A is faster than Machine B (b) Machine B is faster than Machine A (c) Both are same (d) None of these

Q 65.	Consider a 5-stage pipeline processor with operand forwarding, where branches are resolved in the 4th stage. A given program consists of 30% loads, 5% stores, 15% branches and 50% ALU operations. If 30% of the branches are not-taken and only 40% of load instructions are dependent on the instruction in front of them, what is the expected CPI of the processor on this program?_____(round off to 3 decimal places)
Q 66.	Consider a program with branch frequencies (as percentage of all instructions) as follows: Conditional branches 15% out of which 60% are taken, Jumps and calls 1%. This program is executed on a 5-stage pipelined processor where unconditional branches are resolves at second phase and conditional branches at the third phase of the pipeline. Assuming that only the branch instructions results in stall how much faster would the machine be without any branch hazards? _____
Q 67.	Consider that we have a machine with 7-stage pipeline: IF, ID1, ID2, EX, M1, M2, and WB. The branch is resolved at the end of the third cycle for unconditional branches and at the end of the forth cycle for conditional branches. Suppose that 20% of all instructions are conditional branches out of which 60% are taken and 5% are unconditional branches or procedure calls. Assume that only the branch instructions results in stall. What is the CPI for this machine?_____
Q 68.	Consider that we have a machine with 7-stage pipeline: IF, ID1, ID2, EX, M1, M2 and WB. Branch target addresses are calculated in ID2 and branch conditions are evaluated in EX. Assume a base CPI of 1 without any stall. Assume 30% conditional branch frequency and 80% of these are taken. How much faster is the machine with predicted-taken branch prediction than with predicted-not-taken scheme?_____
Q 69.	Consider a 5-stage non-pipelined processor with 2 GHz clock. To improve the performance the processor is converted into 5-stage pipeline. Assume that due to pipeline registers, pipelining the processor lengthens the clock cycle period by 10%. The processor uses a unified cache for data and instruction accesses, resulting in a structural hazard between IF and MEM stages. Suppose that data references represent 30% of the

	instructions executed and that the CPI of the pipelined processor, ignoring the structural hazard is 1. How much speedup can we gain from pipelining?____ ____(round off to 1 decimal place)

Q 70.	An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode (ID), instruction execution (EX), memory access (MEM), and write back (WB) with stage latencies 1 ns, 3 ns, 2 ns, 1 ns, and 0.75 ns, respectively. To gain in terms of frequency, the designers have decided to split the ID stage into three stages (ID1, ID2, ID3) each of latency 1 ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds, respectively. The value of P/Q is _____.
For the next two questions, consider state diagram of the 1- bit and 2-bit dynamic branch predictor as show in figure: 	
Q 71.	Assume that 1 indicates a taken branch and 0 indicate not taken branch. Assume also that this predictor starts in the "Not taken" state. What is the accuracy (in percent) of a 1-bit predictor if the last 24 instance of this branch pattern is 1,1,1,1,0,0,0,1,1,1,1,0,0,0,1,1,1,1,0,0,0,1,1 and 1? Assume that the most recent branch is

	represented in the least significant bit._____
Q 72.	Assume that 1 indicates a taken branch and 0 indicate not taken branch. Assume also that this predictor starts in the '"strongly not taken" state. What is the accuracy (in percent) of a 2-bit predictor if the last 24 instance of this branch pattern is 1,1,1,1,0,0,0,1,1,1,1,0,0,0,1,1,1,1,0,0,0,1,1 and 1? Assume that the most recent branch is represented in the least significant bit._____

INPUT-OUTPUT AND CONTROL UNIT	
Q1.	If a magnetic disc has 1024 cylinders, each containing 512 tracks of 256 sectors each, and each sector can contain 128 bytes, what is the maximum capacity (in GB) of the disk in bytes?_____
Q2.	According to the specifications of a particular hard disk a seek takes 3 msecs (thousandths of a second) between adjacent tracks. If the disk has 100 cylinders how long will it take for the head to move from the innermost cylinder to the outermost cylinder? (a) 30 microseconds (b) 300 msecs (c) 297 msecs (d) 3 microseconds
Q3.	Consider a disk pack with a seek time of 3 milliseconds and rotational speed of 10,000 rotations per minute (RPM). It has 600 sectors per track and each sector can store 8K (2^{13}) bytes of data. How long (in milliseconds) does it take to read a random single sector on average? _____
Q4.	A hard disk system has the following parameters: • Number of tracks = 500 • Number of sectors/track =100 • Number of bytes/sector =500 • Average seek time: 250 ms • Rotation speed =6000 rpm. What is the average time (in ms) taken for transferring a sector from the disk?
Q5.	A hard disk system has the following parameters: • Number of tracks = 3000 • Number of sectors/track = 600 • Time taken by the head to move from one track to adjacent track =1 ms • Rotation speed = 7200 rpm. What is the average time (in ms) taken for reading a random sector from the disk____ (round up two decimal place)

For the next two questions, consider a disk with average seek time of 4 ms, rotation speed of 15,000 rpm, and 512-byte sectors with 500 sectors per track. Suppose that we wish to read a file consisting of 2500 sectors for a total of 1.28 Mbytes.	
Q6.	What is the minimum total time (in ms) for the transfer the file if the *sequential organization* is used i.e. the file occupies all of the sectors on 5 adjacent tracks (5 tracks × 500 sectors/track = 2500 sectors)? _____
Q7.	Consider the same hard disk given in the previous question. What is the minimum total time (in sec) for the transfer the file if the *random organization* is used rather than *sequential organization*, that is, accesses to the sectors are distributed randomly over the disk? _____
Q8.	A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple ⟨*C*, *H*, *S*⟩, where *C* is the cylinder number, *H* is the head/surface number and *S* is the sector number. Thus, the 1st sector is addresses as ⟨0, 0, 1⟩, the 2nd sector as ⟨0, 0, 2⟩, and so on. The address ⟨400, 16, 29⟩ corresponds to sector number: _____
Q9.	Consider a hard disk with 16 recording surfaces (0-15) having 16384 cylinders (0-16383) and each track contains 64 sectors (0-63). Data storage capacity in each sector is 512 bytes. Data are organized cylinder-wise and the addressing format is ⟨Cylinder #, Surface #, Sector #⟩. A file of size 42797 KB is stored in the disk and the starting disk location of the file is ⟨1200, 9, 40⟩. What is the cylinder number of the last sector of the file, if it is stored in a contiguous manner? _____
Q10.	When the processor constantly checks the status of an I/O device, this is called: (a) Memory mapped I/O (b) Asynchronous communication (c) Interrupt-Driven I/O (d) Polling

Q11.	What advantage(s) does Interrupt-Driven I/O have over polling? (a) Interrupt-Driven I/O is synchronous while polling is asynchronous (b) Interrupt-Driven I/O does not require any additional hardware (c) Interrupt-Driven I/O allows the computer to process other tasks while waiting for I/O (d) Interrupt-Driven I/O can be memory-mapped while polling cannot
Q12.	**[MSQ]** Which of the following statements below is/are true? (a) In polling, I/O devices set flags that must be periodically checked by the CPU (b) When using interrupts, the CPU interrupts I/O devices when an I/O event happens (c) The overhead of polling depends on the polling frequency (d) Polling is often a viable option for slow and asynchronous devices
Q13.	When the processor treats I/O devices as locations in memory and uses the same instructions to access them, this is called: (a) Memory mapped I/O (b) Asynchronous communication (c) Synchronous communication (d) Interrupt-Driven I/O
Q14.	**[MSQ]** Which of the following is /are advantages of cycle stealing in DMA. (a) It increases the maximum I/O transfer rate. (b) It reduces the interference by the DMA controller in the CPU's memory access. (c) It is beneficially employed for I/O device with shorter bursts of data transfer. (d) None of the above
Q15.	The main reason for implementing DMA in a computer system is (a) To free off the CPU from cache coherency problems. (b) To simplify the writing of interrupt service routines (c) To remove the need for a buffer on the device interface (d) To speed up the transfer of data between an interface and the main memory

Q16.	In a non-vectored interrupt, the address of interrupt service routine is (a) Obtained from interrupt address table. (b) Supplied by the interrupting I/O device. (c) Obtained through Vector address generator device. (d) Assigned to a fixed memory location.
Q17.	Which of the following I/O methods requires the CPU to initialize the I/O device? i. Programmed I/O ii. Interrupt driven I/O iii. Direct memory access (a) ii and iii only (b) iii only (c) i and ii only (d) All of the above
Q18.	Which of the following I/O methods requires the CPU be able to use interrupts? i. Programmed I/O ii. Interrupt driven I/O iii. Direct memory access (a) ii and iii only (b) iii only (c) i and ii only (d) All of the above
Q19.	Which of the following I/O methods requires the CPU to act as a bridge for moving data between the I/O device and main memory? i. Programmed I/O ii. Interrupt driven I/O iii. Direct memory access (a) ii and iii only (b) iii only (c) i and ii only (d) All of the above
Q20.	A vectored interrupt is one which (a) Does not require all device interfaces to be polled (b) Does not require the cpu to check the interrupt line at the end of each" Fetch and Execute" cycle (c) Reduces the number of control lines needed on the bus (d) Removes the need to enable interrupts on the interface

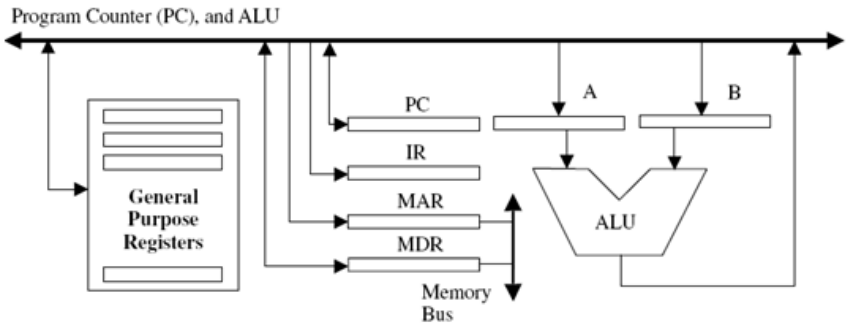
Q21.	In order to execute a program, instructions must be transferred from memory along a bus to the CPU. If the bus has 8 data lines, at most one 8 bit byte can be transferred at a time. How many memory accesses would be needed in this case to transfer a 32 bit instruction from memory to the CPU? (a) 1 (b) 2 (c) 3 (d) 4
Q22.	Consider a printer which can print 20 pages per minute where a page consists of 4000 characters (1 character = 1 byte). it takes 50 microseconds by CPU to handle a interrupt. How much CPU time per minute is consumed in handling the interrupt if output is sent to the printer one character at a time?_____%
Q23.	Assume the number of clock cycles for a polling operation, including transferring to the polling routine, accessing the device, and restarting the user program, is 400 cycles, with a 500 MHz clock. The mouse must be polled 30 times a second to ensure that no user movement is missed. Fraction of CPU time (in %) consumed for polling is_____
Q24.	Suppose we want to read 5000 bytes in programmed I/O mode of transfer, where the bus width is 16 bits. Each time an interrupt occurs, it takes 10 microseconds to service it (i.e. transfer 16 bits). The CPU time required to read 5000 bytes is _____milliseconds.
Q25.	Consider a system employing interrupt-driven I/O for a particular device that transfers data at an average of 10000 bytes per second on a continuous basis. If interrupt processing takes 50 μs, what fraction(in percent) of CPU time is consumed by this I/O device if it interrupts for every byte?_____
Q26.	The size of the data count register of a DMA controller is 16 bits. The processor needs to transfer a file of 32 Mbytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____
Q27.	A hard disk with a transfer rate of 1 Mbytes/ second is constantly transferring data to memory using DMA. The processor runs at 500 MHz, and takes 500 and 1000 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 1 Kbytes, what is the percentage of processor time consumed for the transfer operation?_____(Rounded off to three decimal places)

Q28.	A DMA controller transfers 4 byte words from an input device to memory in one clock cycle using cycle stealing. The input device transmits data at a rate of 9600 bytes per second. The CPU is fetching and executing instructions at an average rate of 1,000,000 instructions per second. Assume that size of each instruction is4bytes. The CPU will be slowed down because of the DMA transfer by _____ percent.
Q29.	A hard drive with a maximum transfer rate of 1MB/sec is connected to a 32-bit, 10 MIPS CPU operating at a clock frequency of 100 MHz. Assume that the I/O interface is DMA based and it takes 500 clock cycles for the CPU to set-up the DMA controller. Also assume that the interrupt handling process at the end of the DMA transfer takes an additional 300 CPU clock cycles. If the data transfer is done using 2000Bytes blocks, what is the percentage of the CPU time consumed in handling the hard drive?_____
For the next two questions, consider a system in which bus cycle takes 500 ns. Transfer of bus control in either direction, from processor to device or vice-versa, takes 250 ns. One of the I/O device has data transfer rate of 75 KB/sec and employs DMA. Data are transferred one byte at a time.	
Q30.	Suppose we employ DMA in a burst mode. That is, the DMA interface gains bus master ship prior to the start of block transfer and maintains control of the bus until the whole block is transferred. For how long (in nanoseconds) would the device tie up with the bus when transferring a block of 256 bytes?_____(Rounding to 2 decimal places)
Q31.	Now suppose we employ DMA in a cycle stealing mode. That is, the DMA interface gains bus master ship prior to the start of each byte of data to be transferred and then return control to the CPU after each byte of data transferred. For how long (in nanoseconds) would the device tie up with the bus when transferring a block of 256 bytes?_____ (Rounding to 2 decimal places)

Q32.	Consider the following sequence of microinstructions t1: MAR ← (PC) t2: MBR ← (memory), PC ← (PC) + 1 t3: IR ← (MBR) t4: MAR ← (PC) t5: MBR ← (memory), PC ← (PC) + 1 t6: R1 ← R1 + (MBR) What operations do the following instructions perform? (a) Add the number NUM to register R1. (b) Add contents of memory location NUM to register R1. (c) Add contents of the memory location whose address is at memory location NUM to register R1 (d) None of the above
Q33.	Consider the following sequence of micro-operations t1: MAR←(PC) t2: MBR←(memory); PC←PC+1 t3: IR←(MBR) Which of the following cycle is performed by this sequence in the instruction cycle? (a) Fetch cycle (b) Execute cycle (c) Indirect cycle (d) Interrupt cycle
Q34.	Consider the following sequence of micro-operations t1: MAR←(IR address) t2: MBR←(memory) t3: R1←R1+(MBR) Which of the following cycle is performed by this sequence in the instruction cycle? (a) Fetch cycle (b) Execute cycle (c) Indirect cycle (d) Interrupt cycle

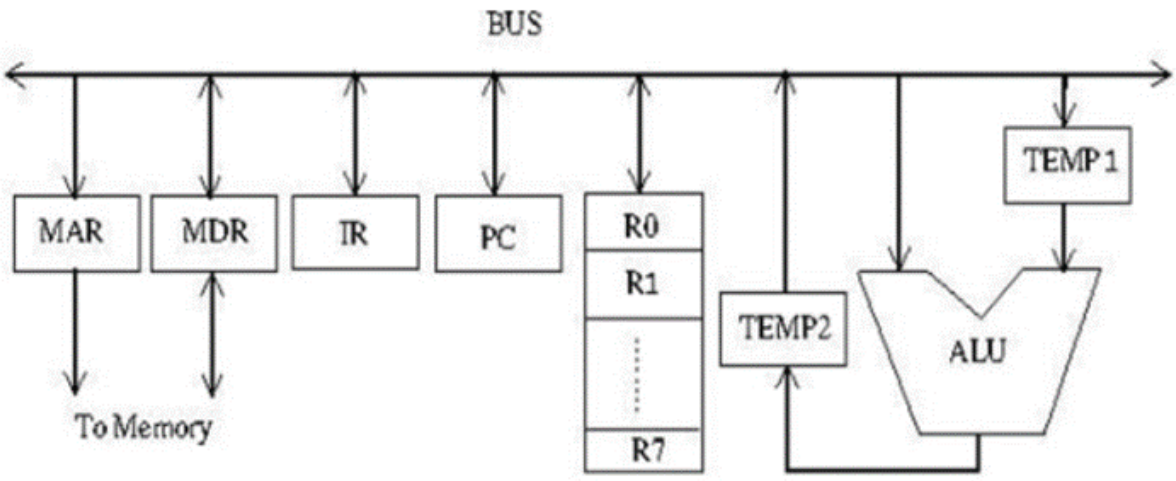
Q35.	Consider the following sequence of micro-operations t1: MBR←(PC) t2: MAR←save-address; PC←routine-address; t3: memory←(MBR) Which of the following cycle is performed by this sequence in the instruction cycle? (a) Fetch cycle (b) Execute cycle (c) Indirect cycle (d) Interrupt cycle
Q36.	Consider the following sequence of micro-operations t1: MAR←(IR address) t2: MBR←(memory) t3: IR address←(MBR address) Which of the following cycle is performed by this sequence in the instruction cycle? (a) Fetch cycle (b) Execute cycle (c) Indirect cycle (d) Interrupt cycle
Q37.	Which of the following set of control signals can be used to transfer data from register R4 to register R5? (a) R4out, R5in (b) R4out, MARin, MDRout (c) R5out, R4in (d) R5out, MARin, R4in
Q38.	Which of the following statements are true when the control signals PCout, MARin, and READ are activated simultaneously? 1. Content of PC is made available in the internal processor bus 2. The content of PC is moved to MAR and MDR 3. The instruction fetch operation is activated 4. The content of PC is moved to MAR (a) 1 and 3 only (b) 2, 3 and 4 only (c) 2 and 4 only (d) 1, 3 and 4 only

For the next two questions, consider the following Single data path of a CPU.



Using one bus, the CPU registers and the ALU use a single bus to move outgoing and incoming data. Since a bus can handle only a single data movement within one clock cycle, two-operand operations will need two cycles to fetch the operands for the ALU. PC can incremented locally and all other operations including GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR. Additional registers may also be needed to buffer data for the ALU. The instruction "Add R1, R2, R0". This instruction adds the contents of source registers R1 and R2, and stores the results in destination register R0.

Q39.	The minimum number of clock cycles needed for fetch cycle of this instruction is:_____
Q40.	The minimum number of clock cycles needed for execute cycle of this instruction is:___
Q41.	Consider the following path diagram

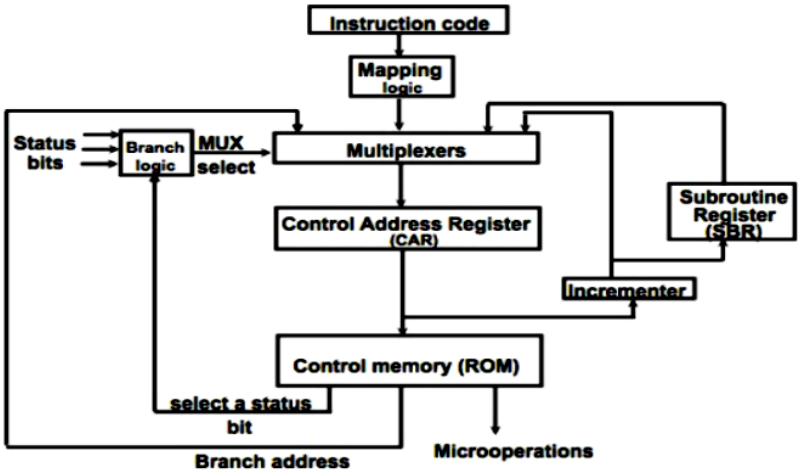


Consider An instruction: R0←R1+R2.the following steps are used to execute it over the given data path. Assume that PC is incremented appropriately. The subscripts r and q indicate read and write operations, respectively.

1. $R2_r$, $TEMP1_r$, $ALU_{ADD,}$ $TEMP2_W$

	2. $R1_r$, $TEMP1_W$ 3. PC_r, MAR_W, MEM_r 4. $TEMP2_r$, $R0_w$ 5.MDR_R, IR_W Which one of the following is the correct order of execution of the above steps? (a)2,1,4,5,3 (b)1,2,4,3,5 (c)3,5,2,1,4 (d)3,5,1,2,4

For the next five questions, the system shown in the figure below uses a control memory of 1024 word of 32 bits each. The microinstruction has three fields as shown in the diagram. The micro-operation field has 16 bits.



Q42.	How many bits are there in the branch address field? _____
Q43.	How many bits are there in the select field? _____
Q44.	If there are 16 status bits in the system, how many bits of the branch logic are used to select a status bit?_____
Q45.	How many bits are left to select an input for the multiplexers? _____
Q46.	If the control memory in the figure above has 4096 words of 24 bits each, How many bits are there in the control address register?_____

Q47.	Which of the following statements are true for horizontal microinstruction encoding? (a) If there are k control signals, every control word stored in control memory (CM) consists of k bits, one bit for every control signal. (b) Parallel activation of several micro-operations in a single time step can be performed. (c) Parallel activation of several micro-operations in a single time step cannot be performed. (d)Both (a) and (b) is correct.
Q48.	Consider the instruction set architecture of a general-purpose machine. Suppose that a total of 20 control signals are present, out of which 7 are mutually exclusive while the rest are not. The number of bits required in the control word (for microprogramming) will beat least_____.
Q49.	Suppose an instruction set architecture of a general-purpose machine has a total of 126 control signals. The number of bits required in control word for horizontal and vertical micro-instruction encoding are: (a) 126, 7 (b) 128, 7 (c) 7, 126 (d) 126, 8
Q50.	Consider the control unit in which the control signals can be divided into the following mutually exclusively groups? **Group 1**: 23 control signals to activate gates that transfer data from the internal bus to the register/ALU input. **Group 2**: 20 control signals to activate gates that transfer data from the registers to the internal bus. **Group 3**: 32 control signals to specify ALU operation. **Group 4**: 8 control signals to specify shifter operation. How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming? _____
Q51.	How many address and data lines will be there for a 16M x 32 memory system? (a) 24 and 5 (b) 20 and 32 (c) 24 and 32 (d) None of the above

Q52.	Assume that a 1G x 1 DRAM memory cell array is organized as 1M rows and 1K columns. The number of address bits required to select a row and a column will be: (a) 20 and 10 (b) 30 and 1 (c) 220 and 210 (d) None of the above
Q53.	To build a 1G x 16 memory system, the number of 256M x 8 memory modules required will be_____
Q54.	RAM chip has a capacity of 1024 words of 8 bits each. The number of 2-to-4 decoders with enable lines needed to construct a 16K x 16 RAM system will be _____

Marks :50	**Computer System Organization Test-1**	**Time:40min**
For next three questions find possible radix of the numbers in each of following operations :-		
Q1.	41/3=13;_____	
Q2.	23 + 44 + 14 + 32 = 223; _____	
Q3.	$41 = 5^2$;_____	
Q4.	A 32-bit IEEE-754 floating-point number consists of 1 sign bit, 8 exponent bits and 23 mantissa bits. Given that +0.1 is represented, in hexadecimal, as 3DCCCCCC, give the first 12 binary digits of -0.4. (a) 1011 1101 1100 (b) 1011 1110 0100 (c) 1011 1110 1100 (d) 0011 1110 1100	
Q5.	A 32-bit IEEE-754 floating point number consists of 1 sign bit, 8 exponent bits and 23 mantissa bits. What decimal number is represented by 40D00000? (a) 6.5 (b) 1.625 (c) 0.625 (d) 2.5	
Q6.	The sexagesimal number system is a number system with base 60. How many bits of information is conveyed with two sexagesimal digits? (To write a number in sexagesimal, use a space to separate digits, e.g., 13 53 26). _____	
Q7.	Suppose we use a floating-point representation with a sign bit, a 4-bit exponent in excess 7notation and a 5-bit unnormalized fractional mantissa with no hidden bit. Then, the largest number that can be represented is (a) 31×2^3 (b) 31×2^8 (c) 31×2^{13} (d) 0.31×2^8	
Q8.	Multiply the following 4 bit two's complement numbers: 1001 × 0110. What is the result in decimal?_____	
Q9.	Look at the following bit-pattern: 1010010100010100 Which of the following statements could be true? (A) This is an odd integer. (B) This is a positive integer in sign-magnitude notation. (C) This is a negative integer in two's complement notation. (D) This is an integer in two's complement notation that is greater than 32,768.	

Q10.	Which of the following addition will result in overflow in 2's complement number system? i) 11010110 +10101001 ii) 10111001 +11010110 iii) 01011101 +00100001 iv) 00100110 +01011010 (A)i& ii (B)ii & iii (C)i& iv (D)ii & iv
Q11.	What is the largest positive number that can be represented in 12 bits in two's complement representation?(in hexadecimal)_____
Q12.	What will be the signed two's complement binary number 11001 when we store in 8 bits? (A)11111001 (B) 11110001 (C) 10011001 (D) 00011001
Q13.	If the floating-point number storage on a certain system has a sign bit, a 3-bit exponent and a 4-bit significant. What is sum of largest positive and the smallest positive number that can be stored on this system if the storage is normalized? (Assume no bits are implied, there is no biasing, exponents use two's complement notation, and exponents of all zeros and all ones are allowed.) ?_____
Q14.	Whatarethevaluesof A, BandC. • $(4401)_{10} = (A)_5$ • $(1518)_{10} = (B)_7$ • $(677)_{10} = (C)_9$ (A) A=120101, B=6642, C=632 (B) A=120101, B=4266, C=862 (C) A=202010, B=4266, C=836 (D) A=120101, B=4266, C=832
Q15.	Given the 8-bit binary number: 10110001 What decimal number does this represent if the computer uses signed magnitude, one's complement and two's complement form. (A) -29(signed magnitude), -78(one's complement), 79(two's complement) (B)-49(signed magnitude), -78(one's complement), -79(two's complement) (C) 177(signed magnitude), -98(one's complement), 99(two's complement) (D) -49(signed magnitude), -100(one's complement), -99(two's complement)

Q16.	Which of the following number is the 4-digit 6's complement representation for -48_{10}? (A)441_{6s} (B) 434_{6s} (C) 435_{6s} (D) 440_{6s}
Q17.	Which of the following is equivalent to binary 11001010? i) 512_8 ii) 100_{10} iii) 202_{10} iv) 312_8 v) CA_{16} (A) iii,iv,v (B) i,iii,iv (C)ii,iv,v (D) i,ii,v
Q18.	$(12A)_{16} = (x)_8$. What is x? (A) 470 (B) 508 (C) 452 (D) 57
Q19.	Converting $(11011.01)_2$ to base 8 yields which of the following results? (A)33.2 (B)63.2 (C)63.1 (D)33.1
Q20.	$(2.3)_4 + (1.2)_4 = (y)_4$. What is y? _____
Q21.	Which one of the following is the correct sequence of the numbers represented in the series given . below $(2)_3,(10)_4,(14)_6,(22)_7$, (A)2,3,4,5,6,..... (B)2,4,6,10,12..... (C) 2,4,10,16,..... (D)2,4,6,10,16.....
Q22.	How Many 1's are present in the binary representation of (4x4096)+(9x256)+7 (A)8 (B)9 (C)6 (D)7
Q23.	What is the sum of maximum and minimum values (in decimal) that can be represented by a four-bit base (-2) system?_____
Q24.	A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example, the base-5 number 24 will be represented by its BCP code 010100. In this number system, the BCP code 100010011001 corresponds to the following number in base-5 system? (A) 423 (B) 1324 (C) 2201 (D) 4231
Q25.	The roots of the quadratic equation $5x^{\wedge 2}-50x+125=0$ are 5 and 8. Find the base(positive)system in which this equation is written?_____

Marks :50	**Computer System Organization Test-2**	**Time:40min**

Q1. How many lines will each way have in a 256kB, 4-way set associative cache with a 32-byte line size?

(A) 8192 (B) 2048 (C) 1024 (D) 512

Q2. What data will be in a 4-entry, direct-mapped cache with one byte per line after the following memory accesses? Address: 0, 1, 2, 3, 4, 5, 3, 2, 1, 2, 5

(A) 1, 2, 3, 4 (B) 0, 2, 4, 5 (C) 2, 3, 4, 5 (D) 0, 1, 3, 4

Q3. What percentage of the data in the array "data" will be reused at least once from a 32kB fully-associative cache with a 64-byte line?

```
int data[1024]; // each int  is 4 byte
for (int i=0; i<=1023 ; i ++) {
data[i] += data[i+1];
data[i+1] -= data[i]
}
```

(A) 100% (B) 75% (C) 50% (D) 25%

Q4. Calculate the cache miss ratio for the previous code (number of miss/number of cache accesses) assuming a 32kB fully associative cache with a 64-byte line (i.e. all the data fits in the cache and we don't have replacements).

(A) Around 8%

(B) Around 6%

(C) Around 4%

(D) 1.04%

Q5. Assume Physical address is 17 bit and cache memory of the computer has 32 blocks of 256 words each. Each block is associated with a "tag". If each word has 16 bits, then each block contains a total of _____ bits if PA is byte addressable (including the tag but not any other "additional" bits).

Q6. Consider a machine with a write-back cache. The cache read and writes times are both 2 nanoseconds. The memory read and writes times are both 50 nanoseconds. The proportion of writes is 15%, and the hit ratio is 90%.What is the average effective memory access time?_____

Q7.	Your computer has 32-bit integers and a direct cache containing 128 32-byte cache lines. In the following code fragment, the compiler allocates a at address 0x800000 and b at address 0x801000. Before the execution of the code fragment, the arrays a and b have never been used, so they are not in the cache. What is the cache hit rate?(in percent)
	int b[1024];
	int a[1024];
	for (i = 0; i < 1024;i++)
	{ sum = a[i] + b[i]
	a[i]=a[i]+1;
	}
	(A) 25 (B) 75 (C) 35 (D) 40

Q8.	Compute the Average Memory Access Time (in cycles) of the following cache system: L1 Has a hit time of 2 cycles, and hits 90% of the time. L2 Has a hit time of 15 cycles, and hits 95% of the time. L3 Has a hit time of 25 cycles, and hits 99% of the time. Main Memory has an access time of 100 cycles.(Approx.) (A) 3 (B) 4 (C) 5 (D) 6
Q9.	What is the probability that a 2-way associative cache with "N" lines will get a hit on an access with a distance of 2 (ABCA)? (A) $1-(2/N)^2$ (B) N^2-4/N^2 (C) Both A and B (D) None of them
Q10.	Consider a direct mapped cache with following characteristics • Cache memory: 256 bytes • Main memory: 1024 bytes • Cache line size/block size: 4 bytes To which cache blocks the following main memory addresses will be mapped: Main memory address 0 Main memory address 100 Main memory address 256 (A) 0,25,0 (B) 0,100,256 (C) 0,0,0 (D) 0,5,8

Q11.	Assume a 8-way set-associative cache with 16-byte blocks. If the cache is 128 KB in size, compute the number of bits for the offset, index and tag respectively assuming a 32-bit address. (A) Offset=4 bit, index=10 bit, tag=18 (B) Offset=4 bit, index=13 bit, tag=15 (C) Offset=3 bit, index=10 bit, tag=19 (D) None
Q12.	Assume a Fully Associative cache of 4K blocks, each block having four 32-bit words. The system is based on 32-bit physical address and uses byte addressing. What is the total number of tag bits in the cache?____Kb
Q13.	Suppose that a cache has 1024 lines. Each line can store 4 consecutive bytes from a byte-addressable memory. What is the maximum size of that main memory? (A) 1024×4=4096 bytes (B) 1024 bytes (C) 1024×1024=1MB (D) There is no maximum size because there is no relation
Q14.	Consider a direct-mapped cache memory where each cache block holds two words. Assume that each word is a one byte and that each memory address is 4-bit number where • The first 2 bits (from left to right) are the tag bits. • The third bit is the set address (index). • The last bit is the offset from the beginning of the block. Assume that the following words are accessed in sequence, according to the following access pattern (from left to right): Word number: 0 1 3 2 4 3 5 15. What is the hit rate(in percent)? (A) 60 (B) 56 (C) 50 (D) 90
Q15.	The parameters of a hierarchical memory system are specified as follows: Main memory size = 8K blocks Cache memory size = 512 blocks Block size = 16 words What is the size of the tag field(in bit) if Set associative mapping with 16 blocks/set is used?_____bit

Q16.	How many bits will be required to implement a 256KB four-way set associative cache? The cache is physically-indexed cache, and has 64-byte blocks. Assume that there are 4 extra bits per entry: 1 valid bit, 1 dirty bit, and 2 LRU bits for the replacement policy. Assume that the physical address is 50 bits wide.____Kbit
For next three questions assume N≥ 4	
Q17.	What is the probability that a direct-mapped cache with "N" lines will get a hit on an access with a distance of 2 (i.e in the reference string ABCA what is the probability of cache hit on the second reference of A)? (A) N-1/N (B) 1-(N-1/N) (C) $(N-1/N)^2$ (D) None
Q18.	What is the probability that fully-associative cache with "N" lines will get a hit on an access with a distance of 2 (ABCA)? (A)N-1/N (B) N^2-4/N^2 (C) $(N-1/N)^2$ (D) 1
Q19.	Consider two caches. Both are 4 cache lines in size and each cache line is 16 bytes and both start out with all lines marked invalid. The only difference is one is fully associative and one is two-way associative. In which of the following reference stream 2-way associative cache would get a hit and the fully-associative cache would get no hits. i) 0x10, 0x20, 0x40, 0x60, 0x80, 0x10 ii) 0x10, 0x30, 0x50, 0x10 (A) i) only (B) ii only (C) both i) & ii) (D) neither i nor ii

Q20.	Given a 16-KB two-way associative cache with 32-byte cache lines and a 64-bit address space there will be ____ bits used for the index. If that same cache were fully-associative you'd need _____ bits to be used for the index. (A) 8,8 (B) 6,8 (C) 8,0 (D) 4,0
Q21.	If you have a 32-bit address space (addresses are 32 bits) and you have a 4-way associative cache that uses 5 bits as the set index and 4 bits as the byte offset, how large is the data portion of the cache (in bytes)? _____
Q22.	Which of these statements is true? (a) Direct-mapped caches usually have a lower miss rate than set-associative caches. (b) Direct-mapped caches have at least 2 blocks per set. (c) A direct-mapped cache will have more tag bits than a set-associative cache with the same capacity. (d) Direct-mapped caches do not need a replacement algorithm
Q23.	Consider an instance of a direct mapped cache Tag 00 01 10 11 0xBC 1 2 3 4 Line 0 0x01 5 6 7 8 Line 1 0x20 9 10 11 12 Line 2 0x 1A 13 14 15 16 Line 3 On which line physical adder 0x012 mapped? (A) Line 0 (B) Line 1 (C) line 2 (D) Line 3
Q24.	Consider a direct map cache with 4 block, Following block address is given by system 8,10,5,6,9,8,26,5. How many cache misses occur? _____
Q25.	Consider a 4 way set associative cache which is LRU, has 32 byte lines and is 512 B cache size. Assuming cache is initially empty and following block addresses are accessed- 0,32,64,128,512,544,0,32,768 . What is the cache hit ratio?_____

Marks: 50 **Computer system organization Test-3** **Time:40min**

Q1. In order to set bits 7,5 and 3 of a byte, we can:

(A) logically XOR with 10101000

(B) logically OR with 01010100

(C) logically AND with 01010100

(D) logically OR with 10101000

Q2. The five stages of a 5-stage pipeline take 2 ns, 3 ns, 1 ns, 4 ns, and 2 ns. If there are 100 instructions, what is the maximum speed up in the execution time of a pipeline implementation compared to a single-cycle implementation?

(A) 2.14

(B) 2.88

(C) 2.94

(D) 3.00

Q3. Your code is required to perform the function (M%16)*3. What should you do to eliminate multiplication and division, assuming M is 32 bits wide?

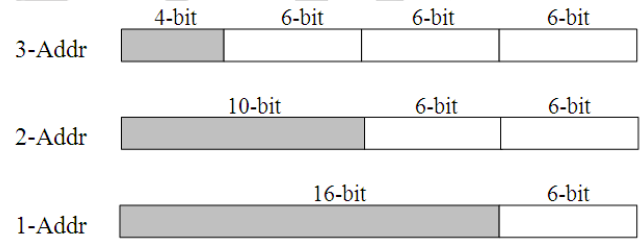
(A) Shift M right by 16, then shift left by 3

(B) Shift M right by 4, shift left by 1, and add current value to itself.

(C) Shift M right by 4, save the result to register, and add the saved result to current result twice.

(D) AND M with 0000000Fh, save the result to register, and add the saved result to current result twice.

For next three questions consider a machine with 22-bit instructions and 6-bit addresses. There are three types of instructions: 3-Addr, 2-Addr and 1-Addr, as shown below:



Assume that there is at least one instruction for each type, and the encoding space is completely utilized.

Q4. What is the maximum number of 3-Addr instructions?

(A)4 (B)10 (C)14 (D)15

Q5.	What is the minimum number of 1-Addr instructions? (A)2^6 (B)2^{10} (C)2^{16} (D)2^{32}
Q6.	What is the maximum number of 2-Addr instructions? (A)84 (B)896 (C)959 (D)1023
Q7.	Consider the following code: li R0, 1 // load immediate sub R1, R1, R0 Which of the following best describes its effect? (A) R1 = 1 – R1 (B) It causes the value in register ‘ R1’ to decrement by 1. (C) “li” loads ‘1’ into register ‘ R1’; the “sub” instruction then sets it to ‘0’. (D) It does nothing: “ R0” always holds a zero, even if “li” tries to store a ‘1’ in it.
Q8.	What will be the contents of register R3 *after* execution of the code segment.(Assume register size is 1 byte) li R1, 17 li R2, 2 mult R1, R2 //Multiply mfhi R3 // store higher order byte of result to R3 (A) 0. (B) 1. (C) 8. (D) 34.
Q9.	Suppose R0 is storing 10, R1 is storing 25. After the following instructions, what will be the value in R2? sub R2, R1, R0 andi R2, R0, 3 xor R2, R2, R0 (A) 6 (B) 9 (C) 10 (D) None of the above.

Q10.	Suppose word array A stores 0,1,2,3,4,5,6,7,8,9, in this order. Assume the starting address of A is in $s0. After the following instructions, what will be the values this array? Word size =4 byte
	addi R0, $s0, 20
	lw R1, 0(R0)
	sw R1, -8(R0)
	(A) 0,1,2,5,4,5,6,7,8,9
	(B) 0,1,4,3,4,5,6,7,8,9
	(C) 0,1,2,3,4,5,4,7,8,9
	(D) 0,1,3,5,4,6,2,7,8,9

Q11.	Suppose R0 and R1 are holding 10 and 5, respectively. After the following instructions, what will be in R0? ***SLT*** -- Set on less than BNE – branch if not equal to zero SLL -- ***Shift left logical*** slt R0, R1, R0 (set R0 if R1<R0) bne R0, $0, L1 sll R0, R1, 2 j L1 L1: addi R0, R0, 1 (A) 1 (B) 2 (C) 21 (D) 12
Q12.	Suppose word array A stores 0,1,2,3,4,5,6,7,8,9, in this order. Assume the starting address of A is currently in $s0. After the following instructions, what will be the value in R1? SLL -- ***Shift left logical*** BLT – branch if less than ori R0, $0, 18 L0: lw R1, 0($s0) sll R1, R1, 2 blt R0, R1, L1 addi $s0, $s0, 8 j L0 L1: (A) 2 (B) 3 (C) 6 (D) 24

Q13. The 5 stages of the processor have the following latencies:

Fetch	Decode	Execute	Memory	Writeback
300ps	400ps	350ps	500ps	100ps

Let the frequency of non- pipeline be x GHz and pipelined processor be y GHz then what is x+y =___?

Q14. If R0 is holding 0, R1 is holding 1, what will be the value stored in R2 after the following instructions?

SRL –- Shift right logical

srl R1, R1, 1

bne R0, R1, L1

addi R2, R0, 1

L1: addi R2, R0, 2

(A) 1.

(B) 2.

(C) 3.

(D) None of the above

Q15. Consider the following code

lw R2, 0(R1)

lw R1, 40(R6)

sub R6, R1, R2

add R6, R2, R2

or R3, R6, 0

sw R6, 50(R1)

How many cycles are required to complete the execution of above code on a 5-stage pipelined processor without forwarding?_____

Q16. Consider the following code

Loop: LW R1, 0(R2)

ADDI R1, R1, 1 SW 0(R2), R1

ADDI R2, R2, 4

SUB R4, R3, R2

BNEZ R4, Loop

How many RAW(a *true dependency)*, WAR(*anti-dependency)* and WAW (*output dependency)* dependencies exists in the above code? Let number of RAW=x, number of WAR=y, number of WAW = z. Find x+y+z_____

Q17.	Consider the following loop. $loop$: $SUBI\ R1,1,\#1$ $LD\ R3,\ 0(R2)$ $LD\ R4,\ 4(R2)$ $MUL\ R5,3,R4$ $ADD\ R3,5,R6$ $ADDI\ R2,2,\#8$ $BNEZ\ R1,\ loop$ $ADD\ R10,11,R12$ Assume a 5-stage pipeline (IF ID EX MEM WB) without any forwarding or bypassing hardware, but with support for a register read and write in the same cycle. Also assume that branches are resolved in the ID stage and handled by stalling the pipeline. All stages take 1 cycle. How many cycles does the program take to execute?_____
Q18.	We have a processor with register-register arithmetic instructions that have the format R1 → R2 op R3. The pipeline for these instructions runs with a 100 MHz clock with the following stages: instruction fetch = 2 clocks, instruction decode = 1 clock, fetch operands = 1 clock, execute = 2 clocks, and store result = 1 clock. At what cycle per instruction rate can we execute the instructions when every instruction depends on the results of the previous instruction?_____
Q19.	Consider a machine with both an L1 cache and an L2 cache 90% of all accesses hit in L1 cache. The hit time is 5ns. The L2 cache has a hit time of 10 ns, a miss rate of 20% and a miss penalty of 75ns. The average memory access time is roughly _____
Q20.	A processor takes 280ns for the longest instruction. Then processor is pipelined with 14 (equal) stages . using pipeline registers that take 10ns. What percentage of the resulting cycle time is used for computation? (A) 33% (B) 66% (C) 96% (D) 100%

Q21.	What is needed to resolve the following hazard?
	add R14, R1, R13
	lw R1, 4(R14)
	add R14, R15, R15
	addi R14, R12, 0
	(A) Forwarding from WB to EX
	(B) Forwarding from WB to MEM
	(C) Can't resolve, need to stall
	(D)There is no hazard to resolve

Q22.	What is needed to resolve the following hazard?
	lw R1, 4(R14)
	add R14, R1, R13
	add R14, R15, R15
	addi R14, R12, 0
	(A) Forwarding from MEM to EX
	(B)Forwarding from WB to MEM
	(C)Can't resolve, need to stall
	(D)There is no hazard to resolve

Q23.	How many register need to be forwarded in the following code?
	xor R3, R4, R7
	add R6, R4, R5
	sub R2, R3, R4
	beq R2, R3, done
	(A) 0 (B) 1 (C) 2 (D) 3

Q24.	A certain statistical observation made on a CPU executing a piece of code shows that the code has 50% arithmetic/logic machine instructions each taking 1 clock cycle, 30% load /store (memory reference) instructions each taking 2.0 clock cycles and 20% branch instructions each taking 1.5 clock cycles. What can be said about the average CPI (cycles per instruction) value of the processor? (A) 1.5 (B)1.4 (C)0.71 (D) Insufficient data to calculate

Q25.	A 11 bit CPU has an arithmetic unit adds bytes and then sets its V,C and Z f lag bits .the V bit is set if arithmetic overflow occurs in 2`s complement arithmetic . the C-bit is set if a carry out is generated form the most significant bit during an operation . The Z –bit is set if the result is zero . if the decimal numbers511and 768 are added using 11 bit addition , what are the values of the V,C, and Z flag bits (A)V-0,C-0,Z-0 (B)V-1,C-1,Z-0 (C)V-1,C-0,Z-1 (D)V-1C-0Z-0