CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

IO Organization

Lecture No.- 04

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Recap of Previous Lecture

Topic Interrupt IO

Topic Types of Interrupt

Topic DMA

Topics to be Covered

Topic DMA

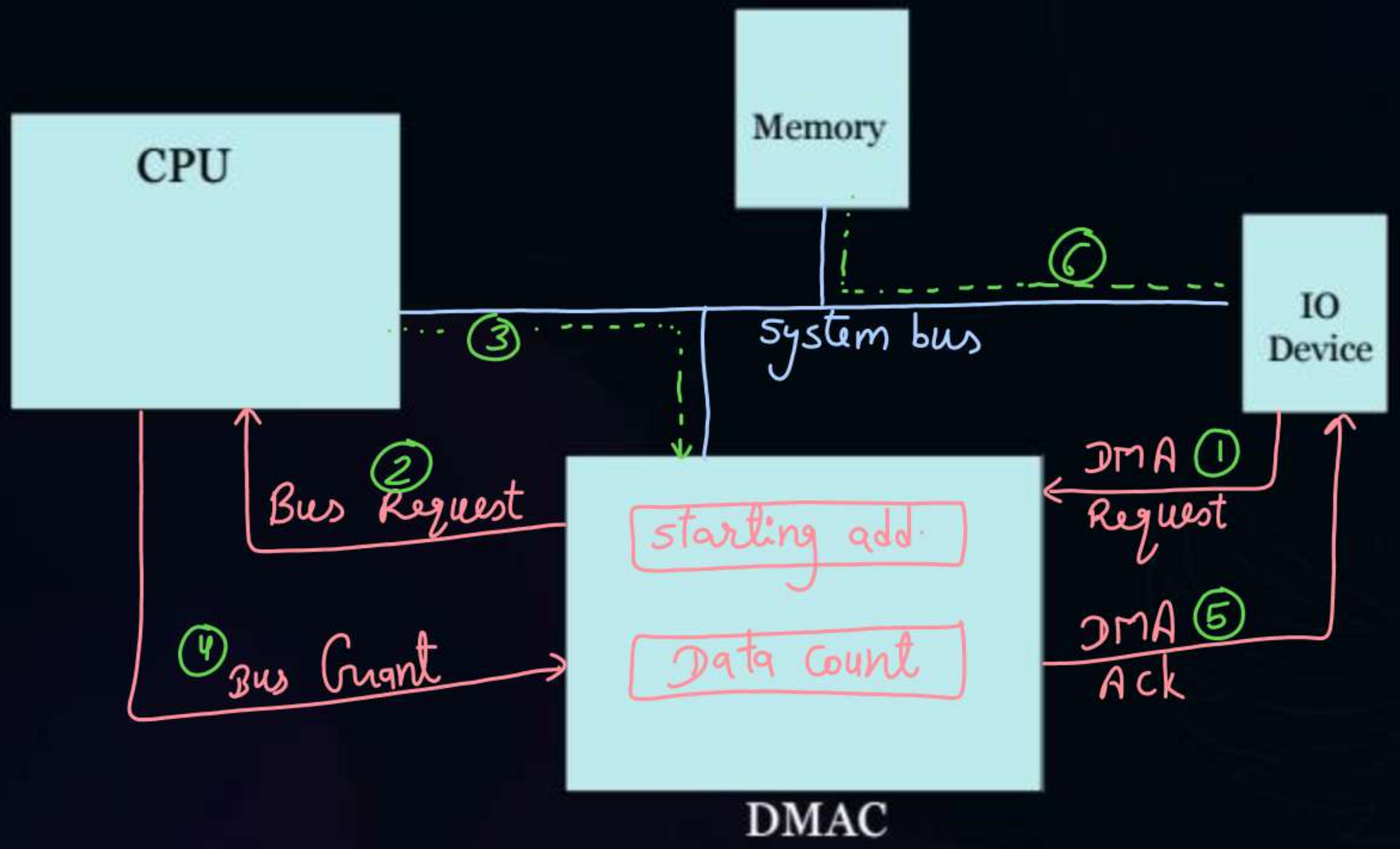
Topic Modes of DMA

Topic Cycle Stealing

Topic : DMA

- Enables data transfer between I/O and memory without CPU intervention
- Need a hardware: DMAC

Topic : DMA


Memory
CPU
IO Device
6
system bus
3
2
Bus Request
DMA 1
Request
starting add
Data count
4
Bus Grant
DMA 5
Ack
DMAC

Topic : DMA

1. Starting Address ✓

2. Data Count ✓

5-bits ⇒ $(11111)_2 = (31)_{10}$ (max value)

During DMA transfer CPU is blocked.

Topic : Modes of DMA Transfer

After how much time CPU takes the control of the buses back from DMAC.

Topic : Modes of DMA Transfer

1. Burst Mode
2. Cycle Stealing
3. Interleaving DMA

Topic : Modes of DMA Transfer

Burst Mode :

when control of the buses is given to DMAC, then it transfers one block of data, before CPU takes back the control.

1 block size ⇒ 512B to 2K bytes
(typically)

Topic : Modes of DMA Transfer

Cycle Stealing :

Slow I/O device takes time to prepare data internally. Hence while I/O device prepares data, CPU keeps the control of the buses. when data is ready, CPU gives control of the buses to DMAC to transmit it to memory and then CPU again takes back the control of the buses.

Time for which control of the buses will be with DMAC => 1 mem. cycle time

Time in which read/write performed on one add. of memory.

Assuming :-

Preparation time of data in I/O device = t_x ← depends on I/O speed

Transfer time of prepared data to memory = t_y ← depends on mem. speed

% of time CPU is blocked due to DMA (burst mode) $= \frac{t_y}{t_x + t_y} * 100\%$

% of time CPU is blocked due to DMA (cycle stealing) $= \frac{t_y}{t_x} * 100\%$

Topic : Modes of DMA Transfer

Interleaving DMA:

CPU gives control of the buses to DMAC only when the buses are not needed.

CPU will be blocked for very-very less time due to DMA.

[NAT]

#Q. Consider a device operating on 1MBPS speed and transferring the data to memory using cycle stealing mode of DMA. If it takes 2 microseconds to transfer 16 bytes data to memory when it is ready/prepared. Then percentage of time CPU is blocked due to DMA is?

$t_y = 2\ \mu sec$

$$\% \text{ of time CPU blocked} = \frac{t_y}{t_x} * 100\%$$

$$= \frac{2\ \mu sec}{16\ \mu sec} * 100\%$$

$$= \underline{12.5\%} \quad \text{Ans.}$$

1MB, data preparation time = 1sec

16 bytes, —— " —— = $\frac{1\,sec}{1MB} * 16\,bytes$

= 16 μsec

From preparation time to I/O speed :-

In 16 μsec time, data = 16 bytes

In 1 μsec —11— $= \frac{16\ B}{16\ \mu s} = 1B/\mu sec$

In 1 sec —11— $= \frac{1\ B}{10^{-6}\ sec}$

$= 1MB/sec$

Ques → If data preparation time in I/O = 100 μsec

→ % of time CPU is blocked due to DMA = 2%

→ cycle stealing mode used

→ memory cycle time = ____ μsec ?

Soln

$$2\% = \frac{ty}{100\ \mu sec} * 100\%$$

$$ty = 2\ \mu sec$$

#Q. If device operates on 2MBPS speed then data preparation time of 4 byte data is ____ μsec ?

Ans)

2MB, preparation time = 1sec

4B ——"—— = $\frac{1\,sec}{2MB} * \frac{2}{4B}$

= 2 μsec Ans

[NAT] GATE – 2022 Ans = 80000

#Q. Consider a computer system with DMA support. The DMA module is transferring one 8-bit character in one CPU cycle from a device to memory through cycle stealing at regular intervals. Consider a 2 MHz processor. If 0.5% processor cycles are used for DMA, the data transfer rate of the device is bits per second?

Data size = 8 bits

t_y = 1 CPU cycle = $\frac{1}{2\,MHz}$ = 0.5 μsec

~~0.5 %~~ = $\frac{\text{~~0.5 μsec~~}}{t_x}$ * ~~100 %~~

t_x = 100 μsec

In 100 μsec. data prepared = 8 bits

In 1 sec, —11— $= \frac{8 \text{ bits}}{100 * 10^{-6} \text{ sec}}$

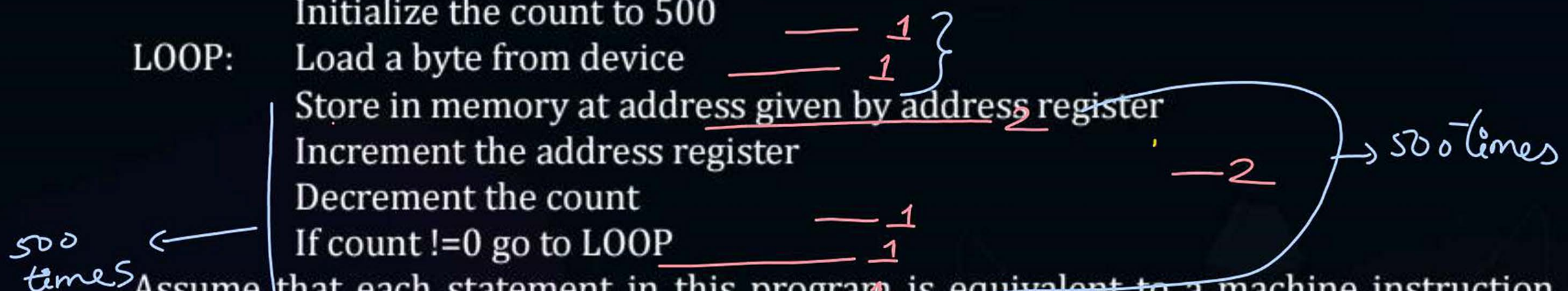
$= \frac{8 * 10^{6} \text{ bits}}{100 \text{ sec}}$

$= 80\,000 \text{ bits/sec}$

GATE PYQ

#Q. On a non-pipelined sequential processor, a program segment, which is the part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

```
        Initialize the address register
        Initialize the count to 500
LOOP:   Load a byte from device
        Store in memory at address given by address register
        Increment the address register
        Decrement the count
        If count !=0 go to LOOP
```



Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.

What is the approximate speed up when the DMA controller based design is used in a place of the interrupt driven program based input-output?

Speed up of DMA as Compared to interrupt mode

$$= \frac{\text{interrupt mode time}}{\text{DMA time}} = \frac{3502}{1020}$$

$$= 3.4$$

Interrupt mode time $= 1 + 1 + 500\,(2 + 2 + 1 + 1 + 1)$

$= 3502$

DMA time $= 20 + 2 * 500 = 1020$

[NAT]

#Q. The DMA controller has data count register of size 8-bits. The memory is byte addressable. The maximum number of bytes the DMA can transfer to memory at a time without giving the control of the buses back to CPU?

max value in data count reg. $= (11111111)_2$

$= (255)_{10}$

[NAT]

#Q. The DMA controller has data count register of size 8-bits. The memory is byte addressable.

1. Minimum how many times DMA needs to take control from CPU to transfer a file of 500 bytes? $\Rightarrow \underline{\underline{2}}$ Ans.
2. Minimum how many times DMA needs to take control from CPU to transfer a file of 15K bytes?

1. $\left\lceil \frac{500\ B}{255\ B} \right\rceil = 2$ times

2. $= \frac{15\ k\ bytes}{255\ bytes} = \left\lceil \frac{15 * 1024}{255} \right\rceil$

$= 61$

[NAT] GATE- PYQ

#Q. The size of the data count register of a DMA controller is 16bits.

The processor needs to transfer a file of 29, 154 kilobytes from disk to main memory.

The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____ .

$$= \left\lceil \frac{29154 * 1024}{(2^{16}-1)} \right\rceil = \left\lceil \frac{29154 * 1024}{65535} \right\rceil = \lceil 455.5 \rceil = 456 \text{ Ans.}$$

[MSQ]

#Q. If a word preparation time in IO device and word transfer time to memory from IO device are same. Then? $t_x = t_y$

A. 100% time CPU is blocked due to DMA in cycle stealing mode

B. 50% time CPU is blocked due to DMA in cycle stealing mode

C. 100% time CPU is blocked due to DMA in burst mode

D. 50% time CPU is blocked due to DMA in burst mode

$$\%\ \text{of time CPU blocked (burst mode)} = \frac{t_y}{t_x + t_y} * 100\% = 50\%$$

$$\text{---}''\text{---} \text{ (cycle stealing)} = \frac{t_y}{t_x} * 100\% = 100\%$$

2 mins Summary

Topic DMA

Topic Modes of DMA

Topic Cycle Stealing

Happy Learning

THANK - YOU