CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

IO Organization

Lecture No.- 01

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Recap of Previous Lecture

Topic Floating-Point Numbers

Topic Biased Exponent

Topic Number Range

Topic IEEE-754 Floating Point Representation

Topic Denormalized Number

Topics to be Covered

- **Topic** Peripheral Device
- **Topic** IO vs Memory Buses
- **Topic** Memory Mapped IO vs IO Mapped IO
- **Topic** Asynchronous Data Transfer

Topic : IEEE-754 Floating Point Representation

S	E	M	Number
0	0----0	0----0	+0
1	0----0	0----0	−0
0	11....1	0.....0	+∞
1	11....1	0.....0	−∞
0/1	11....1	M ≠ 0....0	N.A.N.
0/1	00..0	M ≠ 0	Denormalized
0/1	E ≠ 0....0 and E ≠ 1....1	xxx.....x	Implicit normalizatn

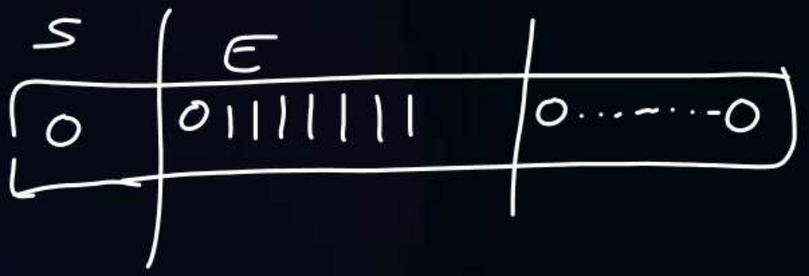
[NAT]

#Q. How to represent +1 and -1 in IEEE-754 single precision floating point number?

$1.0 * 2^0 \Rightarrow e = 0$

$E = 0 + 127 = (127)_{10} = (01111111)_2$

$M = 0 \cdots 0$



-1 1 01111111 00...0

[NAT]

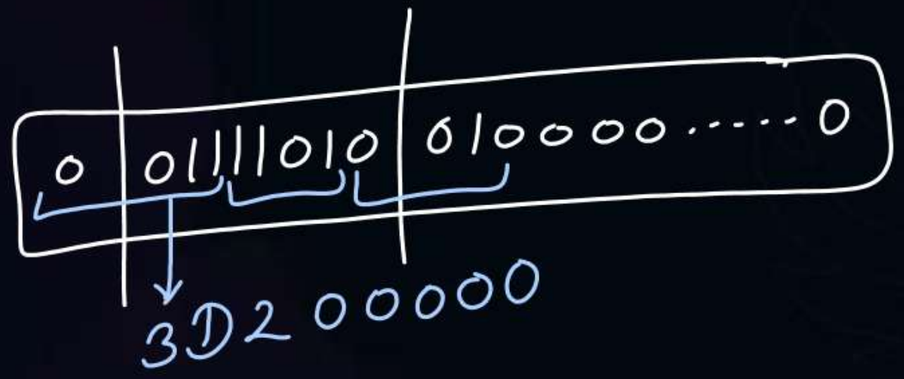
#Q. How to represent $+(0.0000101)_2$ in IEEE-754 single precision floating point number?

$\Downarrow$

Implicit normalizat^n $1.01 * 2^{-5} \Rightarrow e = -5$

$E = -5 + 127 = (122)_{10} = 01111010$

$M = 01$



[MCQ] GATE - PYQ

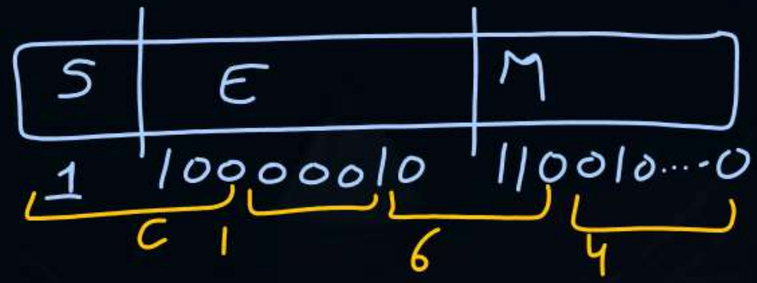
#Q. The value of a float type variable is represented using the single- precision 32-bit floating point format IEEE-754 standard that uses 1bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of −14.25. The representation of X in hexadecimal notation is

A ~~C1640000H~~

B 416C0000H

C 41640000H

D C16C0000H



$(14.25)_{10} = (1110.01)_2$

$\Downarrow$

$1.11001 * 2^3$

$E = 3 + 127 = 130 = (10000010)_2$

$M = 11001$

[NAT] GATE PYQ

#Q. Consider the following representation of a number in IEEE 754 single-precision floating point format with a bias of 127.

S : 1 E : 10000001 $= (129)_{10}$ F: 11110000000000000000000

Here S, E and F denote the sign, exponent and fraction components of the floating-point representation.

The decimal value corresponding to the above representation (rounded to 2 decimal places) is_____

$-(7.75)_2$

Ans.

Value $= 1.1111 * 2^{129-127}$

$= 1.1111 * 2^2$

$= (111.11)_2$

$= (7.75)_{10}$

[NAT] GATE PYQ

#Q. The format of the single-precision floating-point representation of a real number as per the IEEE 754 standard is as follows:

Sign	Exponent	mantissa

Which one of the following choices is correct with respect to the smallest normalized positive number represented using the standard?

A. exponent = 00000001 and mantissa = 00000000000000000000001

B. exponent = 00000001 and mantissa = 00000000000000000000000

C. exponent = 00000000 and mantissa = 00000000000000000000000

D. exponent = 00000000 and mantissa = 00000000000000000000001

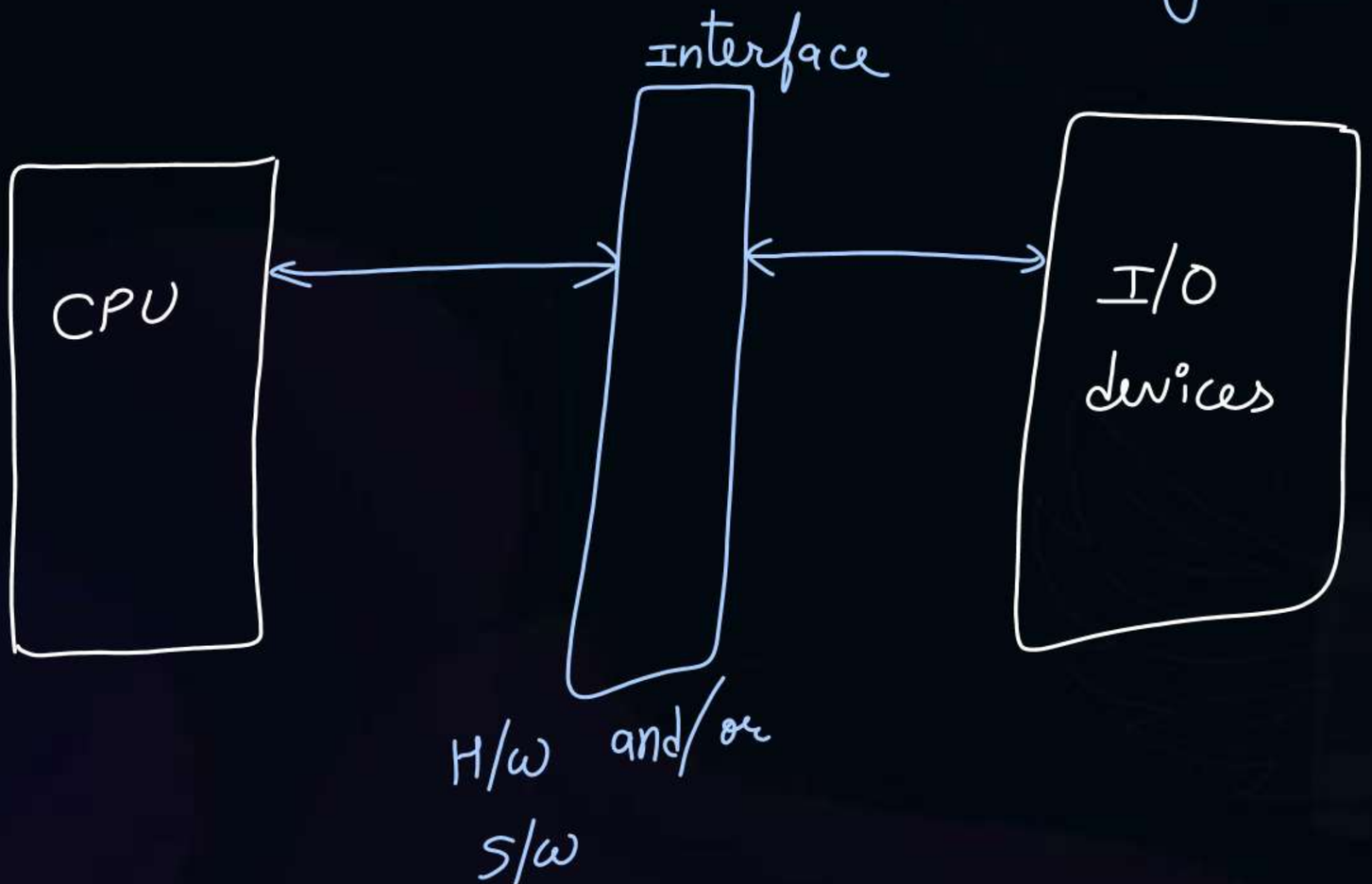
Topic : Peripheral Device (I/O devices)

Devices connected to CPU externally except memory.

Types
- Input devices
- output devices
- storage devices

Topic : CPU Connected to IO Directly?

I/O devices are connected to CPU through I/O interface.

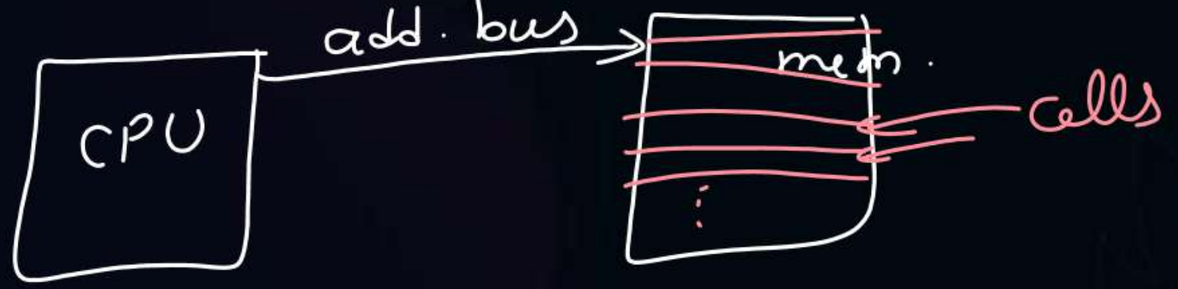


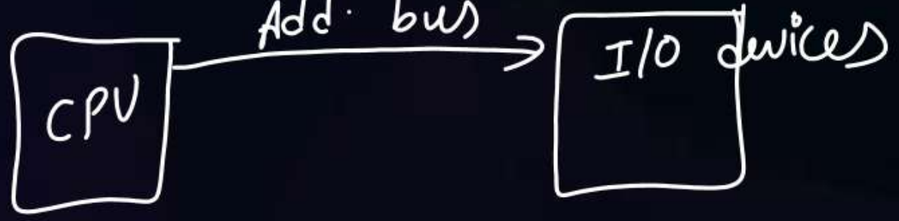
Topic : Need For Interface

1. Peripherals are electromechanical or electromagnetic devices; and their manner of operation is different from the operation of the CPU and memory. Which are electronic devices. So conversion of signal required.
2. The data transfer rate of peripherals is usually slow. So synchronization is required.
3. Data codes and format in peripherals differ from the word format in the CPU and memory. So conversion of formats is required.
4. The operating modes of peripherals are different from each other and each must be controlled so a peripheral does not disturb the operation of other peripherals.

Topic : IO vs Memory Buses

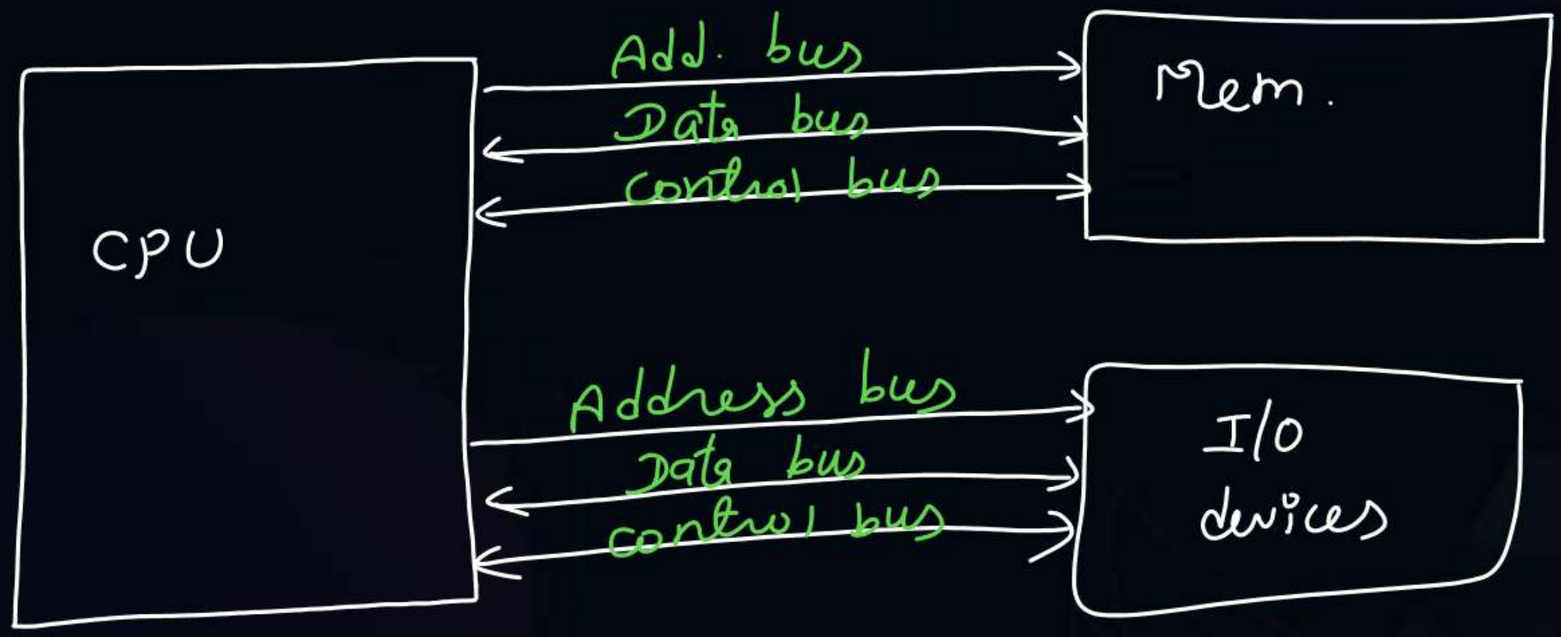
There are 3 ways, the CPU can connect with I/O and mem.





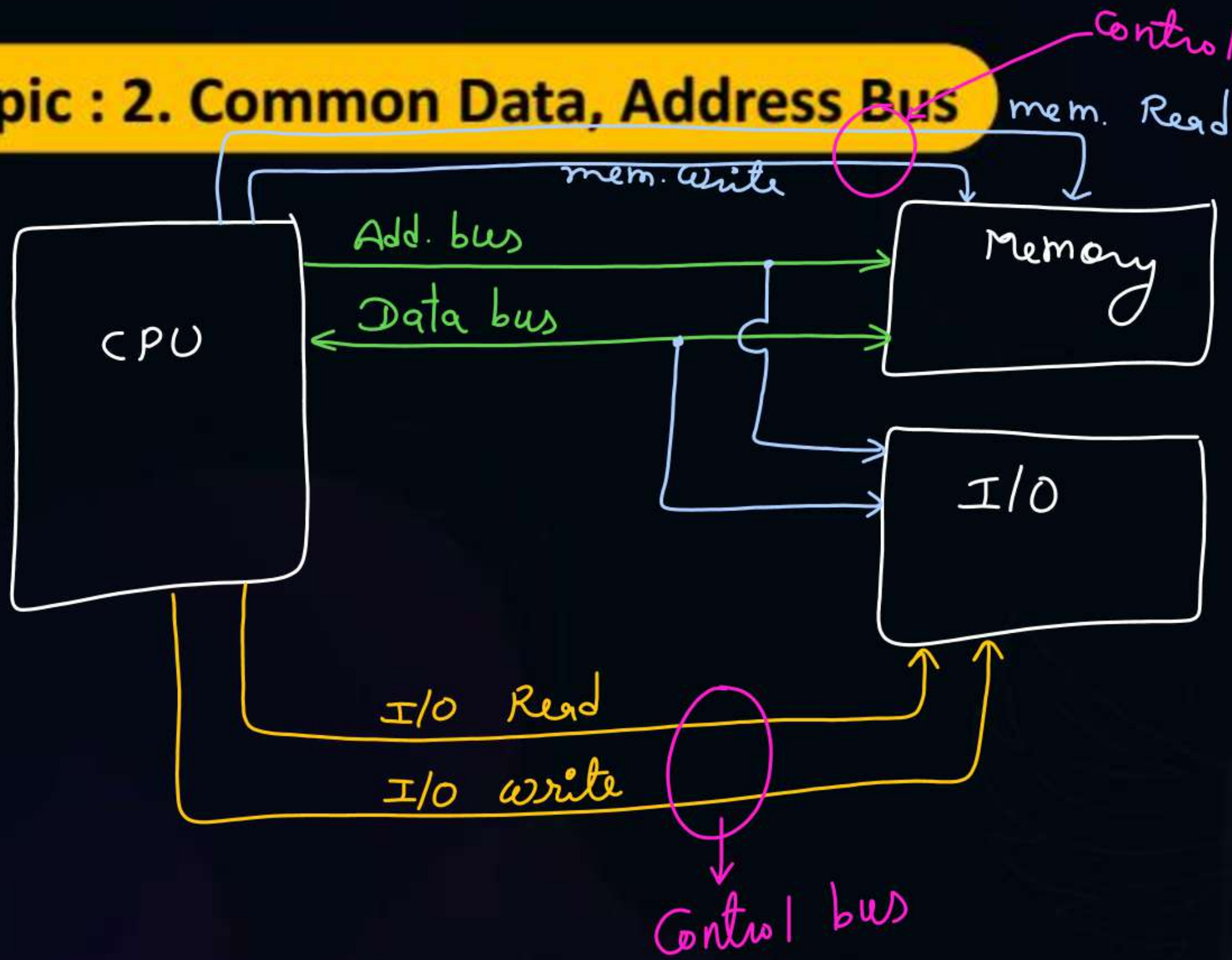
Each I/O device has an address and CPU selects one I/O device by sending it's address through add. bus.

Topic : 1. Separate Buses for Both



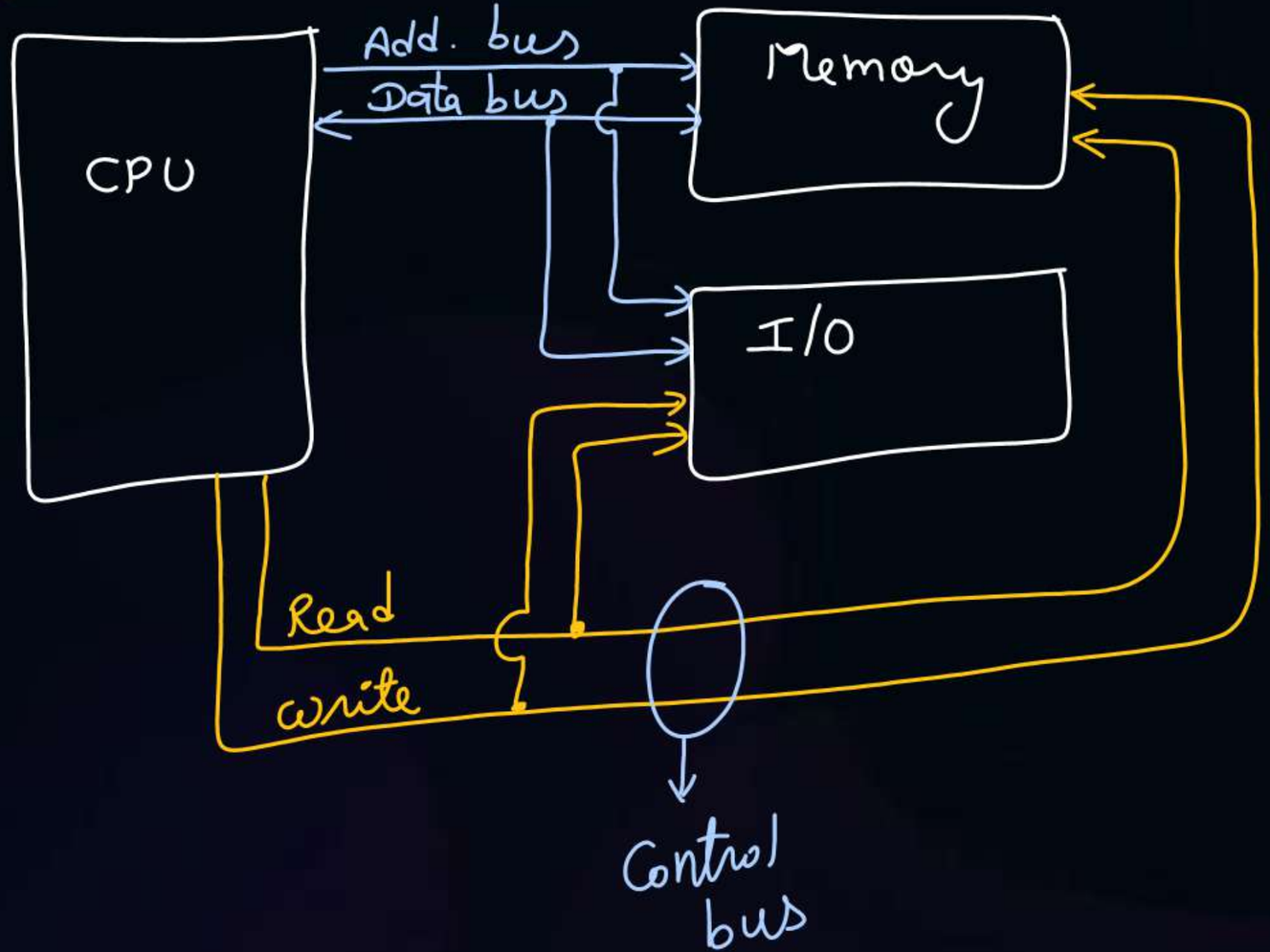
Disadv. ⇒ Costly because at a time CPU can communicate with either mem. or I/O device hence 2 sets of buses are not necessary.

Topic : 2. Common Data, Address Bus



I/O mapped I/O
or
Port mapped I/O
or
Isolated I/O

Topic : 3. Common Address, Data & Control Bus



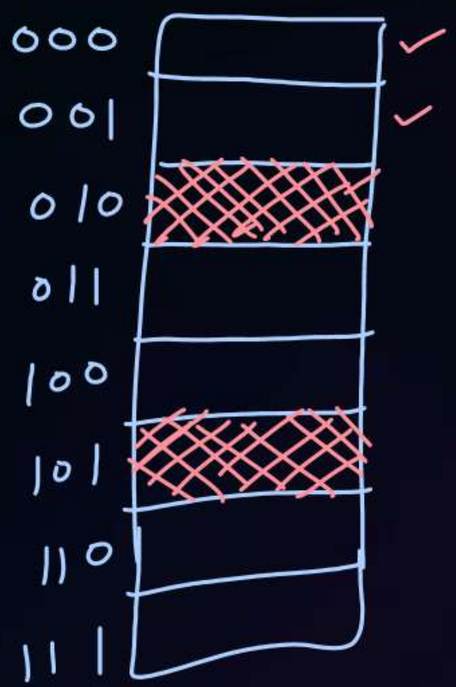
Memory Mapped I/O

Topic : 3. Common Address, Data & Control Bus

Assume a system with 8 bytes (byte addressable) mem.

& 2 I/O devices

some mem. addresses are assigned to I/O devices.



Assume

	assigned addresses
device 1	010
device 2	101

Topic : Memory Mapped IO vs IO Mapped IO

Memory Mapped IO	IO Mapped IO
1. Some mem. wastage	1. No mem. wastage
2. I/O devices do not have their own addresses	2. I/O devices have own address space.
3. All mem. access instns and addressing modes can be used to access I/O devices also.	3. I/O access instns & addressing modes are different than that of memory.
4. I/O access instns and add. modes are more.	4. I/O access instns & add. modes are less.

Topic : Memory Mapped IO vs IO Mapped IO

Memory Mapped IO	IO Mapped IO
5. More I/O devices can be Connected to CPU.	5. Lesser I/O devices can be Connected to CPU.
6. I/O data can be sent to ALU directly.	6. I/O data can not be sent to ALU directly.

2 mins Summary

Topic Peripheral Device

Topic IO vs Memory Buses

Topic Memory Mapped IO vs IO Mapped IO

Topic Asynchronous Data Transfer

Sat. ⇒ 4–6 PM } classes
Sun ⇒ 9–11 am }

12 PM ← discussion

Happy Learning

THANK - YOU