



CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

Cache Organization

Lecture No.- 07

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Recap of Previous Lecture



Topic

Direct Mapping

Topic

Set Associative Mapping

Topic

Fully Associative Mapping

Topics to be Covered



Topic

Direct Mapping

Topic

Set Associative Mapping

Topic

Fully Associative Mapping



Topic : Set Associative Mapping

mm add.

mm add.

mm block no.	byte offset
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Tag	set offset	byte
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given mm add.
maps to which
cm set

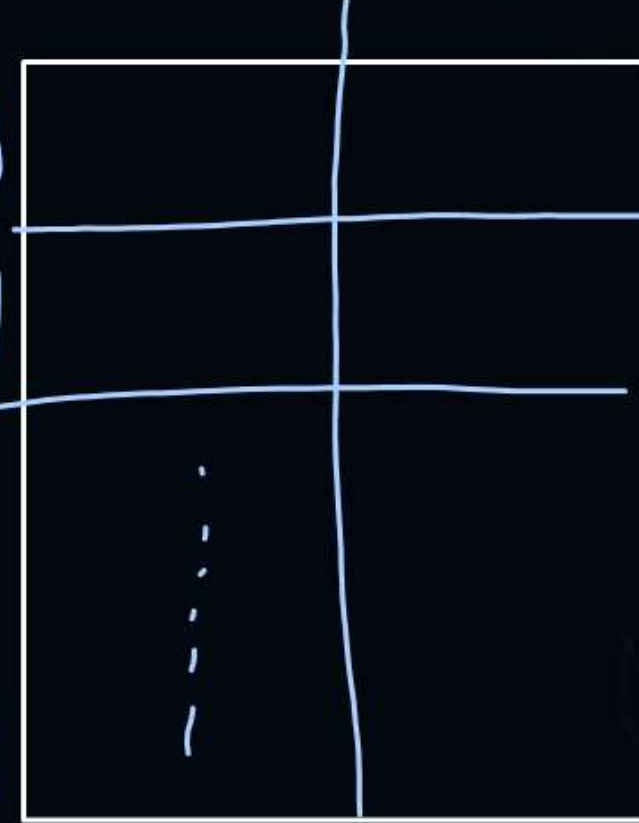
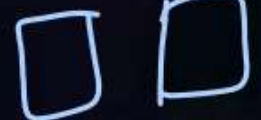
$$\text{cm set no.} = (\text{mm block no.}) \% (\text{no. of sets in cache})$$



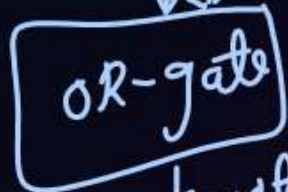
Topic : Checking Hit/Miss in Set Associative Mapping

mm add.

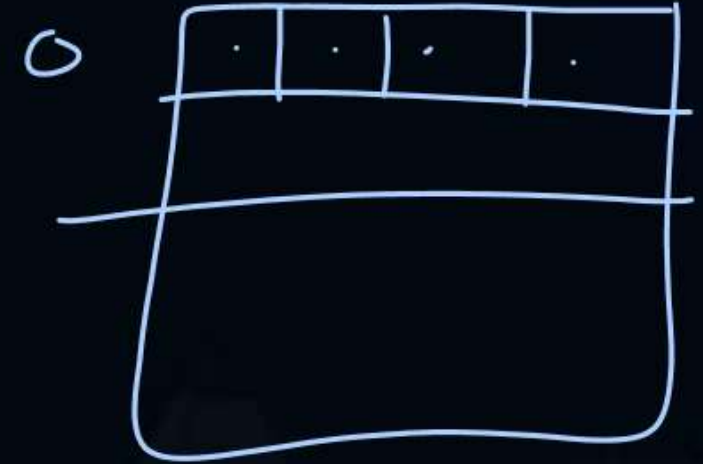
assuming 2-way set associative



cm



hit/Miss



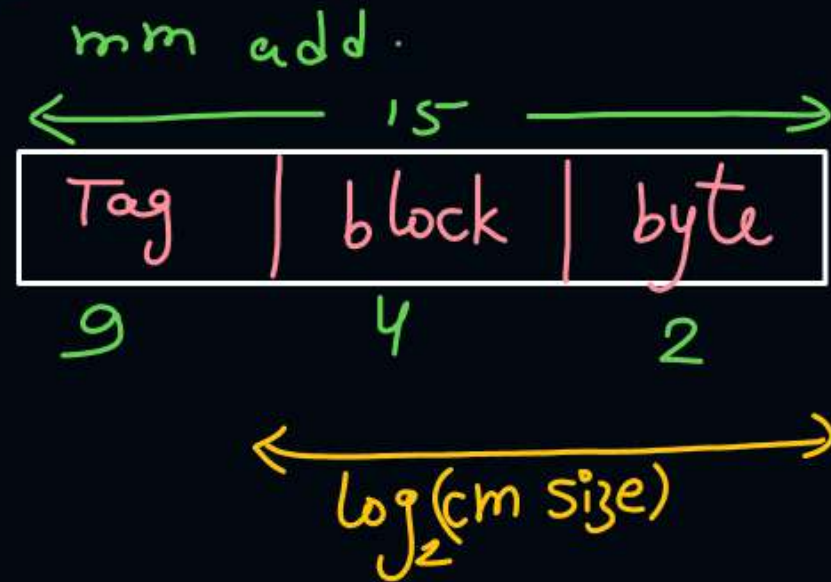
Assume:-

cm size = 64 Bytes

mm add. = 15 bits

Block size = 4 bytes = $2^2 B$

Direct mapping:-

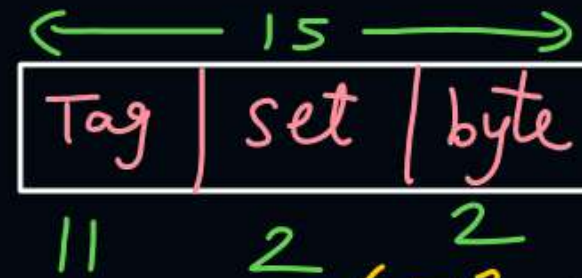
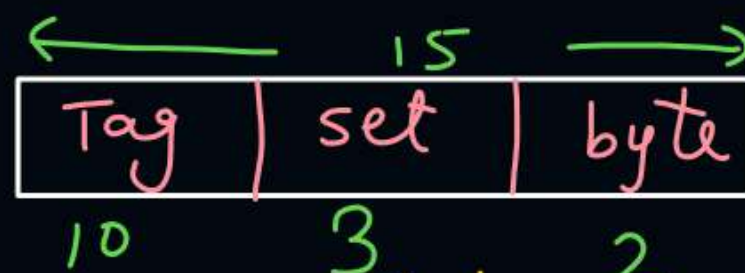


$$\text{no. of blocks in cache} = \frac{64B}{4B} = 16 = 2^4$$

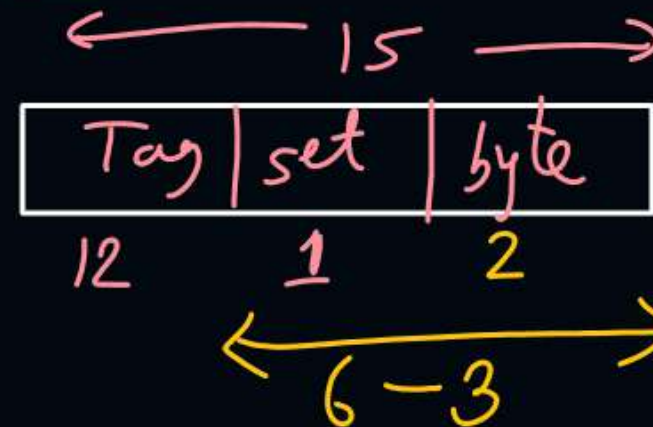
$$\text{no. of sets in cache} = \frac{2^4}{2} = 2^3$$

$$\text{no. of sets} = \frac{2^4}{4} = 2^2$$

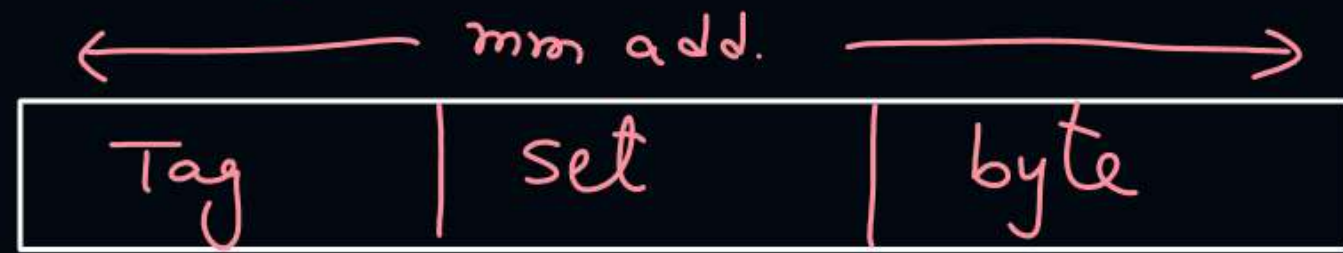
2-way set associative:- 4-way:-



8-way



for k -way set associative cache



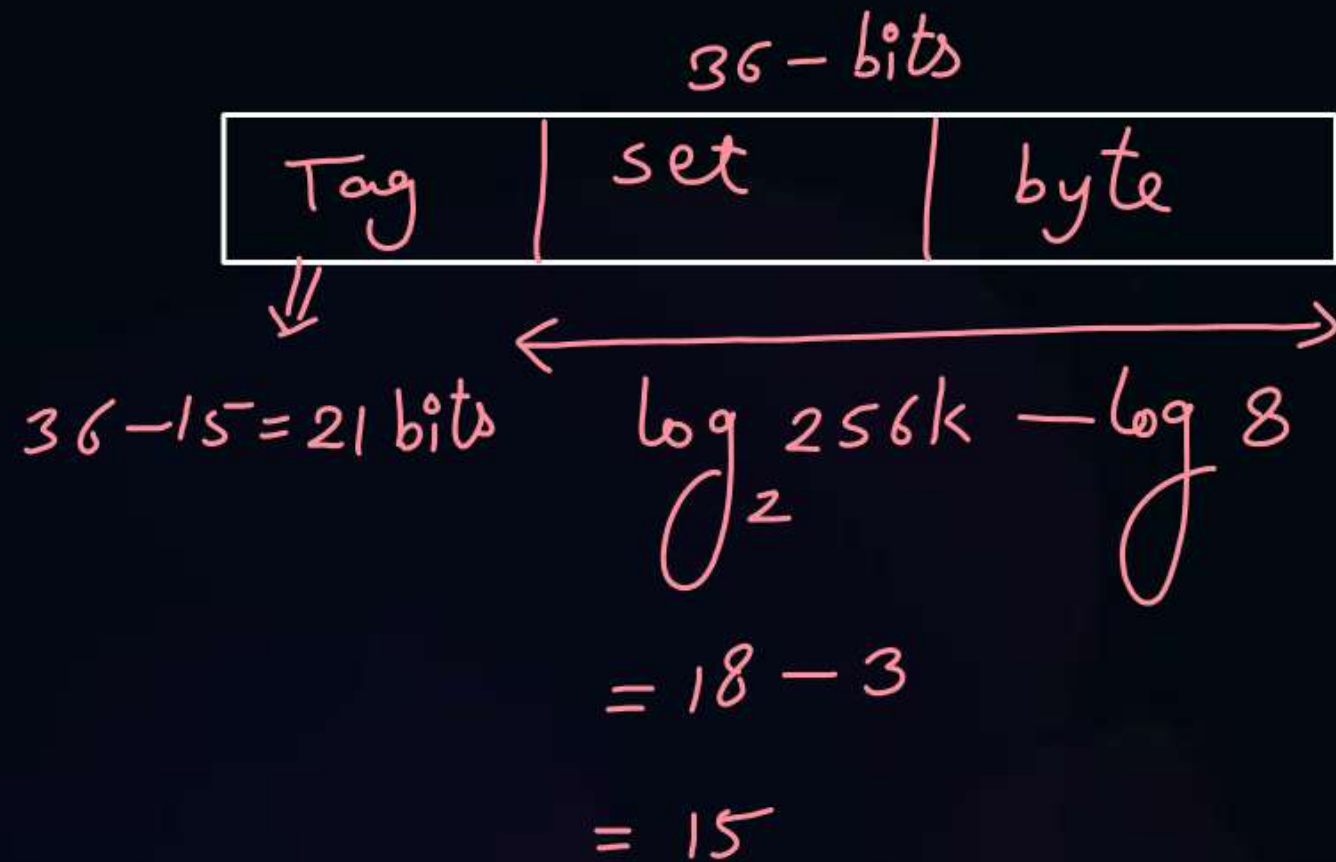
← $\log_2(\text{cm size}) - \log_2 k$ →

$$\text{Tag} = \text{mm add.} - \left[\log_2(\text{cm size}) - \log_2 k \right]$$

$$\text{Tag} = \text{mm add.} - \log_2(\text{cm size}) + \log_2 k$$

mem add.

#Q. The width of the physical address on a machine is 36 bits. The width of the tag field in a 256 KB 8-way set associative cache is 21 bits?



#Q.

cm size = 64MB

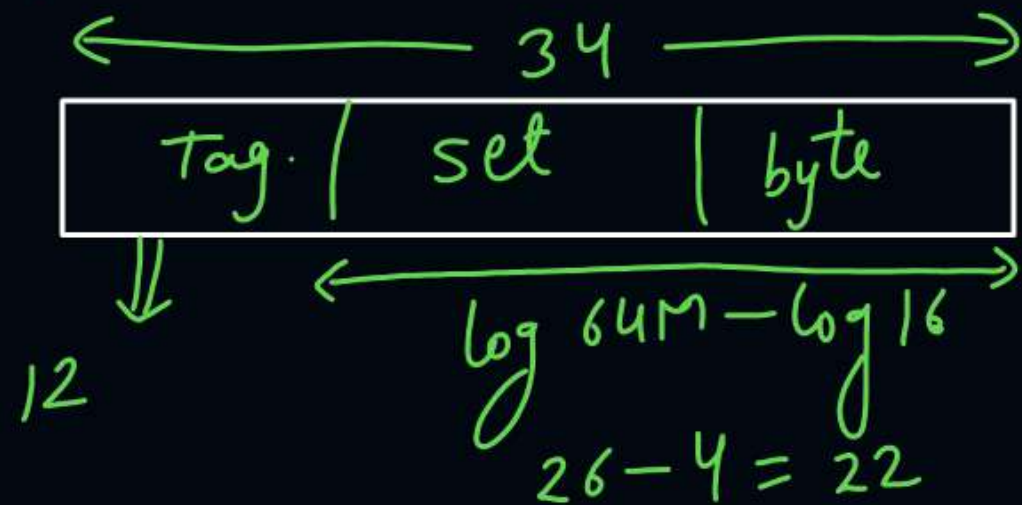
mm size = 16GB = 2^{34} B \Rightarrow add.
= 34 bits

16-way set associative cache

Tag = 12 bits?

Ans: - 12

Solⁿ:-



#Q MM size = 2^P bytes \Rightarrow $\text{add.} = P$ bits

GATE - CM size = 2^N bytes

2018 Block size = 2^M words = $2^M * 2^W$
= 2^{M+W}

(2M) word size = 2^W bytes

k-way set associative cache

Tag size = _____ bits?

$\longleftrightarrow P \longrightarrow$

Tag	set	byte
-----	-----	------

$\xleftarrow{N - \log k - M - W} \xrightarrow{M + W}$

$\xleftarrow{\log 2^N - \log k} \xrightarrow{\quad}$

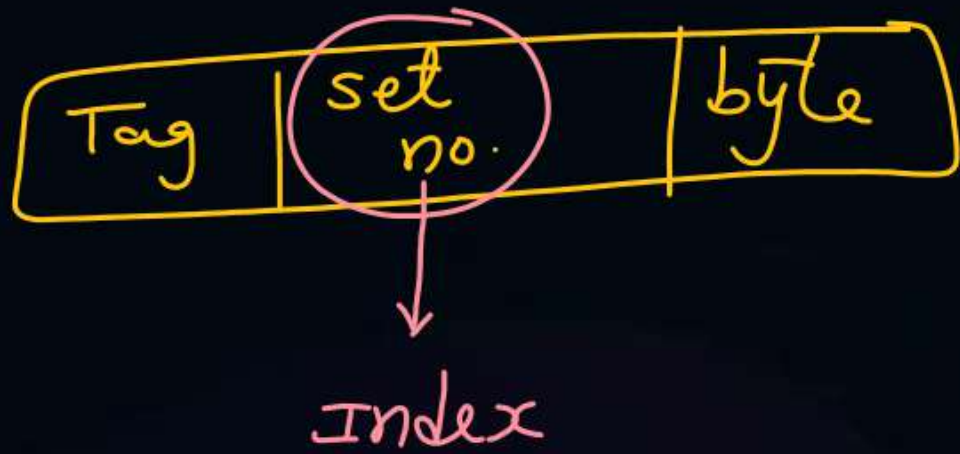
$\xleftarrow{N - \log k} \xrightarrow{\quad}$

$$\begin{aligned} \text{Tag} &= P - (N - \log k) \\ &= P - N + \log k \end{aligned}$$



Topic : Tag and Index in Associative Mapping

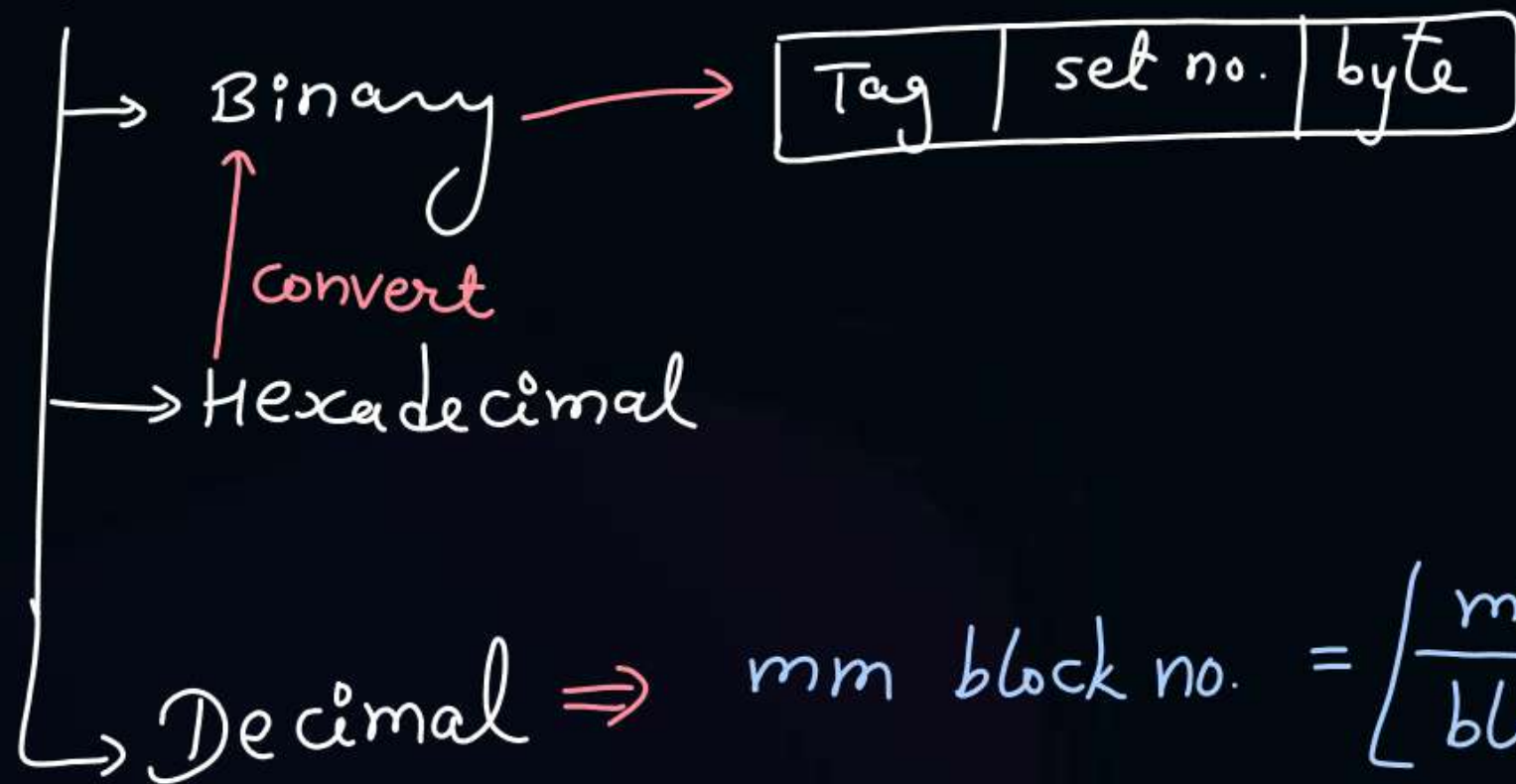
mem add.





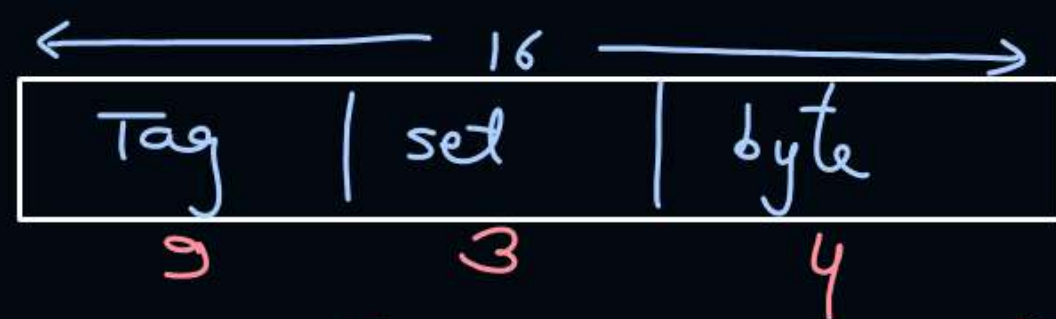
Topic : Calculating CM Set Number from MM Address

mm add.



$$\text{cm set no.} = \text{mm block no.} \% \text{ no. of sets in cache}$$

#Q) MM add. = 16 bits
 cm size = 512 bytes
 4-way set associative cache
 block size = 16 bytes



$$\log_2 2^9 - \log_2 4 = 7 \text{ bits}$$

$$\text{no. of sets in cache} = 2^3 = 8$$

maps to cm set no.

MM add.	
0010101111000000	00101011 100 0000
1111100001010011	101
$(62F5)_{16}$	1111 0101
$(ACD2)_{16}$	101

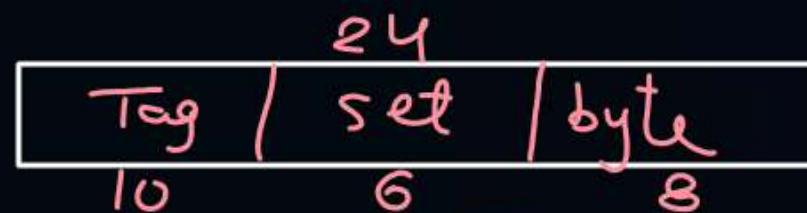
$$(100)_2 = (4)_{10}$$

$$(101)_2 = (5)_{10}$$

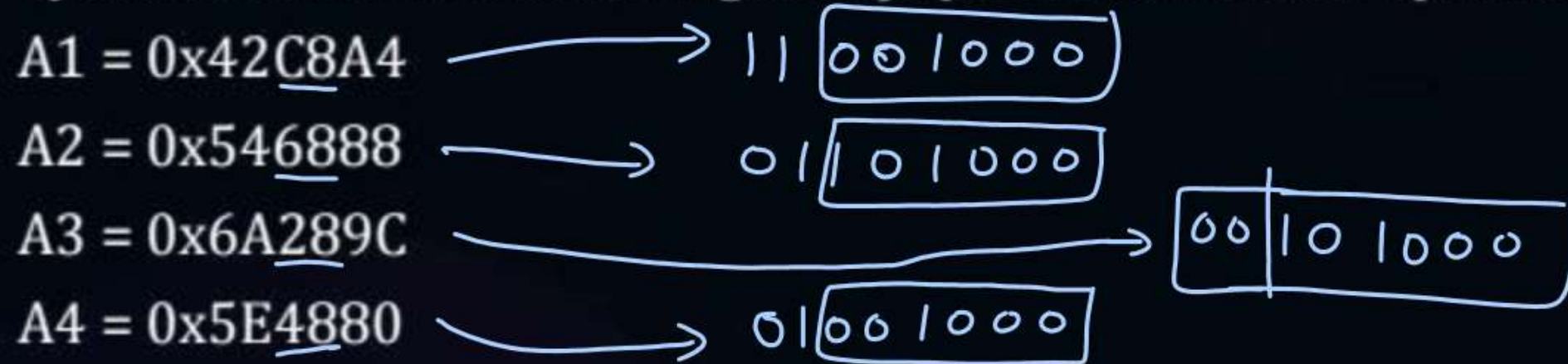
$$(111)_2 = (7)_{10}$$

$$(101)_2 = (5)_{10}$$

[MCQ] GATE-PYQ



#Q. A computer system with a word length of 32 bits has a 16 MB byte-addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four physical addresses represented in hexadecimal notation.



Which one of the following is TRUE?

- A** A1 and A4 are mapped to different cache sets. ✗
- B** ✓ A2 and A3 are mapped to the same cache set. ✓
- C** A3 and A4 are mapped to the same cache set. ✗
- D** A1 and A3 are mapped to the same cache set. ✗



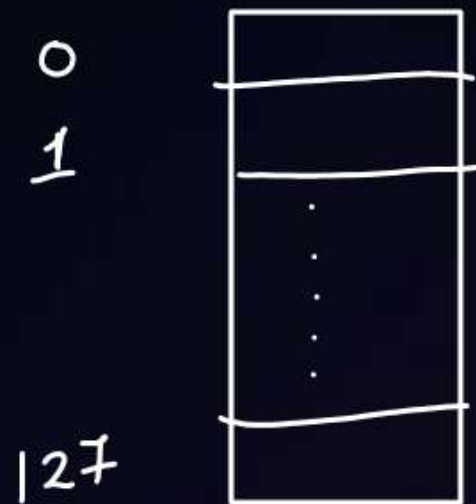
Topic : Fully Associative Mapping

ex:-

cache has 128 blocks

Direct mapped

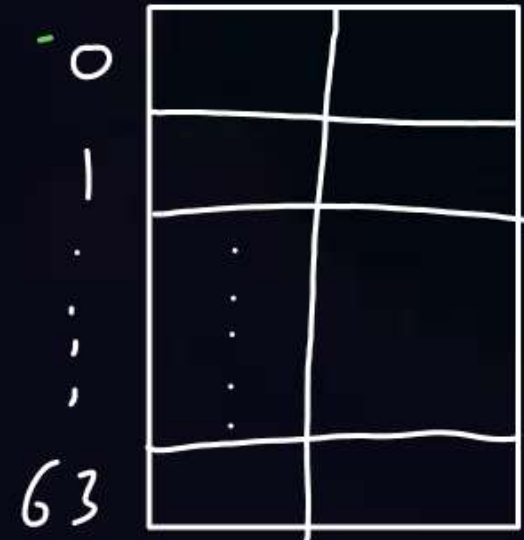
Tag	block	Byte
x	7 bits	y



2-way set

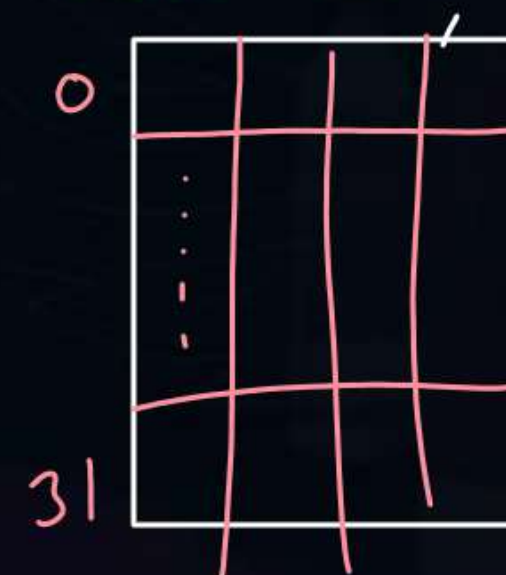
$$\text{no. of sets} = \frac{128}{2} = 64$$

Tag	Set	Byte
$x+1$	6	y

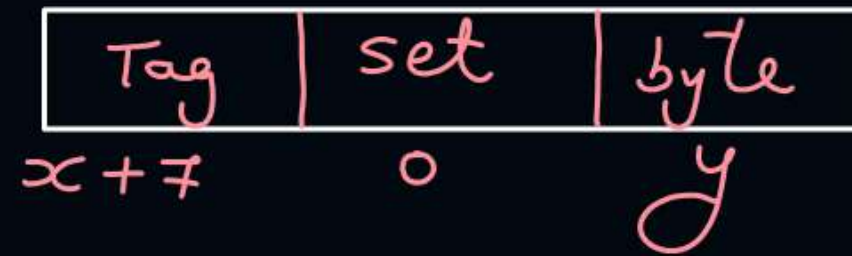


4-way set:-

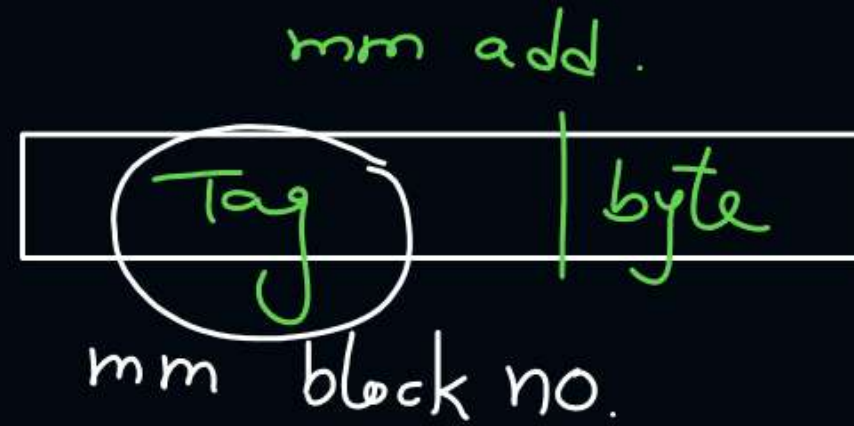
Tag	set	Byte
$x+2$	5	y



128-way set ass. \leftarrow fully ass. cache \leftarrow all blocks are organized in 1 set in cache



\Rightarrow



$$\text{no. of sets} = \frac{128}{128} = 1$$

$$\log_2 1 = 0$$

in fully ass. cache \Rightarrow Index has 0 bits



Topic : Fully Associative Mapping

In fully ass. cache \Rightarrow mem block no = Tag

Tag directory size = no. of blocks in cache * $\left(\text{Tag bits} + \text{Extra bits} \right)$

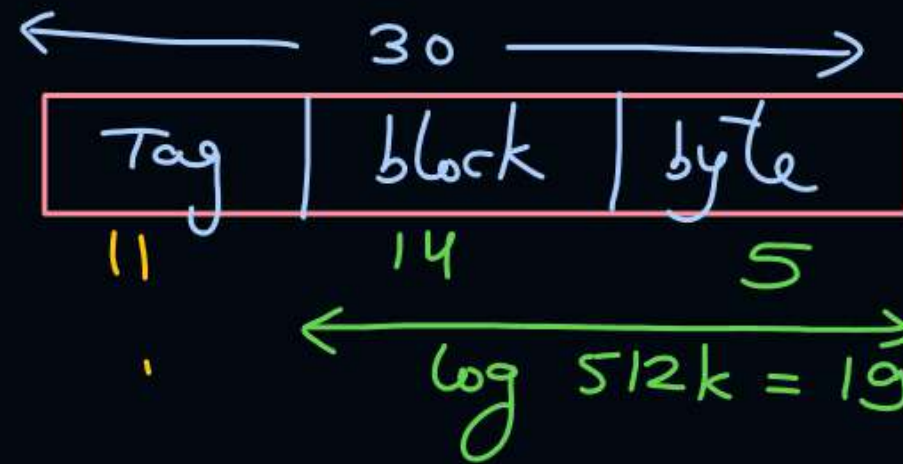
Q.] cm size = 512 kB
block size = 32 B
mm add. = 30 bits

Tag = — bits

Tag directory size = —

- for 1. Direct mapping
2. 4-way set ass.
3. Fully associative

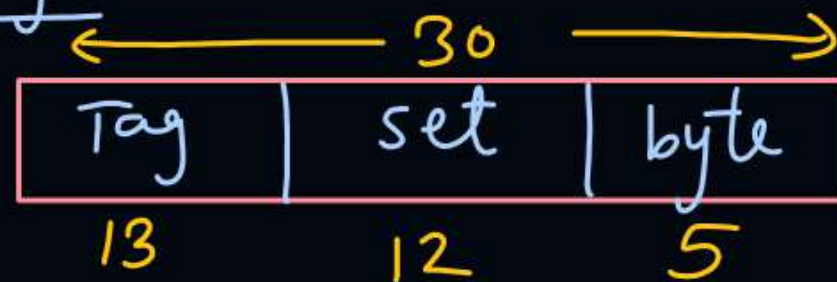
Direct:-



no. of blocks
in cache = $\frac{512 \text{ kB}}{32 \text{ B}}$
 $= \frac{2^{19}}{2^5} = 2^{14}$

Tag directory size = $2^{14} * 11$ bits

4-way:-



$\log 512k - \log_4 = 19 - 2 = 17$

Tag directory size = $2^{14} * 13$ bits

fully:-



Tag directory size = $2^{14} * 25$ bits

	Tag	Index
Direct	Min. Tag size	Max Index size
set-ass.		
fully ass.	Max Tag size	Min. Index (0-bit)

#Q. Consider a fully associative cache with 2^{16} blocks. The main memory contains 2^{24} blocks. The cache Tag directory size = — kbytes?

Ans) 192

Solⁿ

Tag directory size = no. of blocks in cache * Tag bits

$$= 2^{16} * 24\text{-bits} = 2^{16} * 3\text{ bytes} = 2^{10} * 2^6 * 3\text{ B}$$

$$= 192\text{ Kbytes}$$

mm block no. = 24 bits

Tag \Rightarrow mm block no.



2 mins Summary



Topic

Direct Mapping

Topic

Set Associative Mapping

Topic

Fully Associative Mapping



Happy Learning

THANK - YOU