CS & IT ENGINEERING

Computer Organization Architecture

Pipeline Processing

DPP- 01

Discussion Notes

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[NAT]

#Q. Consider a non-pipelined system which takes 100ns to perform a task. The same task can be performed using a 6-segment pipeline with cycle time of 20ns. The speed up of pipeline (rounded up to 2 decimal place) for 1000 tasks is _____?

$t_n = 100\,ns$

$k = 6$

$t_p = 20\,ns$

$n = 1000$

$$S = \frac{n * t_n}{(k+n-1)\,t_p}$$

$$= \frac{1000 * 100}{(6+1000-1)\,20}$$

$$= 4.975$$

$$= \underline{\underline{4.98}}$$

[NAT]

Ans = 4.74

#Q. Consider 6 segment pipeline with segment delay of segments as 140 picoseconds, 109 picoseconds, 160 picoseconds, 154 picoseconds, 125 picoseconds and 170 picoseconds respectively. Pipeline uses an intermediate buffer after every segment with a delay of 10 picoseconds. Speed up of pipeline (rounded up to 2 decimal place) for processing of 1000 tasks is _____ ?

$k = 6$, $n = 1000$

$t_p = \max(140, 109, 160, 154, 125+170) + 10$

$= 180ns$

$t_n = 140 + 109 + 160 + 154 + 125 + 170 = 858$

$$S = \frac{1000 * 858}{(6+1000-1)180}$$

$$= 4.74$$

[MCQ]

#Q. Consider a non-pipelined processor with a clock rate of 5GHz and an average cycle of 4 per instruction. The same processor is upgraded to a pipelined processor with 6 stages and the clock speed of 4GHz. Assume that there are no stalls in the pipeline. MIPS count of the pipeline processor in ideal condition and MIPS count of non-pipeline processor respectively are?

A 4000, 5000

B ✓ 4000, 1250

C 1250, 4000

D 5000, 1250

Pipeline :-

$$CPI = 1$$ ideal condit^n & no stall

$$MIPS = \frac{4\,GHz}{CPI * 10^6}$$

$$= \frac{4000}{1}$$

$$= 4000 \text{ MIPS}$$

Non-pipeline :-

$$MIPS = \frac{5\,GHz}{4 * 10^6}$$

$$= \frac{5000}{4}$$

$$= 1250 \text{ MIPS}$$

[NAT]

Ans = 60

#Q. The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 nanoseconds. The first stage (with delay 800 ~~pico~~ nano seconds) is replaced with a functionally equivalent design involving two stages with respective delays 450 and 350 nanoseconds. The throughput increase of the pipeline is _____ %?

old pipeline

$k = 4$

800, 500, 400, 300

$t_p = 800$

Throughput $= \frac{1}{800}$

new pipeline

$k = 5$

450, 350, 500, 400, 300

$t_p = 500$

Throughput $= \frac{1}{500}$

$$\% \text{ of throughput increase} = \frac{\frac{1}{500} - \frac{1}{800}}{\frac{1}{800}} * 100\%$$

$$= (1.6 - 1) * 100\%$$

$$= 60\%$$

[NAT]

Ans = 234

#Q. Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delay for FI, DI, FO, EI and WO are 9 ns, 8 ns, 12 ns, 10 ns and 11 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 20 instructions I1, I2, I3, ……..,I20 is executed in this pipelined processor. Instruction I7 is only the branch instruction, and its branch target is I17. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is ____?

$t_p = \max(9, 8, 12, 10, 11) + 1 = 13$ ns

$k = 5$

no. of instructions executed $(n) = 7 + 4 = 11$ (I1 to I7, I17 to I20)

no. of cycles without hazard $= 5 + 11 - 1 = 15$

stalls due to 1 branch instruction $= 4 - 1 = 3$

Total $= 18$ cycles

Total time $= 18 * 13$ ns

$= \underline{\underline{234}}$ ns

[NAT]

#Q. Consider a program which contains 500 instructions I1, I2 , I3 .. I500. Further consider a 5-stage pipeline with stages as: Instruction Fetch, Decode, Operand Fetch, Execution and Write-Back. The program contains 3 branch instructions, information of those given in a table below. The number of cycles required to execute this program in the given pipeline is _____?

Branch Instruction	Target Instruction	Branch Taken or Not
I9	I49	Taken
I234	I381	Not Taken
I412	I497	Taken

No. of instructions executed = 9 − 1 + 1 = 9 (I1 to I9)

= 412 − 49 + 1 = 364 (I49 to I412)

= 500 − 497 + 1 = 4 (I497 to I500)

Total (n) = 377

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without hazard, no. of cycles = 5 + 377 − 1 = 381

stall cycles due to branch = 3 * (4 − 1) = 9

390 cycles Ans.

[NAT]

Ans = 3.98

#Q. Consider a non-pipelined processor with a clock rate of 5GHz and an average cycle of 5 per instruction. The same processor is upgraded to a pipelined processor with 6 stages and the clock speed of 4GHz. Assume that there are no stalls in the pipeline. The speed up (rounded up to 2 decimal place) achieved in the pipeline for 1000 instructions is _____?

Non-pipeline

$t_n = 5 * \frac{1}{5GHz}$

$= 1\,ns$

pipeline

$t_p = \frac{1}{4GHz}$

$= 0.25\,ns$

$k = 6$

$n = 1000$

$S = \frac{1000 * 1\,ns}{(6 + 1000 - 1)\,0.25}$

$= 3.98$

THANK - YOU