CS & IT ENGINEERING

COMPUTER ORGANIZATION AND ARCHITECTURE

IO Organization

Lecture No.-02

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Recap of Previous Lecture

Topic Peripheral Device

Topic IO vs Memory Buses

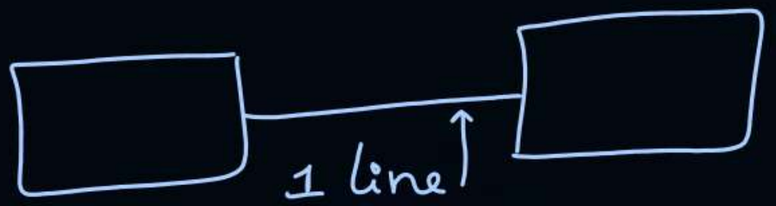
Topic Memory Mapped IO vs IO Mapped IO

Topics to be Covered

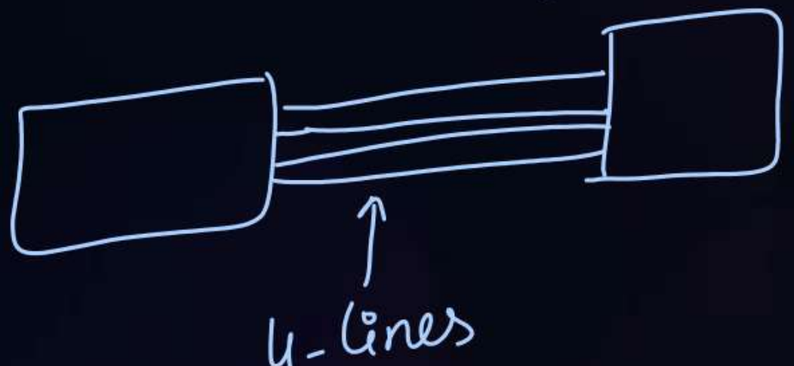
- Topic: Asynchronous Data Transfer
- Topic: Modes of Transfer
- Topic: Programmed IO
- Topic: Interrupt IO

Topic : Asynchronous Data Transfer

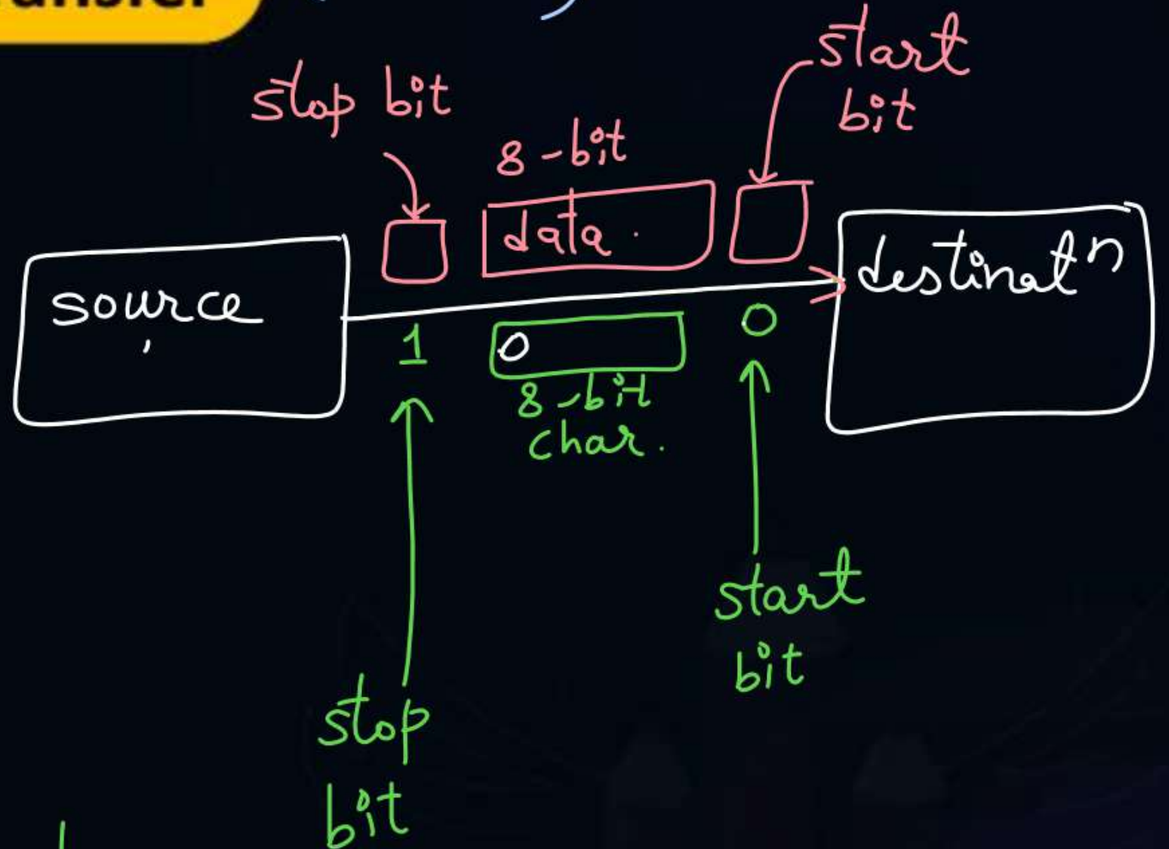
serial transfer

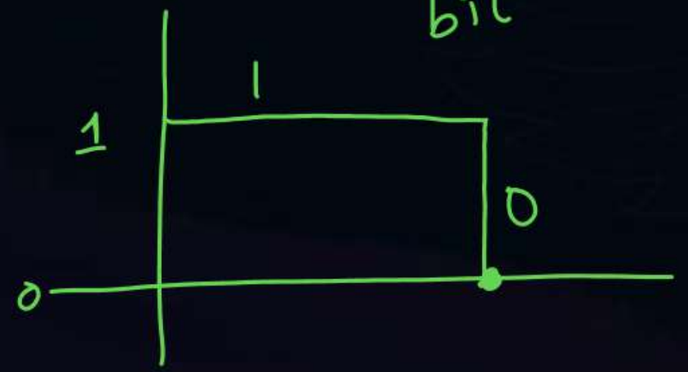


parallel transfer



(serial)





Effective transmission rate = efficiency * actual transfer rate

$$\text{efficiency of transmission line} = \frac{\text{bits in 1 char}}{\text{bits transmitted for each char}}$$

$$= \frac{8}{8+1+1}$$

$$= \frac{8}{10}$$

$$= 0.8 \text{ or } 80\%$$

[NAT]

Ans. = 800

#Q. How many 8-bit characters can be transmitted per second over 9600 bits/sec. serial communication link using a parity synchronous mode of transmission with 1 start bit, 8 data bits, 2 stop bits and 1 parity bit?

bits for 1 char = 1 + 8 + 2 + 1 = 12 bits

$$\text{char/sec} = \frac{9600}{12} = 800 \text{ char/sec.}$$

[NAT]

#Q. An asynchronous serial communication is employing 8 character bits, 1 parity bit, 2 start bits and 1 stop bit. To maintain a rate of 700 char/sec the minimum transfer rate should be required is ____ bits/sec?

for 1 char, bits to be transferred = 8 + 1 + 2 + 1 = 12 bits

700 char, ——"—— ——————— = 700 * 12

= 8400 bits/sec

---

efficiency of line = $\frac{8}{8+1+2+1} = \frac{8}{12}$

[NAT]

#Q. 8-bit characters can be transmitted using a parity synchronous mode of transmission with 1 start bit, 8 data bits, 2 stop bits and 1 parity bit.

1. What is the efficiency of the transmission line? $= \frac{8}{1+8+2+1} = \frac{8}{12}$
2. If the transfer rate of the line is 3000 bits per second, then effective transfer rate is?

2.

Effective transfer rate $= \frac{8}{12} * 3000$ bits/sec

$= \frac{2}{3} * 3000$ bits/sec

$= 2000$ bits/sec $= \frac{2000}{8}$ bytes/sec $= 250$ bytes/sec

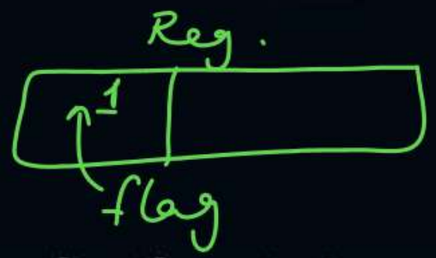
Topic : Modes of Transfer

1. Programmed I/O or Program Controlled I/O
2. Interrupt Initiated I/O or Interrupt Driven I/O

3. DMA (Direct Memory Access) ← between I/O & mem.

Topic : Programmed IO

- There is no any provision through which IO can inform to CPU about data transfer
- IO sets its own status and waits
- CPU runs program periodically and checks the status of each device one-by-one
- If any device has its status set then CPU performs data transfer for it.



polling

☹ ⇒ wastage of CPU time in polling.

Time required in programmed I/O

= status check time + Data transfer time

↓

time needed by device to process & send status Reg. to CPU

↓

depends on I/O operational speed

Ques) Assuming a device operating on 20 MBPs rate. The time needed to check status in programmed I/O if status reg. size is 1 byte?

Soln

20 MB, processing time = 1 sec

1 B —11— $= \frac{1 \text{ sec} * 1\text{B}}{20 \text{ MB}}$

$= \frac{1}{20}$ μsec

$= 0.05$ μsec $= 50$ nsec

Topic : Interrupt Initiated IO

- IO device has a provision (Interrupt Signal) to inform to CPU about communication.

Topic : Interrupt Initiated IO

- IO device has a provision (Interrupt Signal) to inform to CPU about communication.
- When CPU receives interrupt:
  - It completes execution of current instruction
  - Saves the status (PC, PSW etc.) of current process onto the stack
  - Branches to service the interrupt
  - Resumes the previous process by taking out the values from stack

[MCQ] GATE-2018

#Q. The following are some events that occur after a device controller issues an interrupt while process L is under execution.

P. The processor pushes the process status of L onto the control stack

Q. The processor finishes the execution of the current instruction

R. The processor executes the interrupt service routine

S. The processor pops the process status of L from the control stack

T. The processor loads the new PC value based on the interrupt

Which of the following is the correct order in which the events above occur?

A ✓ QPTRS

B PTRSQ

C TRPQS

D QTPRS

Topic : Interrupt Initiated IO

Interrupt Service Routine :- (ISR)

A funct^{n} or a prog. ; execution of which services the interrupt.

Topic : Vectored vs Non-Vectored

(scalar)

device sends interrupt & reference of ISR too.

⇓

CPU runs ISR & services the interrupt

device sends only interrupt

⇓

CPU runs a default service routine to understand → which device sent interrupt, why & where is it's ISR

then CPU runs ISR.

Topic : Maskable vs Non-Maskable

Can be accepted
or
Can be rejected

always accepted

Topic : Internal Vs External

(Software)

(Hardware)

generated by devices

if any unexpected error occurs during execut^n of an instruct^n, then s/w interrupt is occurred.

⇒ First CPU services internal interrupt, then CPU restarts that instruct^n.

example:- Page fault

2 mins Summary

Topic Asynchronous Data Transfer

Topic Modes of Transfer

Topic Programmed IO

Topic Interrupt IO

Happy Learning

THANK - YOU