



29TH INTERNATIONAL SYMPOSIUM ON VLSI DESIGN AND TEST (VDAT-2025)

VLSI Design and Semiconductor Technology for Next Gen Chips & AI Applications

7 - 9 AUGUST 2025

HOTEL SHIVALIK VIEW, SECTOR-17, CHANDIGARH, INDIA

CALL FOR PAPERS

The aim of the VLSI Design & Test Symposium (VDAT-2025) is to foster a platform where academia, researchers, startups, and industrial practitioners can exchange innovative ideas, share experiences, and disseminate knowledge across diverse realms of VLSI Design and Testing. We invite submissions of research papers and accompanying presentations that delve into highly technical content and explore emerging trends across VLSI Design and Testing domains.

Emerging Materials and Devices Technologies

- Emerging materials
- 2-D Material
- High-voltage MOSFET
- Si photonics and optoelectronics
- Spintronics and quantum materials
- MEMS/NEMS
- Organic electronics
- Emerging memory technologies

VLSI Circuit and SoC Design

- Digital, Analog, Mixed signal, RF circuits,
- RTL design,
- Processor Architecture,
- Hardware accelerators
- FPGA based design
- Quantum circuits
- Neuromorphic
- Memory
- Circuits, accelerators, SoC for ML/AI applications

Electronics Design Automation, Testing and Verification

- CAD Tools, software
- CAD for FPGA
- High Level Synthesis
- System software
- Testing and Verification

Embedded Systems Design

- Embedded AI and Machine Learning
- Real-Time Systems and Applications
- Embedded Software and Firmware Development
- Hardware/Software Co-Design
- IoT, Edge, and Wireless Embedded Systems
- Embedded Vision and Multimedia Processing
- Reconfigurable Systems and FPGAs
- Automotive, Healthcare, and Industrial Applications

Packaging and Manufacturing

- Manufacturing technologies
- Packaging
- Signal and Power Integrity

Scan to Submit



<https://softconf.com/vlsi/vdat2025>

Email: vdat2025@iitrpr.ac.in

SUBMISSION INFO

Authors are invited to submit full-length (6 pages maximum), original, unpublished papers along with an abstract of at most 200 words. Paper Format: Submissions should be in camera-ready IEEE two-column format, following the IEEE proceedings specifications.

IMPORTANT DATES

15th April
2025

Paper Submission
Deadline

15th June
2025

Acceptance
Notification

20th June
2025

Early Bird
Registration &
Payment

1st July
2025

Regular
Registration &
Payment

7th - 9th Aug
2025

Conference
Date



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