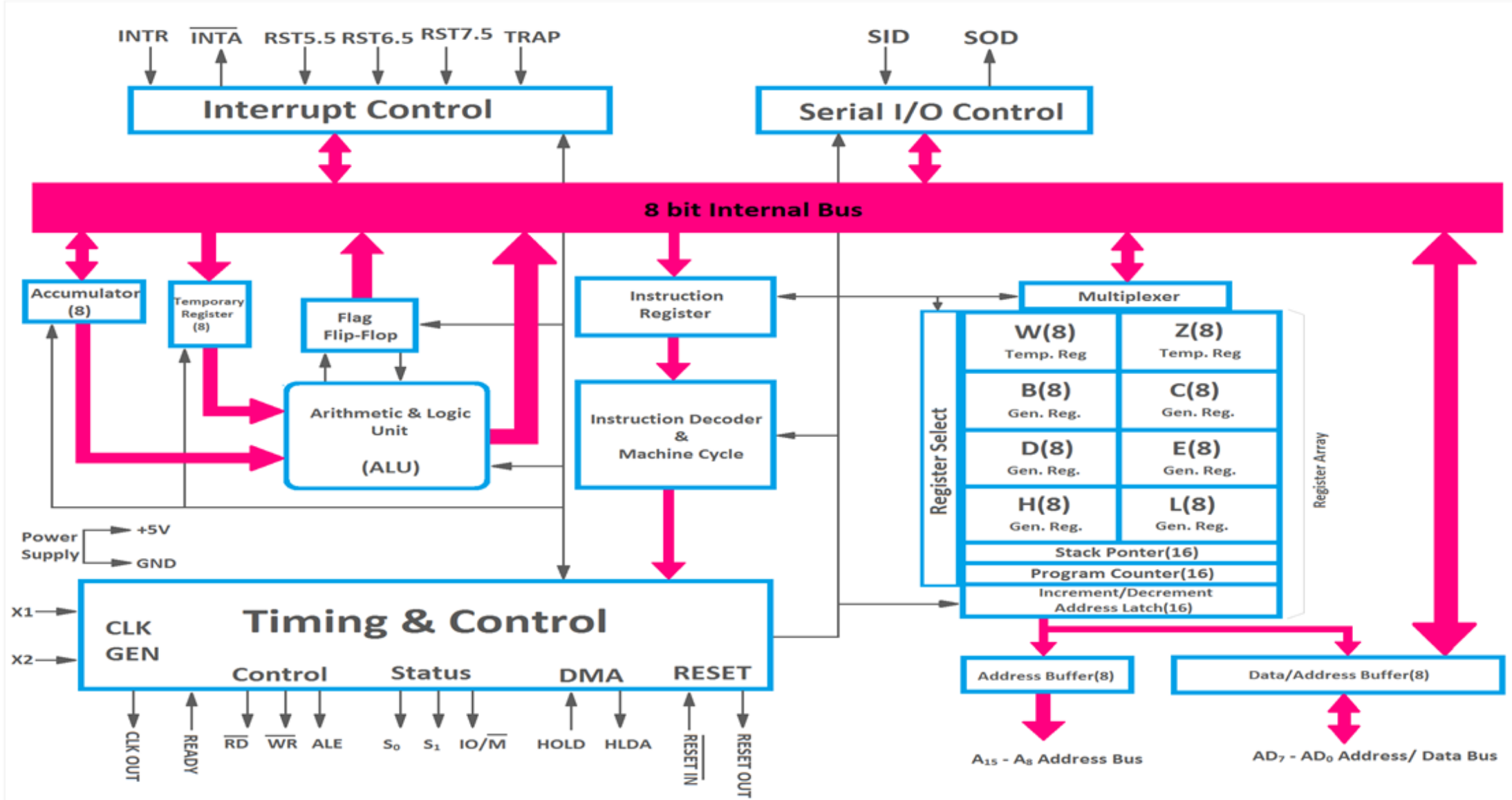
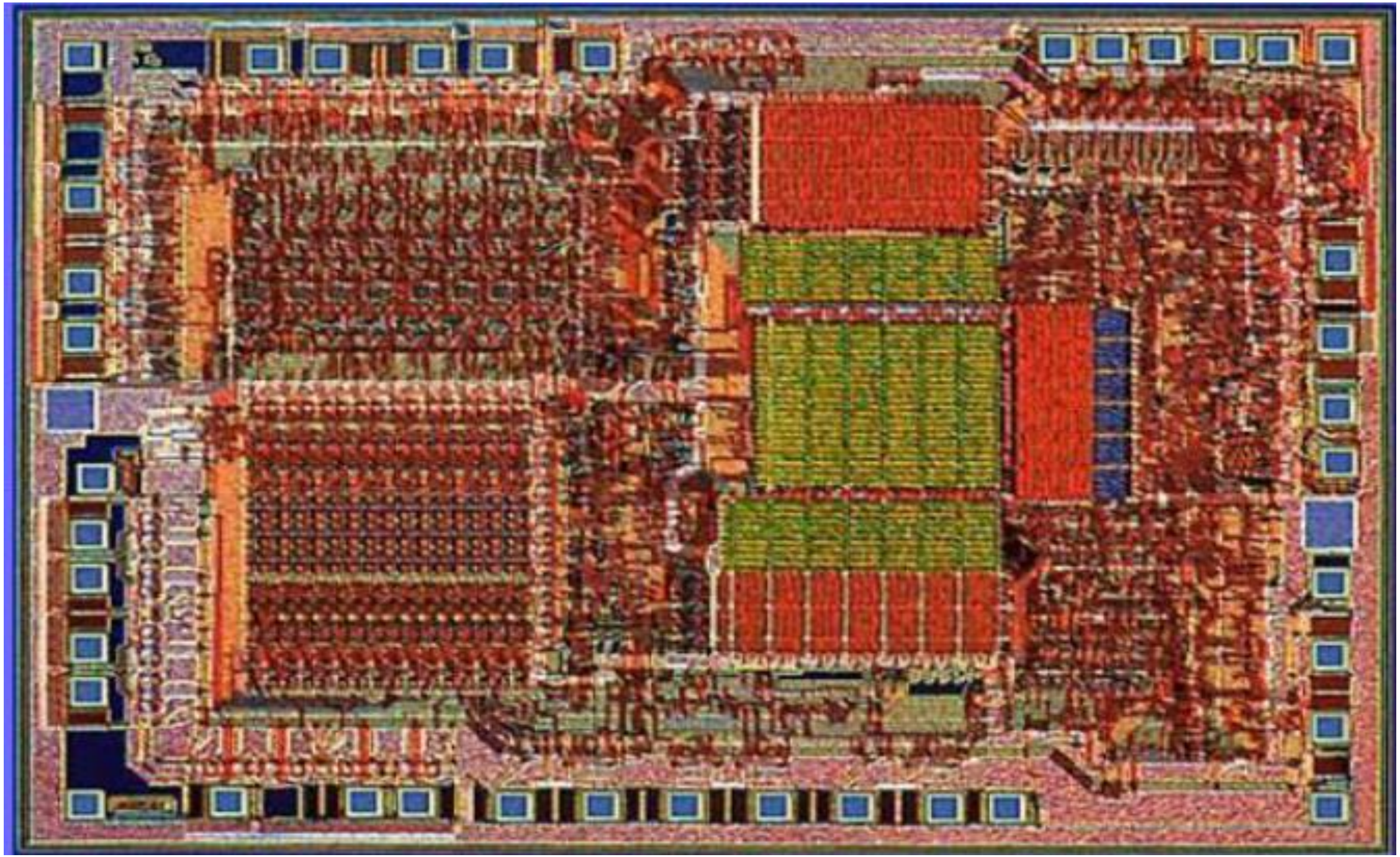
Introduction to Microprocessor



Microprocessor 8085 Block Diagram and Architecture



(1)

Processing	
ALU	*Instruction Decoder*

(2)

Address Data Bus	Address Bus
AD7-AD0	*A8-A15*

(3)

Serial I/O	
SID	*SOD*

(4)

INTERRUPTS					
RST 7.5	RST 6.5	RST 5.5	TRAP	INTA	INTR

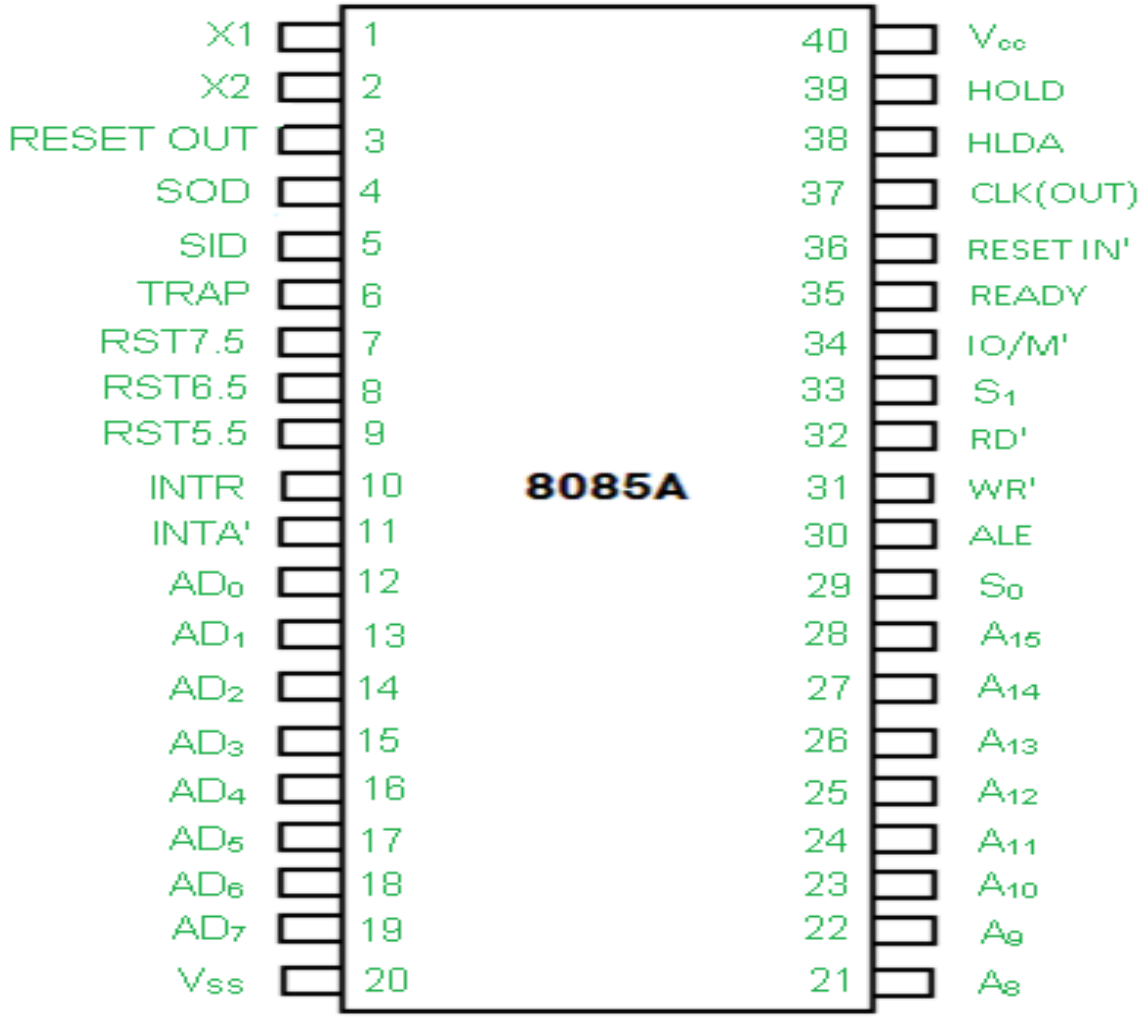
(5)

RESGISTERS									
General Purpose Register		Special Purpose Register			16 Bit Register		Temp Register		
B (8 bits)	*C (8 bits)*	*Accumulator (A)*	*Instruction Register*	*Flag Registers*	*Stack Pointer*	*Program Counter*	*W (8 bits)*	*Z (8 bits)*	*Temp Data Register*
D (8 bits)	*E (8 bits)*								
H (8 bits)	*L (8 bits)*								

(6)

TIMING AND CONTROL UNIT											
Crystal Inputs		Status Signal			Control Signals			DMA		RESET	
X1	X2	S1	S0	IO/$\overline{M}$	$\overline{WR}$	$\overline{RD}$	ALE	HOLD	HLDA	RESET IN	RESET OUT

Pin Diagram of 8085

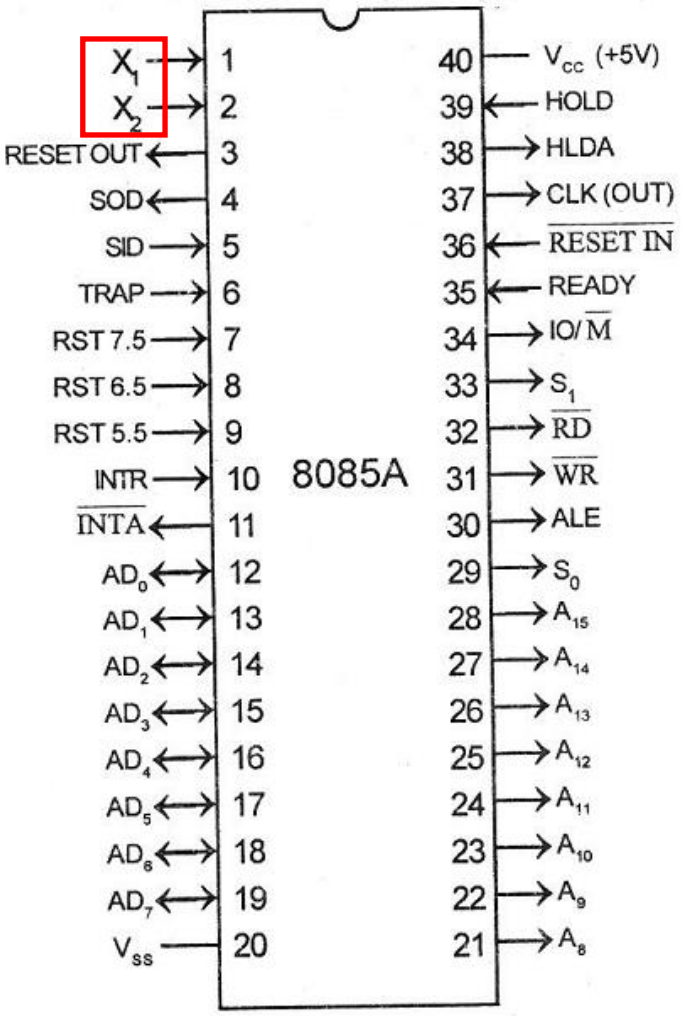


Pin Diagram of 8085 (Cont.….)

Pin 1 and Pin 2 (Input)

- These are also called Crystal Input Pins.

  8085 can generate clock signals internally.
- To generate clock signals internally, 8085 requires external inputs from X1 and X2
- Clock generator provides an output on CLK OUT (pin 37)



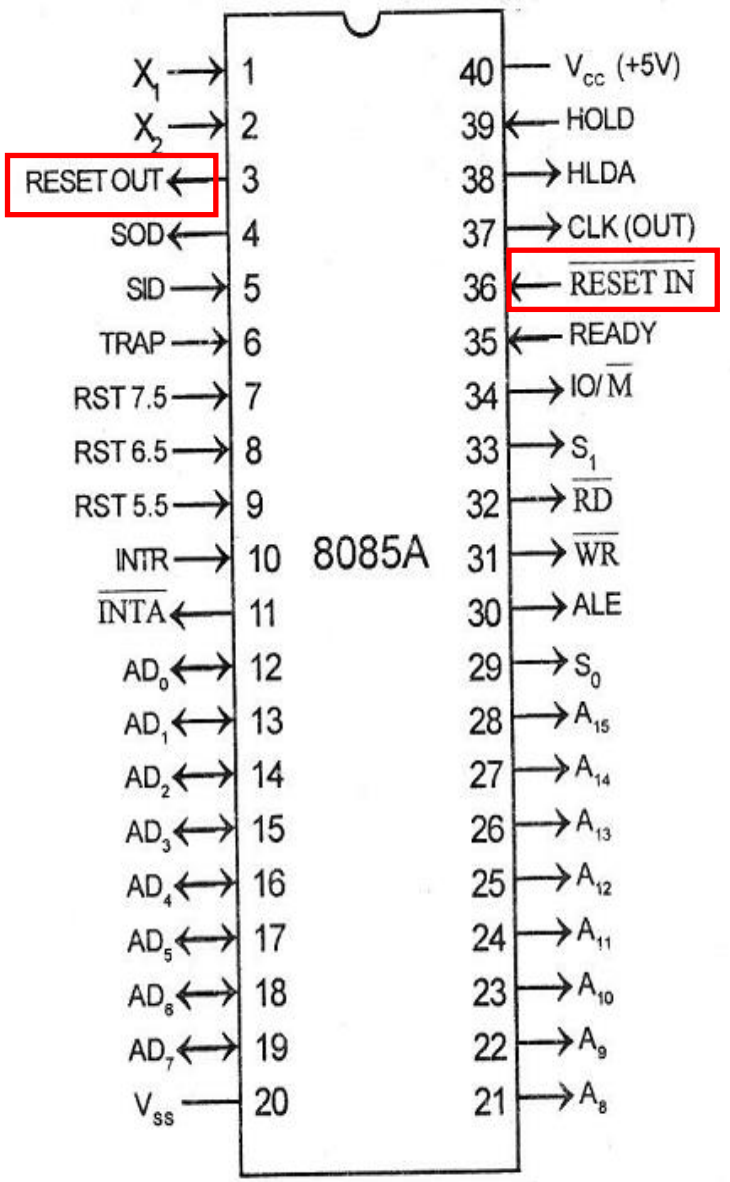
Pin 3 (Output) and Pin 36 (Input)

RESET IN:

- It is used to reset the Microprocessor.
- It is active low signal.
- When the signal on this pin is low for at least 3 clocking cycles, it forces the microprocessor to reset itself.
- The meaning of reset is:
  - Clearing the PC and IR.
  - Disabling all interrupts (except TRAP).
  - Disabling the SOD pin.
  - All the buses (data, address, control) are tri-stated.
  - Gives HIGH output to RESET

RESET OUT:

- It is used to reset the peripheral devices and other ICs on the circuit.
- It is an output signal.
- It is an active high signal.
- The output on this pin goes high whenever RESET IN is given low signal.
- The output remains high as long as RESET IN is kept low.



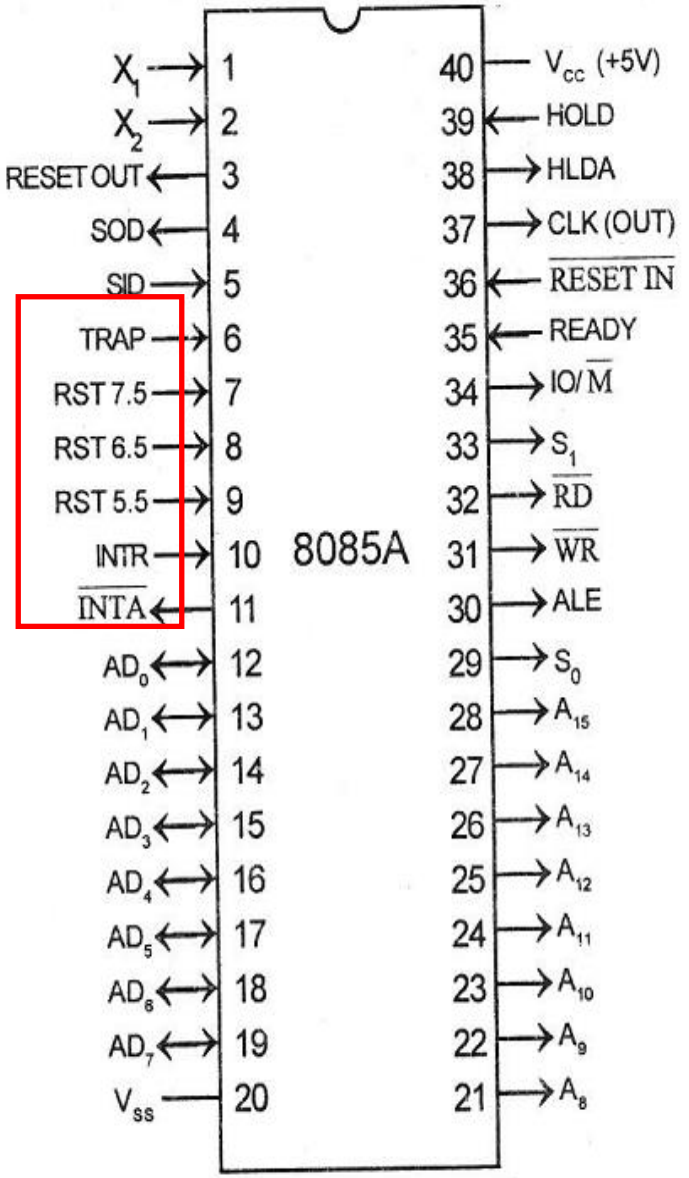
Pin 4 (Input) and Pin 5 (Output)

SID (Serial Input Data):

- It takes 1 bit input from serial port of 8085.
- Stores the bit at the 8th position (MSB) of the Accumulator.
- RIM (Read Interrupt Mask) instruction is used to transfer the bit.

SOD (Serial Output Data):

- It takes 1 bit from Accumulator to serial port of 8085.
- Takes the bit from the 8th position (MSB) of the Accumulator.
- SIM (Set Interrupt Mask) instruction is used to transfer the bit.



Pin (6-11) are Interrupts

- It means interrupting the normal execution of the microprocessor.
- When microprocessor receives interrupt signal, it discontinues whatever it was executing.
- It starts executing new program indicated by the interrupt signal.
- Interrupt signals are generated by external peripheral devices.
- After execution of the new program, microprocessor goes back to the previous program.

Sequence of Steps Whenever There is an Interrupt

1. Microprocessor completes execution of current instruction of the program.
2. PC contents are stored in stack.
3. PC is loaded with address of the new program.
4. After executing the new program, the microprocessor returns back to the previous program.
5. It goes to the previous program by reading the top value of stack.

Address and Data Pins 12-19

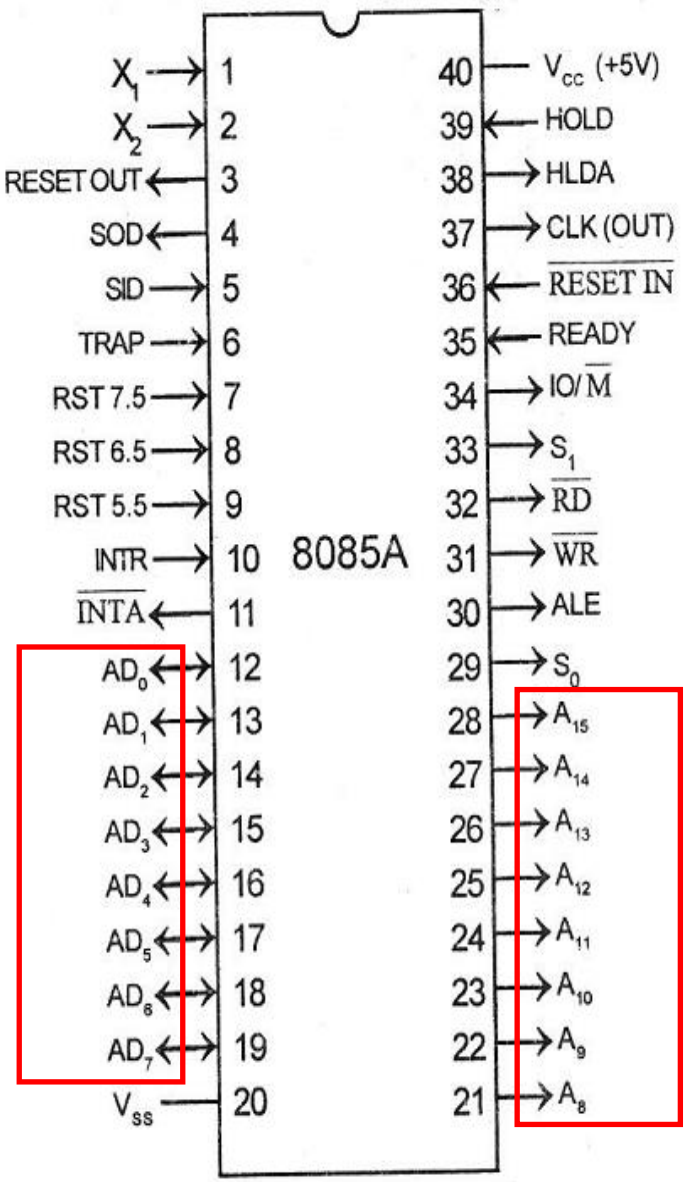
$AD_0 – AD_7$ (Bidirectional)

- These pins serve the dual purpose of transmitting lower order address and data byte.
- During 1st clock cycle, these pins act as lower half of address.
- In remaining clock cycles, these pins act as data bus.
- The separation of lower order address and data is done by address latch.

Address Pins 21-28

$A_8 – A_{15}$ (Unidirectional)

- During all clock cycle, these pins act as upper half of address
- These pins carry the higher order of address bus.
- The address is sent from microprocessor to memory.

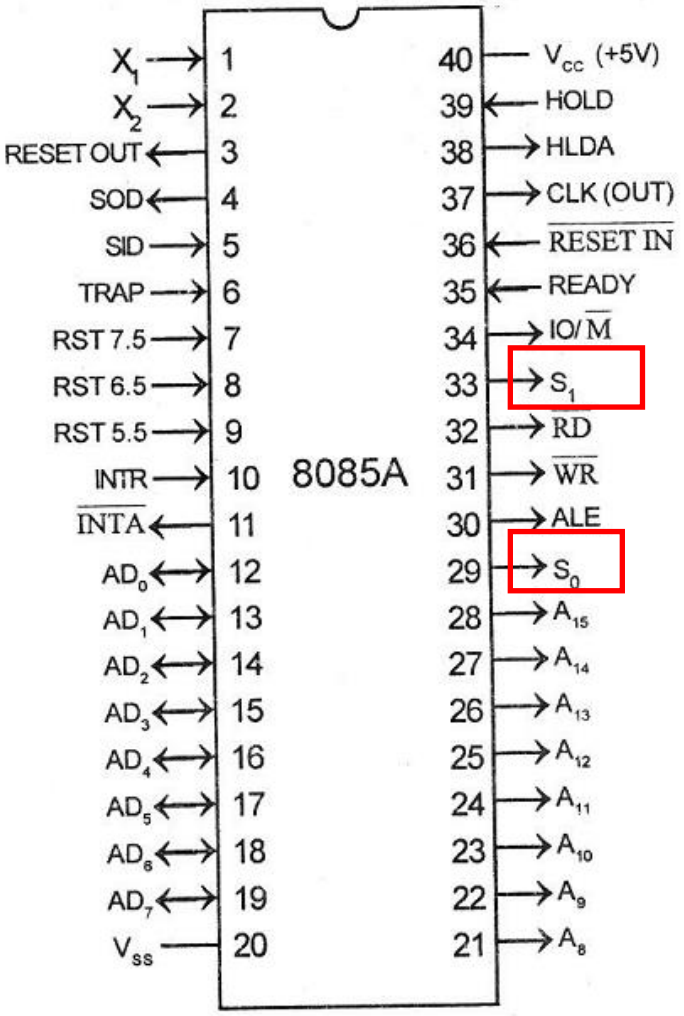


S_0 and S_1

Pin 29 (Output), and Pin 33 (Output)

- S_0 and S_1 are called Status Pins.
- They tell the current operation which is in progress in 8085.

S_0	S_1	Operation
0	0	Halt
0	1	Write
1	0	Read
1	1	Opcode Fetch



Address Latch Enable (ALE) Pin 30 (Output)

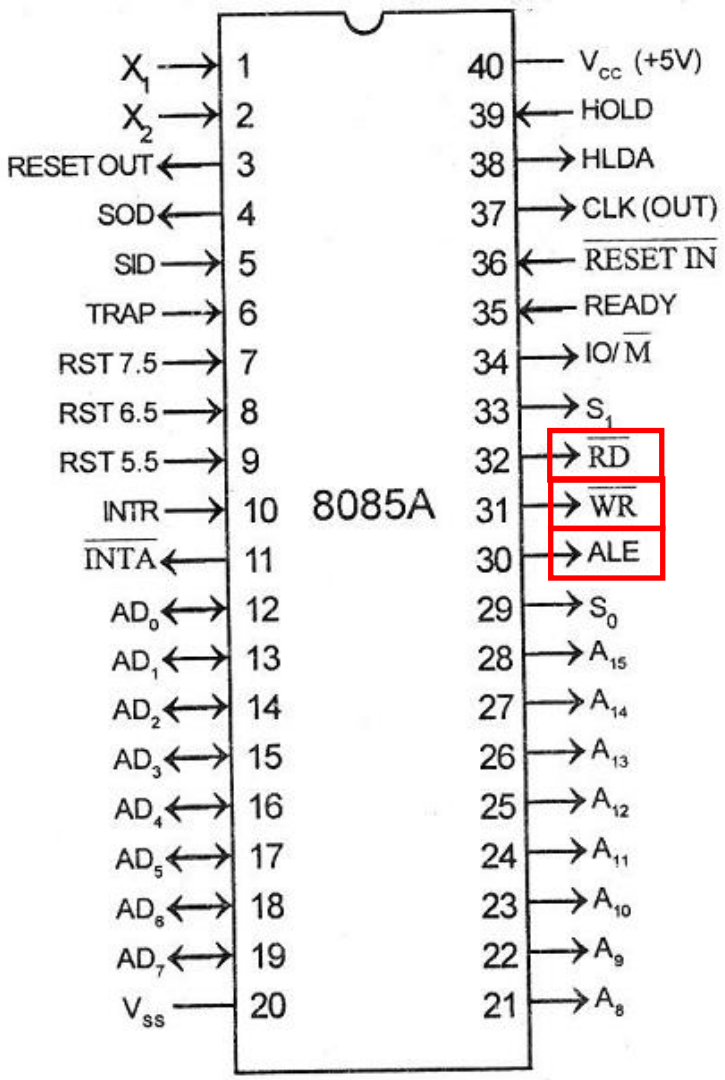
- It is used to enable Address Latch.
- It indicates whether bus functions as address bus or data bus.

If **ALE = 1** then

- Bus functions as address bus.

If **ALE = 0** then

- Bus functions as data bus.



$\overline{WR}$ Pin 31 (Output)

- WR stands for Write.
- It is an active low signal.
- It is a control signal used for Write operation either into memory or into output device.
- A low signal indicates that data on the data bus must be written into selected memory location or into output device.

$\overline{RD}$ Pin 32 (Output)

- RD stands for Read.
- It is an active low signal.
- It is a control signal used for Read operation either from memory or from input device.
- A low signal indicates that data on the data bus must be Read from selected memory location or from input device.

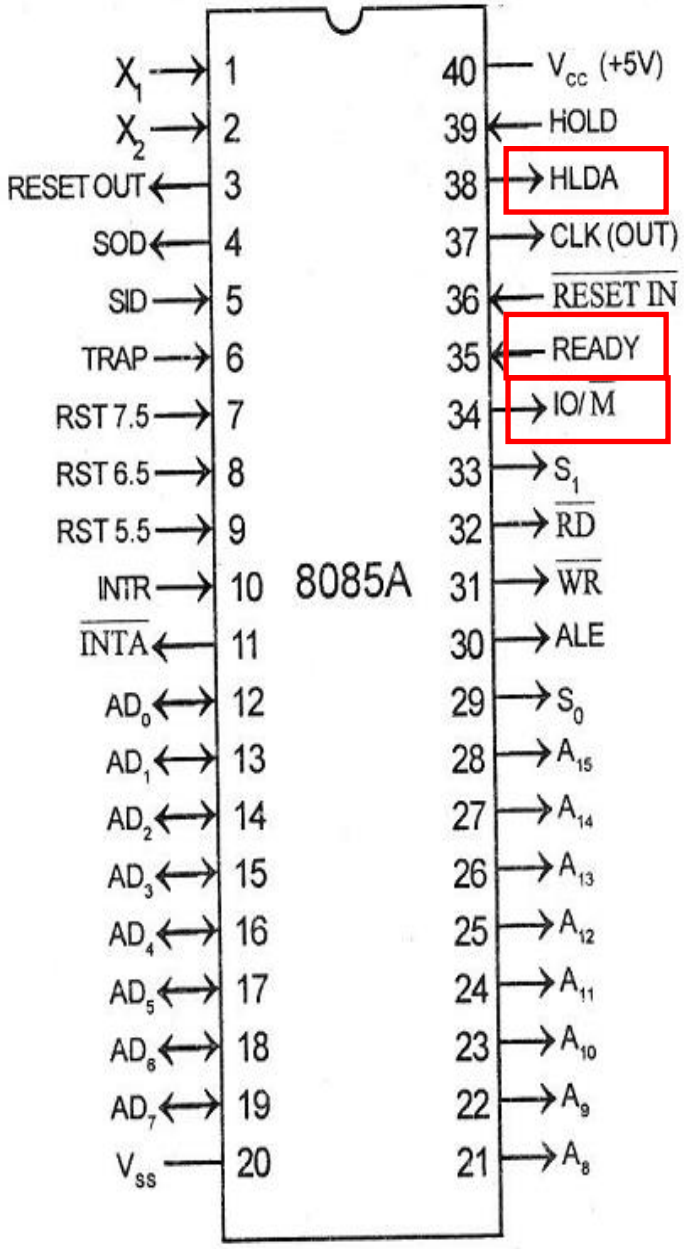
IO/M Pin 34 (Output)

- This pin tells whether I/O or memory operation is being performed.
  If IO/M = 1 then
  - I/O read or Write operation is being performed.

  If IO/M = 0 then
  - Memory read or write operation is being performed.

READY Pin 35 (Input)

- This pin is used to synchronize slower peripheral devices with fast microprocessor.
- A low value causes the microprocessor to enter into ***wait state***.
- The microprocessor remains in wait state until the input at this pin goes high.



DMA: *HOLDA* Pin 38 (output) and *HOLD* Pin 39 (Input)

HOLDA Pin 38 (output)

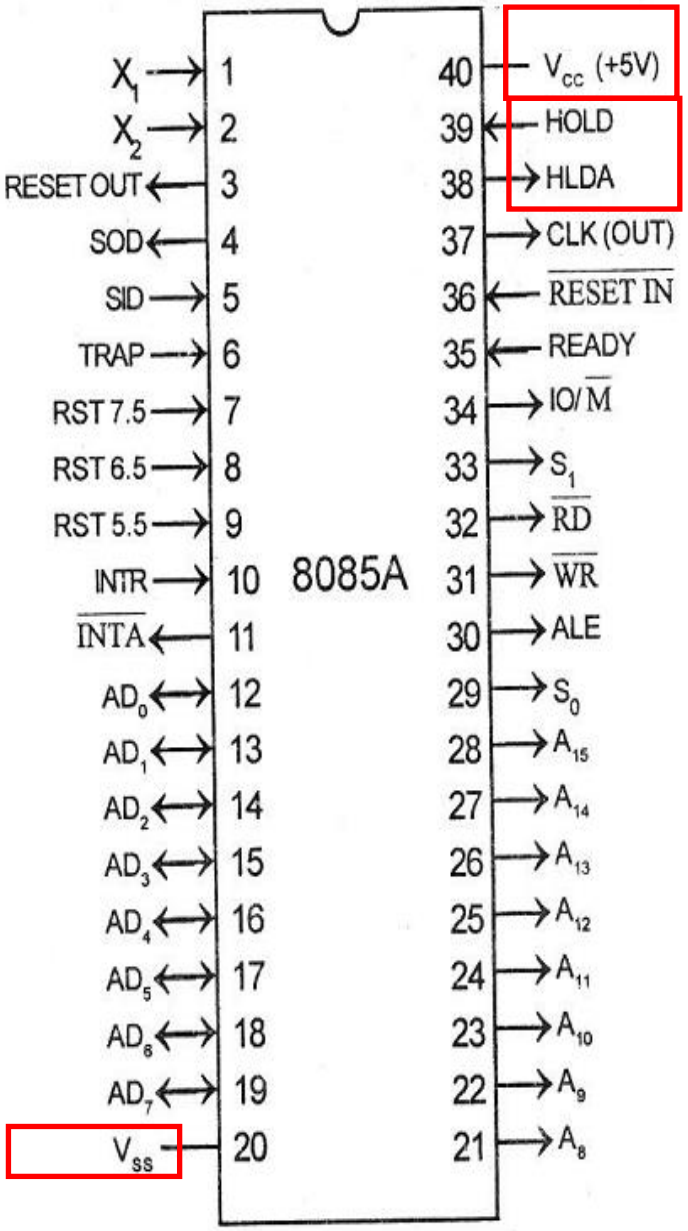
- HLDA stands for Hold Acknowledge.
- The microprocessor uses this pin to acknowledge the receipt of HOLD signal.
- When HLDA signal goes high, address bus, data bus, RD, WR, IO/M pins are ***tri-stated***.
- This means they are cut-off from external environment.

HOLD Pin 39 (Input)

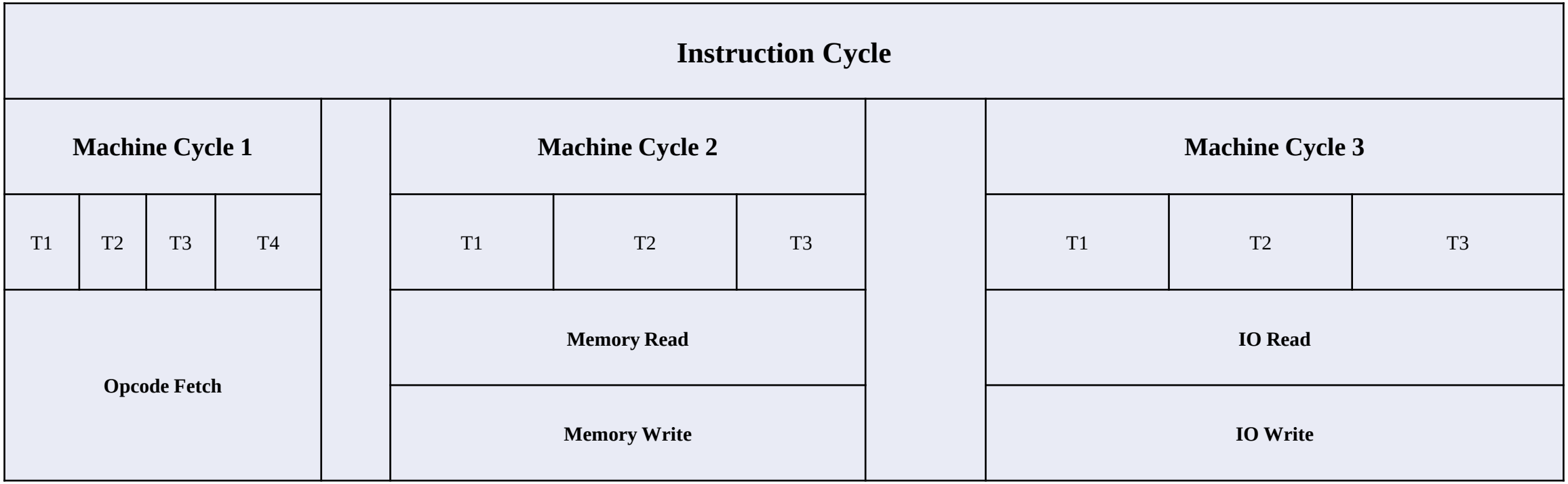
- HOLD pin is used to request the microprocessor for DMA transfer.
- A high signal on this pin is a request to microprocessor to release the hold on buses.
- This request is sent by DMA controller.
- Intel 8257 and Intel 8237 are two DMA controllers.
- When HOLD goes low, HLDA also goes low and the microprocessor takes control of the buses.

Pin 20 (Input) and Pin 40 (Input)

- +5V power supply is connected to V_{CC}.
- Ground signal is connected to V_{SS}



Timing Diagram of 8085



Instruction Cycle:

- The time required to execute an instruction is called instruction cycle.
- It is consist of number of machine cycles.
- An instruction may be consist of one machine cycle or two machine cycle or three machine cycles.
- The number of machine cycle in an instruction depend on the type of instruction going to be execute.

Machine Cycle:

- The time required to access the memory or input and output devices is called as machine cycle.
- It is consist of number of T states.
- In 8085 operations (memory read/write or IO read/write) each machine cycle consists of either 4T states or 3T states.

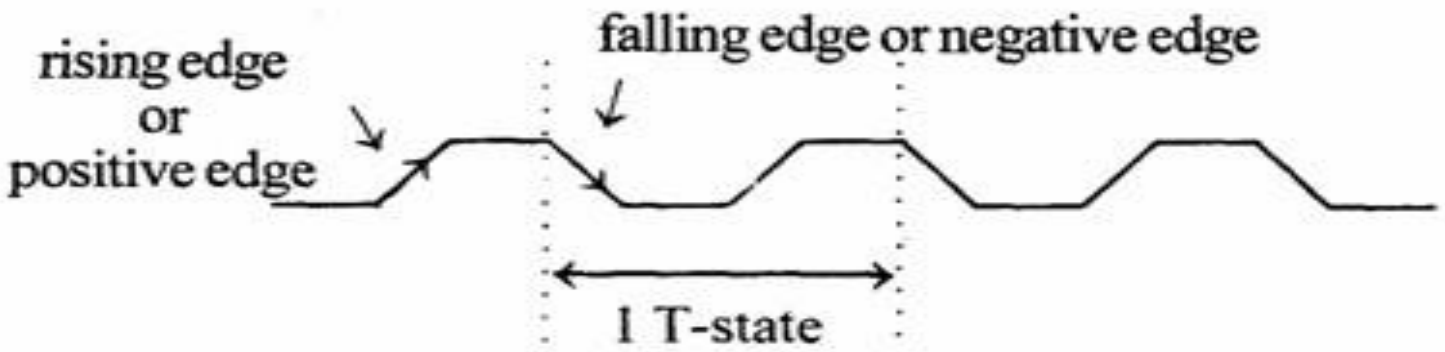
The 8085 microprocessor has 7 basic machine cycle. They are

1. Op-code Fetch cycle(4T or 6T).
2. Memory read cycle (3T)
3. Memory write cycle(3T)
4. I/O read cycle(3T)
5. I/O write cycle(3T)
6. Interrupt Acknowledge cycle(6T or 12T)
7. Bus idle cycle

T states:

- The machine cycle and instruction cycle takes multiple clock periods.
- A portion of an operation carried out in one system clock period is called as T-state

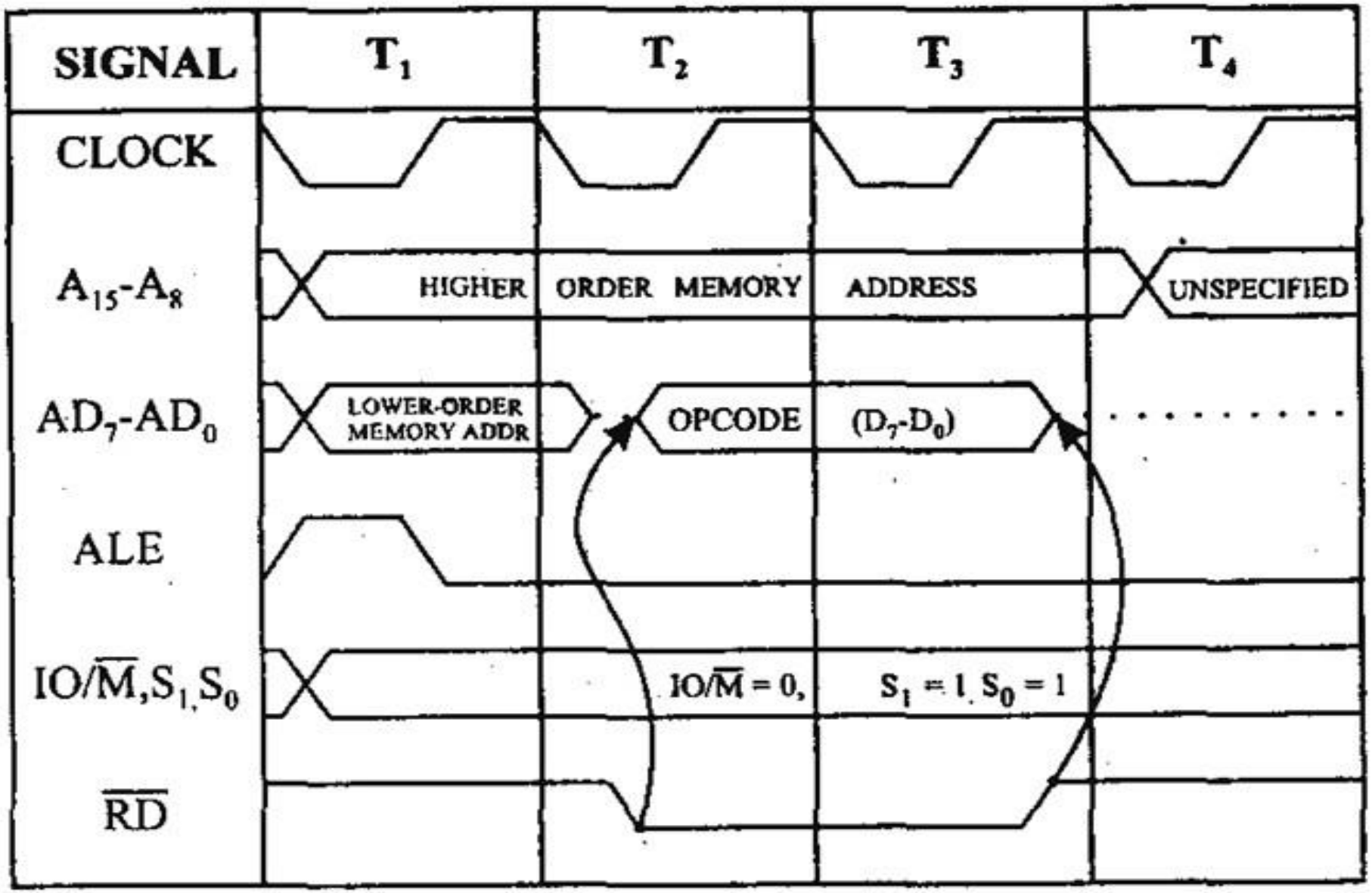
Note : *Time period, T = 1/f ; where f = Internal clock frequency*



After opcode decoding in instruction decoder unit, timing and control unit generated signals value

Machine Cycle	Status Signal			Control Signals	
	S1	***S0***	**IO/$\overline{M}$**	$\overline{WR}$	$\overline{RD}$
Memory Write	0	1	0	0	1
Memory Read	1	0	0	1	0
IO Write	0	1	1	0	1
IO Read	1	0	1	1	0
opcode Fetch	1	1	0	1	0
INTRA	1	1	1	1	1

Machine cycle 1 : OPCODE FETCH



The Opcode fetch cycle, fetches the instructions from memory and delivers it to the instruction register of the microprocessor Opcode fetch machine cycle consists of **4 T-states**.

T1 State:

- During the T1 state, the contents of the program counter are placed on the 16 bit address bus. The higher order 8 bits are transferred to address bus (A8-A15) and lower order 8 bits are transferred to multiplexed A/D (AD0-AD7) bus.
- **ALE (address latch enable)** signal goes **high**. As soon as ALE goes high, the memory latches the AD0-AD7 bus. At the middle of the T state the **ALE goes low.**

T2 State:

- During the beginning of this state, the **RD' signal goes low** to enable memory. It is during this state, the selected memory location is placed on D0-D7 of the Address/Data multiplexed bus.

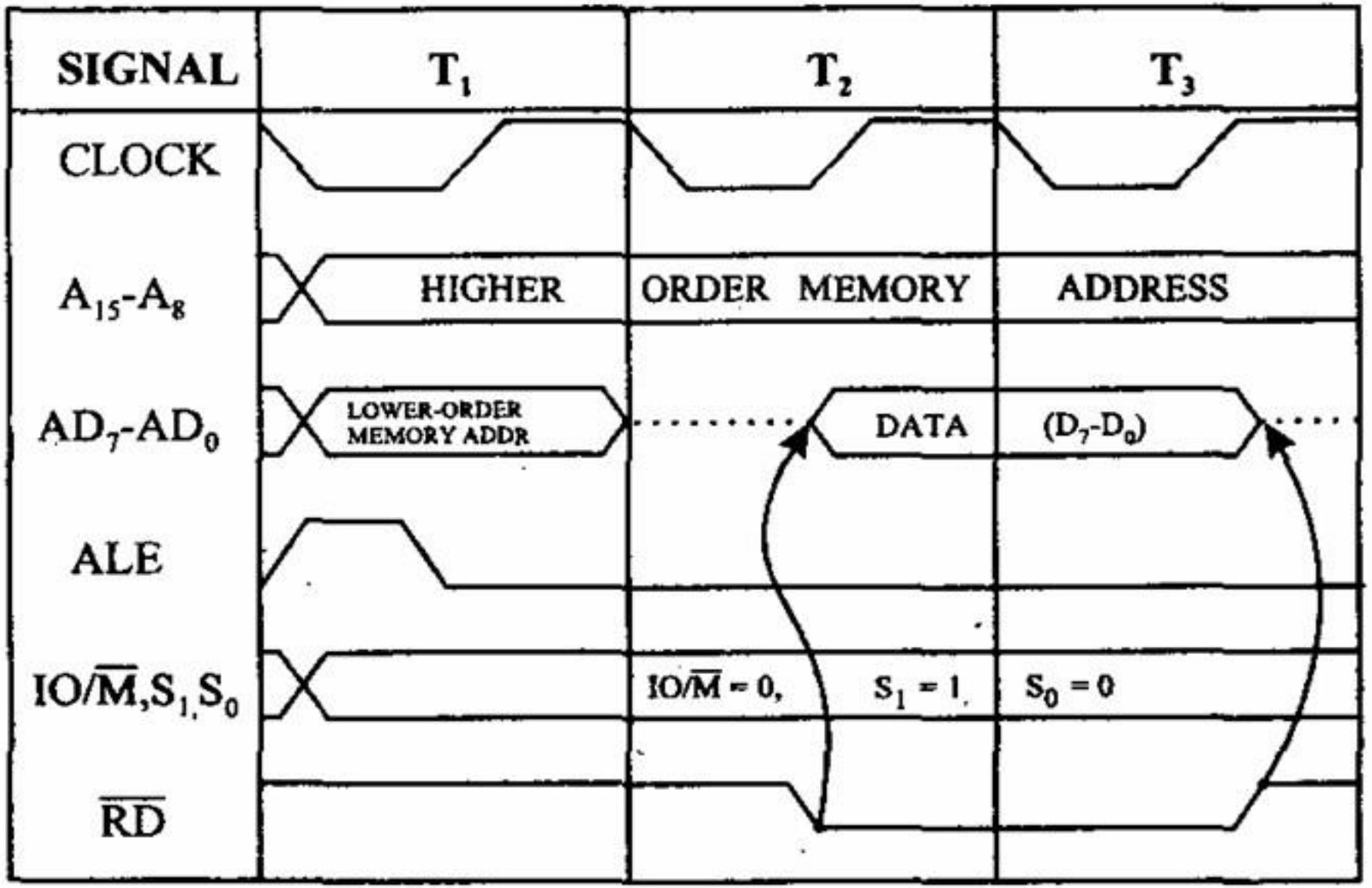
T3 State:

- In the previous state the Opcode is placed in D0-D7 of the A/D bus. In this state of the cycle, the Opcode of the A/D bus is transferred to the instruction register of the microprocessor. Now the **RD' goes high** after this action and thus disables the memory from A/D bus.

T4 State:

- In this state the Opcode which was fetched from the memory is decoded.

Machine Cycle 2: Memory read cycle (3T)



T1 state:

- The higher order address bus **(A8-A15)** and lower order address and data multiplexed (AD0-AD7) bus. **ALE goes high** so that the memory latches the (AD0-AD7) so that complete 16-bit address are available.
- The mp identifies the memory read machine cycle from the status signals **IO/M'=0, S1=1, S0=0**. This condition indicates the memory read cycle.

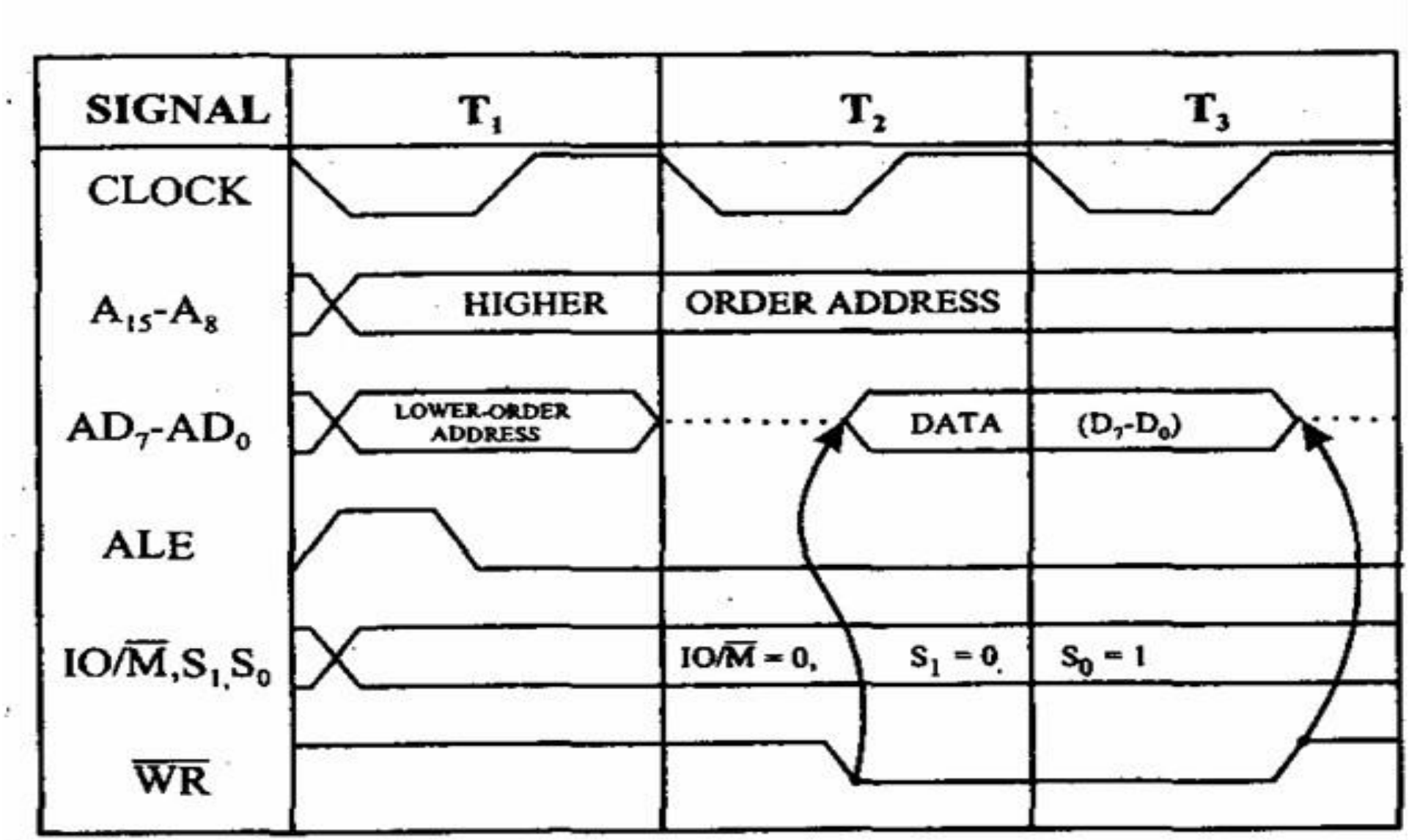
T2 state:

- Selected memory location data is placed on the (D0-D7) of the A/D multiplexed bus. RD' goes **LOW**

T3 State:

- The data which was loaded on the previous state is transferred to the microprocessor. In the middle of the T3 state RD' goes high and disables the memory read operation. The data which was obtained from the memory is then decoded.

Machine Cycle 3: Memory write cycle (3T)



- These machine cycles have 3 T-states.

T1 state:

- The higher order address bus **(A8-A15)** and lower order address and data multiplexed (AD0-AD7) bus. **ALE goes high** so that the memory latches the (AD0-AD7) so that complete 16-bit address are available.

  The mp identifies the memory read machine cycle from the status signals **IO/M'=0, S1=0, S0=1**. This condition indicates the memory write cycle.

T2 state:

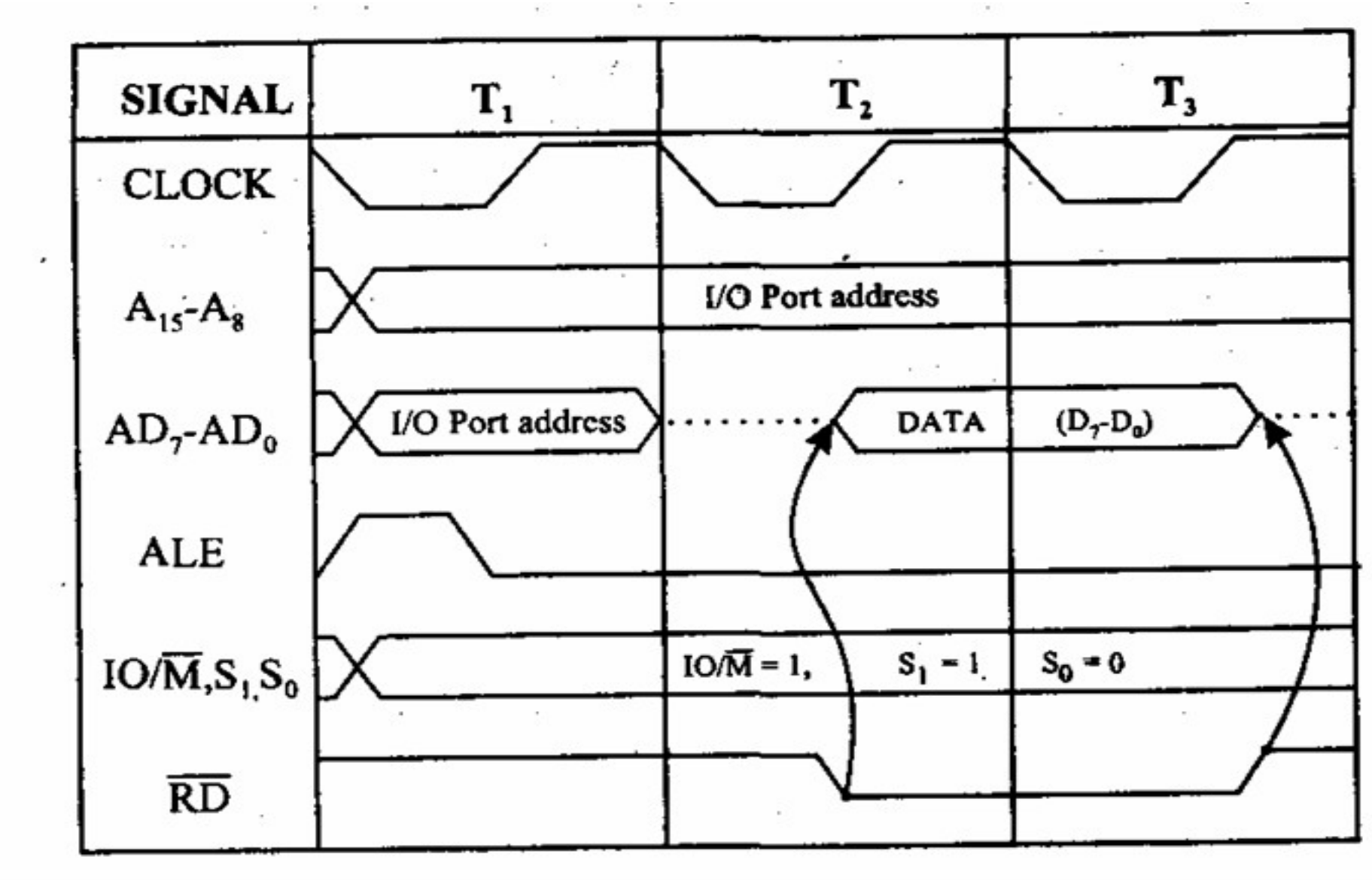
Selected memory location is placed on the (D0-D7) of the A/D multiplexed bus. WR' goes **LOW**

T3 State:

- In the middle of the T3 state WR' goes high and disables the memory write operation. The data which was obtained from the memory is then decoded.

  -

Machine Cycle 4: IO read cycle (3T)



T1 state:

- The higher order address bus **(A8-A15)** and lower order address and data multiplexed (AD0-AD7) bus. **ALE goes high** so that the memory latches the (AD0-AD7) so that complete 16-bit address are available.
- The mp identifies the IO read machine cycle from the status signals **IO/M'=1, S1=1, S0=0**. This condition indicates the IO read cycle.

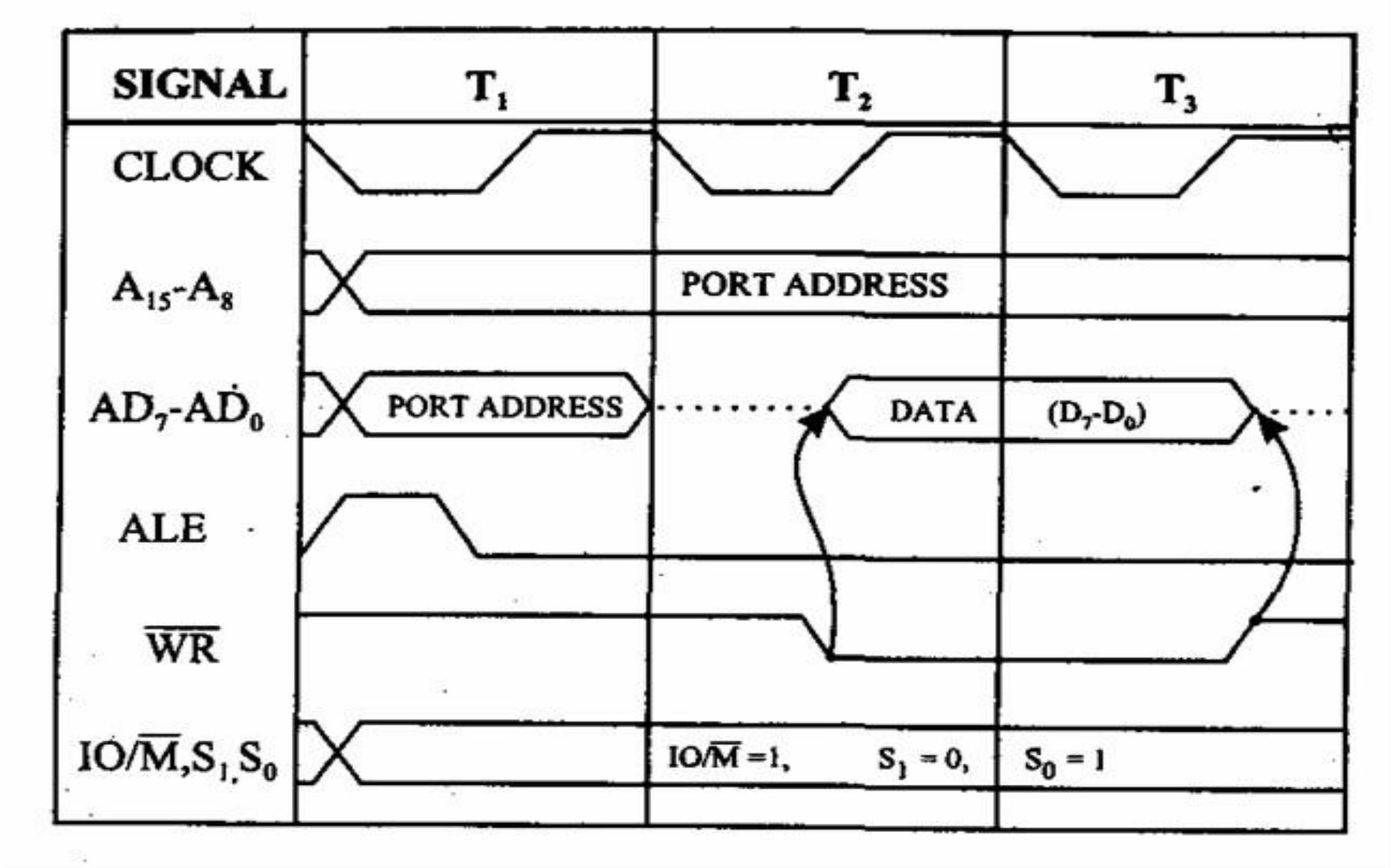
T2 state:

- Selected IO location data is placed on the (D0-D7) of the A/D multiplexed bus. RD' goes **LOW**

T3 State:

- The data which was loaded on the previous state is transferred to the microprocessor. In the middle of the T3 state RD' goes high and disables the IO read operation. The data which was obtained from the memory is then decoded.

Machine Cycle 5: IO read cycle (3T)



- These machine cycles have 3 T-states.

T1 state:

- The higher order address bus **(A8-A15)** and lower order address and data multiplexed (AD0-AD7) bus. **ALE goes high** so that the memory latches the (AD0-AD7) so that complete 16-bit address are available.
- The mp identifies the IO read machine cycle from the status signals **IO/M'=1, S1=0, S0=1**. This condition indicates the IO write cycle.

T2 state:

- Selected memory location is placed on the (D0-D7) of the A/D multiplexed bus. WR' goes **LOW**

T3 State:

- In the middle of the T3 state WR' goes high and disables the IO write operation. The data which was obtained from the memory is then decoded.

-

Example: STA instruction
Instruction: STA 526A

Address	Mnemonics	Opcode
41FF	STA 526AH	32H
4200		6AH
4201		52H

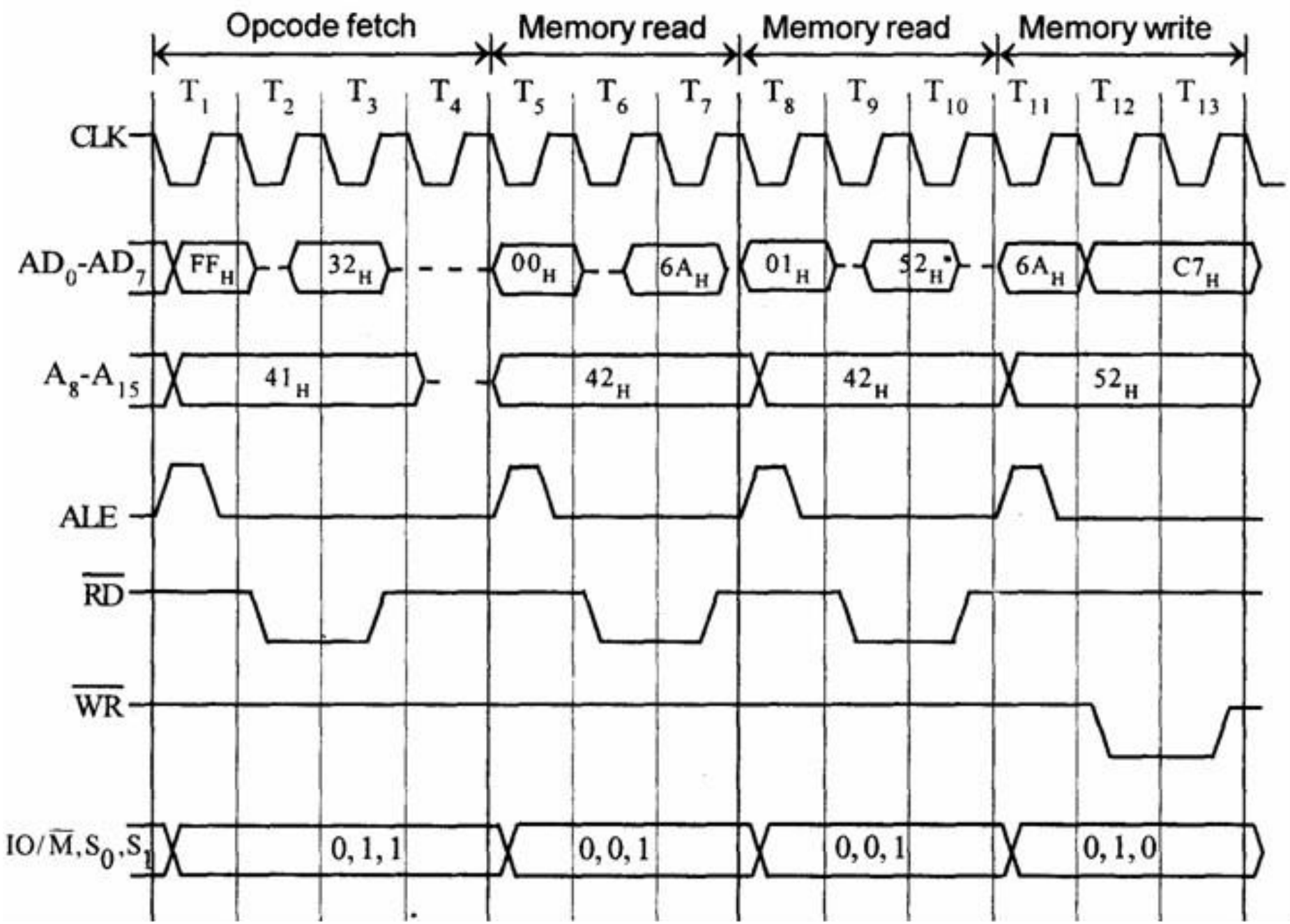
It require 4 m/c cycles 13 T states

1.Opcode fetch(4T)

2.Memory read(3T)

3.Memory read(3T)

4.Memory write(3T)


Opcode fetch
Memory read
Memory read
Memory write
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13
CLK
AD0-AD7
FFH
32H
00H
6AH
01H
52H
6AH
C7H
A8-A15
41H
42H
42H
52H
ALE
RD
WR
IO/M, S0, S1
0, 1, 1
0, 0, 1
0, 0, 1
0, 1, 0

Programing Model of 8085

Addressing modes of 8085

Definition of Addressing mode

- The method by which the address of source of data or the address of destination of result is given in the instruction is called **Addressing Modes.**
- The term addressing mode refers to the way in which the operand of the instruction is specified.

Intel 8085 uses the following addressing modes:

1. Direct Addressing Mode
2. Register Addressing Mode
3. Register Indirect Addressing Mode
4. Immediate Addressing Mode
5. Implicit Addressing Mode

1. Direct Addressing Mode

- In this mode, the address of the operand is given in the instruction itself.

LDA 2500 H	**Load the contents of memory location 2500 H in accumulator.**

- LDA is the operation.
- 2500 H is the address of source.
- Accumulator is the destination.

2. Register Addressing Mode

- In this mode, the operand is in general purpose register.

MOV A, B	**Move the contents of register B to A.**

- MOV is the operation.
- B is the source of data.
- A is the destination.

3. Register Indirect Addressing Mode

- In this mode, the address of operand is specified by a register pair.

MOV A, M	**Move data from memory location specified by H-L pair to accumulator.**

- MOV is the operation.
- M is the memory location specified by H-L register pair.
- A is the destination.

4. Immediate Addressing Mode

- In this mode, the operand is specified within the instruction itself.

MVI A, 05 H	**Move 05 H in accumulator.**

- MVI is the operation.
- 05 H is the immediate data (source).
- A is the destination.

5. Implicit Addressing Mode

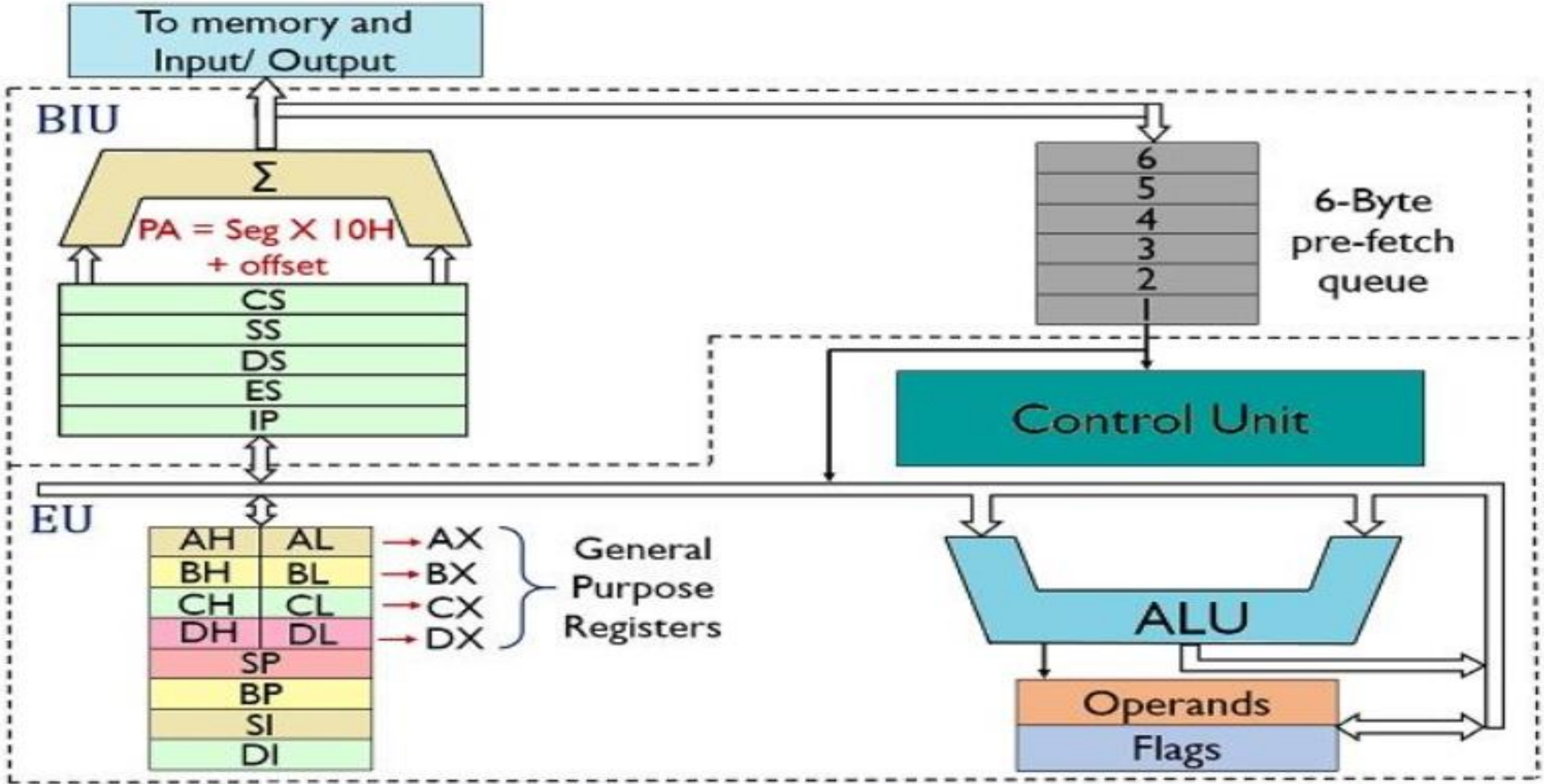
- If address of source of data as well as address of destination of result is fixed, then there is no need to give any operand along with the instruction.

CMA	Complement accumulator.

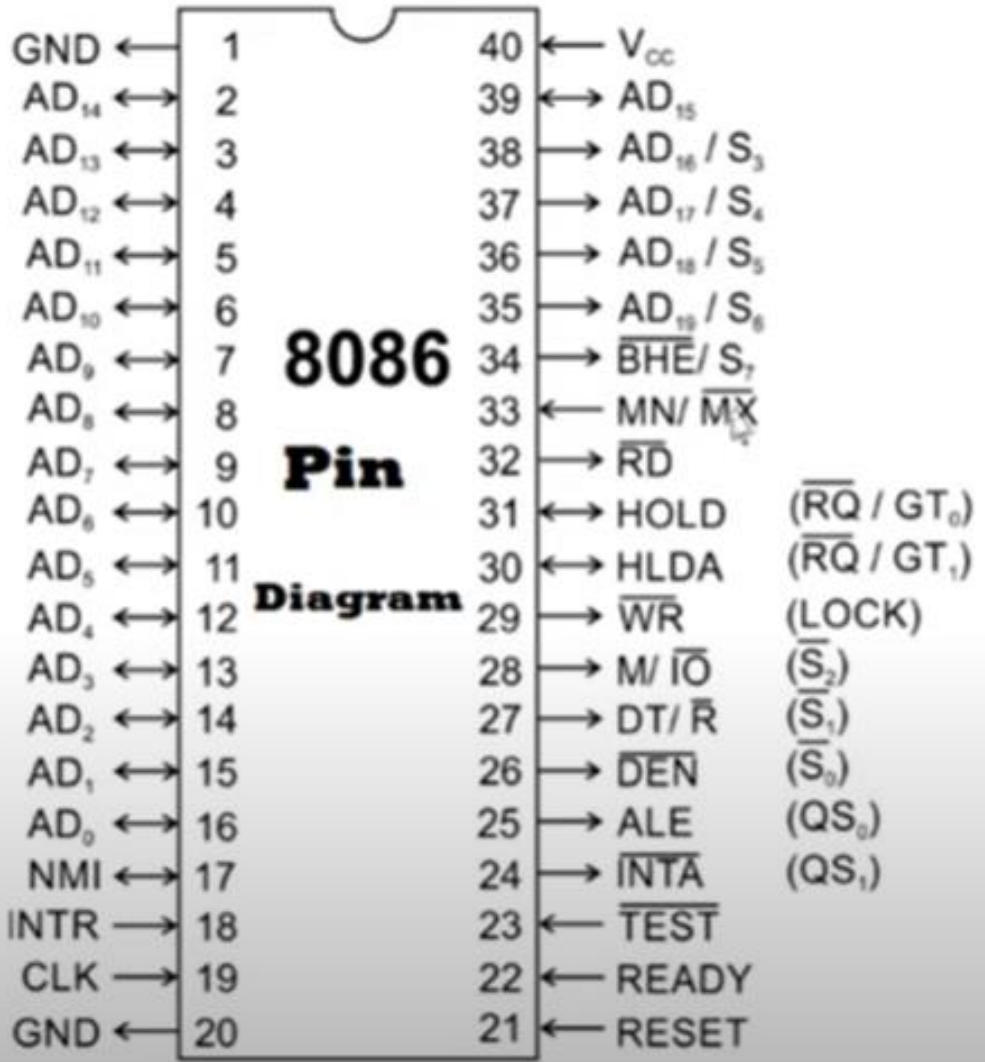
- CMA is the operation.
- A is the source.
- A is the destination.

Internal Architecture of 8086

- The architecture of 8086 microprocessor is composed of 2 major units, the BIU i.e., Bus Interface Unit and EU i.e., Execution Unit. The figure below shows the block diagram of the architectural representation of the 8086 microprocessor:

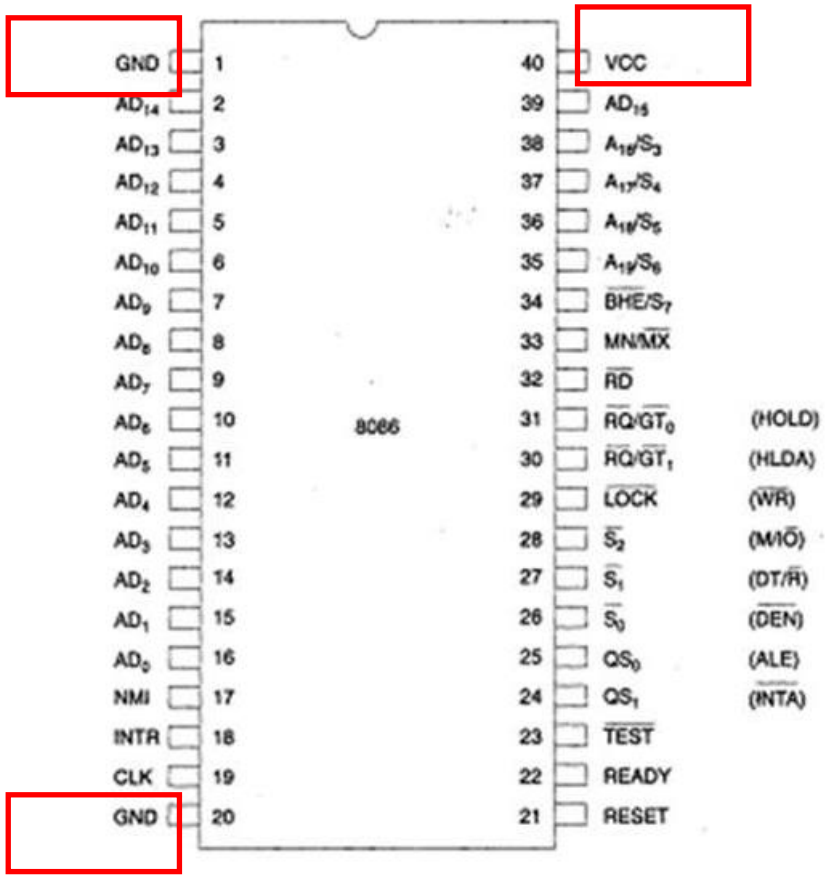


Pin Diagram of Microprocessor 8086



1. Power supply and frequency signals

- **Vcc pin 40:** It uses 5V DC supply, and
- **Pin 1 and Pin 20 :** used as ground.



2. Clock signal

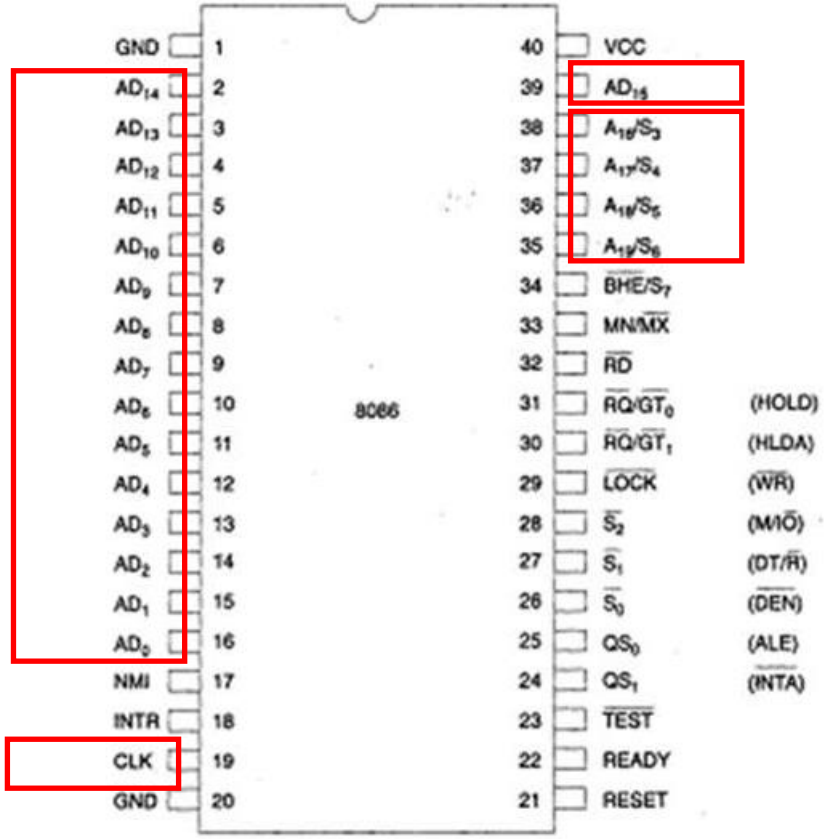
- **Pin 19:** Clock signal is provided through Pin-19. It provides timing to the processor for operations. Its frequency is different for different versions, i.e. 5MHz, 8MHz and 10MHz.

3. Address/data bus

- **Pin 2-16 & Pin 39:** AD0-AD15. These are 16 address/data bus. AD0-AD7 carries low order byte data and AD8AD15 carries higher order byte data. During the first clock cycle, it carries 16-bit address and after that it carries 16-bit data.

4. Address/status bus

- **Pin 35-38:** A16-A19/S3-S6. These are the 4 address/status buses. During the first clock cycle, it carries 4-bit address and later it carries status signals.



5. S7/BHE

- **Pin 34:** BHE stands for Bus High Enable. It is available at pin 34 and used to indicate the transfer of data using data bus D8-D15. This signal is low during the first clock cycle, thereafter it is active.

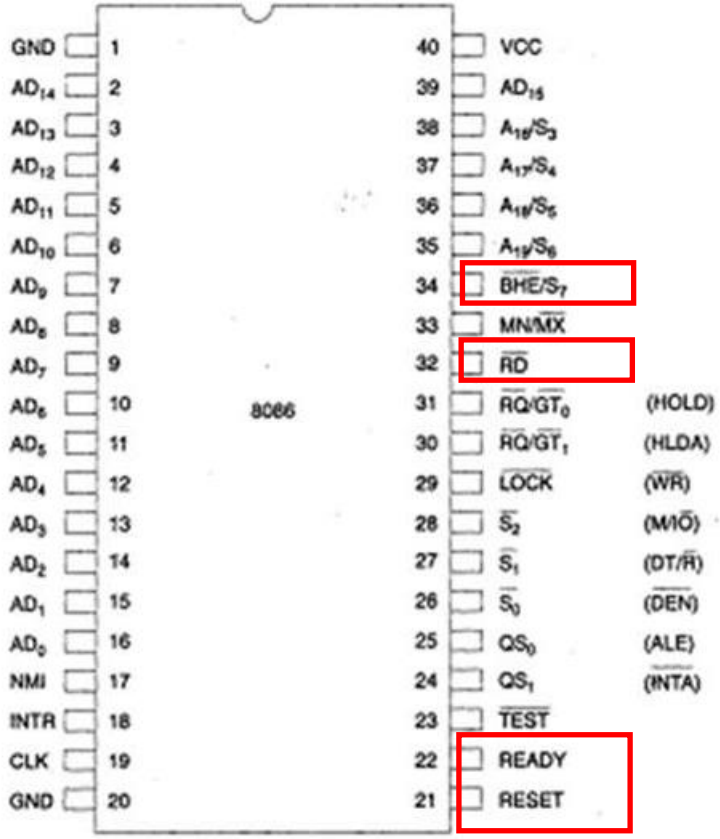
6. Read

- **Pin 32:** It is available at pin 32 and is used to read signal for Read operation.

7. Ready and Reset

- **Pin 22:** It is an acknowledgement signal from I/O devices that data is transferred. It is an active high signal. When it is high, it indicates that the device is ready to transfer data. When it is low, it indicates wait state.

- **Pin 21:** It is used to restart the execution. It causes the processor to immediately terminate its present activity. This signal is active high for the first 4 clock cycles to RESET the microprocessor.

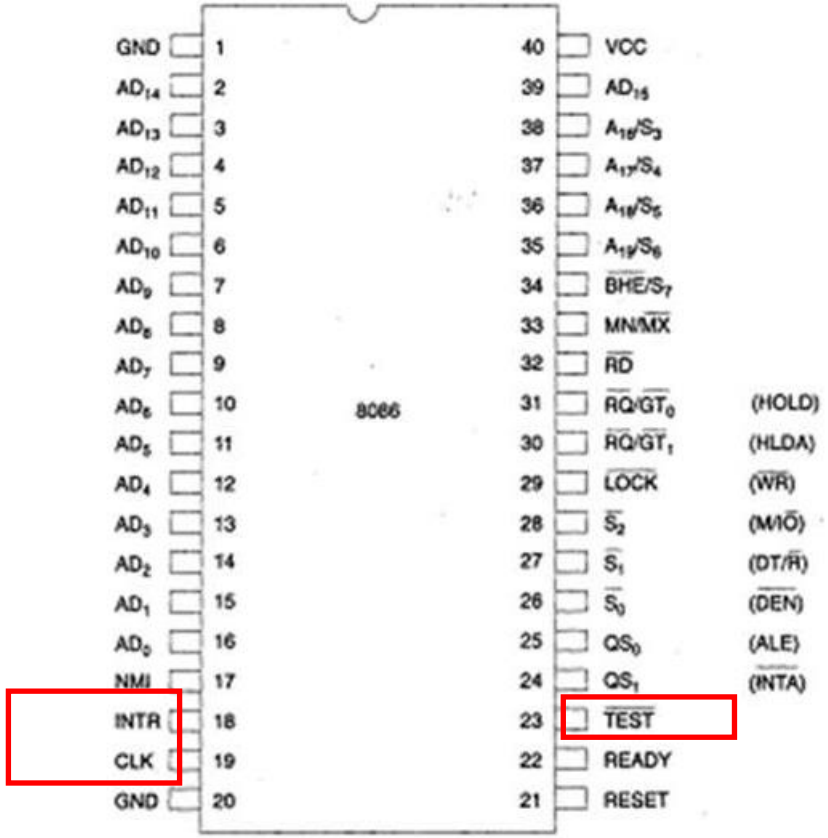


8. INTR, NMI and TEST

- **Pin 18:** It is an interrupt request signal, which is sampled during the last clock cycle of each instruction to determine if the processor considered this as an interrupt or not.

- **Pin 17:** It stands for non-maskable interrupt. It is an edge triggered input, which causes an interrupt request to the microprocessor.

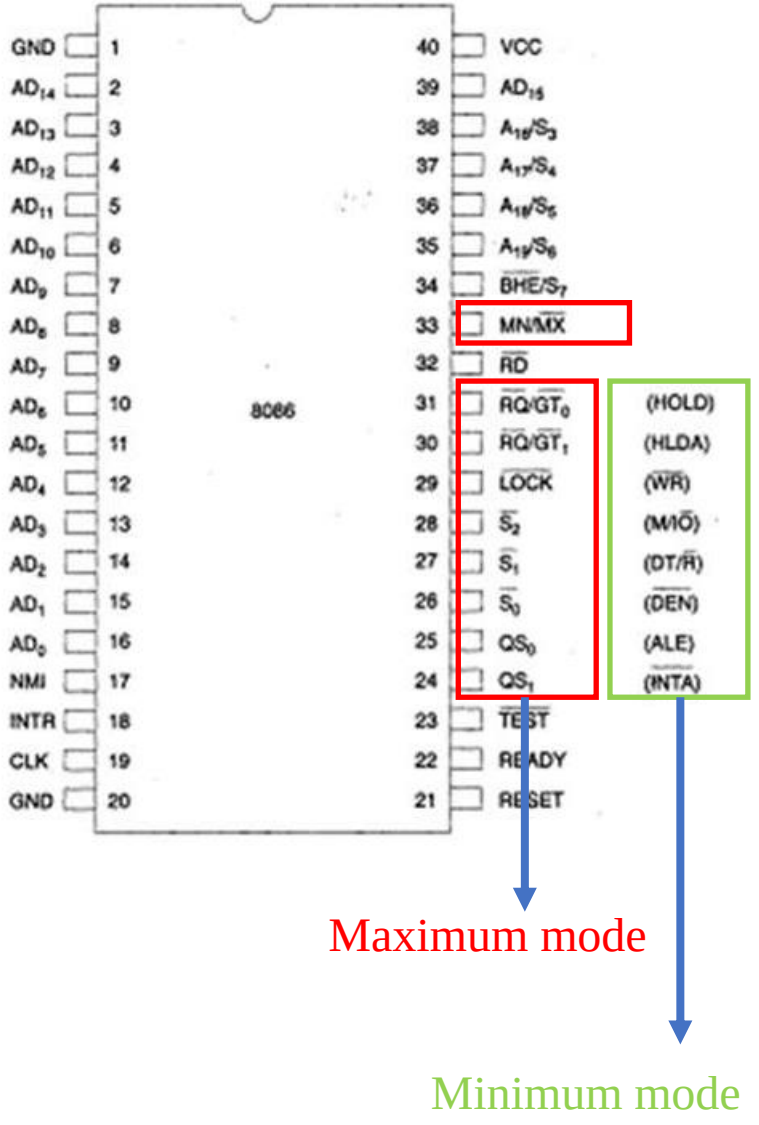
- **Pin 23:** This signal is like wait state and is available at pin 23. When this signal is high, then the processor has to wait for IDLE state, else the execution continues.



9. MN/*MX*

- **Pin 33:** It stands for Minimum/Maximum and is available at pin 33. It indicates what mode the processor is to operate in; when it is high, it works in the minimum mode and at low it work in maximum mode.

Maximum Mode Signals	Minimum mode Signals
RQ/$\overline{GT0}$ and RQ/$\overline{GT1}$	HOLD
$\overline{LOCK}$	HLDA
S0-S1	$\overline{M}$/IO
QS0-QS1	DT/$\overline{R}$
	$\overline{DEN}$
	ALE
	$\overline{INTA}$

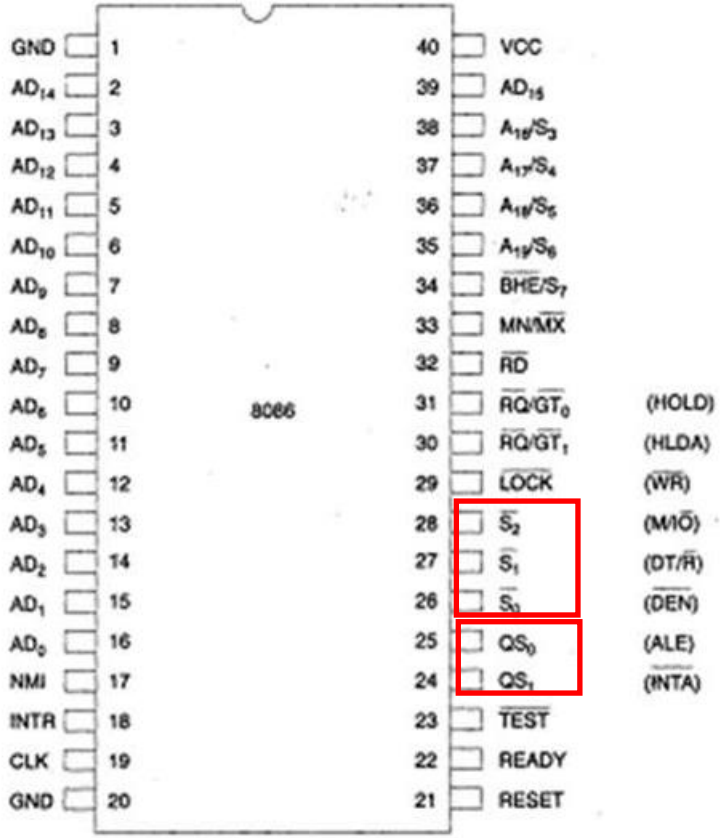


10. Maximum mode

a) QS_1 and QS_0

- **Pin 24 and 25:** These are queue status signals and provide the status of instruction queue. Their conditions are shown in the following table −

QS_0	QS_1	Status
0	0	No operation
0	1	First byte of opcode from the queue
1	0	Empty the queue
1	1	Subsequent byte from the queue



b) S_0, S_1, S_2

- **Pin 26-28**: These are the status signals that provide the status of operation, which is used by the Bus Controller 8288 to generate memory & I/O control signals. Following is the table showing their status −

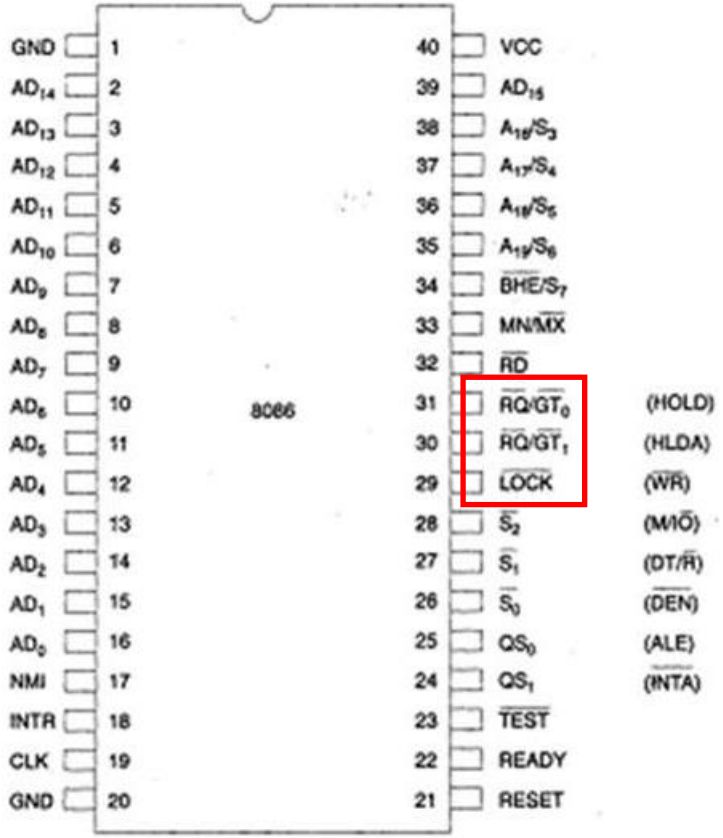
S_2	S_1	S_0	Status
0	0	0	Interrupt acknowledgement
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

10. Maximum mode

c) LOCK When this signal is active, it indicates to the other processors not to ask the CPU to leave the system bus. It is activated using the LOCK prefix on any instruction and is available at pin 29.

d) RQ/GT_1 and RQ/GT_0

These are the Request/Grant signals used by the other processors requesting the CPU to release the system bus. When the signal is received by CPU, then it sends acknowledgment. RQ/GT_0 has a higher priority than RQ/GT_1.



11. Minimum mode

a) INTA

It is an interrupt acknowledgement signal and is available at pin 24. When the microprocessor receives this signal, it acknowledges the interrupt.

b) ALE

It stands for address enable latch and is available at pin 25. A positive pulse is generated each time the processor begins any operation. This signal indicates the availability of a valid address on the address/data lines.

c) DEN

It stands for Data Enable and is available at pin 26. It is used to enable Transreceiver 8286. The transreceiver is a device used to separate data from the address/data bus.

d) DT/R

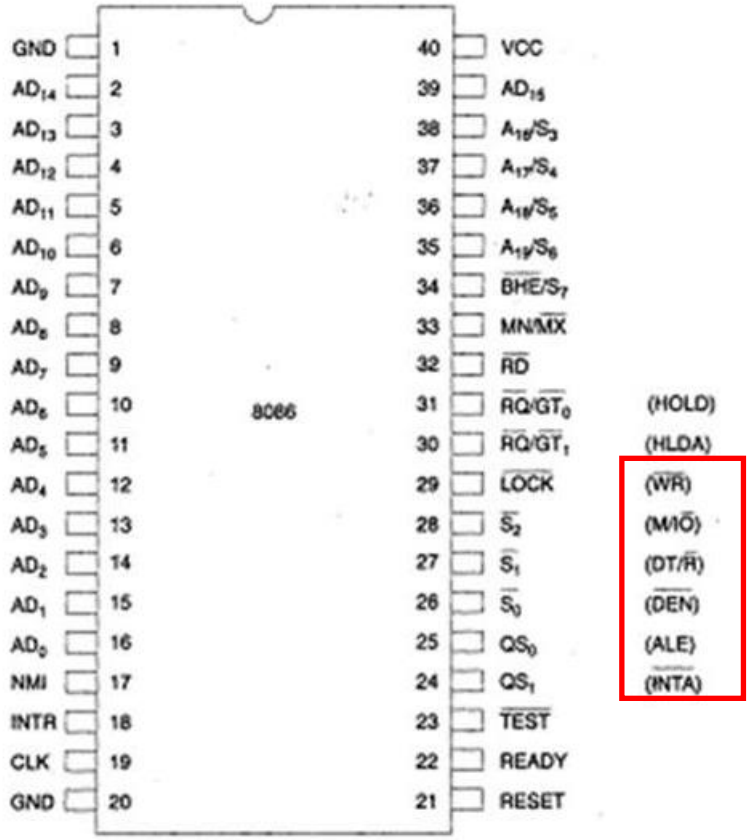
It stands for Data Transmit/Receive signal and is available at pin 27. It decides the direction of data flow through the transreceiver. When it is high, data is transmitted out and vice-a-versa.

e) M/IO

This signal is used to distinguish between memory and I/O operations. When it is high, it indicates I/O operation and when it is low indicates the memory operation. It is available at pin 28.

f) WR

It stands for write signal and is available at pin 29. It is used to write the data into the memory or the output device depending on the status of M/IO signal.



g) HLDA It stands for Hold Acknowledgement signal and is available at pin 30. This signal acknowledges the HOLD signal.

h) HOLD This signal indicates to the processor that external devices are requesting to access the address/data buses. It is available at pin 31.