Ayuub Mohamud

ayuub.mohamud@outlook.com
linkedin.com/in/ayuub-mohamud-405947331 github.com/AyuubMohamud

Education

Imperial College London **Oct 2023 – Jun 2027**

MEng Electronic and Information Engineering

- Currently in 3rd Year
- **Modules:** Digital Electronics and Computer Architecture **(79.78%)**, Instruction Architectures and Compilers **(78.74%)**

Harris Clapham Sixth Form **Sep 2021 - Jun 2023**

A Levels

- **Grades: A*AAA** in Mathematics, Further Mathematics, Physics and Computer Science.

Work Experience

Arm Holdings plc **Jun 2025 - Sep 2025**

Hardware Engineering Intern *Little A-core Memory System design team, Cambridge*

- **Designed** and **delivered** a testbench infrastructure to **correlate prefetcher's with software models**.
- **Collaborated** with modelling and design teams to understand prefetcher architecture, debug issues, and **shape training data requirements**.
- **Raised and addressed** several issues, **collaborating** across multiple teams to resolve and improve prefetcher correlation.

Imperial College London **Oct 2024 - Mar 2025**

Undergraduate Teaching Assistant *Department of Electrical and Electronic Engineering, London*

- Provided live feedback **and demonstrations** during programming sessions, helping students grasp modern C++ concepts such as memory management and object-oriented design.
- Supported first-year students new to programming, strengthening skills in **abstraction**, **decomposition**, and problem-solving.

Projects

Out of Order RISC-V Implementation | SystemVerilog, C++, Hardware **May 2024 - Apr 2025, Oct 2025**

- Built a 2-way **configurable, superscalar, speculative, out-of-order** RISC-V CPU.
- Implemented bimodal **branch prediction**, bit-manipulation instructions, **writeback non-blocking cache**.
- Designed and tested a **Memory Protection Unit** for address protection using physical addresses.
- Implemented a **dedicated test suite** in **make, bash and C++** for finding microarchitectural bugs.
- Runs on a low-speed grade FPGA at **82.5MHZ** whilst taking **around 9K LUTs** and **4/240** of available DSPs.

Custom mathematical accelerator | SystemVerilog, C++, Software/Hardware **May 2025 - Jun 2025**

- Designed a **parallel fixed-point accelerator** with **multi-threaded cores, pipelined arithmetic**, and **real-time streaming output** for fractal rendering.
- Implemented a **custom instruction set, task scheduling**, and **arbitration logic** to coordinate eight compute cores for **maximum throughput**.
- Achieved **2x** the peak throughput of a single threaded program using **-O3** on a modern CPU, while consuming **30000** LUTs, utilising **Verilator** for **functional verification** before **FPGA deployment**.

TileLink IPs | SystemVerilog, Hardware **Nov 2023 - Oct 2024**

- Built a library of **configurable reusable IPs**, for building **embedded SOCs** on FPGAs.
- Block RAM controllers allow for burst accesses **maximising** bus bandwidth, including **atomics**.
- **Arbiters, decoders** and N-M connections for **flexible interconnects** across multiple IPs.
- **PLIC** and **CLINT** controllers for **interrupt delivery and timer management**, alongside a **flexible UART controller** for **external** communication.

EEERover: 1st Year Engineering Project | C++, Software/Hardware **May 2024 - Jun 2024**

- **Collaborated** in a team of 6 to develop a rover capable of object detection via multiple sensors.
- **Designed** an ultrasound demodulation circuit to decode UART signals.
- **Managed** team finances and component sourcing; project awarded a First Class grade.

Skills

Hardware Description Languages: SystemVerilog, Verilog
EDA Tools: Synopsys VCS, Synopsys Verdi, Vivado
Programming Languages: C, C++, Python, ARMv8 Assembly, RISC-V Assembly
Protocols: TileLink, AXI, APB

Interests

Societies: Department of Computing Society, Robotics Society, Electrical Engineering Society
Interests: Languages, History, Mathematics