Ayuub Mohamud

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Education

Imperial College London **Oct 2023 – Jun 2027**

MEng Electronic and Information Engineering

- Currently in 2nd Year
- **Modules:** Digital Electronics and Computer Architecture **(79.8%)**, Programming for Engineers **(72.15%)**, Engineering Project **(70.62%)**

Harris Clapham Sixth Form **Sep 2021 - Jun 2023**

A Levels *London, UK*

- **Grades: A*AAA** in Mathematics, Further Mathematics, Physics and Computer Science.

Projects

Out of Order RISC-V Implementation | Verilog **May 2024**

- Built a 2-way **configurable, superscalar, speculative, out-of-order** RISC-V CPU.
- Implemented bimodal **branch prediction**, machine and user mode.
- Executes **over 140 instructions**, including a **custom DSP extension**.
- **Re-orders** cache requests to allow for more **optimal** cache utilisation.
- Implemented a **dedicated test suite** in **make** and **bash** for finding microarchitectural bugs.
- Utilised **Verilator** and **GTKWave** extensively to simulate and verify design, alongside **on FPGA testing**.
- Runs on a low-speed grade FPGA at **82.5MHZ** whilst taking **~10K LUTs**, **10/240** of the available DSPs and **4/135** available Block RAMs.

1st Year Engineering Project **May-Jun 2024**

- Worked in a **team of 6** to develop a rover that identifies objects in an arena using various sensors.
- Delivered an ultrasound demodulation circuit, selecting necessary parts to **decode UART signals**.
- In charge of managing the team's finances, ordering parts and discussing them with team members.
- Collaborated with team members to help **develop** the rover firmware and radio demodulation circuit.
- Achieved **70.62%** for this project (First Class).

TileLink-based SOC infrastructure | Verilog **Nov 2023**

- Built a library of **configurable reusable modules**, for building **embedded SOCs** for FPGAs.
- GPIO controller allows for I/O pins to be **configured** as inputs or outputs at runtime.
- Block RAM controllers allow for burst accesses **maximising** bus bandwidth, including **atomics**.
- Contains **crossbars, GPIO controller, DMA controller and more** allowing for extensible SOCs.

ARMv8-A C Compiler | Verilog **Nov 2023**

- Built a compiler for a **subset of C in C++** targeting the **ARMv8-A** architecture.
- Hand-wrote the lexer and **recursive descent C parser**.
- **Optimises** multiplications and divisions into bit shifts, by checking if the multiplier/divisor is a power of two, and **reordering code** to achieve this.
- Performs **semantic analysis** on given C code.
- Generates **working assembly** that can interact with standard C library.

Work Experience

Undergraduate Teaching Assistant **Oct 2024 -**

Imperial College London (Department of Electrical and Electronic Engineering)

- Helping students learn modern C++ through live feedback during programming sessions.
- Supporting students new to programming develop critical skills like abstraction, decomposition and more.

Skills and Awards

Technical Skills

Programming Languages: C, C++, Python, ARMv8 Assembly, RISC-V Assembly
Hardware Description Languages: SystemVerilog, Verilog
Toolchain: GCC, Git, Verilator, GTKWave, Vivado, Make, Bash, Linux, Clang