Kevin Lau

Cambridge +44 7311 889669 kevinlauofficial01@gmail.com
linkedin.com/in/kevinlau01 github.com/booth-algo

Education

Imperial College London **Oct 2022 – Jun 2026**

MEng Electronic and Information Engineering (Computer Engineering)

- Predicted 1st class honours, starting penultimate year
- Modules of interest: Instruction Set Architecture and Compilers, Advanced Computer Architecture, Information Processing, Deep Learning, Embedded Systems

Work Experience

3D Gaussian Splatting Quantisation and Acceleration Hardware Research **Jul 2024 – ongoing**

DeepWok Lab (Imperial x Cambridge Research Team)

- Designing quantised hardware for 3D Gaussian Splatting in **SystemVerilog** with custom **cocotb** testbenches
- Implemented quantisation-aware training for 3DGS using **PyTorch**, achieving similar PSNR benchmarks to the official **CUDA** implementation
- Applied in-house compiler MASE's custom quantisers to evaluate the best quantisation scheme for hardware design

University Course FPGA Module Design **Jul – Sept 2024**

Imperial College London (Department of Electrical and Electronic Engineering)

- Redesigned the 2nd year Information Processing module teaching content and lab practicals from scratch
- Introduced concepts of hardware-software codesign and embedded development with Verilog, C++ and Python
- Emphasized on practical skills development with the **FPGA Xilinx** toolchain and edge-computing applications

Undergraduate Teaching Assistant **Oct 2023 – Mar 2024**

Imperial College London (Department of Electrical and Electronic Engineering)

- Worked with the department to provide learning support to 1st year students in Programming for Engineers module
- Guided students on learning fundamental C++ concepts and developing object-oriented programming skills

Full-Stack Web Developer **Jul – Sept 2023**

DiTa Limousine Limited

- Developed a responsive and interactive website using ReactJS and Framer Motion for the company website, which enhanced user engagement and contributed to a 50% increase in new limousine service bookings
- Hosted the website on a self-managed Ubuntu Virtual Private Server, gaining experience with the Linux shell and server management using NGINX

Projects

Graphics Processing Unit (TauriGPU) | *SystemVerilog, Python, GLSL* **Jul 2024 – ongoing**

- Developing an open-source programmable GPU compatible with **OpenGL ES2** and **Xilinx FPGAs**
- In progress of building an LLVM backend for TauriGPU's ISA to enable GLSL compilation

Autonomous Balance Bot with Incident Management Platform | *Python, ROS 2* **May – June 2024**

- Led development of the autonomous navigation and physical incident detection system using SLAM and ROS 2
- Developed a Frontier-based exploration algorithm to enable autonomous exploration capabilities in completely unknown dynamic environments
- Physically implemented system on a Raspberry Pi 4 with a 2D LiDAR sensor and a camera

C90 to RISC-V Compiler | *C++, RISC-V Assembly* **Dec – Mar 2024**

- Developed a compiler with advanced features, e.g. N-dimensional array support and efficient memory management
- **Placed 1st out of 48 teams**, achieving 90% pass rate in seen and unseen test cases

FPGA Computer Vision Acceleration for ESP32 WiFi Car Racing System | *Xilinx, C++* **Feb – Mar 2024**

- Built a commercializable hardware racing game with AWS cloud backend and implemented powerups using OpenCV
- Developed hardware IPs for local OpenCV acceleration on the **PYNQ-Z1 FPGA** using the Xilinx toolchain

Software-Hardware Low Latency Algorithmic Trading System with FPGA | *Xilinx, Python* **Feb 2024**

- Utilised FPGA to accelerate moving average indicators to identify market opening convergence opportunities using the Xilinx toolchain
- **Top 5 finalist** at IC Hack 24's Optiver trading challenge out of 20+ teams, invited to present trading strategy to Optiver representatives

RISC-V CPU | *SystemVerilog, C++, RISC-V Assembly* **Nov – Dec 2023**

- Developed a single-cycle RISC-V 32I processor that runs all base instructions using SystemVerilog
- Implemented pipelining and direct-mapped cache to improve processing and memory access speed
- **Placed 1st out of 24 teams** in both quality of verification and codebase documentation

Skills and Awards

Technical Skills

Programming Languages: C, C++, Python, JavaScript, RISC-V Assembly
Hardware Description Languages: SystemVerilog, Verilog, VHDL
Toolchain: CUDA, OpenGL, PyTorch, Git, Verilator, cocotb, ROS 2, NumPy, OpenCV, ReactJS, NGINX, Conda
FPGA toolchain: Vivado, Vitis, Quartus Prime
Languages: English (native), Cantonese (native), Mandarin Chinese (fluent)

Awards

Hong Kong Scholarship for Excellence Scheme: Awarded title of **Hong Kong Scholar** (since 2022)
Diocesan Boys' School: Top International Baccalaureate scorer (44/45 marks), Subject prize scholarship (2022)