Ayush Maity

Kolkata | maityayush39@gmail.com | 8335048048 | linkedin.com/in/Ayush Maity | |github.com/Ayxux

Summary

Research-oriented 6th semester student with a keen interest in **computer engineering** and its applications in **low-level systems** with experience in research of **IC Fabrication** and in working with **VLSI, CPU design, and assembly applications** with commitment in advancing my knowledge of **computer engineering** to pursue it further and provide meaningful contributions to the field

Education

Narayana School Kolkata, Secondary School (10th) 2020

- **Percentage:** 90.4%

Narayana School Kolkata, Senior Secondary School (12th) 2022

- **Percentage:** 87.8%

KIIT University, B.Tech in Computer Science and Engineering Sept 2022 – June 2026

- **CGPA**: 8.29/10.0
- **Coursework:** Computer Organisation and Architecture, High Performance Computing, Operating Systems, Digital System Design

Experience

Defense Research Development Organization (DRDO) May 2024 – June 2024
Research Intern at Solid State Physics Lab (SSPL)

- Gained hands-on experience in advanced photolithography techniques from crystal growth to metallisation
- Operated in ISO-certified cleanroom environments with strict contamination control
- Conducted experiments on spin-coating, exposure, and resist-thickness measurement, emphasizing precision and sub-micron patterning
- Worked with wet and dry etching methods, including ICPRIE, for high-resolution feature creation on silicon wafers

Publications

FPGA Implementation of Serial Peripheral Interface Transceiver Module April 2024

Ayush Maity, *Pravin Kumar Samanta*, Bishnu Prasad De, S. K. Dash, W. Bhowmik, A. Bakshie

10.1109/ICCECE58645.2024.10497241

Automated Improved Human Activity Recognition using Ensemble Modeling June 2024

S. Das, *A. Maity*, R. Jana, R. Biswas, A. Biswas, P. K. Samanta

10.1109/RAEEUCCI61380.2024.10547875

Projects

FPGA-Based High-Speed Communication System

- Developed a high-speed communication system and focused on optimizing resource utilization, achieving low latency, and validating performance through simulation
- Provided a scalable and power-efficient solution for SPI communication, with applications in industrial automation and sensor interfaces
- Technologies Used: VHDL, Xilinx Vivado, FPGA

Intelligent Sensor-Based Activity Monitoring Framework

- Engineered a robust activity monitoring framework using smartphone sensors and advanced machine learning techniques
- Demonstrated the potential for real-time HAR systems in healthcare, sports analytics, and security

- Technologies Used: Python, Scikit-learn, Pandas, NumPy

RISC-V Processor Pipeline ongoing

- Designed and implemented a 5-stage pipeline simulator for RISC-V processors in C, supporting integer instructions.
- Incorporated advanced features like operand forwarding, stall, and flush mechanisms to handle pipeline hazards efficiently.
- Technologies Used: C, Debugging Tools, Git, RISC-V ISA.
- Current Status: Ongoing; working on refining branch prediction logic and expanding instruction set support.

Technologies

Languages: C (*Proficient*), Python (*Proficient*), C++ (*Learning*), Verilog (*Familiar*), Java (*Familiar*), Assembly (RISC-V/MIPS) (*Proficient*), Bash/Shell Scripting (*Proficient*)

Technologies: Unix, Git, Jupyter Notebook, Matlab, FAISS, Flask, Streamlit, Render, VS Code

Achievements

- **Paper Presentation - IEEE ICCECE 2024**
  Delivered a presentation at the prestigious **IEEE International Conference on Computing, Electronics and Electrical Engineering (ICCECE)**, showcasing original research in front of distinguished professors, researchers, and industry professionals
  Gained invaluable experience presenting at an international conference and engaging in insightful discussions, receiving positive feedback for technical depth and clarity

- **1st Place - Hackocalypse, MLSA KIIT**
  Won the hackathon organized by MLSA KIIT, where the problem statement focused on **Retrieval-Augmented Generation (RAG) using Groq LLM**
  Implemented a scalable solution featuring **Flask-based RESTful endpoints**, middleware integration, and efficient indexing with **FAISS** to power real-time query resolution.
  Collaborated with a diverse team to deliver a production-ready prototype that demonstrated high technical precision and creativity

- **1st Prize - IIT Guwahati Film Festival**
  Awarded for the short film *Andh Bindu* as the **Actor**, **Writer**, **Co-director**, and a key contributor in **Lighting**

- **India Selection - IKSFF**
  Represented India at the International Kolkata Short Film Festival with the short film *Chintu* as the **Writer** and **Co-director**

- **Bassist in College Band**
  Performed live as the bassist in the college band during KIIT Fest 7.0, contributing to the musical success of the event

References

Mr. Jyotiprakash Mishra - *KIIT University*
jyotiprakash.mishrafcs@kiit.ac.in

Mr. Subhendu S. Sarker - *DRDO (SSPL)*
subhendu.sspl@gov.in

Dr. Mahadeva Bhatt - *DRDO (SSPL)*
mahadeva.bhat.sspl@gov.in