UNIVERSITY OF ENGINEERING AND TECHNOLOGY LAHORE, PAKISTAN
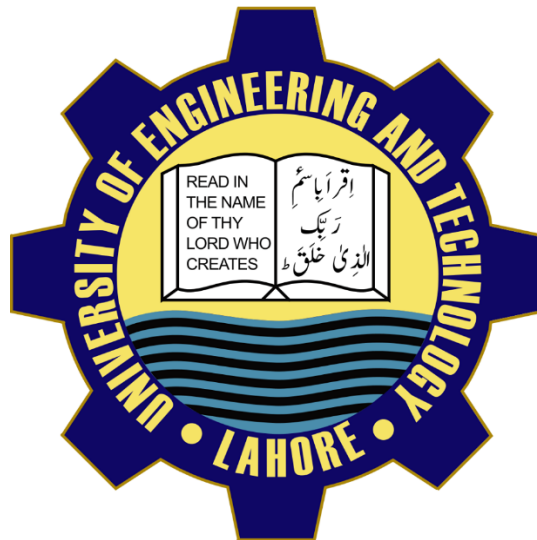

AMBA AHB-Lite Protocol Verification Plan

Submitted By:
Muhammad Ayyaz Tariq
2021-PhD-EE-01

Department of Electrical Engineering
University of Engineering and Technology, Lahore

Introduction to the Device-Under-Test (DUT)

AMBA AHB Lite is an interface between master and slaves. It has write data bus configurations of 64 to 1024 bits in powers of 2. The AHB block diagram is as follows:
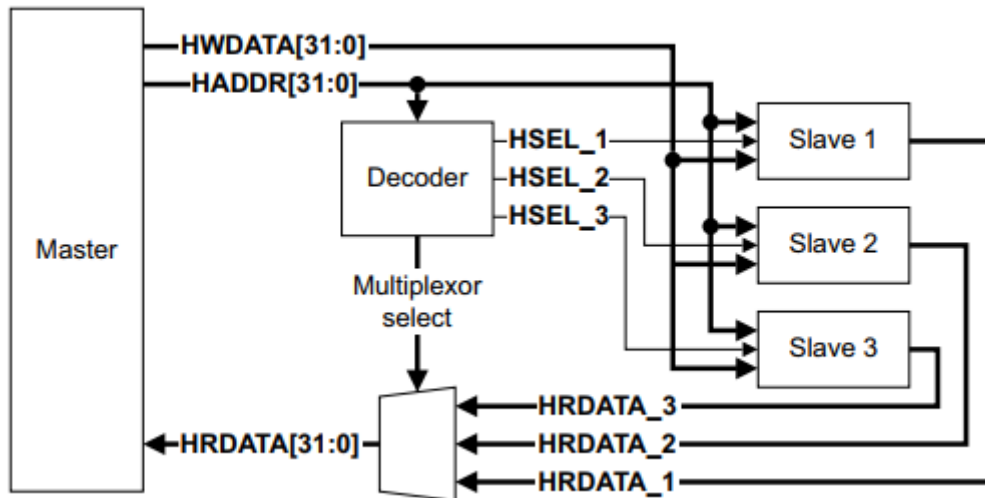

Figure 1: AHB block diagram

In the above figure, one master and three slaves are present. Moreover, decoder selects the slave from the information of the address from Master. Mux gives way back to that particular slave to Master. Master provides address and control information. Slave responds to the transfers initiated by the Master. Every transfer has an address and data cycle each.
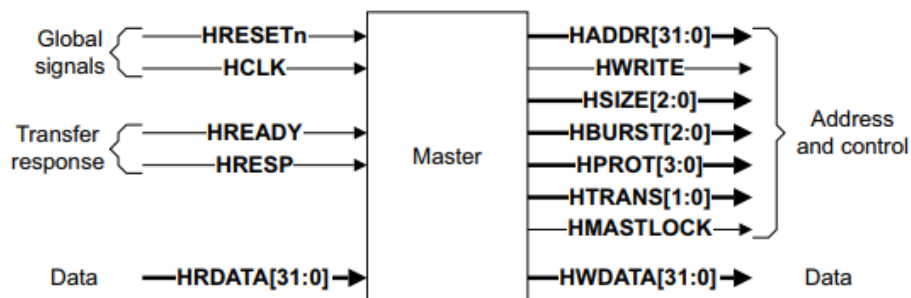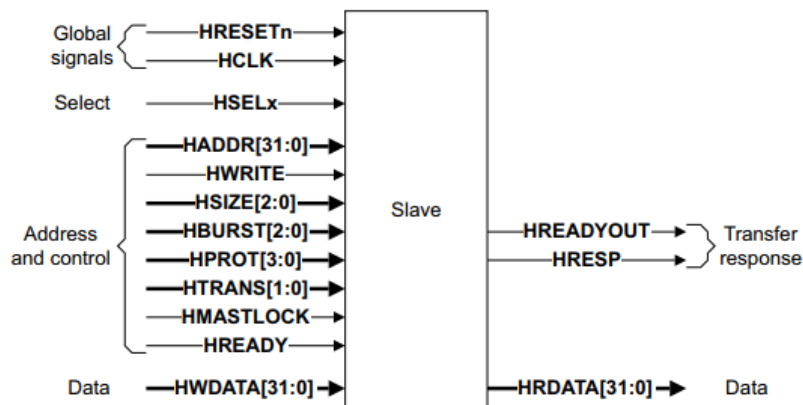

Figure 2: Master Interface

Figure 3: Slave Interface

AHB-Lite Protocol:

Working of Protocol:

Global Signals:

Name	Source	Description
HCLK	Clock source	All signal timing diagrams are related to rising edge of HCLK
HRESTn	Reset Controller	The only active low signal here. It provides asynchronous primary reset for all bus elements.

Master Signals:

Name	Destination	Description
HADDR [31:0]	Slave & Decoder	Address bus of 32 bits
HBURST [2:0]	Slave	Indicates the type of burst signal including wrapping and incrementing bursts with number of beats
HSIZE [2:0]	Slave	Indicates the size of transfer from 8 bits to 1024 bits
HTRANS [1:0]	Slave	Indicates the transfer type: IDLE, BUSY, NON-SEQUENTIAL, SEQUENTIAL
HWDATA [31:0]	Slave	Transfers data from Master to Slave
HWRITE	Slave	Indicates transfer direction.

Slave Signals:

Name	Destination	Description
HRDATA [31:0]	Multiplexor	Read data bus to transfer the data from a Slave's location to the Master via multiplexor
HREADYOUT	Multiplexor	Indicates transfer has finished on the bus and is driven LOW to extend the data phase
HRESP	Multiplexor	Provides additional information that the transfer was successful or failed

Decoder Signals:

Name	Destination	Description
HSELx	Slave	Indicates current transfer is for intended for selected slave

Multiplexor Signals:

Name	Destination	Description
HRDATA [31:0]	Master	Read data bus to rout to Master
HREADY	Master and Slave	Indicates completion of previous transfer
HRESP	Master	Transfer response

Verification Plan

No.	Feature	Test Description	Ref.	Type	Result	Comments
1	Stability of HWRITE during a burst	If HTRANS is such that it depicts SEQ transfer type, HWRITE should be stable to its previous value till HTRANS depicts some other transfer type.	ARM IHI 0033B.b.pdf/Sec.2.2	A	PASS	HWRITE should be stable throughout burst.
2	Try to Read Data when HREADY is LOW	After writing the Data, HREADY is turned LOW and attempt is made to READ the data from slave.	ARM IHI 0033B.b.pdf/Sec.2.4	TR	FAIL	There should not be any data until HREADY is HIGH
3	Checking the WRITE and READ functions (Randomly)	Providing the address **(randomly)** and data (randomly) with HREADY HIGH and in the next clock cycle, READ from the slave with HREADY HIGH. **Multiple** words will be written with **one or two wait states** and then READ.	ARM IHI 0033B.b.pdf/Sec.3.1	TR	PASS	Successful Read from the slave and HRESP should be OKAY
4	Data transfer via IDLE transfer type	Single NON-SEQ burst followed by IDLE transfer followed by NON-SEQ single burst.	ARM IHI 0033B.b.pdf/Sec.3.2	TR	FAIL	IDLE transfer to be ignored by slave
5	OKAY response to IDLE transfer	HRESP should be OKAY immediately after IDLE transfer	ARM IHI 0033B.b.pdf/Sec.3.2	A	PASS	IDLE should be given OKAY response by slave
6	Stability of HWRITE during SEQ transfers	During a sequence of SEQ transfers, HWRITE is toggled	ARM IHI 0033B.b.pdf/Sec.3.2	TR	FAIL	Error should be thrown
7	Verifying different burst operations Part 1	For sequential incremental 4 and 8 beat bursts, READ from the mentioned addresses.	ARM IHI 0033B.b.pdf/Sec.3.5.3	TR	PASS	Successful Read from the slave and HRESP should be OKAY
8	Verifying different burst operations Part 2	For sequential wrapping 4 and 8 beat bursts, READ from the mentioned addresses.	ARM IHI 0033B.b.pdf/Sec.3.5.3	TR	PASS	Successful Read from the slave and HRESP should be OKAY

9	Verifying different burst operations Part 3	For incremental undefined length bursts having different HSIZE, READ from all the mentioned addresses.	ARM IHI 0033B.b.pdf/Sec.3.5.3	TR	PASS	Successful Read from the slave and HRESP should be OKAY
10	Observing HRESP for waited states	If waited transfer goes from type IDLE to NONSEQ and stays this way for HREADY being LOW OR If waited transfer (fixed burst) goes from type BUSY to SEQ and stays this way for HREADY being LOW OR If waited transfer (undefined length burst) goes from type BUSY to any other for HREADY being LOW	ARM IHI 0033B.b.pdf/Sec.3.6.1	TR	PASS	Slave must respond with OKAY response
11	Transfer to non-existent address	SEQ or NON-SEQ transfer at an address that does not exist for the selected slave	ARM IHI 0033B.b.pdf/Sec.4.2.1	TR	FAIL	Error should be thrown
12	Observing HRESP	After writing the Data, HREADY is turned LOW and attempt is made to READ the data from slave. Then in the next cycle, HREADY is turned HIGH, and attempt is made to READ the data. Then we try to write data to inaccessible address.	ARM IHI 0033B.b.pdf/Sec.5.1	TR	PASS	HRESP should first be OKAY but nothing should be read. Then HRESP should be OKAY with data on output. Then HRESP should be ERROR
13	Sampling by slave	For any address and control signals, at positive clock edge, HREADY is kept low and then at next edge, it is turned HIGH	ARM IHI 0033B.b.pdf/Sec.7.1.1 and 7.4	TR	PASS	Sampling must be done at positive clock edge when HREADY is HIGH
14	HREADY while HRESETn	Asserting on HREADY while being on HRESETn	ARM IHI 0033B.b.pdf/Sec.7.1.2	A	PASS	Slave must ensure that HREADY is HIGH during reset
15	HREADY LOW at the instance of ERROR	For the first detection of ERROR, make assertion about HREADY being LOW		A	PASS	ERROR is at-least a 2-cycle response

Explanation of Different Fields

No. The serial number of the test.

Feature The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user.

Test Description A detailed description of the test case being performed. You can be as verbose as you want.

Ref. Reference to the section in the related standard document. The section number as well as page numbers should be described here.

Type Type of the test. Whether the test is an assertion (A) or a transaction (T) type.

Result Pass (P) or Fail (F).

Comments Any other comments about the test or its results that you want to mention.