# UNIVERSITY OF ENGINEERING AND TECHNOLOGY LAHORE, PAKISTAN



#### **AMBA AHB-Lite Protocol Verification Plan**

Submitted To: Dr. Ubaid-Ullah Fayyaz

Submitted By: Muhammad Ayyaz Tariq 2021-PhD-EE-01

Department of Electrical Engineering University of Engineering and Technology, Lahore

# Introduction to the Device-Under-Test (DUT)

AMBA AHB Lite is an interface between master and slaves. It has write data bus configurations of 64 to 1024 bits in powers of 2. The AHB block diagram is as follows:

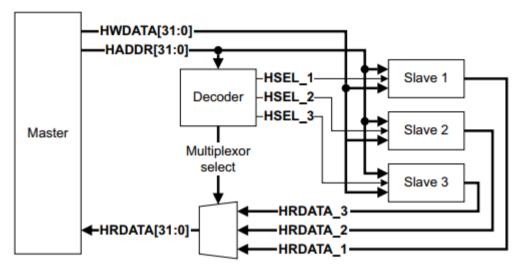


Figure 1: AHB block diagram

In the above figure, one master and three slaves are present. Moreover, decoder selects the slave from the information of the address from Master. Mux gives way back to that particular slave to Master. Master provides address and control information. Slave responds to the transfers initiated by the Master. Every transfer has an address and data cycle each.

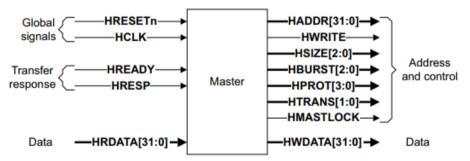


Figure 2: Master Interface

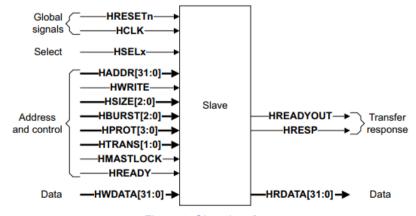


Figure 3: Slave Interface

#### **AHB-Lite Protocol:**

## Working of Protocol:

Global Signals:

Name	Source	Description
HCLK	Clock source	All signal timing diagrams are
		related to rising edge of HCLK
HRESTn	Reset Controller	The only active low signal here. It
		provides asynchronous primary
		reset for all bus elements.

**Master Signals:** 

Name	Destination	Description					
HADDR [31:0]	Slave &	Address bus of 32 bits					
	Decoder						
HBURST [2:0]	Slave	Indicates the type of burst signal					
		including wrapping and					
		incrementing bursts with number of					
		beats					
HSIZE [2:0]	Slave	Indicates the size of transfer from 8					
		bits to 1024 bits					
HTRANS [1:0]	Slave	Indicates the transfer type: IDLE,					
		BUSY, NON-SEQUENTIAL,					
		SEQUENTIAL					
HWDATA [31:0]	Slave	Transfers data from Master to Slave					
HWRITE	Slave	Indicates transfer direction.					

Slave Signals:

Name	Destination	Description						
HRDATA [31:0]	Multiplexor	Read data bus to transfer the data						
		from a Slave's location to the Master						
		via multiplexor						
HREADYOUT	Multiplexor	Indicates transfer has finished on the						
	_	bus and is driven LOW to extend the						
		data phase						
HRESP	Multiplexor	Provides additional information						
	•	that the transfer was successful or						
		failed						

**Decoder Signals:** 

Name	Destination	Description							
HSELx	Slave	Indicates current transfer is for							
		intended for selected slave							

**Multiplexor Signals:** 

Name	Destination	Description							
HRDATA [31:0]	Master	Read data bus to rout to Master							
HREADY	Master and	Indicates completion of previous							
	Slave	transfer							
HRESP	Master	Transfer response							

## Verification Plan

No.	Feature	Test Description	Ref.	Ту	Resu	Expected	Comments
				pe	lt	Result	
1	Stability of HWRITE	During SEQ incremental or Wrap burst (indicated by	ARM IHI	Α	PASS	HWRITE should	
	during a burst	HTRANS), control signal <b>HWRITE</b> should be <b>stable</b> to its	0033B.b.pdf/Sec.2.2			be stable	
		previous value.				throughout	
						burst.	
2	Try to Read Data	After writing the Data, <b>HREADY</b> is turned LOW on the	ARM IHI	TR	PASS	There should	Data will be
	when HREADY is	active edge of next clock cycle for just one cycle and	0033B.b.pdf/Sec.2.4			not be any data	READ on the
	LOW	attempt is made to READ the data from slave during that				until HREADY is	active clock
		cycle.				HIGH	edge when
							HREADY is
							sensed HIGH
3	Checking the	Providing the address (randomly) and data (randomly)	ARM IHI	TR	PASS	Successful Read	Address should
	WRITE and READ	with <b>HREADY</b> HIGH at the active edge of clock and in the	0033B.b.pdf/Sec.3.1			from the slave	not be illegal
	functions	next clock cycle, READ from the slave with <b>HREADY</b> HIGH.				and HRESP	
	(Randomly)					should be OKAY	
4	Writing multiple	Multiple words will be written on one after the other	ARM IHI	TR	PASS	Last Written	This should
	words	active clock edges on the same address and then read from	0033B.b.pdf/Sec.3.1			word must be	justify the
		the same address on the next active clock edge.				the output	overwriting
5	Testing the IDLE	Single <b>NON-SEQ</b> burst on an active edge at address 'A'	ARM IHI	TR	PASS	No data read	No read cycle is
	transfer	followed by <b>IDLE</b> transfer on the next active edge at	0033B.b.pdf/Sec.3.2			from address 'Y'	wasted on IDLE
		address 'Y' followed by <b>NON-SEQ</b> single burst on the next					transfer
		active clock edge at address 'B'. Make an attempt to read					
		twice in the following clock cycles.					
6	OKAY response to	For the validity of slave, detect the <b>IDLE</b> transfer type and	ARM IHI	Α	PASS	HRESP should	IDLE should be
	IDLE transfer	on the next active edge of the clock, <b>HRESP</b> is noted. Both	0033B.b.pdf/Sec.3.2			be OKAY after	given OKAY
		of these signals are related via assertion				completion of	response by
						IDLE	slave

7	Verifying different	For sequential incremental 4 and 8 beat bursts with	ARM IHI	TR	PASS	Successful Read	
	burst operations	specified addresses, after writing in synchronism with	0033B.b.pdf/Sec.3.5.3			from the slave	
	Part 1	clock, READ from the mentioned addresses.				and HRESP	
						should be OKAY	
8	Verifying different	For <b>sequential wrap</b> 4 and 8 beat bursts with specified	ARM IHI	TR	PASS	Successful Read	
	burst operations	addresses, after writing in synchronism with clock, READ	0033B.b.pdf/Sec.3.5.3			from the slave	
	Part 2	from the mentioned addresses.				and HRESP	
						should be OKAY	
9	Verifying different	To transfer a halfword and a word for incremental	ARM IHI	TR	PASS	Successful Read	
	burst operations	undefined length bursts with specified addresses, after	0033B.b.pdf/Sec.3.5.3			from the slave	
	Part 3	writing in synchronism with clock, READ from the				and HRESP	
		mentioned addresses.				should be OKAY	
10	Observing HRESP	Set the HTRANS to IDLE and HREADY LOW at active clock	ARM IHI	Α		Assertion should	HTRANS should
	for waited states	edge. Then initiate <b>NONSEQ</b> transfer in the next clock	0033B.b.pdf/Sec.3.6.1		PASS	remain LOW	not change from
	Part 1	cycle, and assert on <b>stability</b> of <b>HTRANS</b> before <b>HREADY</b>				and HRESP	its NON-SEQ
		goes <b>HIGH</b> .				should be OKAY	state until the
							slave is ready
11	Observing HRESP	For fixed burst transfer, set the HTRANS to BUSY and	ARM IHI	Α		Assertion should	HTRANS should
	for waited states	HREADY LOW at active clock edge. Then initiate SEQ	0033B.b.pdf/Sec.3.6.1		PASS	remain LOW	not change from
	Part 2	transfer in the next clock cycle, and assert on <b>stability</b> of				and HRESP	its SEQ state
		HTRANS before HREADY goes HIGH.				should be OKAY	until the slave is
							ready
12	Observing HRESP	For undefined length burst transfer, set the HTRANS to	ARM IHI	Α		Assertion should	HTRANS should
	for waited states	BUSY and HREADY LOW at active clock edge. Then initiate	0033B.b.pdf/Sec.3.6.1		PASS	remain LOW	not change from
	Part 3	<b>SEQ</b> transfer in the next clock cycle, and assert on <b>stability</b>				and HRESP	its SEQ state
		of HTRANS before HREADY goes HIGH.				should be OKAY	until the slave is
							ready
13	Observing HRESP	For undefined length burst transfer, set the HTRANS to	ARM IHI	Α		Assertion should	HTRANS should
	for waited states	BUSY and HREADY LOW at active clock edge. Then initiate	0033B.b.pdf/Sec.3.6.1		PASS	remain LOW	not change from
	Part 4	NONSEQ transfer in the next clock cycle, and assert on				and HRESP	its NONSEQ
		stability of HTRANS before HREADY goes HIGH.				should be OKAY	state until the
							slave is ready

In this test, we try 3 transfers.  In the mext active clock edge and attempt is made to READ the data.  In the mext active clock edge with address on the next active clock edge with address.  In the mext active clock edge with address and attempt is made to READ the data.  In the mext active clock edge with address and attempt is made to READ the data.  In the READY is under the mext active clock edge with address and attempt is made to READ the data.  In this test, when the mext active clock edge with address and attempt is made to READ the data.  In the READY is under the mext active clock edge. In the transfer is initiated with the transfer is initiated with the mext ac	14	Transfer to non-	Initiate a <b>NON-SEQ single</b> transfer at an address that does	ARM IHI	TR	PASS	Error should be	This happens
In this test, we try 3 transfers.  ARM IHI O338.b.pdf/Sec.5.1  ARM IHI O338.b.pdf/Sec.5.1  TR PASS First, in synchronism with HCLK, after writing the Data, HREADY is turned LOW at the next active clock edge and attempt is made to READ the data from slave.  Then in the next cycle, HREADY is turned HIGH, and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  At active edge of the clock, detect the first HIGH of HRESP ERROR  TR ARM IHI O338.b.pdf/Sec.5.1.3  ASSERTION Should be read. Then HRESP should be OKAY with data on output. Then HRESP should be ERROR  Assertion should remain LOW PASS Assertion should remain LOW REROR IS attent of the Institute of the In		existent address	not exist for the selected slave.	0033B.b.pdf/Sec.4.2.1			thrown	because the
First, in synchronism with HCLK, after writing the Data, HREADY is turned LOW at the next active clock edge and attempt is made to READ the data from slave.    Then in the next cycle, HREADY is turned HIGH, and attempt is made to READ the data. Then HRESP should be CREAD the data. Then write data to inaccessible address and attempt is made to READ the data.    Then write data to inaccessible address and attempt is made to READ the data. Then HRESP should be ERROR with data on output. Then HRESP should be ERROR with data on output. Then HRESP should be ERROR with data on output. Then HRESP should be ERROR with data on output. Then HRESP should be ERROR with data on output. Then HRESP should be ERROR with data on output. Then HRESP should be ERROR with data on output. Then HRESP should be ERROR with address with made to READ the data.    A PASS   Assertion should remain LOW   Least a 2-cycle response with address w								address is illegal
First, in synchronism with HCLK, after writing the Data, HREADY is turned LOW at the next active clock edge and attempt is made to READ the data from slave.  Then in the next cycle, HREADY is turned HIGH, and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  At active edge of the clock, detect the first HIGH of HRESP ERROR  Then write data to inaccessible address and attempt is made to READ the data.  At active edge of the clock, detect the first LOW of HREADY while HRESPT and assert on HREADY being HIGH throughout that duration  Then write data to inaccessible address and attempt is made to READ the data.  At active edge of the clock, detect the first LOW of HRESPT and assert on HREADY being HIGH throughout that duration  Then write data to inaccessible address and attempt is made to READ the data.  At active edge of the clock, detect the first LOW of HRESPT and assert on HREADY being HIGH throughout that duration  Then write data to inaccessible address and attempt is made to READ the data.  ARM IHI 0033B.b.pdf/Sec.7.1.2  A PASS Assertion should remain LOW remain LOW wait state Ok.  Then remain LOW remain LOW wait state Ok.  Then remain LOW remain LOW wait state Ok.  Then remain LOW			In this test, we try 3 transfers.				HRESP should	
HREADY is turned LOW at the next active clock edge and attempt is made to READ the data from slave.  Then in the next cycle, HREADY is turned HIGH, and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  A William A PASS Assertion should remain LOW and HREAD is HIGH throughout that duration  Then write data to inaccessible address and attempt is made to READ the data.  A PASS Assertion should remain LOW and HREAD is HIGH throughout remain LOW and HREAD is HIGH throughout and the READ is HIGH throughout that duration  Then write data to inaccessible address and attempt is made to READ the data.  A PASS Assertion should remain LOW and HREAD is HIGH throughout remain LOW and HREAD is HIGH throughout and the READ is HIGH throughout that duration and the READ is HIGH throughout and HREAD is HI				ARM IHI	TR	PASS	first be OKAY	
15 Observing HRESP (3 scenarios)  Then in the next cycle, HREADY is turned HIGH, and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  At active edge of the clock, detect the first HIGH of HRESP (ERROR), and assert on HREADY being LOW at that instant the HRESP is HIGH of HRESP (ERROR), and assert on HREADY being HIGH throughout that duration  Then HRESP should be ERROR  ARM IHI (Machine HRESP) is HIGH of HRESP (HRESP) is HIGH of HRESP (HRESP) is HIGH of HRESP is HIGH of HRESP) is HIGH of HRESP is HI			First, in synchronism with <b>HCLK</b> , after writing the Data,	0033B.b.pdf/Sec.5.1			but nothing	Error should
Then in the next cycle, HREADY is turned HIGH, and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  At active edge of the clock, detect the first HIGH of HRESP (ERROR), and assert on HREADY being LOW at that instant that duration  At active edge of the clock, detect the first LOW of HRESET and assert on HREADY being HIGH throughout that duration  At active edge of the clock, detect the first LOW of HRESET and assert on HREADY being HIGH throughout that duration  At active edge of the clock, detect the first LOW of HRESET and assert on HREADY being HIGH throughout that duration  At active edge of the clock, detect the first LOW of HRESET and assert on HREADY being HIGH throughout that duration  ARM IHI O333B.b.pdf/Sec.3.2  ARM IHI O333B.b.pdf/Sec.3.3  A PASS Assertion should remain LOW remain LOW provide zero wait state OK response to IDLE transfer at active clock edge  Death of the next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  ARM IHI O333B.b.pdf/Sec.3.3			HREADY is turned LOW at the next active clock edge and				should be read.	only be there
Then in the next cycle, HREADY is turned HIGH, and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  At active edge of the clock, detect the first HIGH of HRESP the instance of ERROR  THREADY LOW at the instance of ERROR  THREADY while HRESETn HREADY being LOW at that instant that duration  THREADY while HRESETn HRESETn and assert on HREADY being HIGH throughout that duration  Then write data to inaccessible address and attempt is made to READ the data.  At active edge of the clock, detect the first HIGH of HRESP (ERROR), and assert on HREADY being LOW at that instant that instant that the instance of ERROR  THREADY while HRESETn and assert on HREADY being HIGH throughout that duration  The very data to the clock edge of the clock, detect the first LOW of HRESETn and assert on HREADY being HIGH throughout that duration  The very data to the clock edge, start a sequential INCR4 burst which is followed by IDLE transfer on the next active clock edge. Assert that HRESP is LOW and HREADY is HIGH on the next active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  The next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  The next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  The next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  The next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  The next active clock edge in the data.  The HIGH AT A CAPASS Assertion should remain LOW and PREADY is HIGH on other transfer and the next active clock edge with address 'A' and HMRITE HIGH. HMASTLOCK	15	Observing HRESP	attempt is made to READ the data from slave.				Then HRESP	when READ is
attempt is made to READ the data.  Then write data to inaccessible address and attempt is made to READ the data.  16 HREADY LOW at the instance of ERROR  17 HREADY while HRESETn and assert on HREADY being LOW at that instant that duration  18 Zero Wait State Response  19 Locked Transfer  19 Locked Transfer  19 Locked Transfer  19 Locked Transfer  10 HREADY is made to READ the data.  At active edge of the clock, detect the first HIGH of HRESP (ERROR), and assert on HREADY being LOW at that instant that duration  19 Locked Transfer  20 Locked Transfer  30 Locked Transfer  40 Locked Transfer  50 Locked Transfer  40 Locked Transfer  50 Locked Transfer  50 Locked Transfer  50 Locked Transfer  60 Locked		(3 scenarios)					should be OKAY	demanded from
Then write data to inaccessible address and attempt is made to READ the data.  16 HREADY LOW at the instance of ERROR  17 HREADY while HRESET At a trive edge of the clock, detect the first HIGH of HRESP (ERROR), and assert on HREADY being LOW at that instant that duration  18 Zero Wait State Response  19 Locked Transfer  19 Locked Transfer  19 Locked Transfer  10 HREADY Low at the instance of ERROR  10 At active edge of the clock, detect the first LOW of HRESET and assert on HREADY being HIGH throughout that duration  19 Locked Transfer  20 At a transfer at active clock edge with address ('A' and HWRITE HIGH our ing both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.			Then in the next cycle, <b>HREADY</b> is turned HIGH, and				with data on	inaccessible
Then write data to inaccessible address and attempt is made to READ the data.  At active edge of the clock, detect the first HIGH of HRESP (ERROR), and assert on HREADY being LOW at that instant the instance of ERROR  THEADY while HRESETIN HRESETIN HRESETIN AT A HRESE			attempt is made to READ the data.				output. Then	address
made to READ the data.  16 HREADY LOW at the instance of (ERROR), and assert on HREADY being LOW at that instant the instance of (ERROR), and assert on HREADY being LOW at that instant that instant the instance of (ERROR), and assert on HREADY being LOW at that instant that instant the instance of (ERROR), and assert on HREADY being LOW at that instant that instant the instance of (ERROR), and assert on HREADY being LOW at that instant that instant the instance of (ERROR), and assert on HREADY being LOW at that instant that instant the instance of (ERROR), and assert on HREADY being HIGH throughout that duration  17 HREADY while HRESETn and assert on HREADY being HIGH throughout that duration  18 Zero Wait State Response Which is followed by IDLE transfer on the next active clock edge. Assert that HRESP is LOW and HREADY is HIGH on the next active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  19 Locked Transfer  10 Locked Transfer  11 Locked Transfer  12 Locked Transfer  13 Locked Transfer  14 Locked Transfer  15 Locked Transfer  16 Locked Transfer  17 Locked Transfer  18 Locked Transfer  18 Locked Transfer							HRESP should	
HREADY LOW at the instance of ERROR and assert on HREADY being LOW at that instant the instance of ERROR and assert on HREADY being LOW at that instant the instance of ERROR and assert on HREADY being LOW at that instant the instance of ERROR and assert on HREADY being HIGH throughout that duration assert on HREADY is HIGH on the next active clock edge. Assert that HRESP is LOW and HREADY is HIGH on the next active clock edge at next active clock edge with address of the next active clock edge with address at next active clock edge with address of the next active clock edge, IDLE transfer is initiated with HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  ARM IHI O033B.b.pdf/Sec.7.1.2  ARM IHI O033B.b.pdf/Sec.3.2  ARM IHI O033B.b.pdf/Sec.3.2  ARM IHI O033B.b.pdf/Sec.3.2  ARM IHI O033B.b.pdf/Sec.3.2  ARM IHI O033B.b.pdf/Sec.3.3			Then write data to inaccessible address and attempt is				be ERROR	
the instance of ERROR  17 HREADY while HRESETn At a ctive edge of the clock, detect the first LOW of HRESETn At a sacret on HREADY being HIGH throughout that duration  18 Zero Wait State Response Assert that HRESP is LOW and HREADY is HIGH on the next active clock edge. Assert that HRESP is LOW and HREADY is HIGH on the next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  19 Locked Transfer HREADY is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  19 Locked Transfer HREADY is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  10 ARM IHI O033B.b.pdf/Sec. 7.1.2  A PASS Assertion should remain LOW and HREADY is HIGH on Slave must of the next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  10 ARM IHI O033B.b.pdf/Sec. 7.1.2  A PASS Assertion should remain LOW and HREADY is HIGH on Slave must of the next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.			made to READ the data.					
### PASS   Response	16	HREADY LOW at	At active edge of the clock, detect the first HIGH of <b>HRESP</b>	ARM IHI	Α	PASS	Assertion should	ERROR is at-
HREADY while HRESETn HRESETn HRESETn and assert on HREADY being HIGH throughout that duration  ARM IHI O033B.b.pdf/Sec.7.1.2  Basertion should remain LOW HREADY is HIG during reset  ARM IHI O033B.b.pdf/Sec.3.2  ARM IHI O033B.b.pdf/Sec.3.2  ARM IHI A PASS Assertion should remain LOW HREADY is HIG during reset  ARM IHI O033B.b.pdf/Sec.3.2  ARM IHI O033B.b.pdf/Sec.3.3  Assertion should remain LOW Slave must ovait state OK response to IDLE transfer VA' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.		the instance of	(ERROR), and assert on <b>HREADY</b> being LOW at that instant	0033B.b.pdf/Sec.5.1.3			remain LOW	least a 2-cycle
HRESETn and assert on HREADY being HIGH throughout that duration  2 Zero Wait State Response  At the active clock edge, start a sequential INCR4 burst which is followed by IDLE transfer on the next active clock edge. Assert that HREADY is HIGH on the next active clock edge  19 Locked Transfer  Start a NONSEQ transfer at active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  HRESETn and assert on HREADY being HIGH throughout that duration  O033B.b.pdf/Sec.7.1.2  ARM IHI O033B.b.pdf/Sec.3.2  ARM IHI O033B.b.pdf/Sec.3.3  TR PASS Data at 'A' should be available to be read on second transfer starting edge. Data at 'A' should be written on third transfer are processed are processed.		ERROR						response
that duration  Zero Wait State Response  At the active clock edge, start a sequential INCR4 burst which is followed by IDLE transfer on the next active clock edge. Assert that HRESP is LOW and HREADY is HIGH on the next active clock edge  Locked Transfer  Start a NONSEQ transfer at active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  HREADY is HIG during reset  ARM IHI  O033B.b.pdf/Sec.3.2  ARM IHI  O033B.b.pdf/Sec.3.3  ARM IHI  O033B.b.pdf/Sec.3.3  TR  PASS  Data at 'A' should be available to be read on second transfer starting edge. Data at 'A' should be written on third transfer  other transfer are processed	17	HREADY while	At active edge of the clock, detect the first LOW of	ARM IHI	Α	PASS	Assertion should	Slave must
2 Zero Wait State Response  At the active clock edge, start a sequential INCR4 burst which is followed by IDLE transfer on the next active clock edge. Assert that HRESP is LOW and HREADY is HIGH on the next active clock edge  19  Locked Transfer  Start a NONSEQ transfer at active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  ARM IHI 0033B.b.pdf/Sec.3.2  TR PASS  Data at 'A' should be available to be read on second transfer starting edge. Data at 'A' should be written on third transfer are processed		HRESETn	HRESETn and assert on HREADY being HIGH throughout	0033B.b.pdf/Sec.7.1.2			remain LOW	ensure that
At the active clock edge, start a sequential INCR4 burst which is followed by IDLE transfer on the next active clock edge. Assert that HRESP is LOW and HREADY is HIGH on the next active clock edge  19 Locked Transfer  Start a NONSEQ transfer at next active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  ARM IHI O033B.b.pdf/Sec.3.2  ARM IHI O033B.b.pdf/Sec.3.3			that duration					HREADY is HIGH
Response which is followed by IDLE transfer on the next active clock edge. Assert that HRESP is LOW and HREADY is HIGH on the next active clock edge  19 Locked Transfer Start a NONSEQ transfer at active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  Nonsequence be read on second transfer starting edge. Data at 'A' should be written on third transfer are processed.								during reset
edge. Assert that HRESP is LOW and HREADY is HIGH on the next active clock edge  19 Locked Transfer  Start a NONSEQ transfer at active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  ARM IHI  O033B.b.pdf/Sec.3.3  TR  PASS  Data at 'A' should be available to be read on second transfer starting edge. Data at 'A' should be written on third transfer are processed.	18	Zero Wait State			Α	PASS	Assertion should	
the next active clock edge  19 Locked Transfer  Start a NONSEQ transfer at active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  TR PASS Data at 'A' should be available to be read on second transfer starting edge. Data at 'A' should be written on third transfer are processed.		Response	·	0033B.b.pdf/Sec.3.2			remain LOW	provide zero
Locked Transfer  Start a NONSEQ transfer at active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  HOLE transfer SARM IHI O033B.b.pdf/Sec.3.3  ARM IHI O033B.b.pdf/Sec.3.3  PASS Data at 'A' should be available to be read on second transfer starting edge. Data at 'A' should be written on third transfer on third transfer are processed.			edge. Assert that <b>HRESP</b> is LOW and <b>HREADY</b> is HIGH on					wait state OKAY
19 Locked Transfer  Start a NONSEQ transfer at active clock edge with address 'A' and HWRITE LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and HWRITE HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  ARM IHI  0033B.b.pdf/Sec.3.3  TR  PASS  Data at 'A' should be available to be read on second transfer starting edge. Data at 'A' should be written on third transfer are processed.			the next active clock edge					response to
'A' and <b>HWRITE</b> LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and <b>HWRITE</b> HIGH. <b>HMASTLOCK</b> is HIGH during both these cycles. On the next active clock edge, <b>IDLE</b> transfer is initiated with <b>HMASTLOCK</b> as LOW.  O033B.b.pdf/Sec.3.3  be available to be read on second transfer starting edge. Data at 'A' should be written on third transfer are processed.								IDLE transfer
at next active clock edge with address 'A' and <b>HWRITE</b> HIGH. <b>HMASTLOCK</b> is HIGH during both these cycles. On the next active clock edge, <b>IDLE</b> transfer is initiated with <b>HMASTLOCK</b> as LOW.  read on second transfer starting edge. Data at 'A' should be written on third transfer are processed	19	Locked Transfer	_	ARM IHI	TR	PASS		Current transfer
HIGH. HMASTLOCK is HIGH during both these cycles. On the next active clock edge, IDLE transfer is initiated with HMASTLOCK as LOW.  transfer starting edge. Data at 'A' should be written on third transfer are processed.				0033B.b.pdf/Sec.3.3				sequence be
the next active clock edge, <b>IDLE</b> transfer is initiated with <b>HMASTLOCK</b> as LOW.  edge. Data at 'A' should be written on third transfer are processed			at next active clock edge with address 'A' and HWRITE					processed
HMASTLOCK as LOW.  should be written on third transfer are processed.			HIGH. <b>HMASTLOCK</b> is HIGH during both these cycles. On					before any
HMASTLOCK as LOW. on third transfer are processed			the next active clock edge, <b>IDLE</b> transfer is initiated with					other transfers
			HMASTLOCK as LOW.					are processed
l l Starting edge. I							starting edge.	

20	IDLE/BUSY	At the active clock edge, start a sequential INCR4 burst	ARM IHI	Α	PASS	Assertion should	Slave must
	transfers to non-	which is followed by <b>BUSY</b> transfer to non-existent address	0033B.b.pdf/Sec.4.2.1			remain LOW	provide zero
	existent address	on the next active clock edge. Assert that <b>HRESP</b> is LOW					wait state OKAY
		and HREADY is HIGH on the next active clock edge					response to
							IDLE/BUSY
							transfer
21	HREADY-HRESP	At an active clock edge, write on an address. Before the	ARM IHI	Α	PASS	Assertion should	
	Scenario 1	next active edge, <b>HREADY</b> is low, assert that <b>HRESP</b> is LOW	0033B.b.pdf/Sec.5.1.2			remain LOW	
		using overlapping operator					
22	HREADY-HRESP	At an active clock edge, detect <b>HRESP</b> as <b>HIGH</b> , assert that	ARM IHI	Α	PASS	Assertion should	
	Scenario 2	it should remain stable before the detection of <b>HREADY</b>	0033B.b.pdf/Sec.5.1.2			remain LOW	
		HIGH					
23	Enable of slave	HSELx of particular slave is set HIGH and at active clock		TR	PASS	In first part,	
		edge, data is written at particular legal address with	ARM IHI			correct data	
		HREADY HIGH and on the next active edge of HCLK, data is	0033B.b.pdf/Sec.2.4			must be	Slave will
		read.				available on	respond only
		Now in the next active clock edge, <b>HSELx</b> is set to LOW and				HREAD. In	when it is
		the same procedure is repeated				second scenario,	chosen
						nothing should	
						be available on	
						HREAD	
24	Protection	At positive clock edge, write instruction with wrong	ARM IHI	TR	PASS	HRESP should	Illegal
	Scenario 1	opcode and keep <b>LSB</b> of <b>HPROT</b> LOW. Observe the slave	0033B.b.pdf/Sec.3.7			be high in the	instruction code
		response in the next cycle. You can also try to read from				second clock	
		the address that you gave for storing the answer after				cycle	
		opcode performance.					
25	Protection	At positive edge of the clock, try to write data in privileged	ARM IHI	TR	PASS	HRESP should	No write
	Scenario 2	address range while keeping the HPROT[1] LOW. Observe	0033B.b.pdf/Sec.3.7			become high	operation on
		the response of the slave.					the privileged
							addresses in
							USER mode

## **Explanation of Different Fields**

**No.** The serial number of the test.

**Feature** The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level

of a user.

**Test Description** A detailed description of the test case being performed. You can be as verbose as you want.

**Ref.** Reference to the section in the related standard document. The section number as well as page numbers

should be described here.

**Type** Type of the test. Whether the test is an assertion (A) or a transaction (T) type.

Result Pass (P) or Fail (F).

**Comments** Any other comments about the test or its results that you want to mention.