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AMBA AHB-Lite Protocol Verification Plan

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2021-PhD-EE-01

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Introduction to the Device-Under-Test (DUT)

AMBA AHB Lite is an interface between master and slaves. It has write data bus configurations of 64 to 1024 bits in powers of 2. The AHB block diagram is as follows:

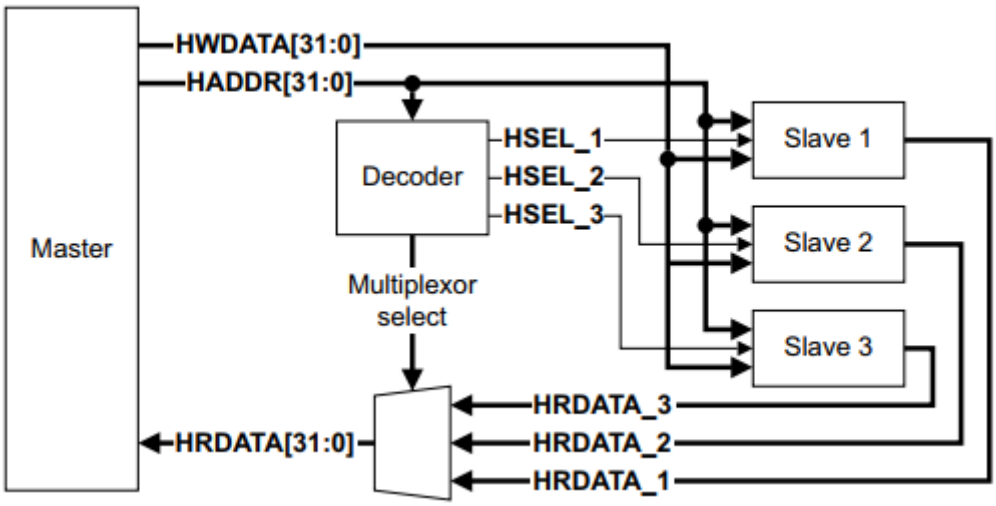

Figure 1: AHB block diagram

In the above figure, one master and three slaves are present. Moreover, decoder selects the slave from the information of the address from Master. Mux gives way back to that particular slave to Master. Master provides address and control information. Slave responds to the transfers initiated by the Master. Every transfer has an address and data cycle each.

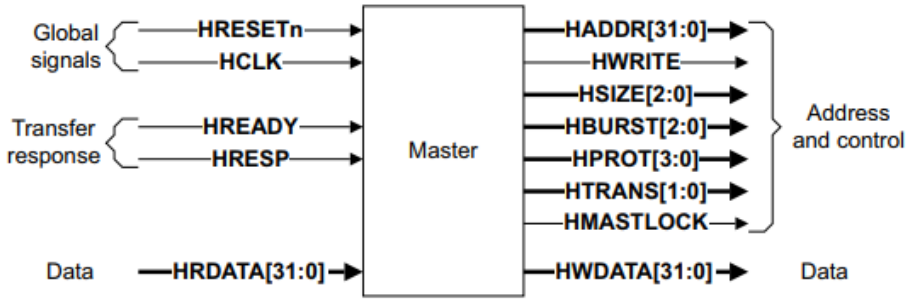

Figure 2: Master Interface

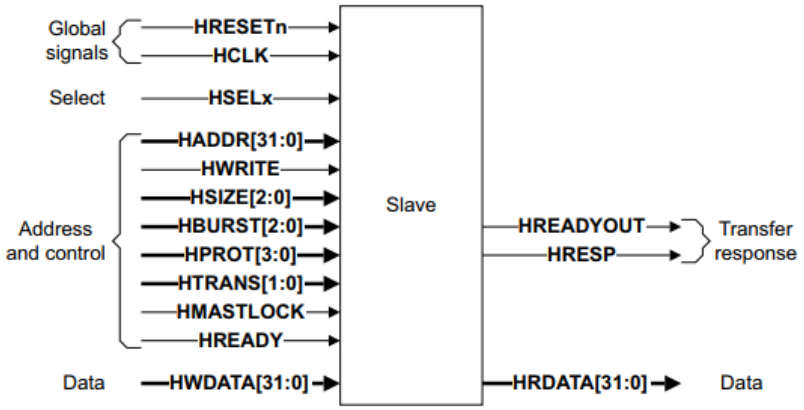

Figure 3: Slave Interface

AHB-Lite Protocol:

Working of Protocol:

Global Signals:

Name	Source	Description
HCLK	Clock source	All signal timing diagrams are related to rising edge of HCLK
HRESTn	Reset Controller	The only active low signal here. It provides asynchronous primary reset for all bus elements.

Master Signals:

Name	Destination	Description
HADDR [31:0]	Slave & Decoder	Address bus of 32 bits
HBURST [2:0]	Slave	Indicates the type of burst signal including wrapping and incrementing bursts with number of beats
HSIZE [2:0]	Slave	Indicates the size of transfer from 8 bits to 1024 bits
HTRANS [1:0]	Slave	Indicates the transfer type: IDLE, BUSY, NON-SEQUENTIAL, SEQUENTIAL
HWDATA [31:0]	Slave	Transfers data from Master to Slave
HWRITE	Slave	Indicates transfer direction.

Slave Signals:

Name	Destination	Description
HRDATA [31:0]	Multiplexor	Read data bus to transfer the data from a Slave's location to the Master via multiplexor
HREADYOUT	Multiplexor	Indicates transfer has finished on the bus and is driven LOW to extend the data phase
HRESP	Multiplexor	Provides additional information that the transfer was successful or failed

Decoder Signals:

Name	Destination	Description
HSELx	Slave	Indicates current transfer is for intended for selected slave

Multiplexor Signals:

Name	Destination	Description
HRDATA [31:0]	Master	Read data bus to rout to Master
HREADY	Master and Slave	Indicates completion of previous transfer
HRESP	Master	Transfer response

Verification Plan

No.	Feature	Test Description	Ref.	Type	Result	Expected Result	Comments
1	Stability of HWRITE during a burst	During **SEQ incremental** or **Wrap burst** (indicated by HTRANS), control signal **HWRITE** should be **stable** to its previous value.	ARM IHI 0033B.b.pdf/Sec.2.2	A	PASS	HWRITE should be stable throughout burst.	
2	Try to Read Data when HREADY is LOW	After writing the Data, **HREADY** is turned LOW on the active edge of next clock cycle for just one cycle and attempt is made to READ the data from slave during that cycle.	ARM IHI 0033B.b.pdf/Sec.2.4	TR	PASS	There should not be any data until HREADY is HIGH	Data will be READ on the active clock edge when HREADY is sensed HIGH
3	Checking the WRITE and READ functions (Randomly)	Providing the address **(randomly)** and data **(randomly)** with **HREADY** HIGH at the active edge of clock and in the next clock cycle, READ from the slave with **HREADY** HIGH.	ARM IHI 0033B.b.pdf/Sec.3.1	TR	PASS	Successful Read from the slave and HRESP should be OKAY	Address should not be illegal
4	Writing multiple words	**Multiple** words will be written on one after the other active clock edges on the same address and then read from the same address on the next active clock edge.	ARM IHI 0033B.b.pdf/Sec.3.1	TR	PASS	Last Written word must be the output	This should justify the overwriting
5	Testing the IDLE transfer	Single **NON-SEQ** burst on an active edge at address 'A' followed by **IDLE** transfer on the next active edge at address 'Y' followed by **NON-SEQ** single burst on the next active clock edge at address 'B'. Make an attempt to read **twice** in the following clock cycles.	ARM IHI 0033B.b.pdf/Sec.3.2	TR	PASS	No data read from address 'Y'	No read cycle is wasted on IDLE transfer
6	OKAY response to IDLE transfer	For the validity of slave, detect the **IDLE** transfer type and on the next active edge of the clock**, HRESP** is noted. Both of these signals are related via assertion	ARM IHI 0033B.b.pdf/Sec.3.2	A	PASS	HRESP should be OKAY after completion of IDLE	IDLE should be given OKAY response by slave

7	Verifying different burst operations Part 1	For **sequential incremental** 4 and 8 beat bursts with specified addresses, after writing in synchronism with clock, READ from the mentioned addresses.	ARM IHI 0033B.b.pdf/Sec.3.5.3	TR	PASS	Successful Read from the slave and HRESP should be OKAY	
8	Verifying different burst operations Part 2	For **sequential wrap** 4 and 8 beat bursts with specified addresses, after writing in synchronism with clock, READ from the mentioned addresses.	ARM IHI 0033B.b.pdf/Sec.3.5.3	TR	PASS	Successful Read from the slave and HRESP should be OKAY	
9	Verifying different burst operations Part 3	To transfer a halfword and a word for **incremental undefined length** bursts with specified addresses, after writing in synchronism with clock, READ from the mentioned addresses.	ARM IHI 0033B.b.pdf/Sec.3.5.3	TR	PASS	Successful Read from the slave and HRESP should be OKAY	
10	Observing HRESP for waited states Part 1	Set the **HTRANS** to **IDLE** and **HREADY LOW** at active clock edge. Then initiate **NONSEQ** transfer in the next clock cycle, and assert on **stability** of **HTRANS** before **HREADY** goes **HIGH**.	ARM IHI 0033B.b.pdf/Sec.3.6.1	A	PASS	Assertion should remain LOW and HRESP should be OKAY	HTRANS should not change from its NON-SEQ state until the slave is ready
11	Observing HRESP for waited states Part 2	For fixed burst transfer, set the **HTRANS** to **BUSY** and **HREADY LOW** at active clock edge. Then initiate **SEQ** transfer in the next clock cycle, and assert on **stability** of **HTRANS** before **HREADY** goes **HIGH**.	ARM IHI 0033B.b.pdf/Sec.3.6.1	A	PASS	Assertion should remain LOW and HRESP should be OKAY	HTRANS should not change from its SEQ state until the slave is ready
12	Observing HRESP for waited states Part 3	For undefined length burst transfer, set the **HTRANS** to **BUSY** and **HREADY LOW** at active clock edge. Then initiate **SEQ** transfer in the next clock cycle, and assert on **stability** of **HTRANS** before **HREADY** goes **HIGH**.	ARM IHI 0033B.b.pdf/Sec.3.6.1	A	PASS	Assertion should remain LOW and HRESP should be OKAY	HTRANS should not change from its SEQ state until the slave is ready
13	Observing HRESP for waited states Part 4	For undefined length burst transfer, set the **HTRANS** to **BUSY** and **HREADY LOW** at active clock edge. Then initiate **NONSEQ** transfer in the next clock cycle, and assert on **stability** of **HTRANS** before **HREADY** goes **HIGH**.	ARM IHI 0033B.b.pdf/Sec.3.6.1	A	PASS	Assertion should remain LOW and HRESP should be OKAY	HTRANS should not change from its NONSEQ state until the slave is ready

14	Transfer to non-existent address	Initiate a **NON-SEQ single** transfer at an address that does not exist for the selected slave.	ARM IHI 0033B.b.pdf/Sec.4.2.1	TR	PASS	Error should be thrown	This happens because the address is illegal
15	Observing HRESP (3 scenarios)	In this test, we try 3 transfers. First, in synchronism with **HCLK**, after writing the Data, **HREADY** is turned LOW at the next active clock edge and attempt is made to READ the data from slave. Then in the next cycle, **HREADY** is turned HIGH, and attempt is made to READ the data. Then write data to inaccessible address and attempt is made to READ the data.	ARM IHI 0033B.b.pdf/Sec.5.1	TR	PASS	HRESP should first be OKAY but nothing should be read. Then HRESP should be OKAY with data on output. Then HRESP should be ERROR	Error should only be there when READ is demanded from inaccessible address
16	HREADY LOW at the instance of ERROR	At active edge of the clock, detect the first HIGH of **HRESP** (ERROR), and assert on **HREADY** being LOW at that instant	ARM IHI 0033B.b.pdf/Sec.5.1.3	A	PASS	Assertion should remain LOW	ERROR is at-least a 2-cycle response
17	HREADY while HRESETn	At active edge of the clock, detect the first LOW of **HRESETn** and **assert** on **HREADY** being HIGH **throughout** that duration	ARM IHI 0033B.b.pdf/Sec.7.1.2	A	PASS	Assertion should remain LOW	Slave must ensure that HREADY is HIGH during reset
18	Zero Wait State Response	At the active clock edge, start a **sequential INCR4** burst which is followed by **IDLE** transfer on the next active clock edge. Assert that **HRESP** is LOW and **HREADY** is HIGH on the next active clock edge	ARM IHI 0033B.b.pdf/Sec.3.2	A	PASS	Assertion should remain LOW	Slave must provide zero wait state OKAY response to IDLE transfer
19	Locked Transfer	Start a **NONSEQ** transfer at active clock edge with address 'A' and **HWRITE** LOW. This is followed by NONSEQ transfer at next active clock edge with address 'A' and **HWRITE** HIGH. **HMASTLOCK** is HIGH during both these cycles. On the next active clock edge, **IDLE** transfer is initiated with **HMASTLOCK** as LOW.	ARM IHI 0033B.b.pdf/Sec.3.3	TR	PASS	Data at 'A' should be available to be read on second transfer starting edge. Data at 'A' should be written on third transfer starting edge.	Current transfer sequence be processed before any other transfers are processed

20	IDLE/BUSY transfers to non-existent address	At the active clock edge, start a **sequential INCR4** burst which is followed by **BUSY** transfer to non-existent address on the next active clock edge. Assert that **HRESP** is LOW and **HREADY** is HIGH on the next active clock edge	ARM IHI 0033B.b.pdf/Sec.4.2.1	A	PASS	Assertion should remain LOW	Slave must provide zero wait state OKAY response to IDLE/BUSY transfer
21	HREADY-HRESP Scenario 1	At an active clock edge, write on an address. Before the next active edge**, HREADY** is low, assert that **HRESP** is LOW using overlapping operator	ARM IHI 0033B.b.pdf/Sec.5.1.2	A	PASS	Assertion should remain LOW	
22	HREADY-HRESP Scenario 2	At an active clock edge, detect **HRESP** as **HIGH**, assert that it should remain stable before the detection of **HREADY** HIGH	ARM IHI 0033B.b.pdf/Sec.5.1.2	A	PASS	Assertion should remain LOW	
23	Enable of slave	**HSELx** of particular slave is set HIGH and at active clock edge, data is written at particular legal address with **HREADY** HIGH and on the next active edge of **HCLK**, data is read. Now in the next active clock edge, **HSELx** is set to LOW and the same procedure is repeated	ARM IHI 0033B.b.pdf/Sec.2.4	TR	PASS	In first part, correct data must be available on HREAD. In second scenario, nothing should be available on HREAD	Slave will respond only when it is chosen
24	Protection Scenario 1	At positive clock edge, write instruction with wrong opcode and keep **LSB** of **HPROT** LOW. Observe the slave response in the next cycle. You can also try to read from the address that you gave for storing the answer after opcode performance.	ARM IHI 0033B.b.pdf/Sec.3.7	TR	PASS	HRESP should be high in the second clock cycle	Illegal instruction code
25	Protection Scenario 2	At positive edge of the clock, try to write data in privileged address range while keeping the **HPROT[1]** LOW. Observe the response of the slave.	ARM IHI 0033B.b.pdf/Sec.3.7	TR	PASS	HRESP should become high	No write operation on the privileged addresses in USER mode

Explanation of Different Fields

No.	The serial number of the test.
Feature	The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user.
Test Description	A detailed description of the test case being performed. You can be as verbose as you want.
Ref.	Reference to the section in the related standard document. The section number as well as page numbers should be described here.
Type	Type of the test. Whether the test is an assertion (A) or a transaction (T) type.
Result	Pass (P) or Fail (F).
Comments	Any other comments about the test or its results that you want to mention.