PrimisAI

www.primis.ai

Not leveraging AI-Assistance in your ASIC/FPGA projects yet? Don't get left behind!

Join us for a live webinar where we will hands-on show how to get the most out of AI-Assistance in real-world scenarios.

LIVE ONLINE WORKSHOP

We will hands-on demonstrate the complete specification, design, verification and debug workflow of a 32-bit RISC-V implementing the RV32I+M ISA using the Magnus EDA AI-assistant, including:

1. Requirements Analysis
2. Micro Architecture
3. RTL Coding
4. Design Review
5. Test Bench Generation
6. Memory Model Generation
7. Assembly Test Programming
8. Simulation Set Up
9. Running Hello World!
10. Debug and Optimization

Contact us to schedule
No Cost
Limited to 5-10 participants per session

Contact:
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