MEMORY DESIGN AND TESTING

UE20EC333

PROJECT REPORT

Hands on Sessions on Memory Design

(Assignment 1)

Submitted from:

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Submitted To :

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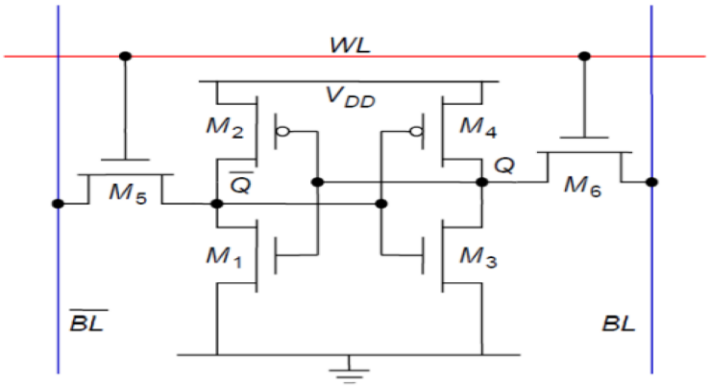
Introduction

6T static random-access memory is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance, but is still volatile in conventional

sense, that data is eventually lost when memory is not powered. This report works with design of 6T SRAM using Cadence Virtuoso.

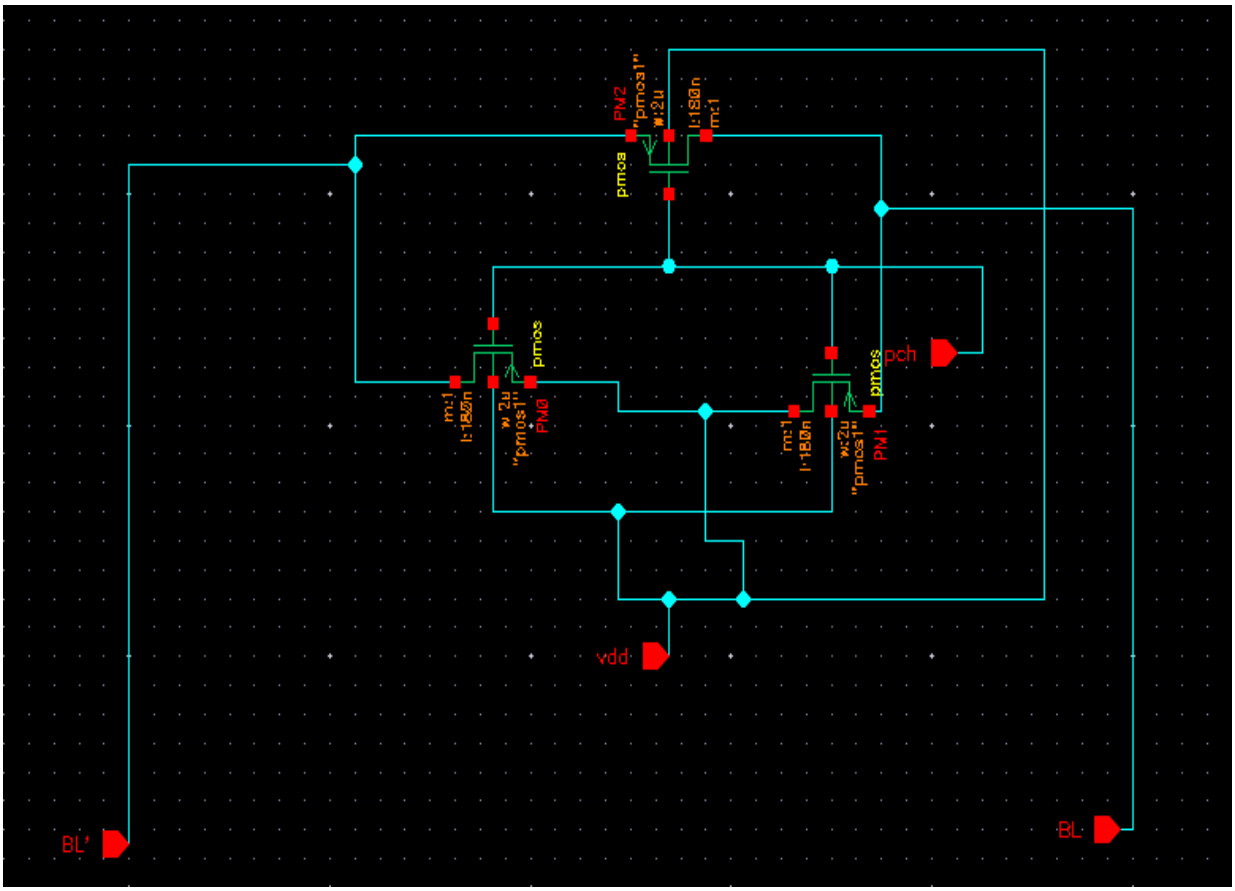
We have finally designed 4x4 memory array by below shown 6T sram

6T SRAM cell

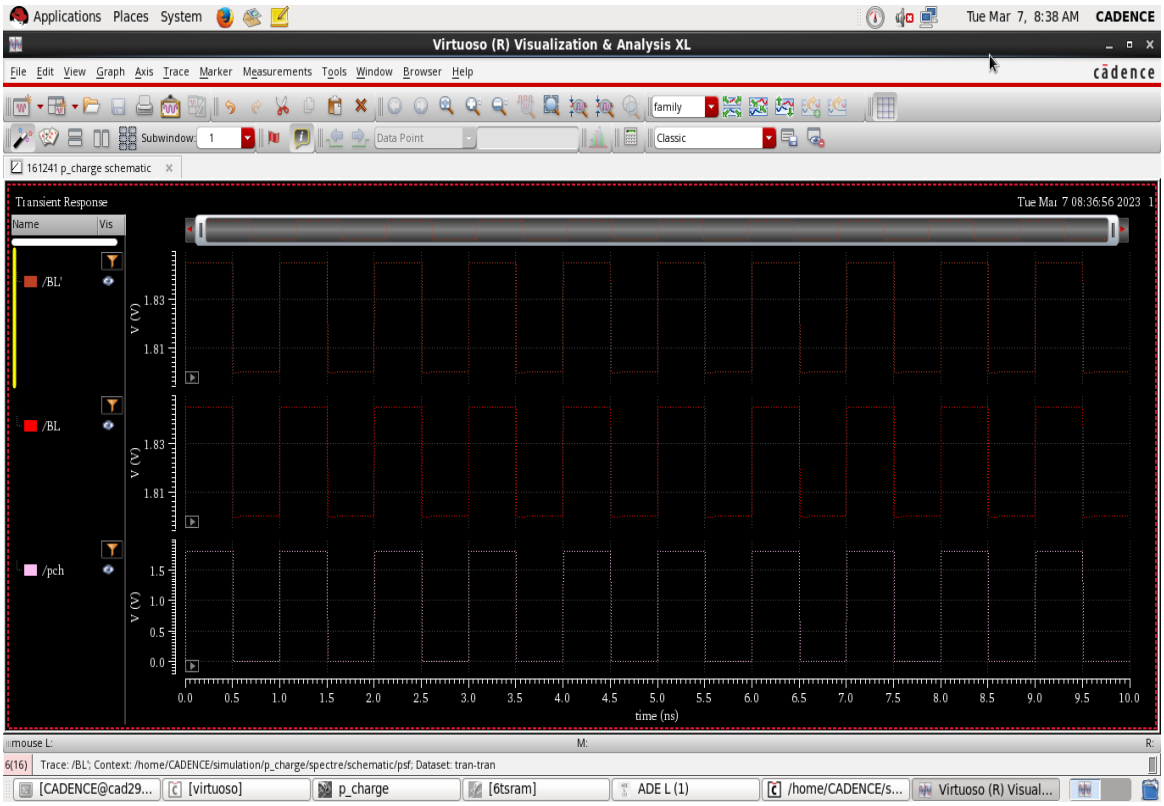


Implementation and Simulation Results

1. Design a pre-charge circuit to charge a BL and BL'th with capacitance of 120f in 0.5n Seconds.



Circuit diagram

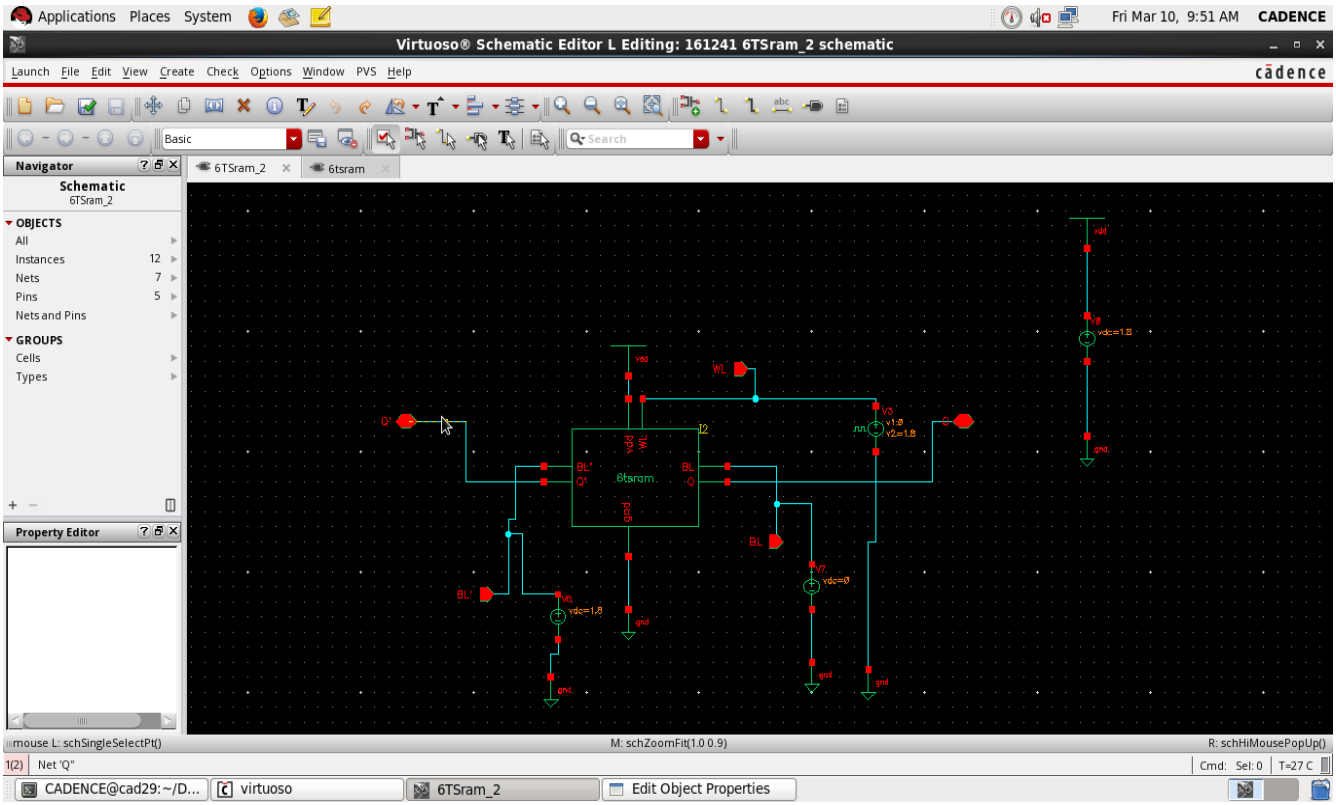


Timing analysis for pre-charge circuit

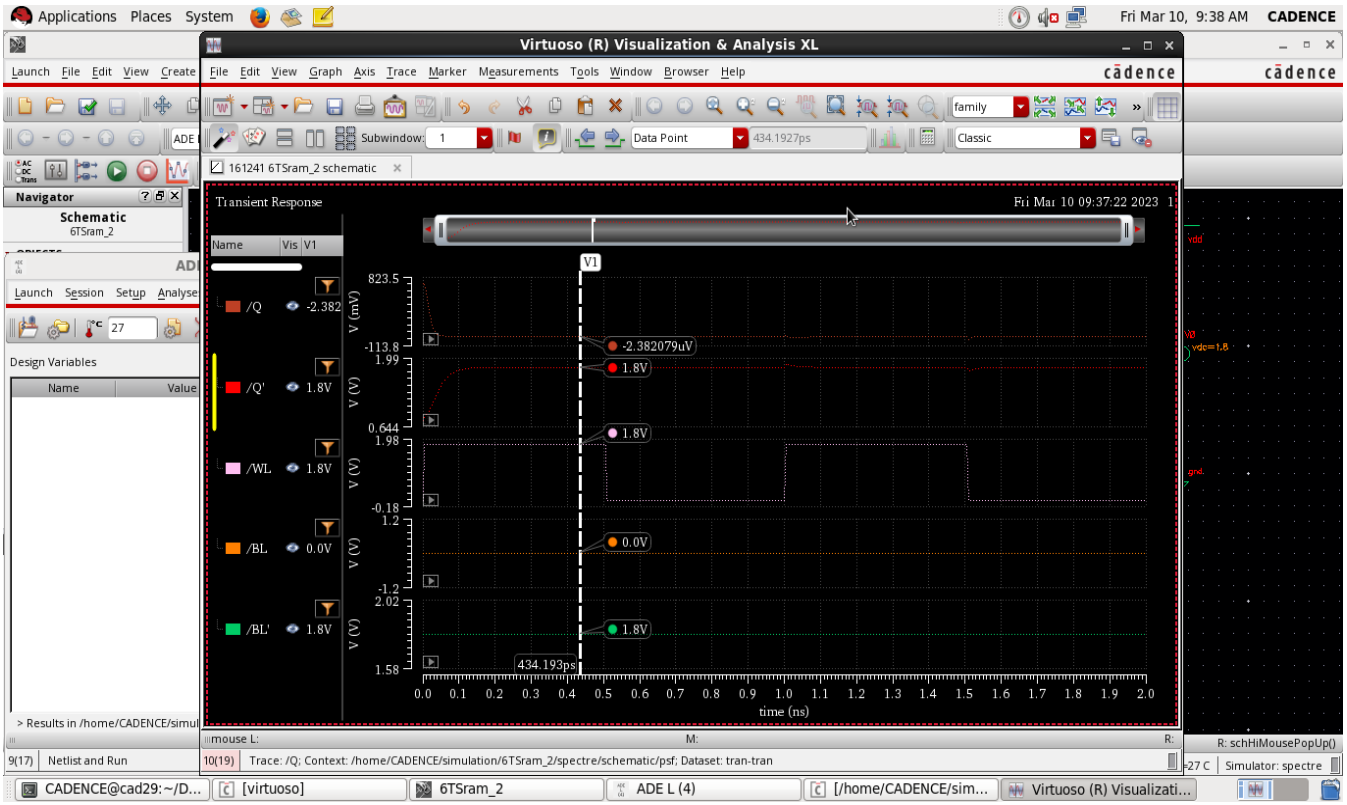
2. Implement a 6T SRAM with CR=1.25 and PR=0.85 using 180nm technology. Keep Length (L) of all devices minimum and Wp=400n. Verify
    a) Write '0' and Read '0' operation.
    b) Write '1' and Read '1' operation
    c) Draw butterfly curve and measure SNM for Hold state, Read state and Write state.

WRITE operation

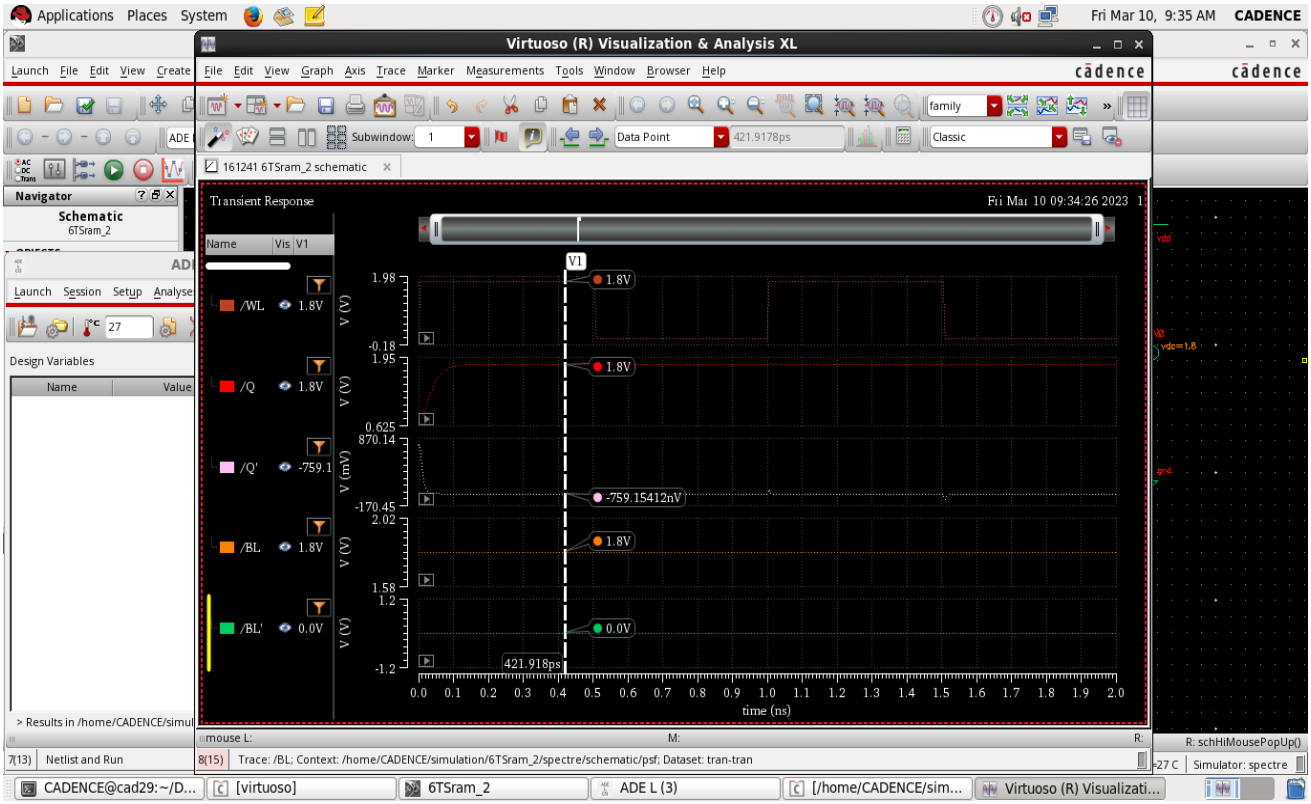
WL is made high. For write0: BL =0 and BL' = 1 and for write1: BL = 1 and BL' = 0. So corresponding access transistors are turned on and data is written as based on the operation(Q=0 or Q=1). For a successful write operation, access transistors should be stronger than the pull up transistors which is taken care by the pull-up ratio.



Timing diagram for Write ‘0’

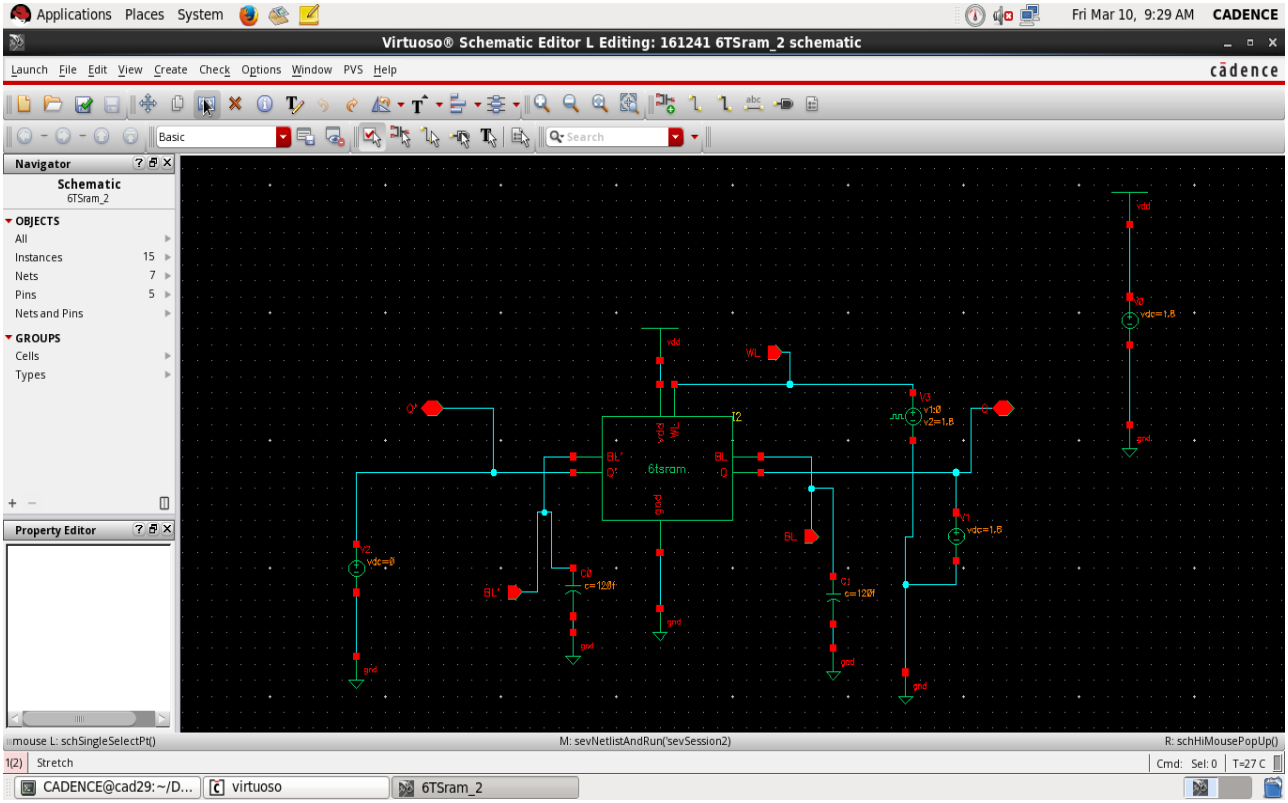


Timing diagram for Write ‘1’



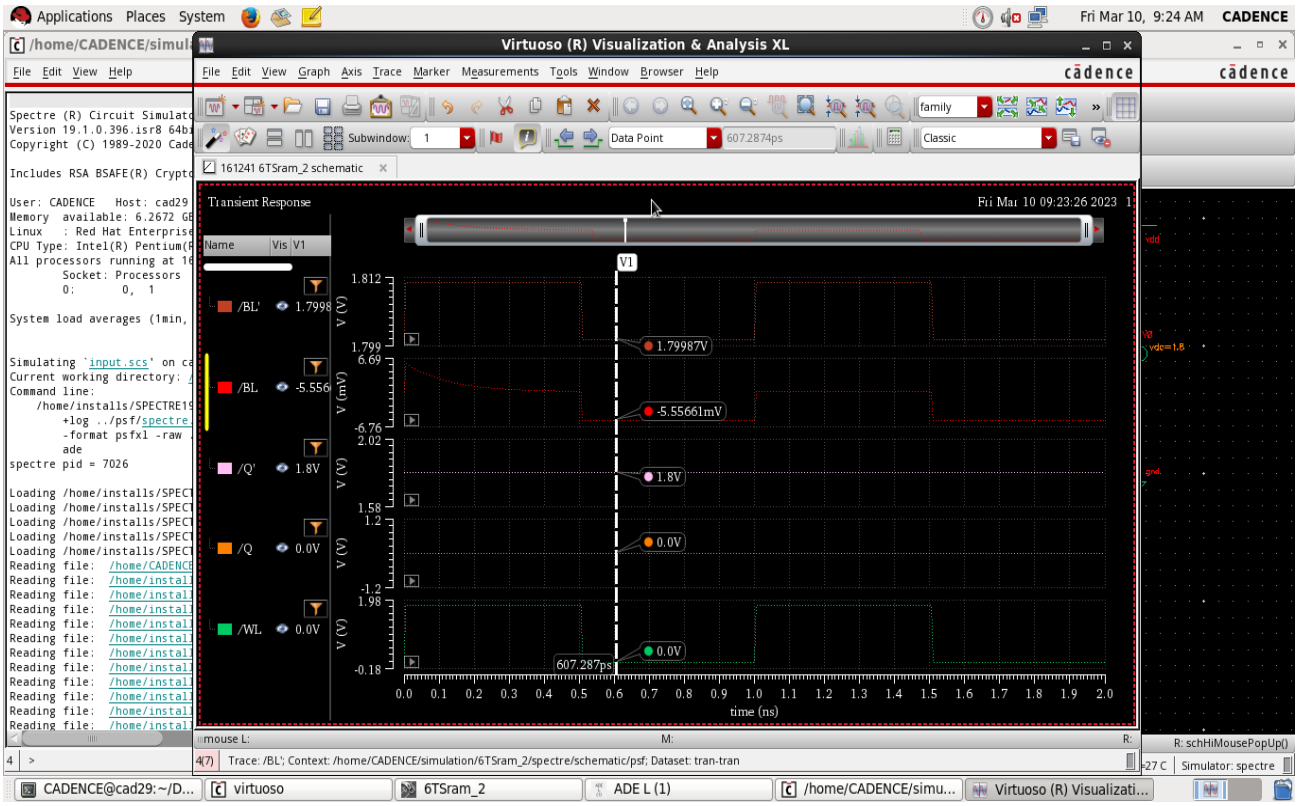
READ operation

During read operation WL is made high assuming the Cell already has been written with value ‘1’ and bit lines are precharged to VDD. Therefore we are trying to read 1), which which causes BL’ to discharge through series transistors and BL will remain in precharge state



Timing diagram for Read ‘1’

Timing diagram for Read ‘0’



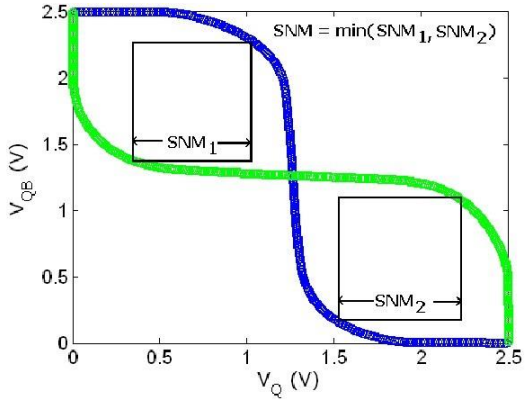
Stability of SRAM cell

Butterfly curve is used to determine the stability of SRM cell.

It is plotter by the VTC with respect to both Q and Q'

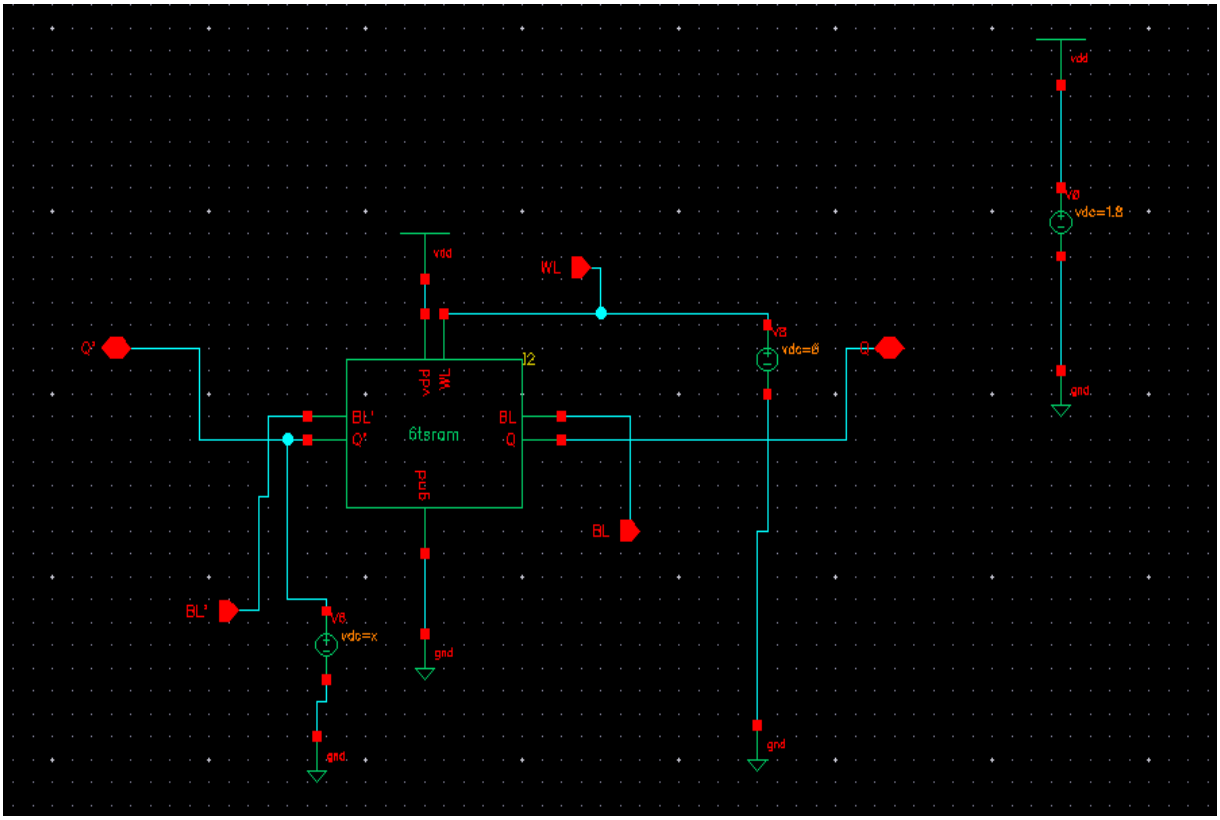
SNM(Signal Noise Margin) is determined using below diagram

SNM is determined for Hold and Read state of SRAM

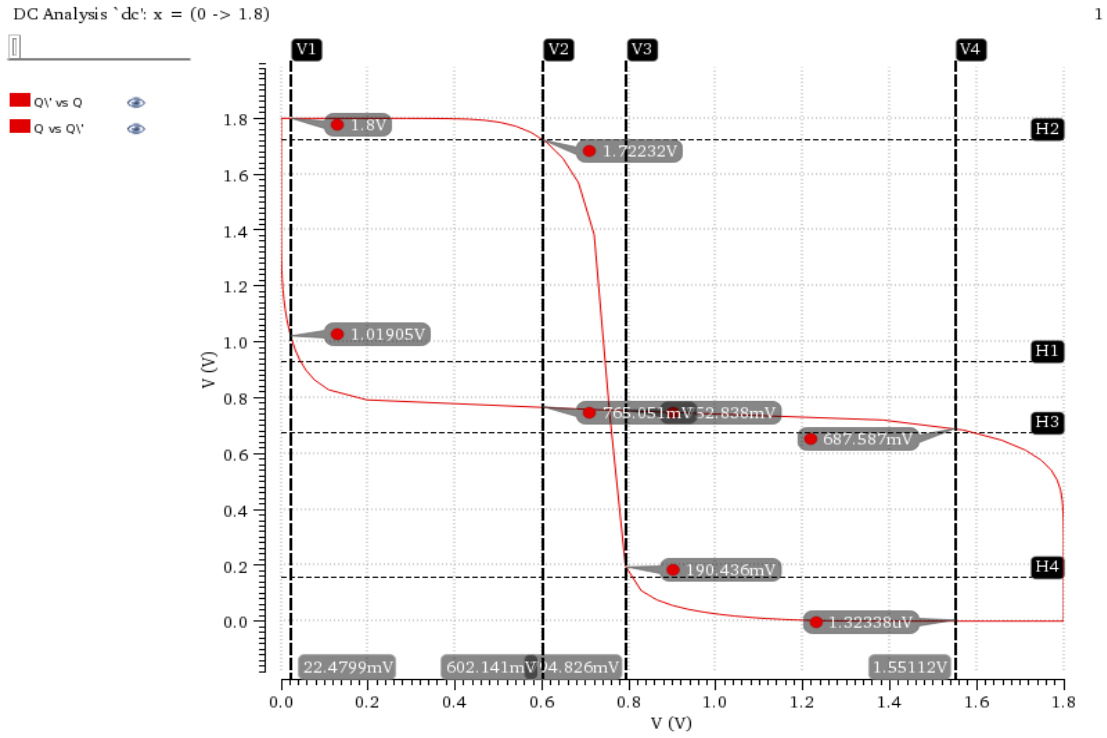


Butterfly curve for the SRAM cell

Hold state



Butterfly curve for Hold state



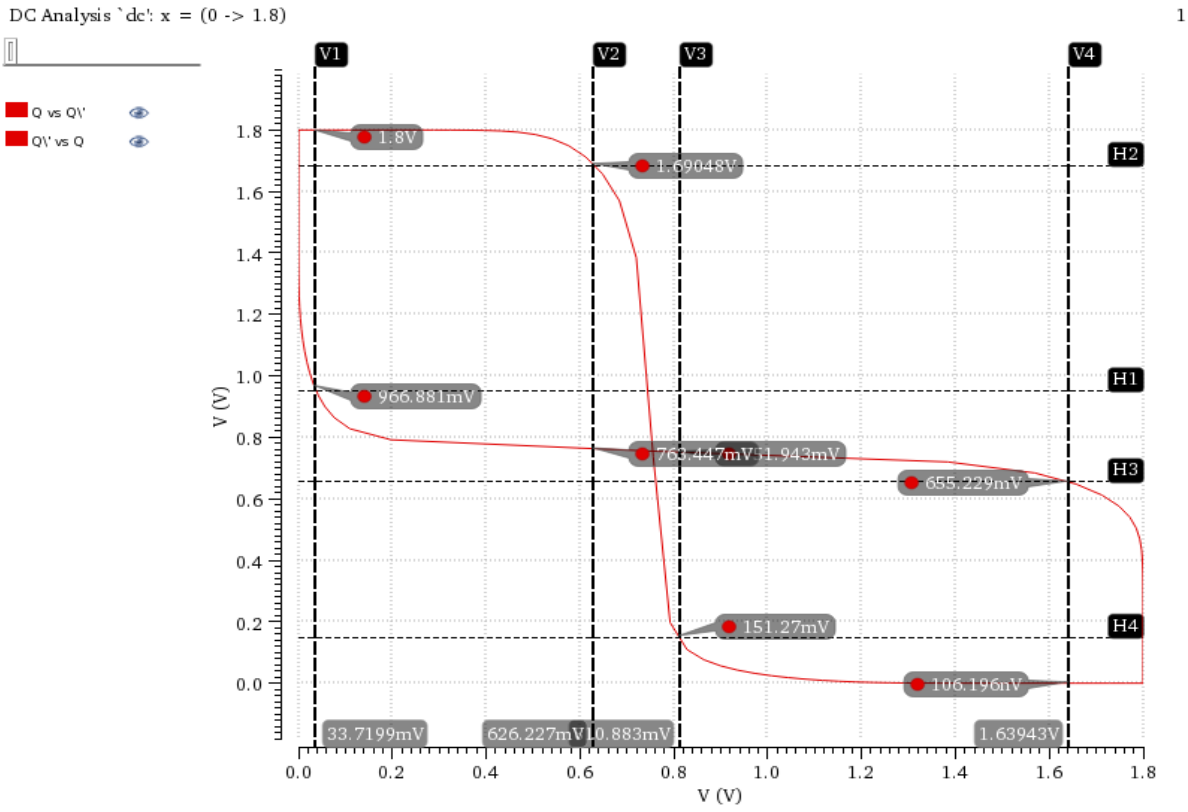
Hold state Static noise margin is expected to be maximum.

SNM = min (SNM1, SNM2)

= min(578.241,789.12)

= 578.241m

Butterfly curve for Read state



The stability reduces due to flattening of curve which is because of addition of noise to access transistor which are connected to BL and BL'

SNM = min (SNM1, SNM2)
= min (592.5,828.547)
= 592.5m

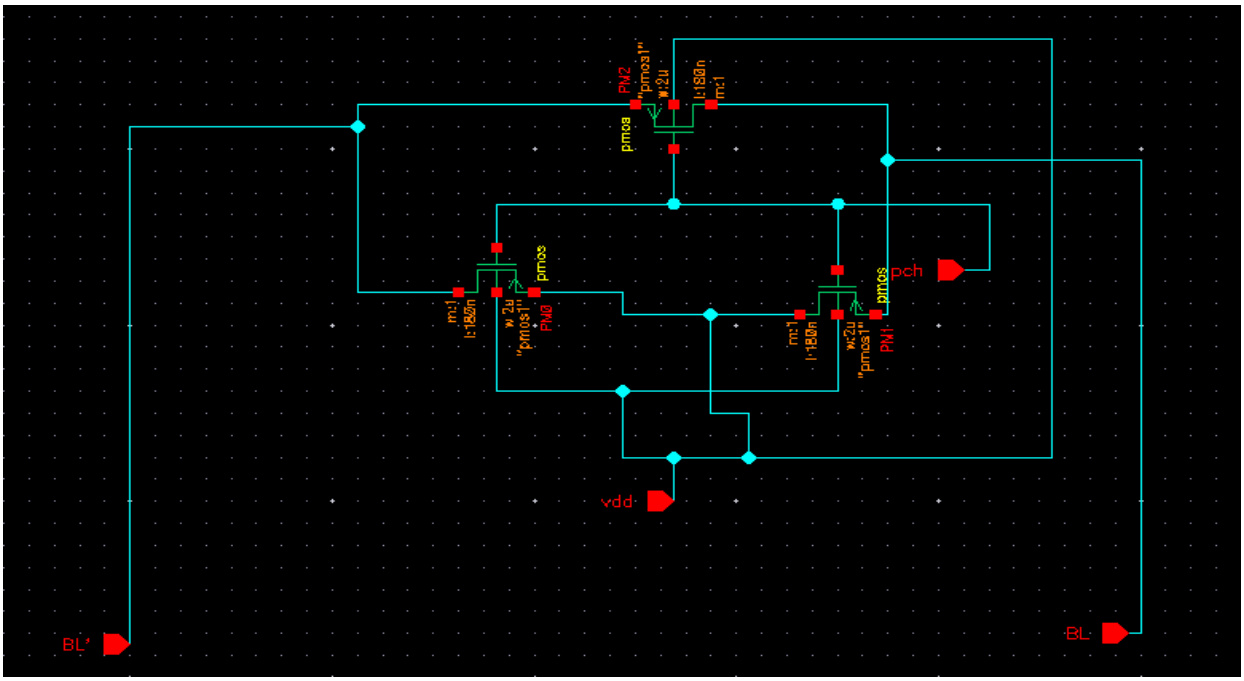
3. Draw a schematic of 6T SRAM and simulate for for read and write operation.

Length of all the MOS	180nm
Width of PMOS devices (Wp)	Minimum width
Access Tarnsistors Width (Wa)	1.2 x Wp
Pull down NMOS trasistors (Wn)	1.5 x Wn

To account for BL and BL' parasitic capacitance use a external capacitance of 120fF connected at BL and BL' terminals.

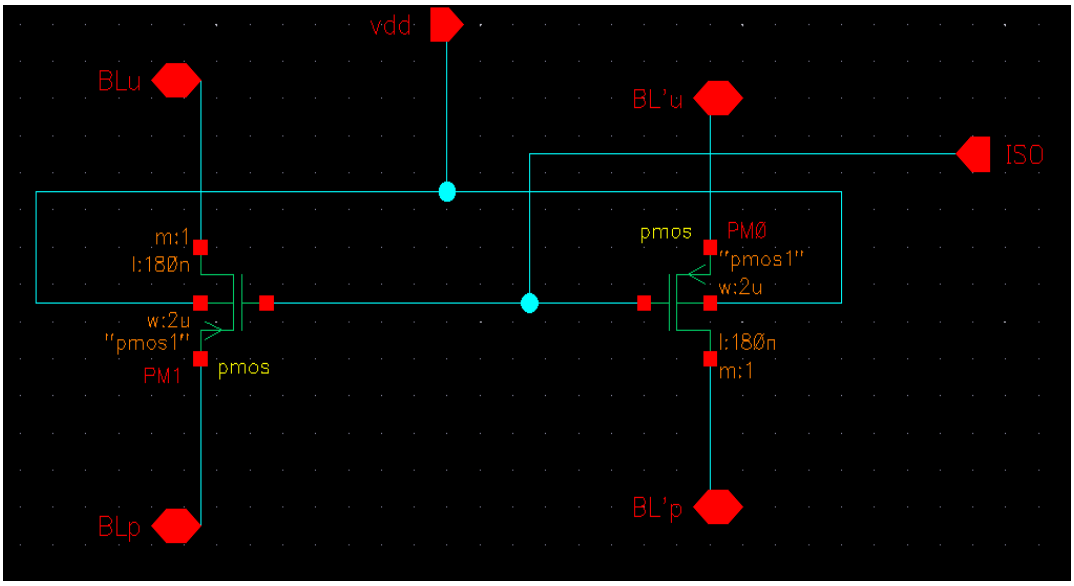
Pre-charge circuit

Pre- circuit is used to pre-charge the bit lines to Vdd before the Read operation. It consists of: a) Equalizer transistor which reduces the required pre-charge time by ensuring that both bit lines are at nearly equal voltages even if they are not pre-charged to Vdd. b) Bias transistors which pulls each of the bit lines to Vdd.



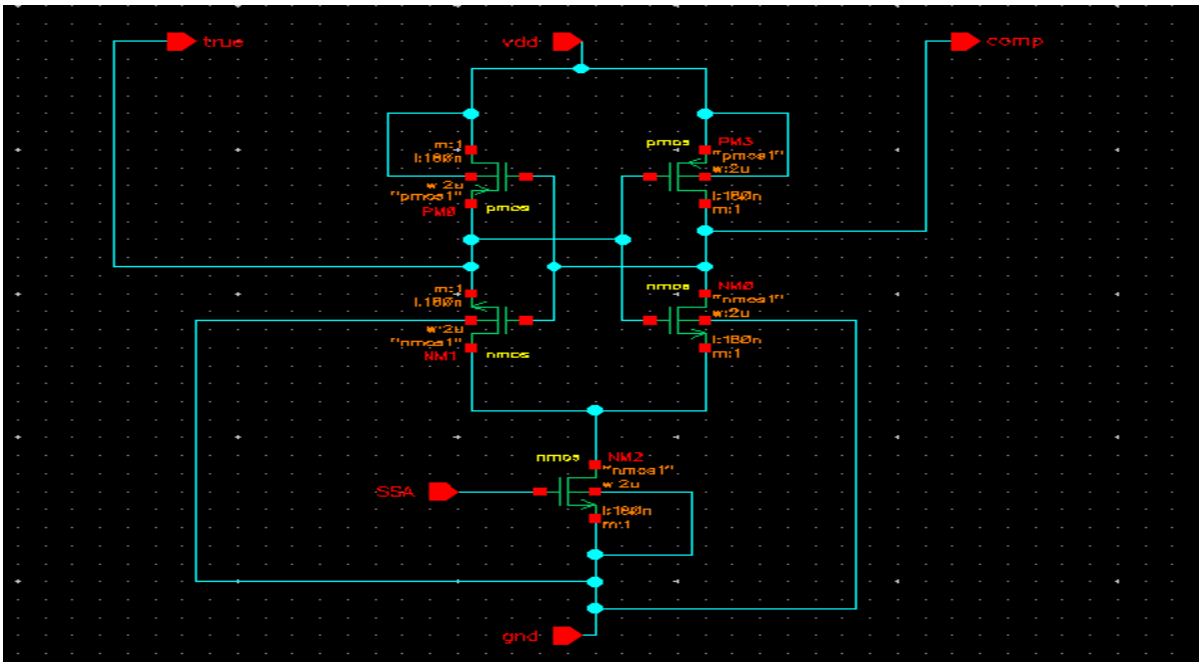
Isolation circuit

Isolation circuit is used to isolate the sense amplifier from the bit lines once a small change on the bit lines is detected.



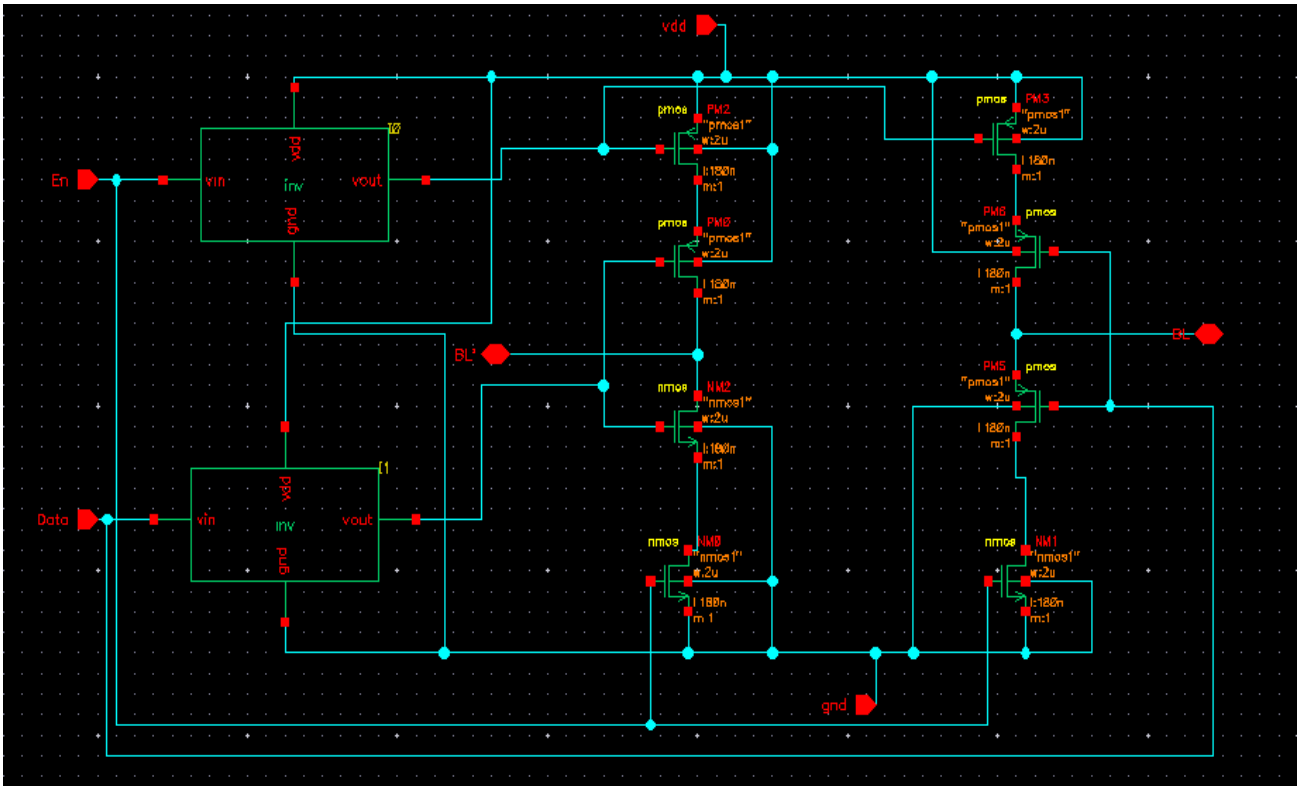
Sense Amplifier

The sense amplifier is responsible for detecting the value stored in the SRAM cell during the read operation and displaying that value at the output.

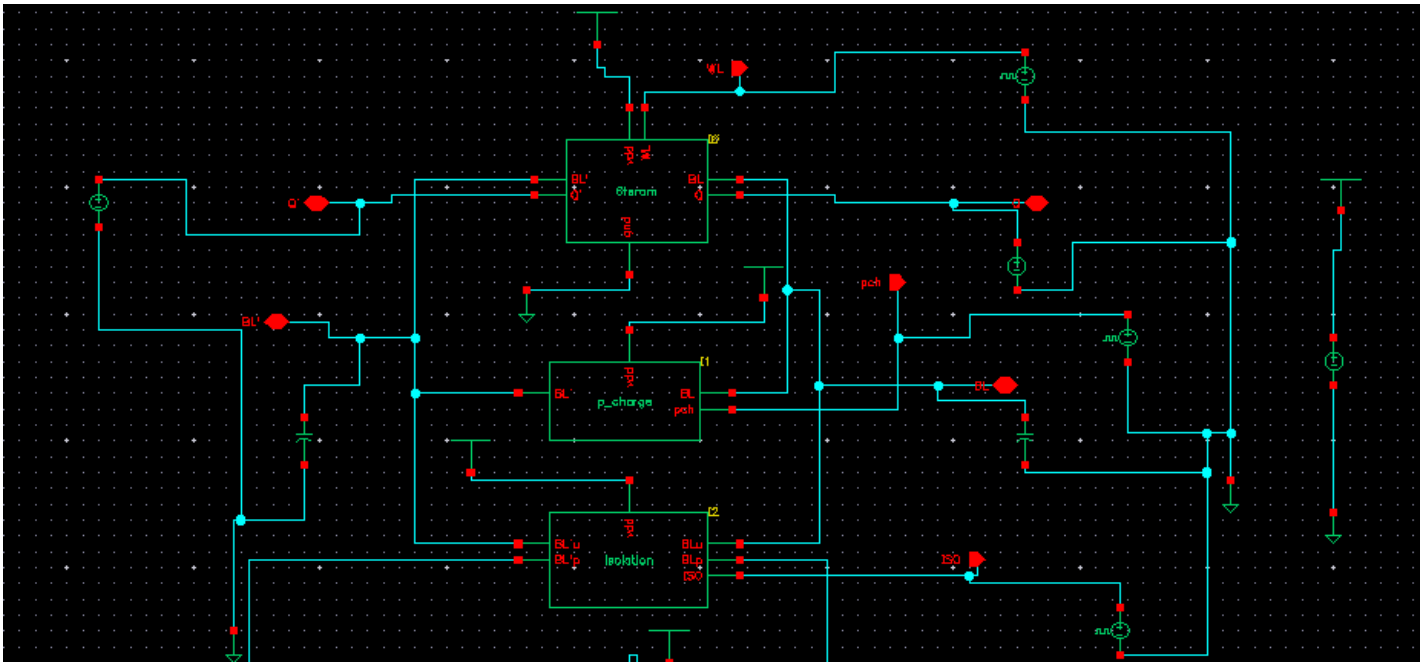


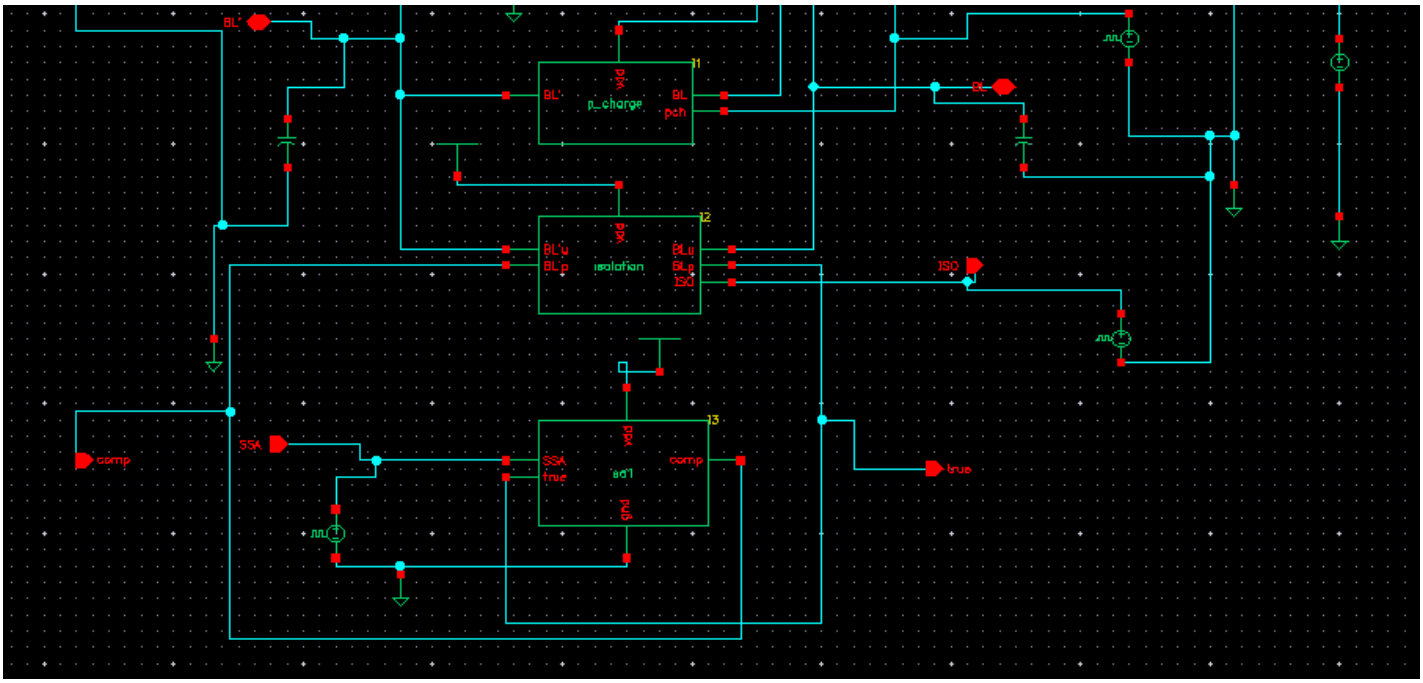
Write driver circuit

Write driver circuit is responsible to write the data onto the bit lines BL and BL’ during the write operation

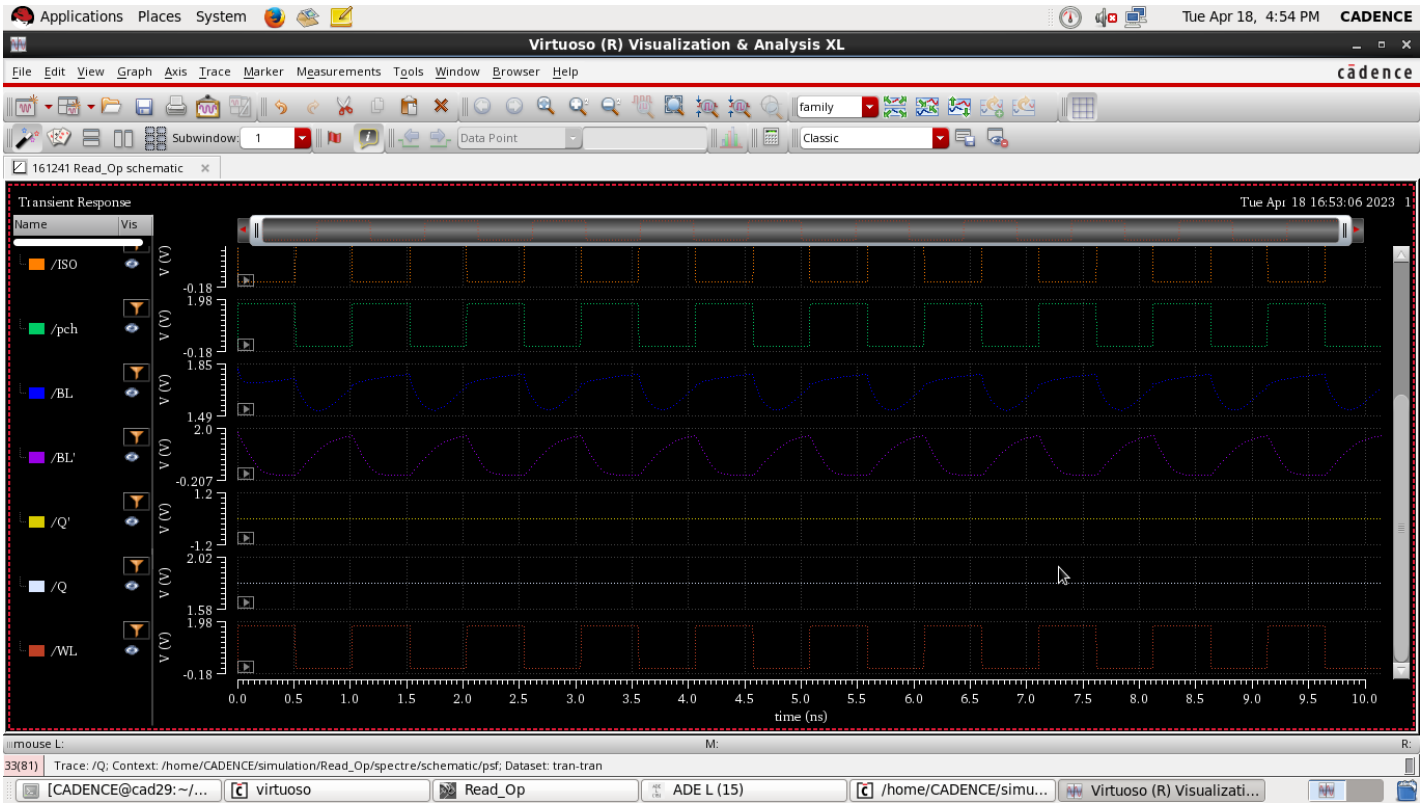


a. Read Operation (Read 1)



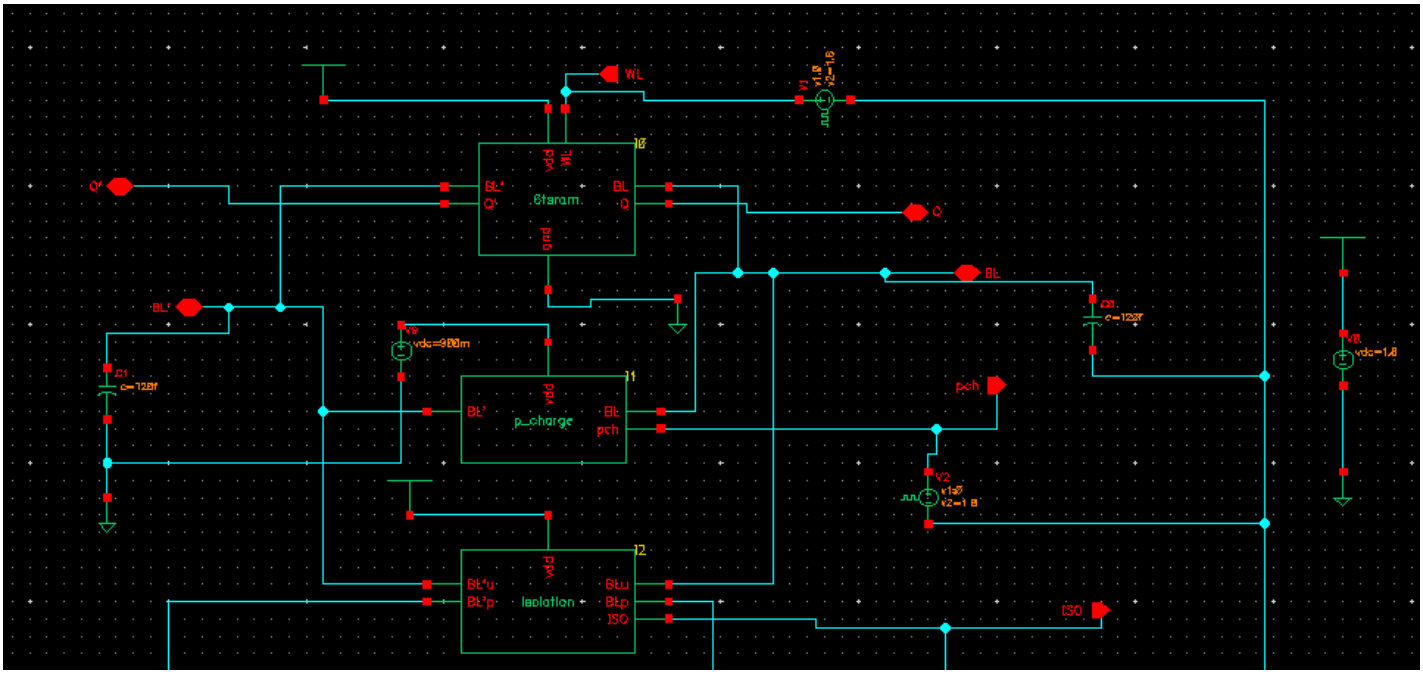


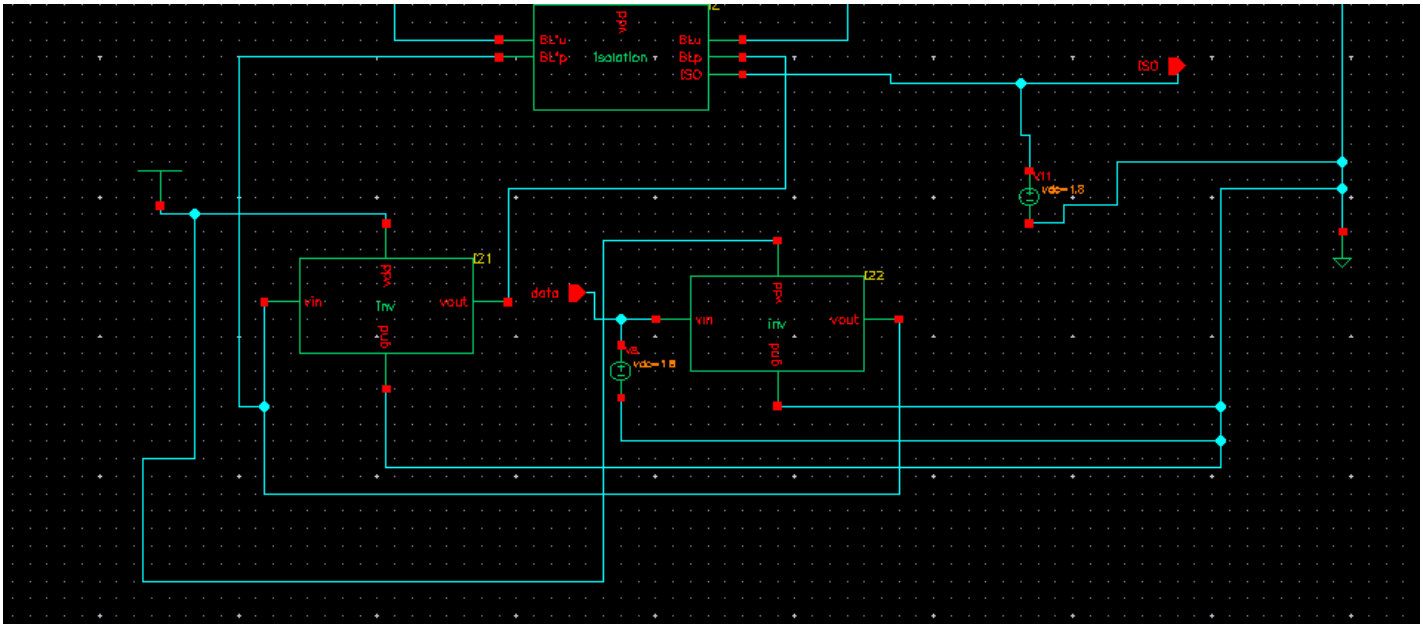
Timing diagram



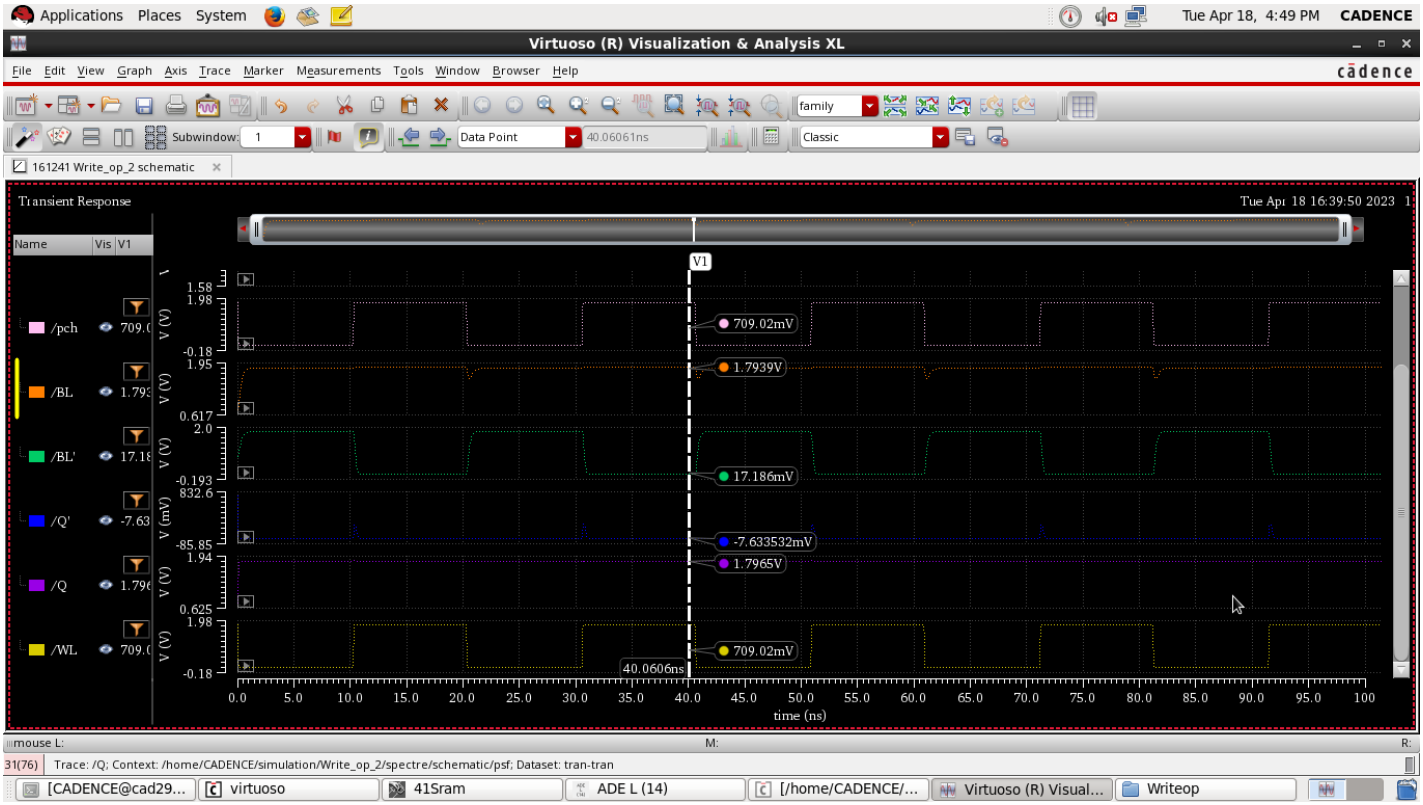
- WL = 0 , BLPC = 0 (Pre charge circuit is ON). The bit lines BL and BL’ are pre-charged
- WL = 1, BLPC = 1(Pre-charge circuit is OFF), ISO = 0 (Isolation circuit is ON).
- BL’ starts discharging. Once a small differential change in BL and BL’ is obtained,
- ISO = 1 : bit lines are isolated from sense amplifier
- SSA = 1: Sense amplifier is turned ON which then gives the output on True and Complement lines.
- Pre-charge circuit is turned ON (BLPC = 0) in-order to pre-charge the bit lines for the next cycle.

b. Write operation (Write 1)





Timing diagram



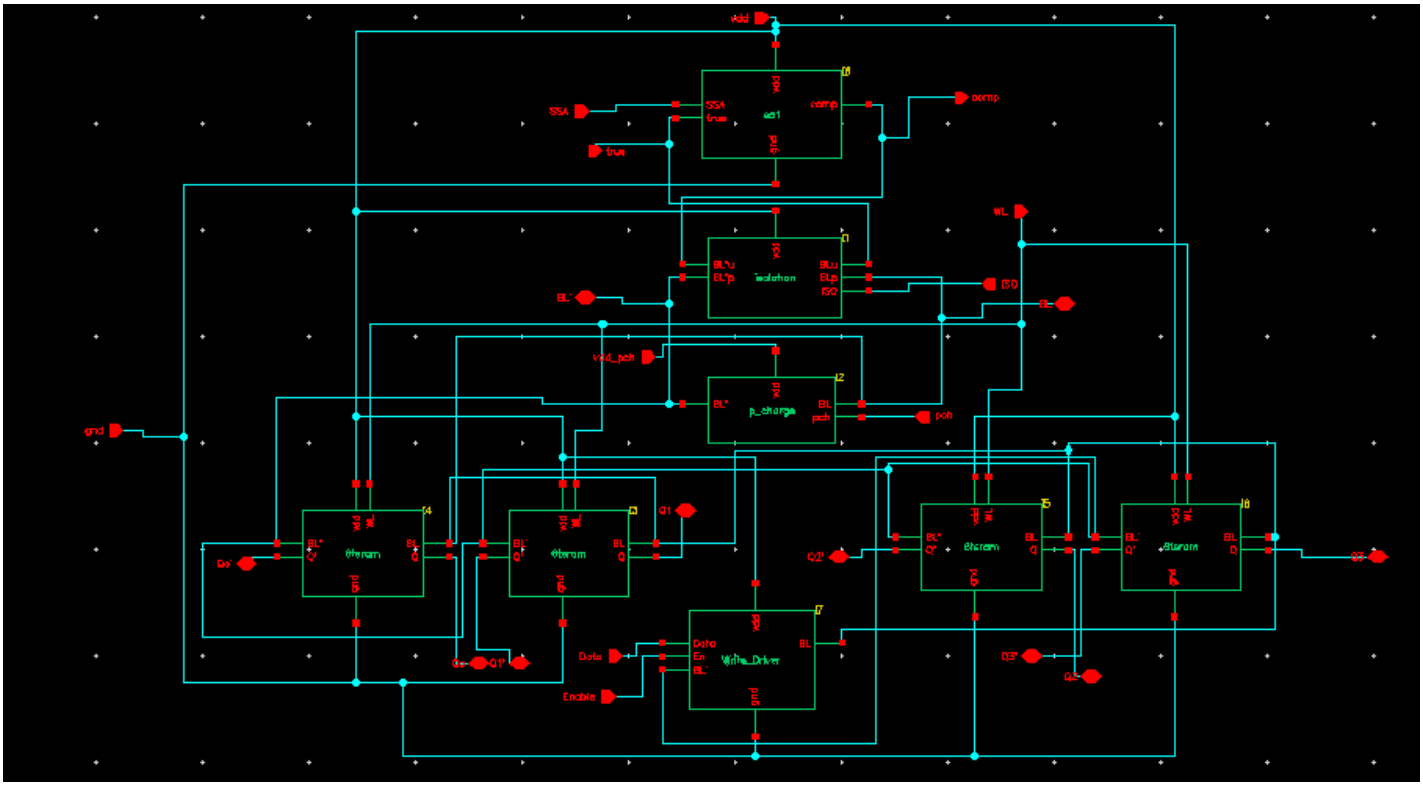
□ WL = 1, Data = 1. Therefore BL = 1 and BL' = 0. Hence data '1' is written to the cell (Q=1)

4. Finally, we have designed a 4X4 memory array and performed the write and read operation on a cell

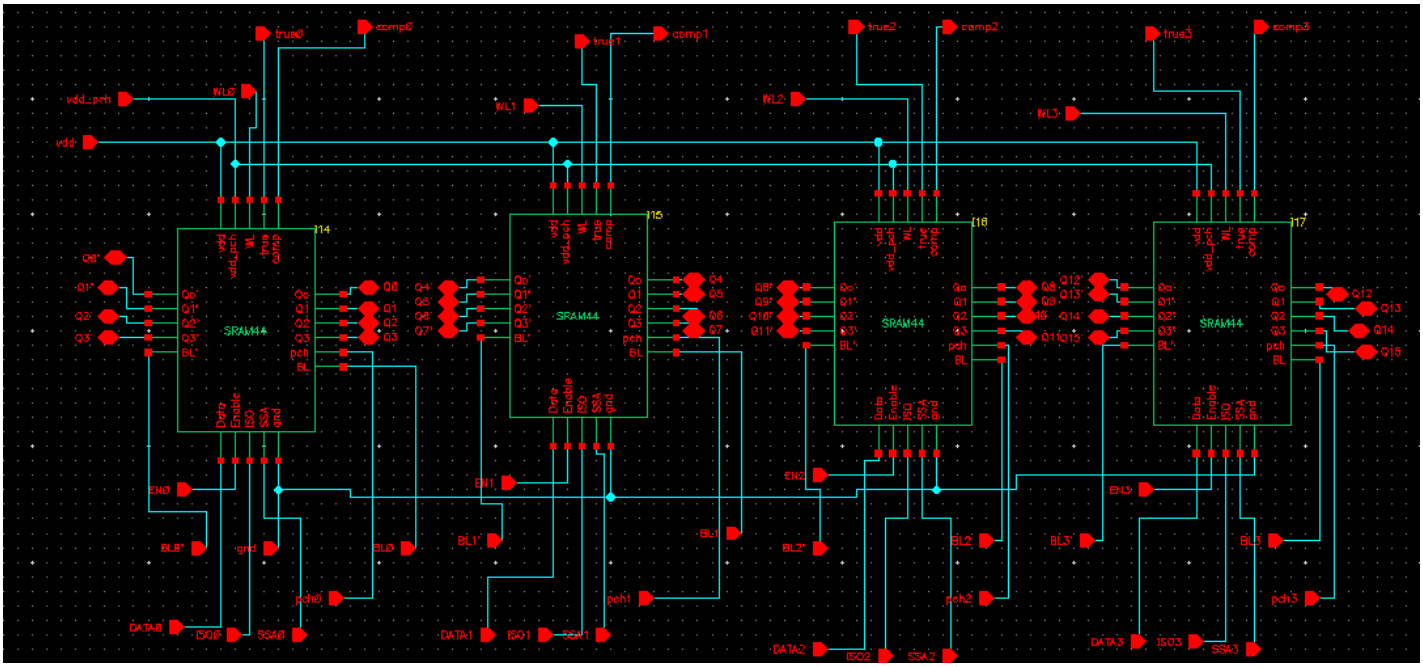
First we did 4x1 column which has one peripheral each and 4 6T Sram cells in parallel

Then we did 4x4 by placing 4x1 cells in series

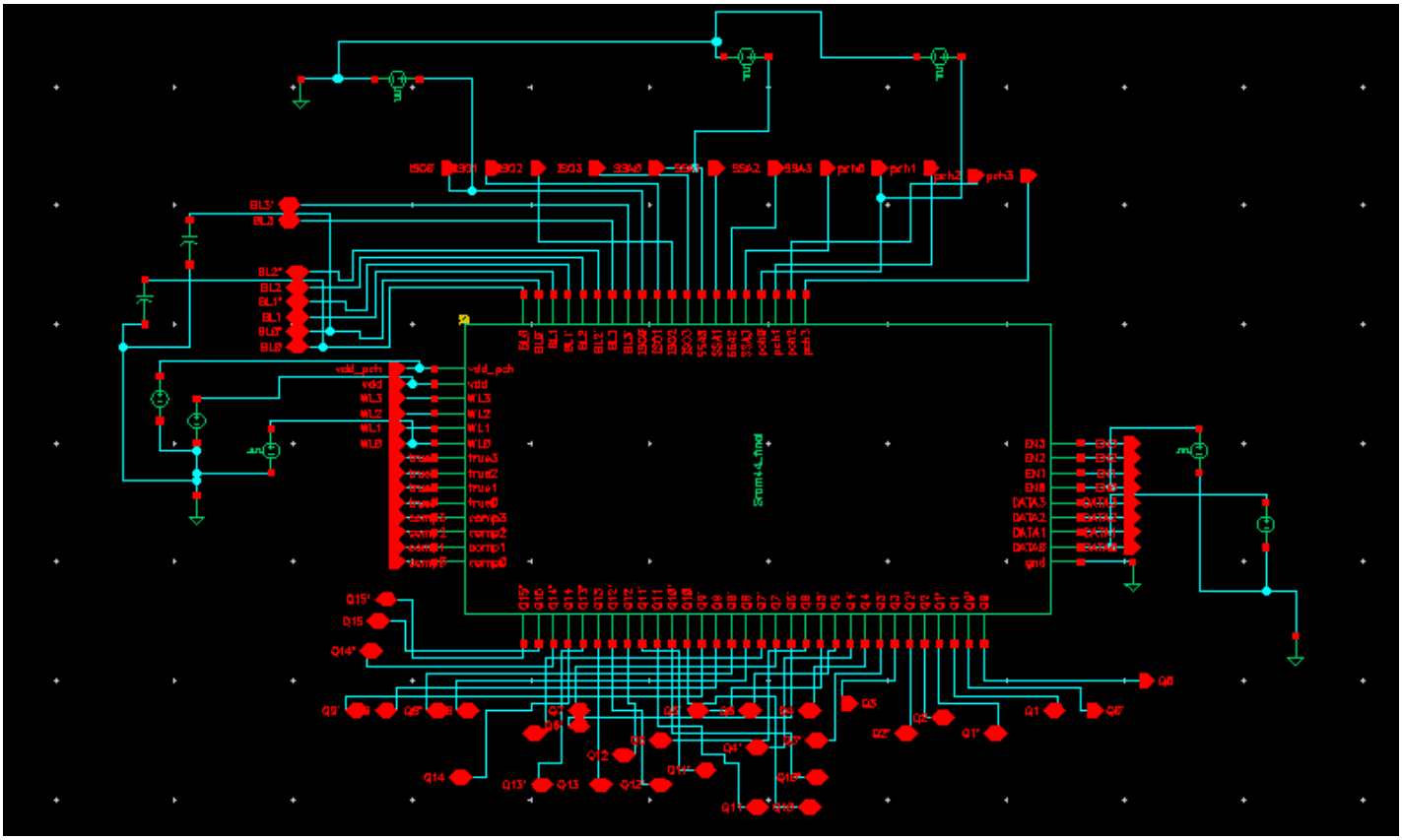
4X1 memory array



4X4 Memory Array

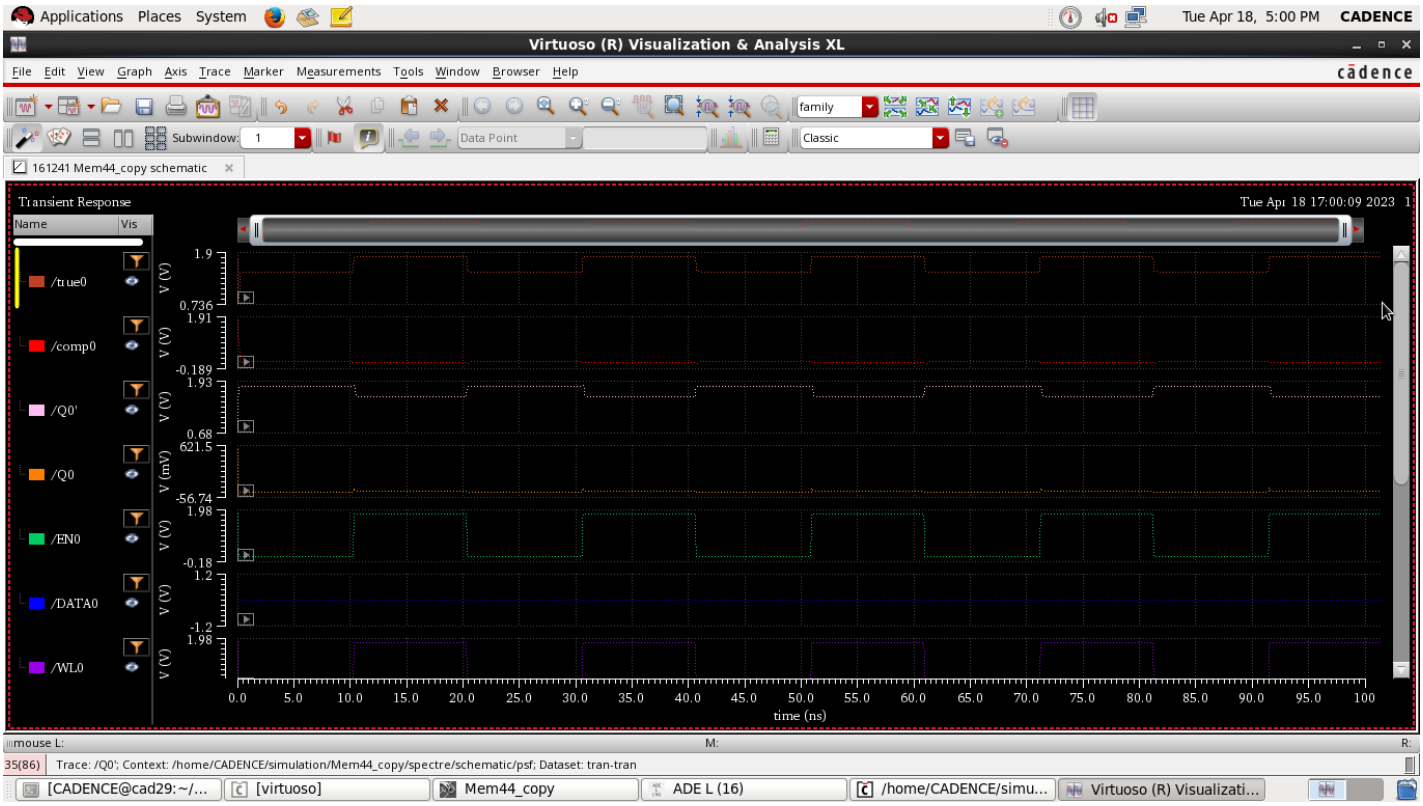


Test cell view for 4x4 Memory Array



Timing diagram

Write 0 followed by Read 0 from Cell 0



Write 1 and Read 1 from Cell 0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Conclusion

In our project

We have analyzed read and write operation of 6T Sram with and without peripherals (Precharge , Sense Amplifier ,Writedriver ,Isolation cell)

We have also saw SNM using Butterfly curve for Hold and Read State of 6T Sram

We have designed 4x4 Memory array of 6T Sram cells and analyzed read and write operation.