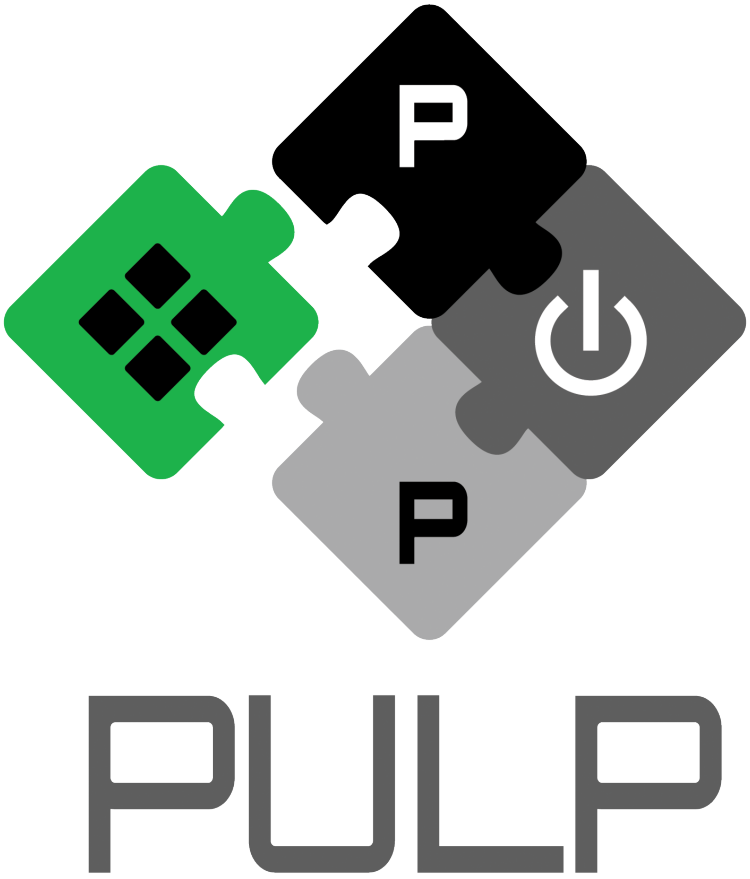
PULPissimo: Datasheet



The PULP team
pulp-info@list.ee.ethz.ch

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Contents

1 Overview

PULPissimo is a 32 bit RI5CY single-core System-on-a-Chip. PULPissimo is the second version of the PULPino system and it can be extended with the multi-core cluster of the PULP project.

Differently from the simpler PULPino system, PULPissimo uses a more complex memory subsystem, an autonoumous I/O subsystem which uses the uDMA, new peripherals (eg the camera interface) and a new SDK.

Figure 1.1 shows a simplified block diagram of the SoC. As for PULPino, PULPissimo can be configured at design time to use either the RISC-V or zero-riscy. The peripherals are connected to the uDMA which transfers the date to the memory subsystem efficiently. The JTAG and the AXI plug have also access to the SoC. The AXI plug can be used to extend the microcontroller with a multi-core cluster or an accelerator. As for PULPino, the advanced debug unit is used to access to system and core registers, memories and memory-mapped IO via JTAG. A logarithmic interconnect allows to link the core and the uDMA to the memory banks simultaneously.

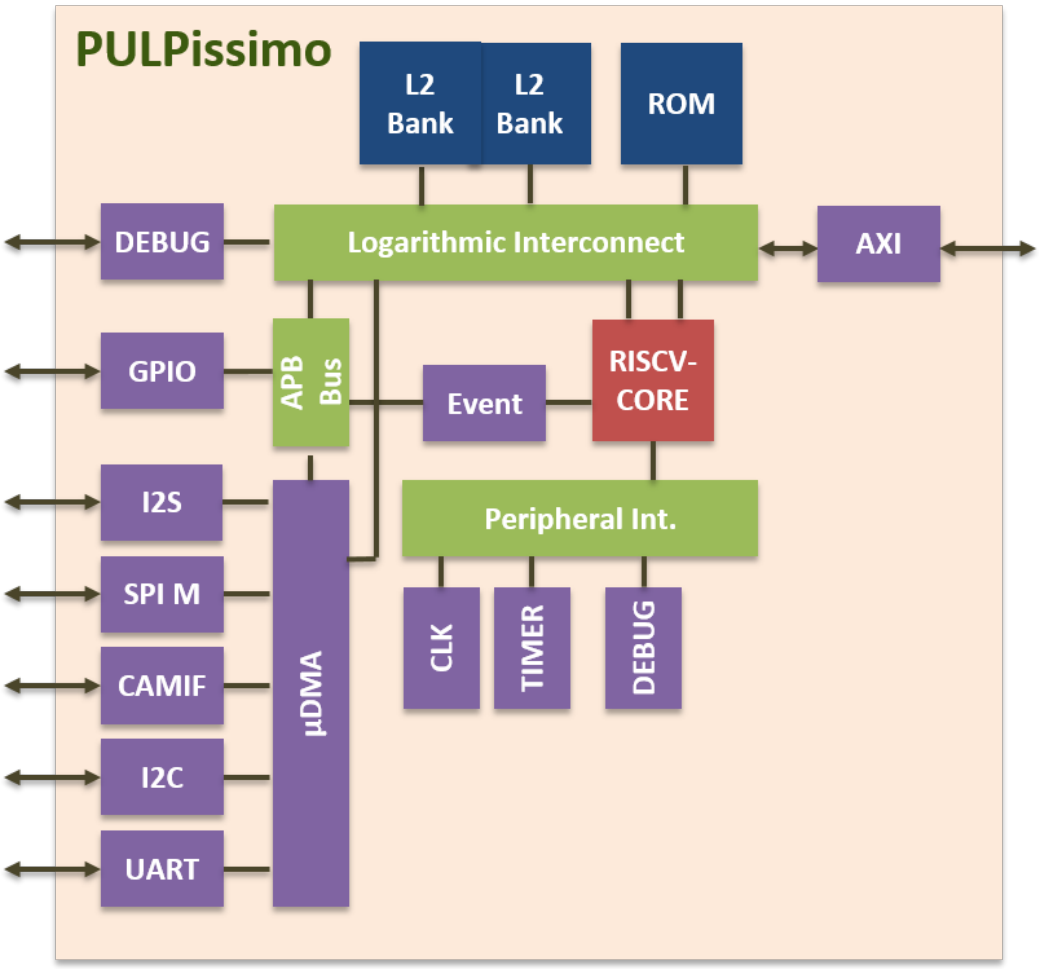


Figure 1.1: PULPissimo Overview.

PULPissimo is mainly targeted at RTL simulation and ASICs. The FPGA versions has not yet been implemented.

2 Memory Map

Figure 2.1 shows the default memory-map of PULPissimo, whereas Please, consult the uDMA documentation for the peripherals attached to the uDMA memory-map of configuration.

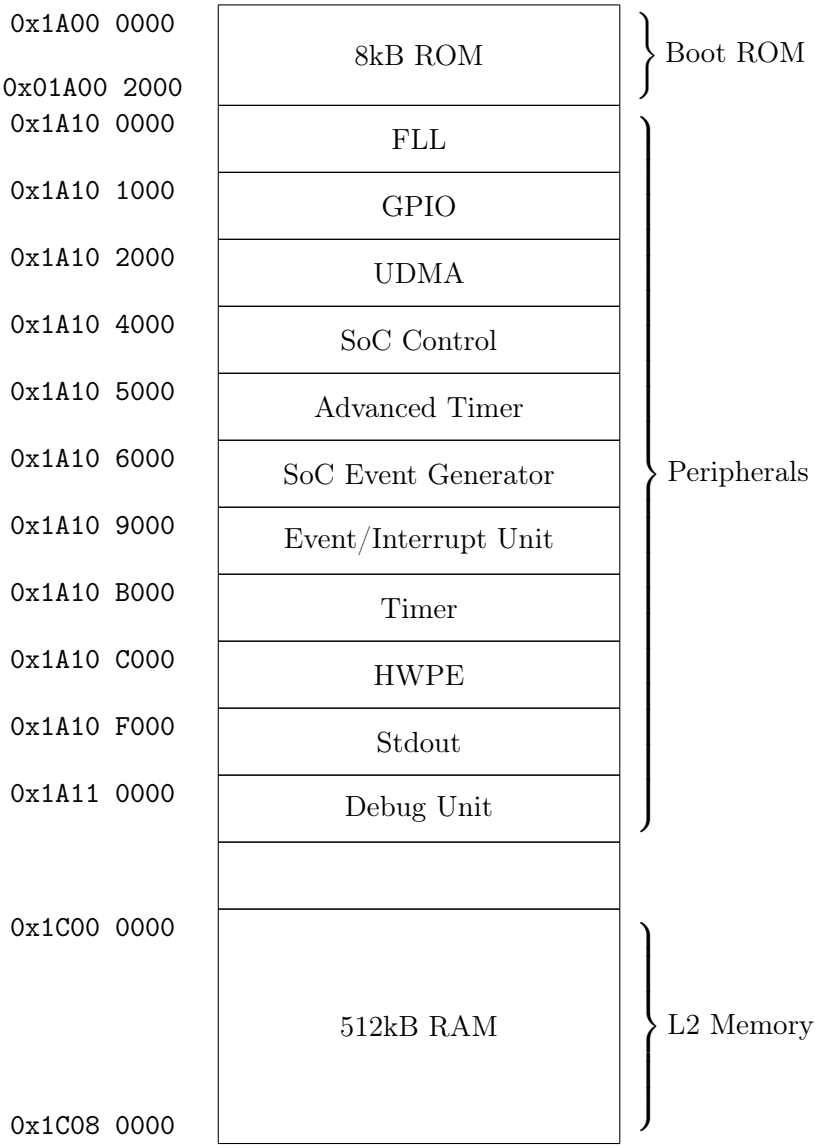


Figure 2.1: PULPissimo memory-map.

3 CPU Core

PULPissimo supports both the RISC-V and the zero-riscy RI5CY core. The two cores have the same external interfaces and are thus plug-compatible. Figure 3.1 and 3.2 show the two cores architectures.

For debugging purposes, all core registers have been memory mapped which allows to them to be accessed over the logaritmic-interconnect subsystem. The debug unit inside the core handles the request over this bus and reads/sets the core registers and/or halts the core.

The core supports performance counters. Those are mainly used for counting core internal events like stalls, but it is possible to count core-external events as well. For this purpose there is the `ext_perf_counters_i` port where arbitrary events can be attached. The core then increases its internal performance counter for this event type every time a logic high is seen on this port.

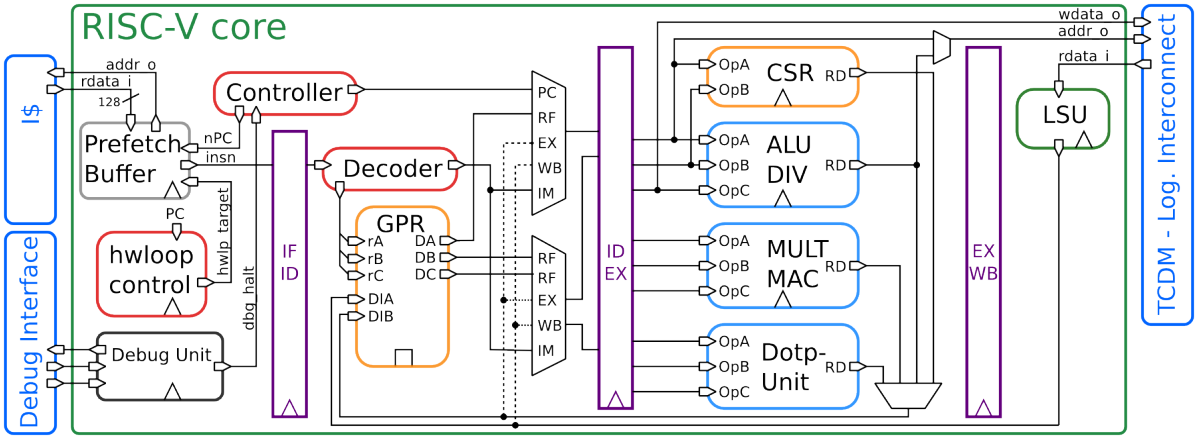


Figure 3.1: RISCY core overview

Take a look at the cores documentation for more details.

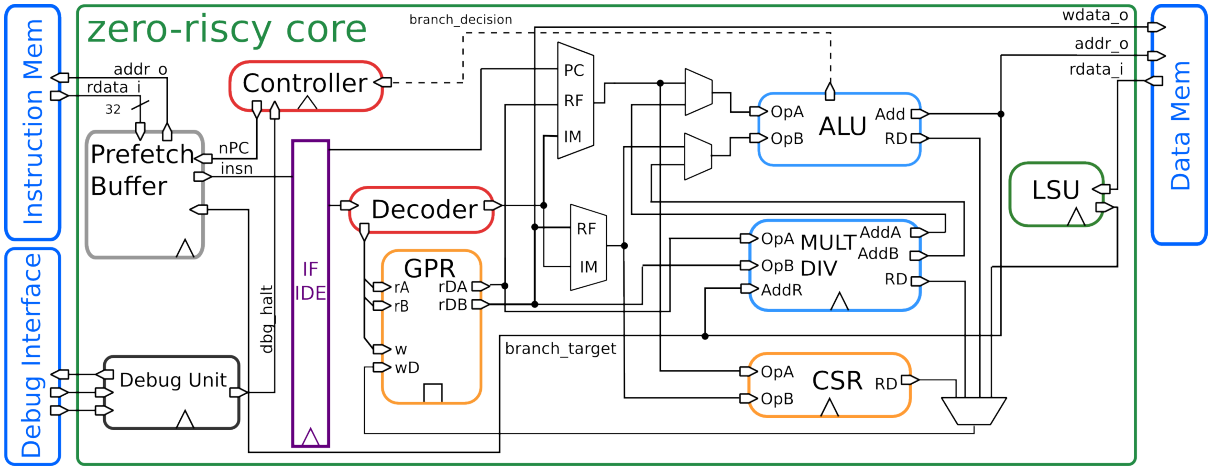


Figure 3.2: zero-riscy core overview

4 Peripherals

Most of the peripherals in PULPissimo are connected to the uDMA subsystem which efficiently handles all the data-transfers autonoumsly. The uDMA must be programmed by the core via memory-mapped read and write operations to receive commands.

See the uDMA documentation for more details under the uDMA repository.

The GPIO, timers, event unit and event generator, debug and the FLLs are not connected to the uDMA instead but to the APB bus. Following a brief overview about these units is given.

4.1 FLL

PULPissimo containts 3 FLLs. One FLL is meant for generating the clock for the peripheral domain, one for the core domain (core, memories, event unit etc) and one is meant for the cluster. The latter is not used.

All the FLLs can be bypassed by writing to the JTAG register before the reset signal is asserted. See Section 4.3 for more details about the bypass register.

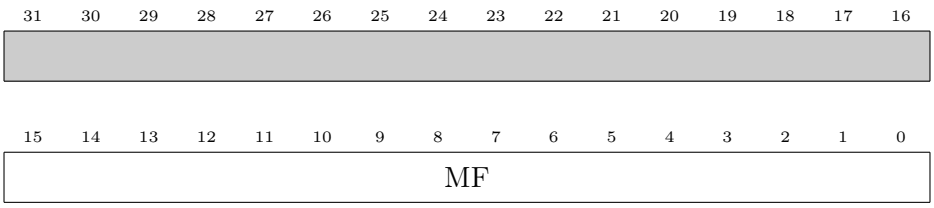
4.1.1 SoC FLL registers

Name	Address	Size	Type	Access	Default	Description
STATUS	0x1A100000	32	Status	R	0x00000000	FLL status register
CFG1	0x1A100004	32	Config	R/W	0x00000000	FLL configuration 1 register
CFG2	0x1A100008	32	Config	R/W	0x00000000	FLL configuration 2 register
INTEG	0x1A10000C	32	Config	R/W	0x00000000	FLL integrator configuration register.

Table 4.2: SoC FLL register table

4.1.2 STATUS

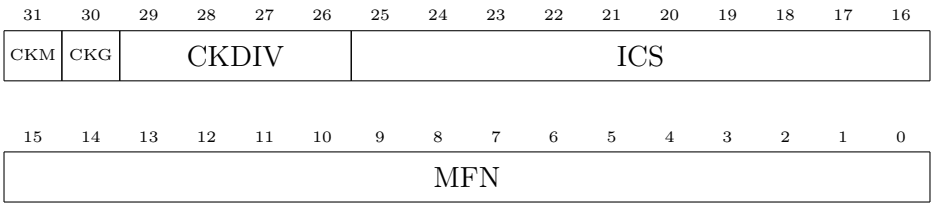
Address: 0x1A10_0000
Reset Value: 0x0000_0000



Bit 15-0 **MF** *(R)* Current DCO multiplication factor value bitfield

4.1.3 CFG1

Address: 0x1A10_0004
Reset Value: 0x0000_0000



`Bit 31` **CKM** *(R/W)* FLL operation mode configuration bitfield

- 0b0: standalone
- 0b1: normal

`Bit 30` **CKG** *(R/W)* FLL output clock divider configuration

- 0b0: not gated
- 0b1: gated

`Bit 29-26` **CKDIV** *(R/W)* FLL output clock divider configuration

`Bit 25-16` **ICS** *(R/W)* DCO input code in standalone

`Bit 15-0` **MFN** *(R/W)* Target clock multiplication factor in normal mode

4.1.4 CFG2

Address: `0x1A10_0008`
Reset Value: `0x0000_0000`

`Bit 31` **DITH** *(R/W)* Dithering activation

`Bit 30` **CKM** *(R/W)* Open loop when locked

- 0b0: disabled
- 0b1: enabled

`Bit 29` **CKSEL** *(R/W)* Configuration clock selection in standalone mode

- 0b0: DCO clock
- 0b1: Reference clock

`Bit 27-16` **LT** *(R/W)* Lock tolerance configuration. It is the margin around the multiplication factor within which the output clock is considered stable.

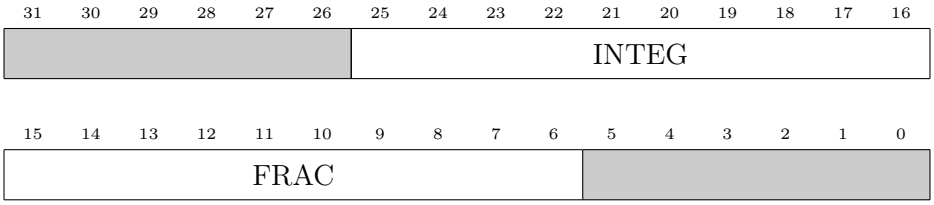
`Bit 15-10` **SCKL** *(R/W)* Number of stable REFCLK cycles until LOCK assert in normal mode. Uppper 6 bits of LOCK assert counter target in standalone mode.

`Bit 9-4` **UCKL** *(R/W)* Number of unstable REFCLK cycles until LOCK de-assert in normal mode. Lower 6 bits of LOCK assert counter target in standalone mode.

`Bit 3-0` **LG** *(R/W)* FLL loop gain setting

4.1.5 INTEG

Address: 0x1A10_000C
Reset Value: 0x0000_0000



Bit 25-16 **INTEG** *(R/W)* Integer part of integrator state bitfield. It corresponds to DCO unit bits.

Bit 15-6 **FRAC** *(R/W)* Fractional part of integrator state bitfield. It corresponds to dither unit input.

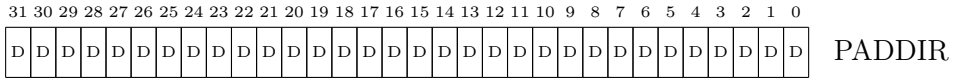
4.2 GPIO

Table 4.3: GPIO Signals

Signal	Direction	Description
`gpio_in[31:0]`	**input**	Transmit Data
`gpio_out[31:0]`	**output**	Receive Data
`gpio_dir[31:0]`	**output**	Request to Send
`gpio_padcfg[5:0][31:0]`	**output**	Pad Configuration
`interrupt`	**output**	Interrupt (Rise or Fall or Level)

4.2.1 PADDIR (Pad Direction)

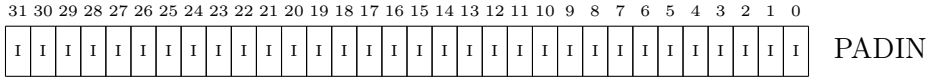
Address: `0x1A10_1000`
Reset Value: `0x0000_0000`



`Bit 31:0` **PADDIR**: Pad Direction.
Control the direction of each of the GPIO pads. A value of `1` means it is configured as an output, while `0` configures it as an input.

4.2.2 PADIN (Input Values)

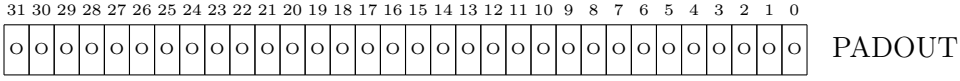
Address: `0x1A10_1004`
Reset Value: `0x0000_0000`



`Bit 31:0` **PADIN**: Input Values.

4.2.3 PADOUT (Output Values)

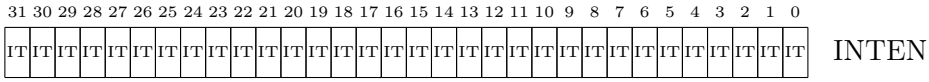
Address: `0x1A10_1008`
Reset Value: `0x0000_0000`



`Bit 31:0` **PADOUT**: Output Values.

4.2.4 INTEN (Interrupt Enable)

Address: `0x1A10_100C`
Reset Value: `0x0000_0000`



`Bit 31:0` **INTEN**: Interrupt Enable.
Interrupt enable per input bit. INTTYPE0 and INTTYPE1 control the interrupt triggering behavior.

There are four triggers available

- `INTTYPE0 = 0, INTTYPE1 = 0`: Level 1
- `INTTYPE0 = 1, INTTYPE1 = 0`: Level 0
- `INTTYPE0 = 0, INTTYPE1 = 1`: Rise
- `INTTYPE0 = 1, INTTYPE1 = 1`: Fall

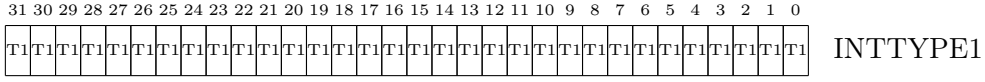
4.2.5 INTTYPE0 (Interrupt Type 0)

Address: `0x1A10_1010`
Reset Value: `0x0000_0000`

`Bit 31:0` **INTTYPE0**: Interrupt Type 0.
Controls the interrupt trigger behavior together with INTTYPE1. Use INTEN to enable interrupts first.

4.2.6 INTTYPE1 (Interrupt Type 1)

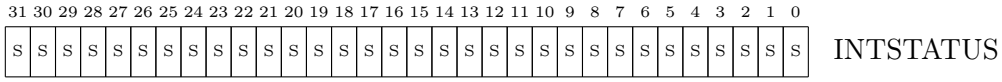
Address: `0x1A10_1014`
Reset Value: `0x0000_0000`



`Bit 31:0` **INTTYPE1**: Interrupt Type 1.
Controls the interrupt trigger behavior together with INTTYPE0. Use INTEN to enable interrupts first.

4.2.7 INTSTATUS (Interrupt Status)

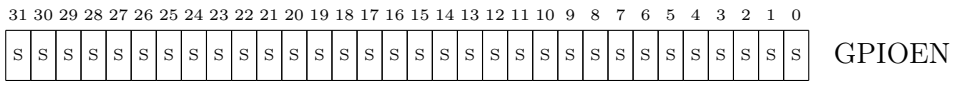
Address: `0x1A10_1018`
Reset Value: `0x0000_0000`



`Bit 31:0` **INTSTATUS**: Interrupt Status.
Contains interrupt status per GPIO line. The status register is cleared when read. Similarly the `interrupt` line is high while a bit is set in interrupt status and will be deasserted when the status register is read.

4.2.8 GPIOEN (GPIO Enable)

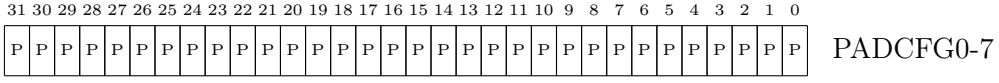
Address: `0x1A10_101C`
Reset Value: `0x0000_0000`



`Bit 31:0` **GPIOEN**: GPIO Enable.
Contains the enable bit per GPIO line.

4.2.9 PADCFG0-7 (Pad Configuration Registers 0-7)

Address: `0x1A10_1020 - 0x1A10_103C`
Reset Value: `0x0000_0000`



`Bit 31:0` **PADCFG0-7**: Pad Configuration Registers.
The pad configuration registers control various aspects of the pads that are typically used in ASICs, e.g. drive strength, Schmitt-Triggers, Slew Rate, etc. Since those configuration parameters depend on the exact pads used, each implementation is free to use the PADCFG0-7 registers in every way it wants and also leave them unconnected, if unneeded.

Writing to the PADOUTSET address (0x1A10_1040), the content of the PADOUT register is updated with its content "ored" with the write data.

Writing to the PADOUTCLR address (0x1A10_1044), the content of the PADOUT register is updated with its content "anded" with the inverted write data.

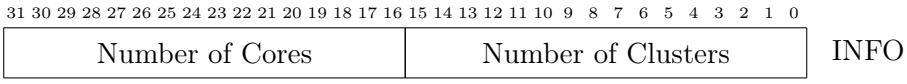
4.3 SoC Control

PULPissimo features a small and simple APB peripheral which provides information about the platform and provides the means for pad muxing on the ASIC.

The following registers can be accessed.

4.3.1 Info

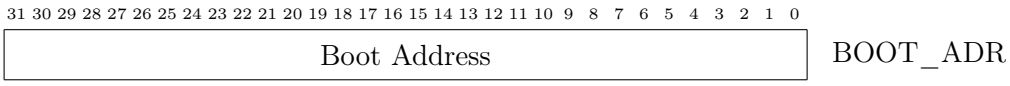
Address: `0x1A10_4000`
Reset Value: `0x0000_0000`



`Bit 31:0` **Info**: This register holds the number of clusters and the number of cores in the each cluster. It is a read-only register.

4.3.2 Boot Address

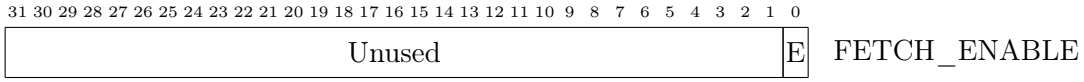
Address: `0x1A10_4004`
Reset Value: `0x1A10_0000`



`Bit 31:0` **Boot Address**: This register holds the boot address.

4.3.3 Fetch Enable

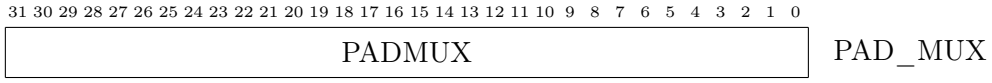
Address: `0x1A10_4008`
Reset Value: `0x0000_0001`



`Bit 31:0` **Fetch Enable**: This register contains the value of the fetch enable signal of the core.

4.3.4 PAD Mux

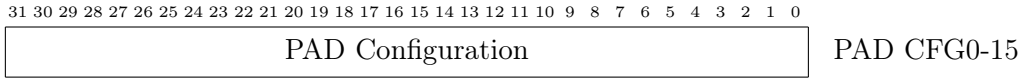
Address: `0x1A10_4010 - 0x1A10_401C`
Reset Value: `0x0000_0000`



`Bit 31:0` **PADMUX**: The content of these registers can be used to multiplex pads when targeting an ASIC. The first register (0x1A10_4010) can be used to sets the mux (2 bit select) from pin 0 (bits [1:0]) to 15 (bits [31:30]). The second register (0x1A10_4014) can be used to sets the mux (2 bit select) from pin 16 (bits [1:0]) to 31 (bits [31:30]). The third register (0x1A10_4018) can be used to sets the mux (2 bit select) from pin 32 (bits [1:0]) to 47 (bits [31:30]). The forth register (0x1A10_401C) can be used to sets the mux (2 bit select) from pin 48 (bits [1:0]) to 63 (bits [31:30]).

4.3.5 PAD Configuration

Address: `0x1A10_4020 - 0x1A10_405C`
Reset Value: `0x0000_0000`



`Bit 31:0` **PAD CFG0-15**: These 16 registers can be used for ASIC targets to configure pads, e.g. pull up, pull down values.

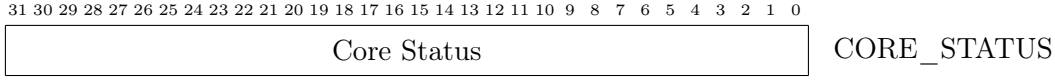
4.3.6 JTAG Register

Address: `0x1A10_4074`
Reset Value: `0x0000_0000`

`Bit 31:0` **JTAG Register**: This register contains the value of the input from the JTAG and can be used to write 8bit in the JTAG output register for system-to-JTAG communications.

4.3.7 Core Status

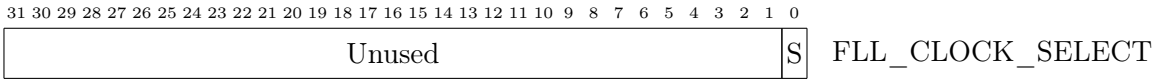
Address: `0x1A10_40A0 and 0x1A10_40C0`
Reset Value: `0x0000_0001`



`Bit 31:0` **Core Status**: These 2 registers contain the status of the system for testing/verification purposes like End Of Computation. The 0x1A10_40C0 register is read-only.

4.3.8 FLL Clock Select

Address: `0x1A10_40C8`
Reset Value: `0x0000_0000`



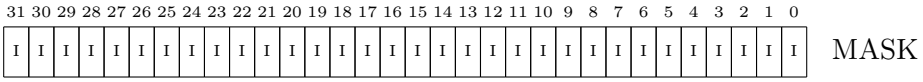
`Bit 31:0` **FLL Clock Select**: This register contains whether the system clock is coming from the FLL or the FLL is bypassed. It is a read-only register by the core but it can be written via JTAG.

4.4 Event/Interrupt Controller

PULPissimo features a lightweight event and interrupt controller which supports vectorized interrupts and events of up to 32 lines. It contains a FIFO of events from the peripherals or SW events. When an interrupt is ready and it is enabled (not masked), the unit sends the 5-bit ID to the core and the interrupt request line is raised up. If the core takes the interrupt, it replies with the ID of the interrupt taken and the acknowledge signal. The communication between the interrupt controller and the core is completly asynchronous. Note that the interrupt controller can change the interrupt ID anytime but it must rely on the ID sent by the core to know which interrupt has been taken. This is an important feature that covers the situation where a higher priority interrupt request prevent another one that has been already sent to the core. Depending on the core state and core interrupt enable, the interrupt can be accepted within a couple of clock cycles.

4.4.1 Mask

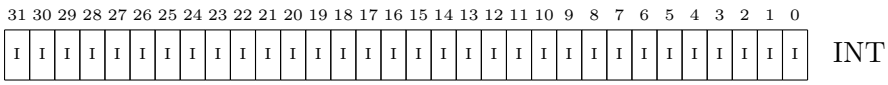
Address: `0x1A10_9000`
Reset Value: `0x0000_0000`



`Bit 31:0` **MASK**: This register contains the MASK (interrupt enable) for each of the 32 interrupts or events. Writing to 0x1A10_9004 sets the bits of the MASK register selected. Writing to 0x1A10_9008 clears the bits of the MASK register selected.

4.4.2 Interrupt

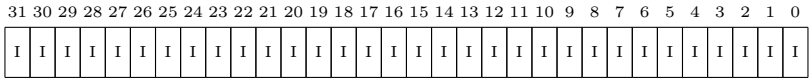
Address: `0x1A10_900C`
Reset Value: `0x0000_0000`



`Bit 31:0` **INT**: This register contains the pending interrupts or events. Writing to 0x1A10_9010 sets the bits of the INT register selected. Writing to 0x1A10_9014 clears the bits of the INT register selected.

4.4.3 Int Ack

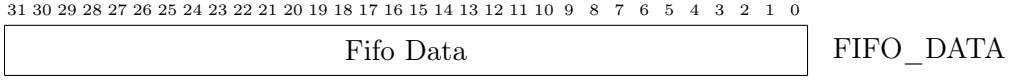
Address: `0x1A10_9018`
Reset Value: `0x0000_0000`



Bit 31:0 **ACK**: This register contains the ACK (interrupt enable) for each of the 32 interrupts or events. Writing to 0x1A10_901C sets the bits of the ACK register selected. Writing to 0x1A10_9020 clears the bits of the ACK register selected.

4.4.4 FIFO Content

Address: `0x1A10_9024`
Reset Value: `0x0000_0000`



Bit 31-0 **FIFO_DATA**: Fifo Content.
This is a read-only register that contain the first valid value of the FIFO.

4.5 SoC Event Generator

Events from peripherals and other sources can be forwarded to the fabric controller, cluster or (back) to certain peripherals, though for PULPissimo we don't have a cluster.

It is the SoC Event Generator's (`soc_event_generator.sv`) job to control which events are to be forwarded and where to. There are three set of masks available to do this:

FC Masks	Control which events are to be forwarded to the fabric controller
Cluster Masks	Control which events are to be forwarded to the cluster (disabled)
Peripheral Masks	Control which events are to be forwarded to peripherals

4.5.1 SoC Event Generator Registers

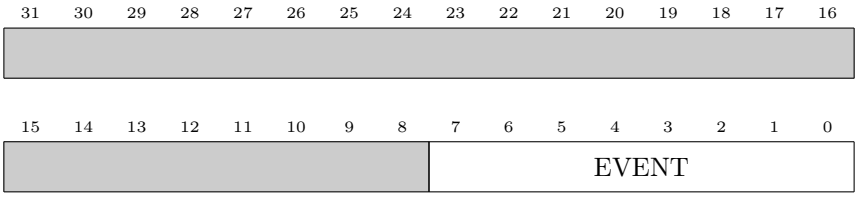
Name	Address	Size	Type	Access	Default	Description
SW_EVENT	0x1A106000	32	Config	W	0x00000000	SoC software events trigger register
FC_MASK0	0x1A106004	32	Config	R/W	0xFFFFFFFF	Events 0-31 dispatch mask to FC
FC_MASK1	0x1A106008	32	Config	R/W	0xFFFFFFFF	Events 32-63 dispatch mask to FC
FC_MASK2	0x1A10600C	32	Config	R/W	0xFFFFFFFF	Events 64-95 dispatch mask to FC
FC_MASK3	0x1A106010	32	Config	R/W	0xFFFFFFFF	Events 96-127 dispatch mask to FC
FC_MASK4	0x1A106014	32	Config	R/W	0xFFFFFFFF	Events 128-159 dispatch mask to FC
FC_MASK5	0x1A106018	32	Config	R/W	0xFFFFFFFF	Events 160-191 dispatch mask to FC
FC_MASK6	0x1A10601C	32	Config	R/W	0xFFFFFFFF	Events 191-223 dispatch mask to FC
FC_MASK7	0x1A106020	32	Config	R/W	0xFFFFFFFF	Events 224-255 dispatch mask to FC
PR_MASK0	0x1A106044	32	Config	R/W	0xFFFFFFFF	Events 0-31 dispatch mask to peripherals
PR_MASK1	0x1A106048	32	Config	R/W	0xFFFFFFFF	Events 32-63 dispatch mask to peripherals
PR_MASK2	0x1A10604C	32	Config	R/W	0xFFFFFFFF	Events 64-95 dispatch mask to peripherals
PR_MASK3	0x1A106050	32	Config	R/W	0xFFFFFFFF	Events 96-127 dispatch mask to peripherals
PR_MASK4	0x1A106054	32	Config	R/W	0xFFFFFFFF	Events 128-159 dispatch mask to peripherals
PR_MASK5	0x1A106058	32	Config	R/W	0xFFFFFFFF	Events 160-191 dispatch mask to peripherals
PR_MASK6	0x1A10605C	32	Config	R/W	0xFFFFFFFF	Events 191-223 dispatch mask to peripherals
PR_MASK7	0x1A106060	32	Config	R/W	0xFFFFFFFF	Events 224-255 dispatch mask to peripherals

ERR0	0x1A106064	32	Status	R	0x00000000	Events 0-31 event queue overflow
ERR1	0x1A106068	32	Status	R	0x00000000	Events 32-63 event queue overflow
ERR2	0x1A10606C	32	Status	R	0x00000000	Events 64-95 event queue overflow
ERR3	0x1A106070	32	Status	R	0x00000000	Events 96-127 event queue overflow
ERR4	0x1A106074	32	Status	R	0x00000000	Events 128-159 event queue overflow
ERR5	0x1A106078	32	Status	R	0x00000000	Events 160-191 event queue overflow
ERR6	0x1A10607C	32	Status	R	0x00000000	Events 191-223 event queue overflow
ERR7	0x1A106080	32	Status	R	0xFFFFFFFF	Events 224-255 event queue overflow
TIMER_LO	0x1A106084	32	Status	R/W	0xFFFFFFFF	Trigger Timer LO of APB Timer with event
TIMER_HI	0x1A106088	32	Status	R/W	0xFFFFFFFF	Trigger Timer HI of APB Timer with event

Table 4.5: SoC Event Generator register table

4.5.2 SW_EVENT

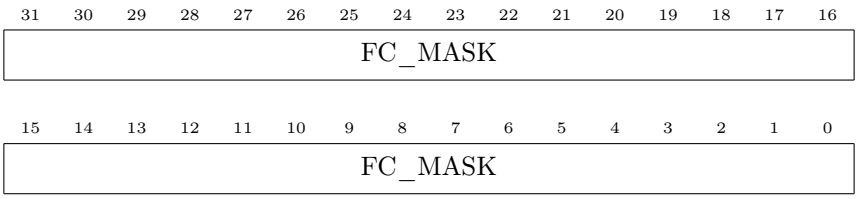
Address: 0x1A10_6000
Reset Value: 0x0000_0000



Bit 7-0 **EVENT** *(W)* Writing a one-hot value into EVENT triggers a SoC software event. 8 software events are available.

4.5.3 FC_MASKX, $X = 0...7$

Address: 0x1A10_6004 + 0x4 * X
Reset Value: 0xFFFF_FFFF

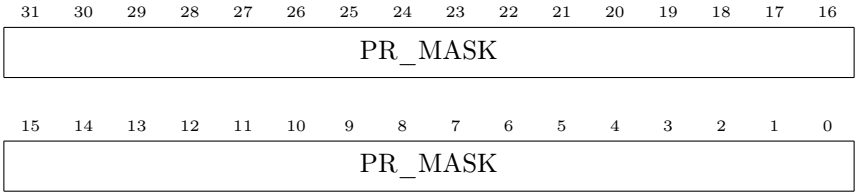


`Bit 31-0` **FC_MASK** *(R/W)* Event Mask to enable/disable event dispatch to FC interrupt controller.

- Setting $bit[i]$ to $0b1$ disables dispatching $event[32 * X + i]$ to FC interrupt controller.
- Setting $bit[i]$ to $0b0$ enables dispatching $event[32 * X + i]$ to FC interrupt controller.

4.5.4 PR_MASKX, $X = 0...7$

Address: `0x1A10_6044 + 0x4 *` X
Reset Value: `0xFFFF_FFFF`

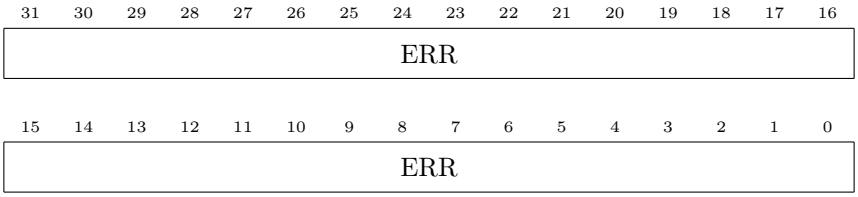


`Bit 31-0` **PR_MASK** *(R/W)* Event Mask to enable/disable event dispatch to peripherals.

- Setting $bit[i]$ to $0b1$ disables dispatching $event[32 * X + i]$ to peripherals.
- Setting $bit[i]$ to $0b0$ enables dispatching $event[32 * X + i]$ to peripherals.

4.5.5 ERRX, $X = 0...7$

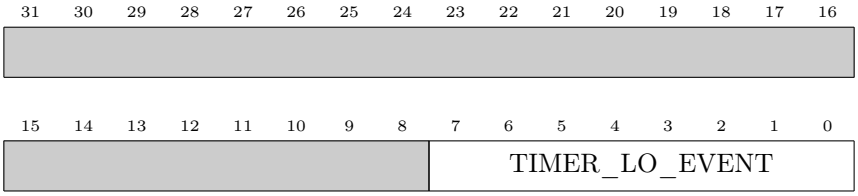
Address: `0x1A10_6064 + 0x4 *` X
Reset Value: `0x0000_0000`



`Bit 31-0` **ERR** *(R/W)* Event queue overflow. Clear after read. Reading $0b1$ at $ERR[i]$ means the event queue of event with id $32 * X + i$ overflowed.

4.5.6 TIMER_LO

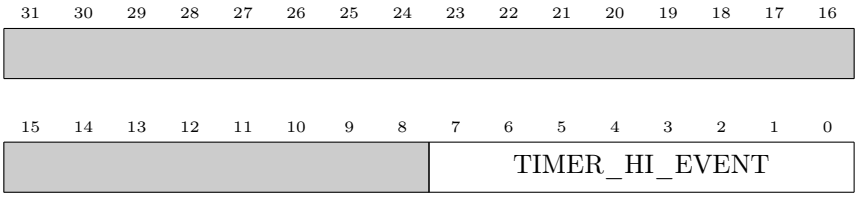
Address: `0x1A10_6084`
Reset Value: `0x0000_0000`



`Bit 7-0` **TIMER_LO_EVENT** *(R/W)* Trigger and start APB Timer LO by the event with id that equals TIMER_LO_EVENT

4.5.7 TIMER_HI

Address: `0x1A10_6088`
Reset Value: `0x0000_0000`



`Bit 7-0` **TIMER_HI_EVENT** *(R/W)* Trigger and start APB Timer HI by the event with id that equals TIMER_HI_EVENT

4.6 APB Timer

The APB Timer (`apb_timer_unit.sv`) has the following features:

- 2 general purpose 32-bit upwards counters
- Can be triggered by multiple sources:
  - FLL clock
  - FLL clock + Prescale
  - Reference clock at 32 kHz
  - Any event
- 8-bit programmable prescaler (divides the FLL clock frequency)
- Different counting modes:
  - One shot mode: timer is stopped after the first comparison match
  - Continuous mode: timer continues couting after a match
  - 64-bit cascaded mode: use both 32-bit timers as a 64-bit timer
- Interrupt request generation on comparison match

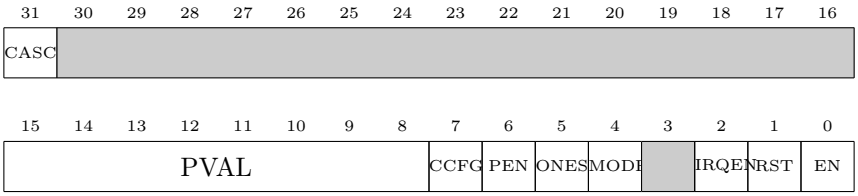
4.6.1 APB Timer Registers

Name	Address	Size	Type	Access	Default	Description
CFG_LO	0x1A10B000	32	Config	R/W	0x00000000	Timer Low Configuration register
CFG_HI	0x1A10B004	32	Config	R/W	0x00000000	Timer High Configuration register
CNT_LO	0x1A10B008	32	Data	R/W	0x00000000	Timer Low counter value register
CNT_HI	0x1A10B00C	32	Data	R/W	0x00000000	Timer High counter value register
CMP_LO	0x1A10B010	32	Config	R/W	0x00000000	Timer Low comparator value register
CMP_HI	0x1A10B014	32	Config	R/W	0x00000000	Timer High comparator value register
START_LO	0x1A10B018	32	Config	R/W	0x00000000	Start Timer Low counting register
START_HI	0x1A10B01C	32	Config	R/W	0x00000000	Start Timer High counting register
RESET_LO	0x1A10B020	32	Config	R/W	0x00000000	Reset Timer Low counter register
RESET_HI	0x1A10B024	32	Config	R/W	0x00000000	Reset Timer High counter register

Table 4.7: APB Timer register table

4.6.2 CFG_LO

Address: `0x1A10_B000`
Reset Value: `0x0000_0000`



`Bit 31` **CASC** *(R/W)* Timer low and Timer high 64-bit cascaded mode enable bit

`Bit 15-8` **PVAL** *(R/W)* Timer low prescaler value. $f_{timer} = f_{clk}/(1 + PVAL)$

`Bit 7` **CCFG** *(R/W)* Timer low clock source configuration

- $0b0$: FLL or FLL plus Prescaler
- $0b1$: 32 kHz reference clock

`Bit 6` **PEN** *(R/W)* Timer low prescaler enable bit

`Bit 5` **ONES** *(R/W)* Timer low one shot configuration

- $0b0$: Timer stays enabled after a compare match with CMP_LO
- $0b1$: Timer is disabled after a compare match with CMP_LO

`Bit 4` **MODE** *(R/W)* Timer low continuous mode configuration

- $0b0$: Continue incrementing timer low counter after a compare match with CMP_LO
- $0b1$: Reset timer to after a compare match with CMP_LO

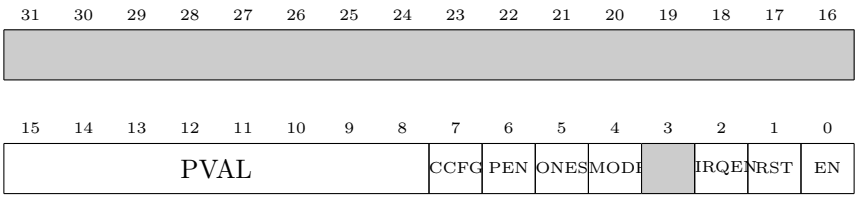
`Bit 2` **IRQEN** *(R/W)* Timer low interrupt generation on compare match enable

`Bit 1` **RST** *(R/W)* Timer low reset, cleared after the reset happened

`Bit 0` **EN** *(R/W)* Timer enable (starts couting) bit

4.6.3 CFG_HI

Address: `0x1A10_B004`
Reset Value: `0x0000_0000`



`Bit 16-8` **PVAL** *(R/W)* Timer hi prescaler value. $f_{timer} = f_{clk}/(1 + PVAL)$

`Bit 7` **CCFG** *(R/W)* Timer hi clock source configuration

- $0b0$: FLL or FLL plus Prescaler

- 0*b*1: 32 kHz reference clock

`Bit 6` **PEN** *(R/W)* Timer hi prescaler enable bit

`Bit 5` **ONES** *(R/W)* Timer hi one shot configuration

- 0*b*0: Timer stays enabled after a compare match with CMP_HI
- 0*b*1: Timer is disabled after a compare match with CMP_HI

`Bit 4` **MODE** *(R/W)* Timer hi continuous mode configuration

- 0*b*0: Continue incrementing timer hi counter after a compare match with CMP_HI
- 0*b*1: Reset timer to after a compare match with CMP_HI

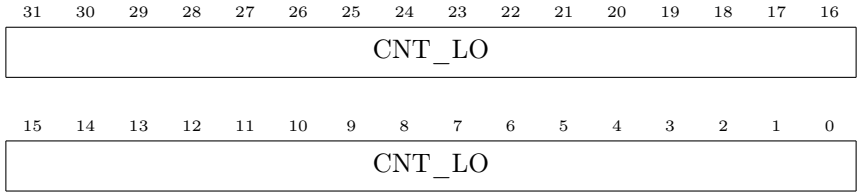
`Bit 2` **IRQEN** *(R/W)* Timer hi interrupt generation on compare match enable

`Bit 1` **RST** *(R/W)* Timer hi reset, cleared after the reset happened

`Bit 0` **EN** *(R/W)* Timer enable (starts couting) bit

4.6.4 CNT_LO

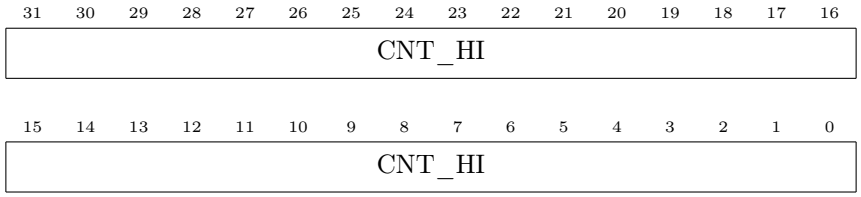
Address: `0x1A10_B008`
Reset Value: `0x0000_0000`



`Bit 31-0` **CNT_LO** *(R/W)* Timer low counter value

4.6.5 CNT_HI

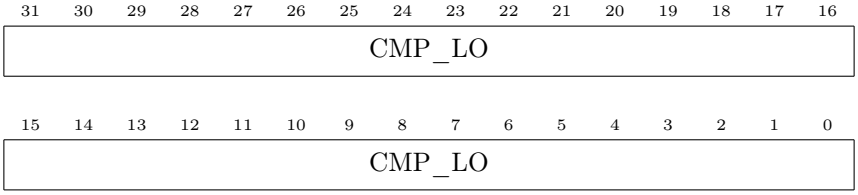
Address: `0x1A10_B00C`
Reset Value: `0x0000_0000`



`Bit 31-0` **CNT_HI** *(R/W)* Timer high counter value

4.6.6 CMP_LO

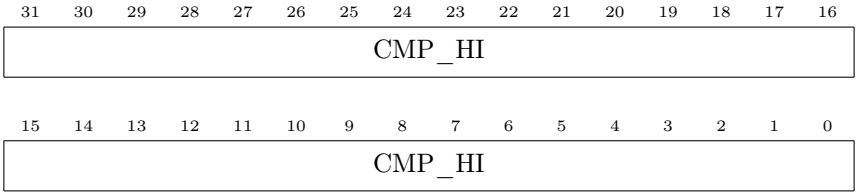
Address: 0x1A10_B010
Reset Value: 0x0000_0000



Bit 31-0 **CMP_LO** *(R/W)* Timer low comparator value

4.6.7 CMP_HI

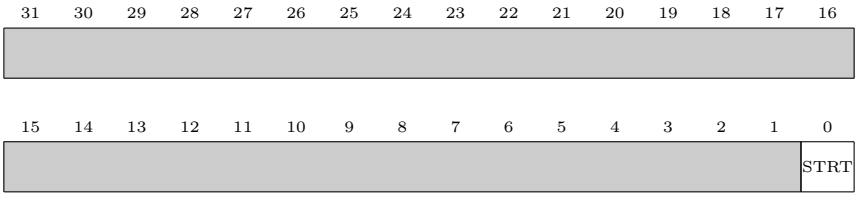
Address: 0x1A10_B014
Reset Value: 0x0000_0000



Bit 31-0 **CMP_HI** *(R/W)* Timer high comparator value

4.6.8 START_LO

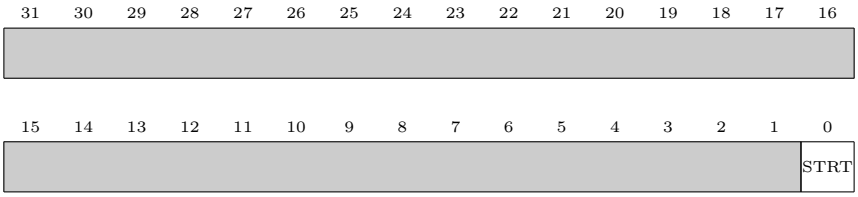
Address: 0x1A10_B018
Reset Value: 0x0000_0000



Bit 0 **STRT** *(W)* Timer high start command (sets EN in CFG_LO)

4.6.9 START_HI

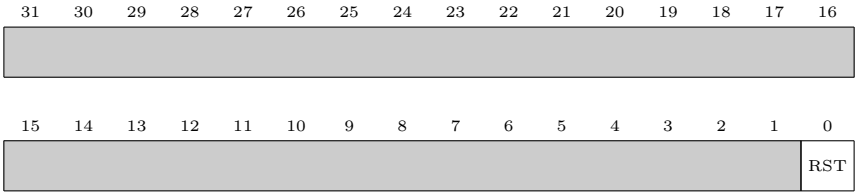
Address: `0x1A10_B01C`
Reset Value: `0x0000_0000`



`Bit 0` **STRT** *(W)* Timer high start command (sets EN in CFG_HI)

4.6.10 RESET_LO

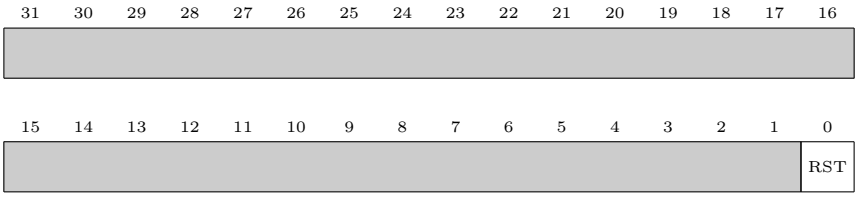
Address: `0x1A10_B020`
Reset Value: `0x0000_0000`



`Bit 0` **RST** *(W)* Timer high reset command (writes RST in CFG_LO)

4.6.11 RESET_HI

Address: `0x1A10_B024`
Reset Value: `0x0000_0000`



`Bit 0` **RST** *(W)* Timer high reset command (sets RST in CFG_HI)

4.7 APB Advanced Timer

4.7.1 APB Advanced Timer Registers

Name	Address	Size	Type	Access	Default	Description
T0_CMD	0x1A104000	32	Config	R/W	0x00000000	ADV_TIMER0 command register.
T0_CONFIG	0x1A104004	32	Config	R/W	0x00000000	ADV_TIMER0 configuration register.
T0_THRESHOLD	0x1A104008	32	Config	R/W	0x00000000	ADV_TIMER0 threshold configuration register.
T0_TH_CHANNEL0	0x1A10400C	32	Config	R/W	0x00000000	ADV_TIMER0 channel 0 threshold configuration register.
T0_TH_CHANNEL1	0x1A104010	32	Config	R/W	0x00000000	ADV_TIMER0 channel 1 threshold configuration register.
T0_TH_CHANNEL2	0x1A104014	32	Config	R/W	0x00000000	ADV_TIMER0 channel 2 threshold configuration register.
T0_TH_CHANNEL3	0x1A104018	32	Config	R/W	0x00000000	ADV_TIMER0 channel 3 threshold configuration register.
T0_COUNTER	0x1A10402C	32	Status	R	0x00000000	ADV_TIMER0 counter register.
T1_CMD	0x1A104040	32	Config	R/W	0x00000000	ADV_TIMER1 command register.
T1_CONFIG	0x1A104044	32	Config	R/W	0x00000000	ADV_TIMER1 configuration register.
T1_THRESHOLD	0x1A104048	32	Config	R/W	0x00000000	ADV_TIMER1 threshold configuration register.
T1_TH_CHANNEL0	0x1A10404C	32	Config	R/W	0x00000000	ADV_TIMER1 channel 0 threshold configuration register.
T1_TH_CHANNEL1	0x1A104050	32	Config	R/W	0x00000000	ADV_TIMER1 channel 1 threshold configuration register.
T1_TH_CHANNEL2	0x1A104054	32	Config	R/W	0x00000000	ADV_TIMER1 channel 2 threshold configuration register.

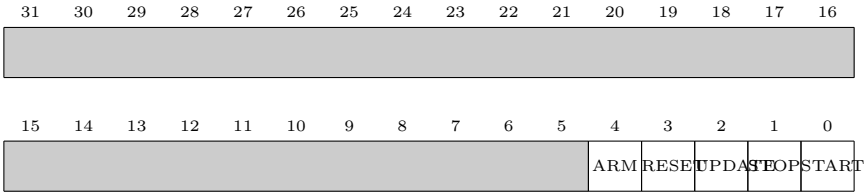
T1_TH_CHANNEL3	0x1A104058	32	Config	R/W	0x00000000	ADV_TIMER1 channel 3 threshold configuration register.
T1_COUNTER	0x1A10406C	32	Status	R	0x00000000	ADV_TIMER1 counter register.
T2_CMD	0x1A104080	32	Config	R/W	0x00000000	ADV_TIMER2 command register.
T2_CONFIG	0x1A104084	32	Config	R/W	0x00000000	ADV_TIMER2 configuration register.
T2_THRESHOLD	0x1A104088	32	Config	R/W	0x00000000	ADV_TIMER2 threshold configuration register.
T2_TH_CHANNEL0	0x1A10408C	32	Config	R/W	0x00000000	ADV_TIMER2 channel 0 threshold configuration register.
T2_TH_CHANNEL1	0x1A104090	32	Config	R/W	0x00000000	ADV_TIMER2 channel 1 threshold configuration register.
T2_TH_CHANNEL2	0x1A104094	32	Config	R/W	0x00000000	ADV_TIMER2 channel 2 threshold configuration register.
T2_TH_CHANNEL3	0x1A104098	32	Config	R/W	0x00000000	ADV_TIMER2 channel 3 threshold configuration register.
T2_COUNTER	0x1A1040AC	32	Status	R	0x00000000	ADV_TIMER2 counter register.
T3_CMD	0x1A1040C0	32	Config	R/W	0x00000000	ADV_TIMER3 command register.
T3_CONFIG	0x1A1040C4	32	Config	R/W	0x00000000	ADV_TIMER3 configuration register.
T3_THRESHOLD	0x1A1040C8	32	Config	R/W	0x00000000	ADV_TIMER3 threshold configuration register.
T3_TH_CHANNEL0	0x1A1040CC	32	Config	R/W	0x00000000	ADV_TIMER3 channel 0 threshold configuration register.
T3_TH_CHANNEL1	0x1A1040D0	32	Config	R/W	0x00000000	ADV_TIMER3 channel 1 threshold configuration register.
T3_TH_CHANNEL2	0x1A1040D4	32	Config	R/W	0x00000000	ADV_TIMER3 channel 2 threshold configuration register.

T3_TH_CHANNEL3	0x1A1040D8	32	Config	R/W	0x00000000	ADV_TIMER3 channel 3 threshold configuration register.
T3_COUNTER	0x1A1040EC	32	Status	R	0x00000000	ADV_TIMER3 counter register.
EVENT_CFG	0x1A104100	32	Config	R/W	0x00000000	ADV_TIMERS events configuration register.
CG	0x1A104104	32	Config	R/W	0x00000000	ADV_TIMERS channels clock gating configuration register.

Table 4.8: APB Advanced Timer

4.7.2 T0_CMD

Address: 0x1A104000
Reset Value: 0x00000000



Bit 4 **ARM** *(R/W)* ADV_TIMER0 arm command bitfield.

Bit 3 **RESET** *(R/W)* ADV_TIMER0 reset command bitfield.

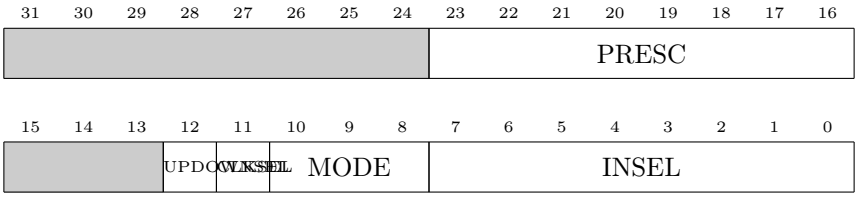
Bit 2 **UPDATE** *(R/W)* ADV_TIMER0 update command bitfield.

Bit 1 **STOP** *(R/W)* ADV_TIMER0 stop command bitfield.

Bit 0 **START** *(R/W)* ADV_TIMER0 start command bitfield.

4.7.3 T0_CONFIG

Address: 0x1A104004
Reset Value: 0x00000000



Bit 23 - 16 **PRESC** *(R/W)* ADV_TIMER0 prescaler value configuration bitfield.

`Bit 12` **UPDOWNSEL** *(R/W)* ADV_TIMER0 center-aligned mode configuration bitfield:
- 1'b0: The counter counts up and down alternatively.
- 1'b1: The counter counts up and resets to 0 when reach threshold.

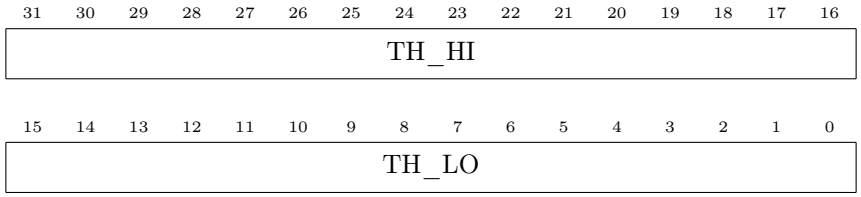
`Bit 11` **CLKSEL** *(R/W)* ADV_TIMER0 clock source configuration bitfield:
- 1'b0: FLL
- 1'b1: reference clock at 32kHz

`Bit 10 - 8` **MODE** *(R/W)* ADV_TIMER0 trigger mode configuration bitfield:
- 3'h0: trigger event at each clock cycle.
- 3'h1: trigger event if input source is 0
- 3'h2: trigger event if input source is 1
- 3'h3: trigger event on input source rising edge
- 3'h4: trigger event on input source falling edge
- 3'h5: trigger event on input source falling or rising edge
- 3'h6: trigger event on input source rising edge when armed
- 3'h7: trigger event on input source falling edge when armed

`Bit 7 - 0` **INSEL** *(R/W)* ADV_TIMER0 input source configuration bitfield:
- 0-31: GPIO[0] to GPIO[31]
- 32-35: Channel 0 to 3 of ADV_TIMER0
- 36-39: Channel 0 to 3 of ADV_TIMER1
- 40-43: Channel 0 to 3 of ADV_TIMER2
- 44-47: Channel 0 to 3 of ADV_TIMER3

4.7.4 T0_THRESHOLD

Address: `0x1A104008`
Reset Value: `0x00000000`

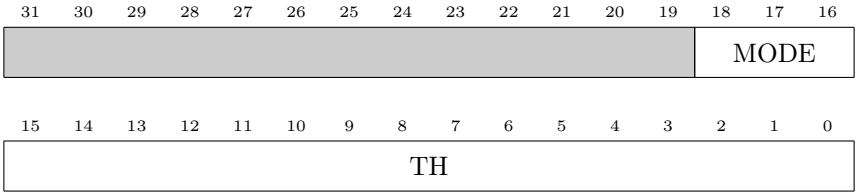


`Bit 31 - 16` **TH_HI** *(R/W)* ADV_TIMER0 threshold high part configuration bitfield. It defines end counter value.

`Bit 15 - 0` **TH_LO** *(R/W)* ADV_TIMER0 threshold low part configuration bitfield. It defines start counter value.

4.7.5 T0_TH_CHANNEL0

Address: `0x1A10400C`
Reset Value: `0x00000000`

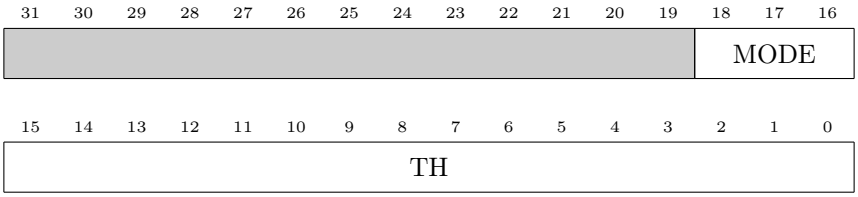


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER0 channel 0 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER0 channel 0 threshold configuration bitfield.

4.7.6 T0_TH_CHANNEL1

Address: `0x1A104010`
Reset Value: `0x00000000`

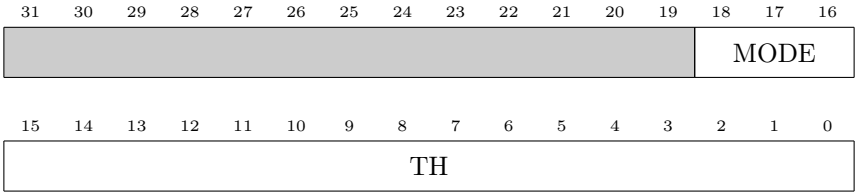


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER0 channel 1 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER0 channel 1 threshold configuration bitfield.

4.7.7 T0_TH_CHANNEL2

Address: `0x1A104014`
Reset Value: `0x00000000`

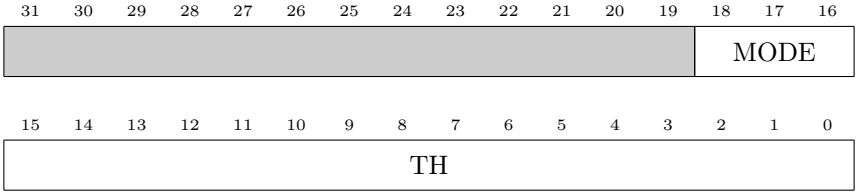


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER0 channel 2 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER0 channel 2 threshold configuration bitfield.

4.7.8 T0_TH_CHANNEL3

Address: `0x1A104018`
Reset Value: `0x00000000`

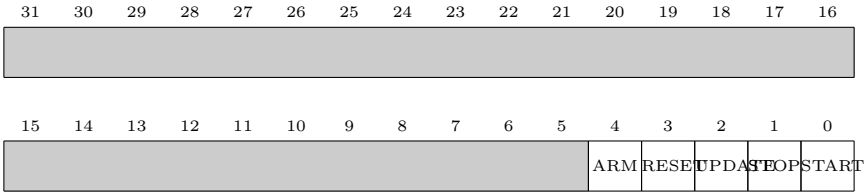


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER0 channel 3 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER0 channel 3 threshold configuration bitfield.

4.7.9 T1_CMD

Address: `0x1A104040`
Reset Value: `0x00000000`



`Bit 4` **ARM** *(R/W)* ADV_TIMER1 arm command bitfield.

`Bit 3` **RESET** *(R/W)* ADV_TIMER1 reset command bitfield.

`Bit 2` **UPDATE** *(R/W)* ADV_TIMER1 update command bitfield.

`Bit 1` **STOP** *(R/W)* ADV_TIMER1 stop command bitfield.

`Bit 0` **START** *(R/W)* ADV_TIMER1 start command bitfield.

4.7.10 T1_CONFIG

Address: `0x1A104044`
Reset Value: `0x00000000`

`Bit 23 - 16` **PRESC** *(R/W)* ADV_TIMER1 prescaler value configuration bitfield.

`Bit 12` **UPDOWNSEL** *(R/W)* ADV_TIMER1 center-aligned mode configuration bitfield:
- 1'b0: The counter counts up and down alternatively.
- 1'b1: The counter counts up and resets to 0 when reach threshold.

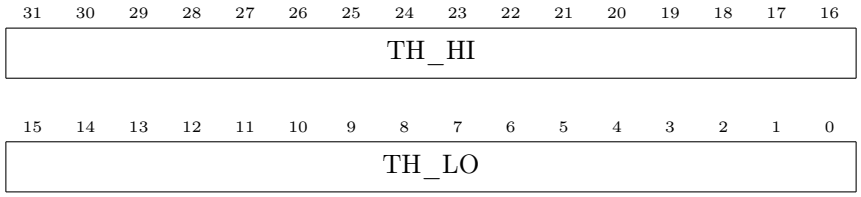
`Bit 11` **CLKSEL** *(R/W)* ADV_TIMER1 clock source configuration bitfield:
- 1'b0: FLL
- 1'b1: reference clock at 32kHz

`Bit 10 - 8` **MODE** *(R/W)* ADV_TIMER1 trigger mode configuration bitfield:
- 3'h0: trigger event at each clock cycle.
- 3'h1: trigger event if input source is 0
- 3'h2: trigger event if input source is 1
- 3'h3: trigger event on input source rising edge
- 3'h4: trigger event on input source falling edge
- 3'h5: trigger event on input source falling or rising edge
- 3'h6: trigger event on input source rising edge when armed
- 3'h7: trigger event on input source falling edge when armed

`Bit 7 - 0` **INSEL** *(R/W)* ADV_TIMER1 input source configuration bitfield:
- 0-31: GPIO[0] to GPIO[31]
- 32-35: Channel 0 to 3 of ADV_TIMER0
- 36-39: Channel 0 to 3 of ADV_TIMER1
- 40-43: Channel 0 to 3 of ADV_TIMER2
- 44-47: Channel 0 to 3 of ADV_TIMER3

4.7.11 T1_THRESHOLD

Address: 0x1A104048
Reset Value: 0x00000000

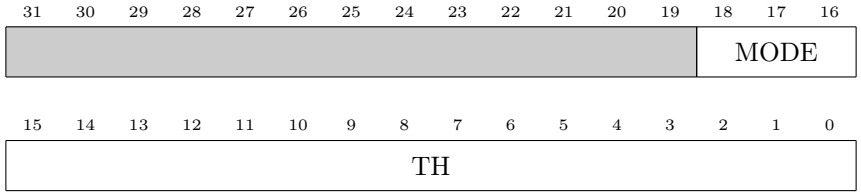


Bit 31 - 16 **TH_HI** *(R/W)* ADV_TIMER1 threshold high part configuration bitfield. It defines end counter value.

Bit 15 - 0 **TH_LO** *(R/W)* ADV_TIMER1 threshold low part configuration bitfield. It defines start counter value.

4.7.12 T1_TH_CHANNEL0

Address: 0x1A10404C
Reset Value: 0x00000000

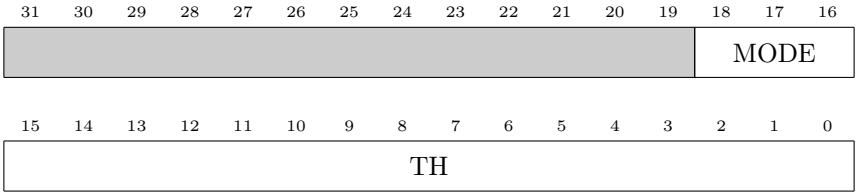


Bit 18 - 16 **MODE** *(R/W)* ADV_TIMER1 channel 0 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

Bit 15 - 0 **TH** *(R/W)* ADV_TIMER1 channel 0 threshold configuration bitfield.

4.7.13 T1_TH_CHANNEL1

Address: 0x1A104050
Reset Value: 0x00000000

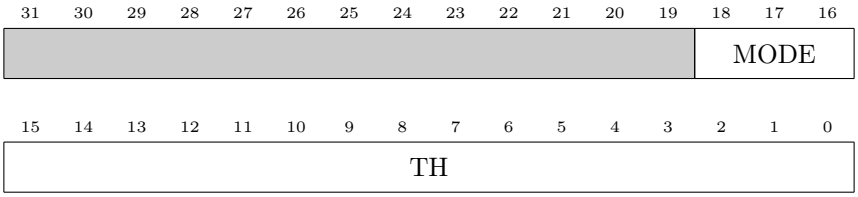


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER1 channel 1 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER1 channel 1 threshold configuration bitfield.

4.7.14 T1_TH_CHANNEL2

Address: `0x1A104054`
Reset Value: `0x00000000`

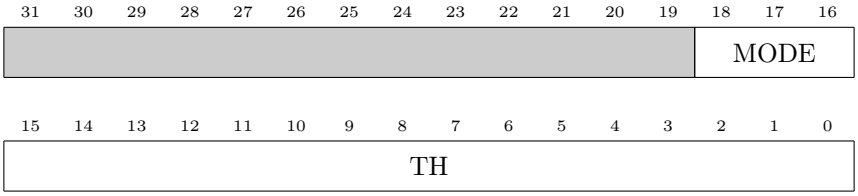


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER1 channel 2 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER1 channel 2 threshold configuration bitfield.

4.7.15 T1_TH_CHANNEL3

Address: `0x1A104058`
Reset Value: `0x00000000`

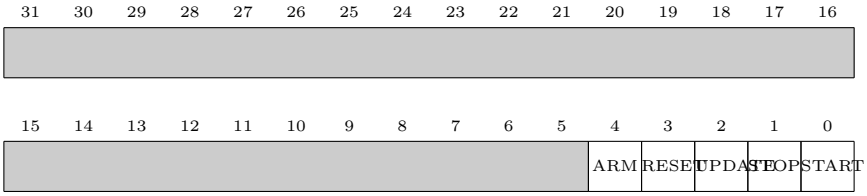


Bit 18 - 16 **MODE** *(R/W)* ADV_TIMER1 channel 3 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

Bit 15 - 0 **TH** *(R/W)* ADV_TIMER1 channel 3 threshold configuration bitfield.

4.7.16 T2_CMD

Address: 0x1A104080
Reset Value: 0x00000000



Bit 4 **ARM** *(R/W)* ADV_TIMER2 arm command bitfield.

Bit 3 **RESET** *(R/W)* ADV_TIMER2 reset command bitfield.

Bit 2 **UPDATE** *(R/W)* ADV_TIMER2 update command bitfield.

Bit 1 **STOP** *(R/W)* ADV_TIMER2 stop command bitfield.

Bit 0 **START** *(R/W)* ADV_TIMER2 start command bitfield.

4.7.17 T2_CONFIG

Address: 0x1A104084
Reset Value: 0x00000000

Bit 23 - 16 **PRESC** *(R/W)* ADV_TIMER2 prescaler value configuration bitfield.

`Bit 12` **UPDOWNSEL** *(R/W)* ADV_TIMER2 center-aligned mode configuration bitfield:
- 1'b0: The counter counts up and down alternatively.
- 1'b1: The counter counts up and resets to 0 when reach threshold.

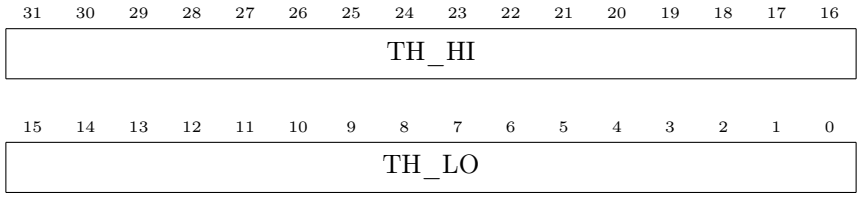
`Bit 11` **CLKSEL** *(R/W)* ADV_TIMER2 clock source configuration bitfield:
- 1'b0: FLL
- 1'b1: reference clock at 32kHz

`Bit 10 - 8` **MODE** *(R/W)* ADV_TIMER2 trigger mode configuration bitfield:
- 3'h0: trigger event at each clock cycle.
- 3'h1: trigger event if input source is 0
- 3'h2: trigger event if input source is 1
- 3'h3: trigger event on input source rising edge
- 3'h4: trigger event on input source falling edge
- 3'h5: trigger event on input source falling or rising edge
- 3'h6: trigger event on input source rising edge when armed
- 3'h7: trigger event on input source falling edge when armed

`Bit 7 - 0` **INSEL** *(R/W)* ADV_TIMER2 input source configuration bitfield:
- 0-31: GPIO[0] to GPIO[31]
- 32-35: Channel 0 to 3 of ADV_TIMER0
- 36-39: Channel 0 to 3 of ADV_TIMER1
- 40-43: Channel 0 to 3 of ADV_TIMER2
- 44-47: Channel 0 to 3 of ADV_TIMER3

4.7.18 T2_THRESHOLD

Address: `0x1A104088`
Reset Value: `0x00000000`

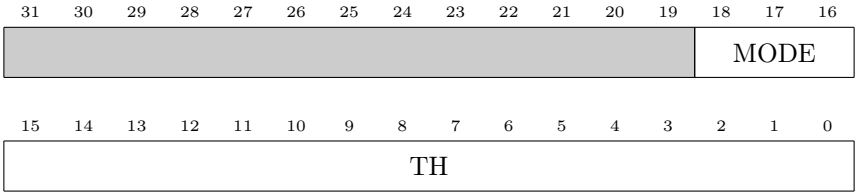


`Bit 31 - 16` **TH_HI** *(R/W)* ADV_TIMER2 threshold high part configuration bitfield. It defines end counter value.

`Bit 15 - 0` **TH_LO** *(R/W)* ADV_TIMER2 threshold low part configuration bitfield. It defines start counter value.

4.7.19 T2_TH_CHANNEL0

Address: `0x1A10408C`
Reset Value: `0x00000000`

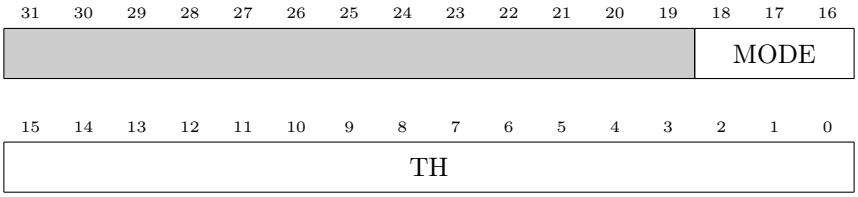


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER2 channel 0 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER2 channel 0 threshold configuration bitfield.

4.7.20 T2_TH_CHANNEL1

Address: `0x1A104090`
Reset Value: `0x00000000`

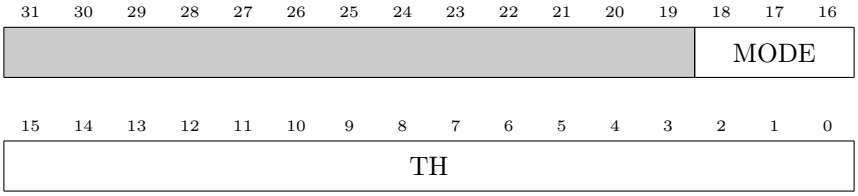


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER2 channel 1 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER2 channel 1 threshold configuration bitfield.

4.7.21 T2_TH_CHANNEL2

Address: `0x1A104094`
Reset Value: `0x00000000`

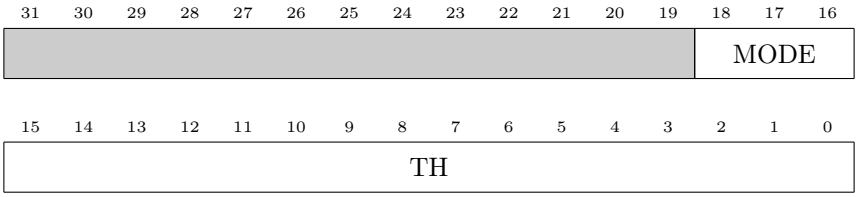


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER2 channel 2 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER2 channel 2 threshold configuration bitfield.

4.7.22 T2_TH_CHANNEL3

Address: `0x1A104098`
Reset Value: `0x00000000`

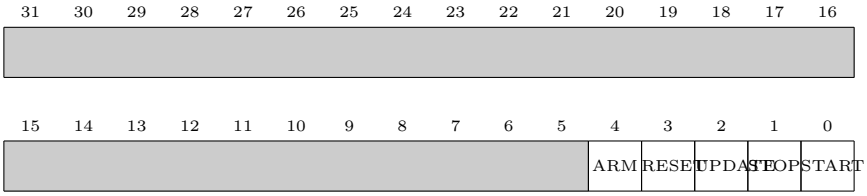


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER2 channel 3 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER2 channel 3 threshold configuration bitfield.

4.7.23 T3_CMD

Address: `0x1A1040C0`
Reset Value: `0x00000000`



`Bit 4` **ARM** *(R/W)* ADV_TIMER3 arm command bitfield.

`Bit 3` **RESET** *(R/W)* ADV_TIMER3 reset command bitfield.

`Bit 2` **UPDATE** *(R/W)* ADV_TIMER3 update command bitfield.

`Bit 1` **STOP** *(R/W)* ADV_TIMER3 stop command bitfield.

`Bit 0` **START** *(R/W)* ADV_TIMER3 start command bitfield.

4.7.24 T3_CONFIG

Address: `0x1A1040C4`
Reset Value: `0x00000000`

`Bit 23 - 16` **PRESC** *(R/W)* ADV_TIMER3 prescaler value configuration bitfield.

`Bit 12` **UPDOWNSEL** *(R/W)* ADV_TIMER3 center-aligned mode configuration bitfield:
- 1'b0: The counter counts up and down alternatively.
- 1'b1: The counter counts up and resets to 0 when reach threshold.

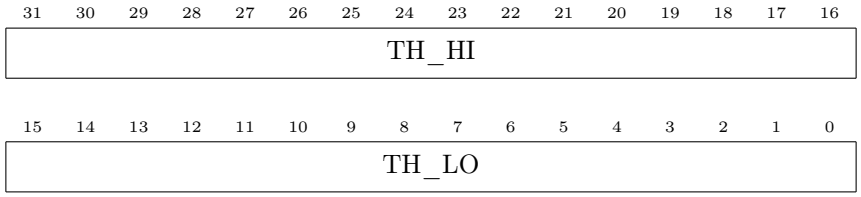
`Bit 11` **CLKSEL** *(R/W)* ADV_TIMER3 clock source configuration bitfield:
- 1'b0: FLL
- 1'b1: reference clock at 32kHz

`Bit 10 - 8` **MODE** *(R/W)* ADV_TIMER3 trigger mode configuration bitfield:
- 3'h0: trigger event at each clock cycle.
- 3'h1: trigger event if input source is 0
- 3'h2: trigger event if input source is 1
- 3'h3: trigger event on input source rising edge
- 3'h4: trigger event on input source falling edge
- 3'h5: trigger event on input source falling or rising edge
- 3'h6: trigger event on input source rising edge when armed
- 3'h7: trigger event on input source falling edge when armed

`Bit 7 - 0` **INSEL** *(R/W)* ADV_TIMER3 input source configuration bitfield:
- 0-31: GPIO[0] to GPIO[31]
- 32-35: Channel 0 to 3 of ADV_TIMER0
- 36-39: Channel 0 to 3 of ADV_TIMER1
- 40-43: Channel 0 to 3 of ADV_TIMER2
- 44-47: Channel 0 to 3 of ADV_TIMER3

4.7.25 T3_THRESHOLD

Address: 0x1A1040C8
Reset Value: 0x00000000

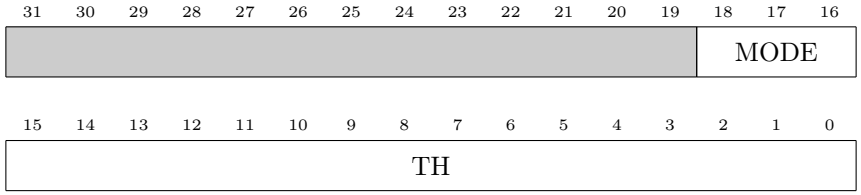


Bit 31 - 16 **TH_HI** *(R/W)* ADV_TIMER3 threshold high part configuration bitfield. It defines end counter value.

Bit 15 - 0 **TH_LO** *(R/W)* ADV_TIMER3 threshold low part configuration bitfield. It defines start counter value.

4.7.26 T3_TH_CHANNEL0

Address: 0x1A1040CC
Reset Value: 0x00000000

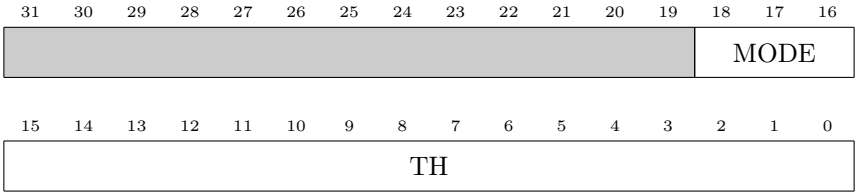


Bit 18 - 16 **MODE** *(R/W)* ADV_TIMER3 channel 0 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

Bit 15 - 0 **TH** *(R/W)* ADV_TIMER3 channel 0 threshold configuration bitfield.

4.7.27 T3_TH_CHANNEL1

Address: 0x1A1040D0
Reset Value: 0x00000000

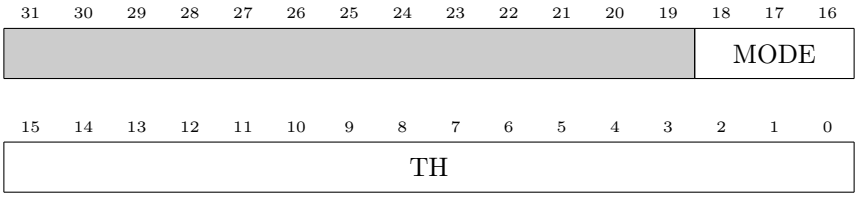


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER3 channel 1 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER3 channel 1 threshold configuration bitfield.

4.7.28 T3_TH_CHANNEL2

Address: `0x1A1040D4`
Reset Value: `0x00000000`

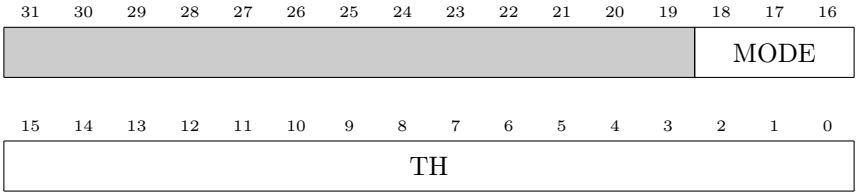


`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER3 channel 2 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER3 channel 2 threshold configuration bitfield.

4.7.29 T3_TH_CHANNEL3

Address: `0x1A1040D8`
Reset Value: `0x00000000`



`Bit 18 - 16` **MODE** *(R/W)* ADV_TIMER3 channel 3 threshold match action on channel output signal configuration bitfield:
- 3'h0: set.
- 3'h1: toggle then next threshold match action is clear.
- 3'h2: set then next threshold match action is clear.
- 3'h3: toggle.
- 3'h4: clear.
- 3'h5: toggle then next threshold match action is set.
- 3'h6: clear then next threshold match action is set.

`Bit 15 - 0` **TH** *(R/W)* ADV_TIMER3 channel 3 threshold configuration bitfield.

4.7.30 EVENT_CFG

Address: `0x1A104100`
Reset Value: `0x00000000`

`Bit 19 - 16` **ENA** *(R/W)* ADV_TIMER output event enable configuration bitfield. ENA[i]=1 enables output event i generation.

`Bit 15 - 12` **SEL3** *(R/W)* ADV_TIMER output event 3 source configuration bitfiled:
- 4'h0: ADV_TIMER0 channel 0.
- 4'h1: ADV_TIMER0 channel 1.
- 4'h2: ADV_TIMER0 channel 2.
- 4'h3: ADV_TIMER0 channel 3.
- 4'h4: ADV_TIMER1 channel 0.
- 4'h5: ADV_TIMER1 channel 1.
- 4'h6: ADV_TIMER1 channel 2.
- 4'h7: ADV_TIMER1 channel 3.
- 4'h8: ADV_TIMER2 channel 0.
- 4'h9: ADV_TIMER2 channel 1.
- 4'hA: ADV_TIMER2 channel 2.
- 4'hB: ADV_TIMER2 channel 3.
- 4'hC: ADV_TIMER3 channel 0.
- 4'hD: ADV_TIMER3 channel 1.
- 4'hE: ADV_TIMER3 channel 2.
- 4'hF: ADV_TIMER3 channel 3.

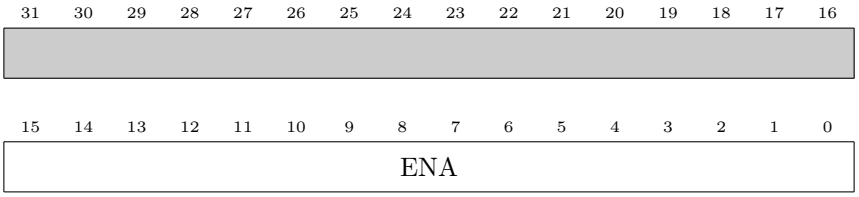
Bit 11 - 8 **SEL2** *(R/W)* ADV_TIMER output event 2 source configuration bitfiled:
- 4'h0: ADV_TIMER0 channel 0.
- 4'h1: ADV_TIMER0 channel 1.
- 4'h2: ADV_TIMER0 channel 2.
- 4'h3: ADV_TIMER0 channel 3.
- 4'h4: ADV_TIMER1 channel 0.
- 4'h5: ADV_TIMER1 channel 1.
- 4'h6: ADV_TIMER1 channel 2.
- 4'h7: ADV_TIMER1 channel 3.
- 4'h8: ADV_TIMER2 channel 0.
- 4'h9: ADV_TIMER2 channel 1.
- 4'hA: ADV_TIMER2 channel 2.
- 4'hB: ADV_TIMER2 channel 3.
- 4'hC: ADV_TIMER3 channel 0.
- 4'hD: ADV_TIMER3 channel 1.
- 4'hE: ADV_TIMER3 channel 2.
- 4'hF: ADV_TIMER3 channel 3.

Bit 7 - 4 **SEL1** *(R/W)* ADV_TIMER output event 1 source configuration bitfiled:
- 4'h0: ADV_TIMER0 channel 0.
- 4'h1: ADV_TIMER0 channel 1.
- 4'h2: ADV_TIMER0 channel 2.
- 4'h3: ADV_TIMER0 channel 3.
- 4'h4: ADV_TIMER1 channel 0.
- 4'h5: ADV_TIMER1 channel 1.
- 4'h6: ADV_TIMER1 channel 2.
- 4'h7: ADV_TIMER1 channel 3.
- 4'h8: ADV_TIMER2 channel 0.
- 4'h9: ADV_TIMER2 channel 1.
- 4'hA: ADV_TIMER2 channel 2.
- 4'hB: ADV_TIMER2 channel 3.
- 4'hC: ADV_TIMER3 channel 0.
- 4'hD: ADV_TIMER3 channel 1.
- 4'hE: ADV_TIMER3 channel 2.
- 4'hF: ADV_TIMER3 channel 3.

Bit 3 - 0 **SEL0** *(R/W)* ADV_TIMER output event 0 source configuration bitfiled:
- 4'h0: ADV_TIMER0 channel 0.
- 4'h1: ADV_TIMER0 channel 1.
- 4'h2: ADV_TIMER0 channel 2.
- 4'h3: ADV_TIMER0 channel 3.
- 4'h4: ADV_TIMER1 channel 0.
- 4'h5: ADV_TIMER1 channel 1.
- 4'h6: ADV_TIMER1 channel 2.
- 4'h7: ADV_TIMER1 channel 3.
- 4'h8: ADV_TIMER2 channel 0.
- 4'h9: ADV_TIMER2 channel 1.
- 4'hA: ADV_TIMER2 channel 2.
- 4'hB: ADV_TIMER2 channel 3.
- 4'hC: ADV_TIMER3 channel 0.
- 4'hD: ADV_TIMER3 channel 1.
- 4'hE: ADV_TIMER3 channel 2.
- 4'hF: ADV_TIMER3 channel 3.

4.7.31 CG

Address: `0x1A104104`
Reset Value: `0x00000000`



`Bit 15 - 0` **ENA** *(R/W)* ADV_TIMER clock gating configuration bitfield.
- ENA[i]=0: clock gate ADV_TIMERi.
- ENA[i]=1: enable ADV_TIMERi.

5 Debug Module for External Debug Support

The debug module in PULPissimo is compliant with the RISC-V External Debug Support specification $v1.13.1$. For more details please take a look at the documentation in the debug module folder and consult the RISC-V External Debug Support specification.