HIGH-VOLTAGE ANALOG-SIGNAL IC

UCi7065

40-channel SEG/COM Driver for
Dot Matrix LCD

PP Specifications
Datasheet Revision: 0.8

IC Version: c_A
December 24, 2013

ULTRACHIP

The Coolest LCD Driver, Ever!!

Table of Content

UCi7065

40-channel SEG/COM Driver for Dot Matrix LCD

INTRODUCTION

The UCi7065c is a SEG/COM driver for dot matrix type LCD display. It features 40 channels with 20x2 bits bi-directional shift registers, data latches, LCD drivers and logic control circuits. It is fabricated by high voltage CMOS process wth low current consumption.

The UCi7065c can conver serial data received from an LCD controller, such as UCi7066u, into parallel data and send out LCD driving waveforms to the LCD panel. The UCi7065c is designed for general purpose LCD drivers. It can drive both static and dynamic drive LCD. The LSI can be used as SEG/COM driver.

The UCi7065c has pin funciton compatibility with the KS0063(B) that allows the user to easily replace it with an UCi7065c.

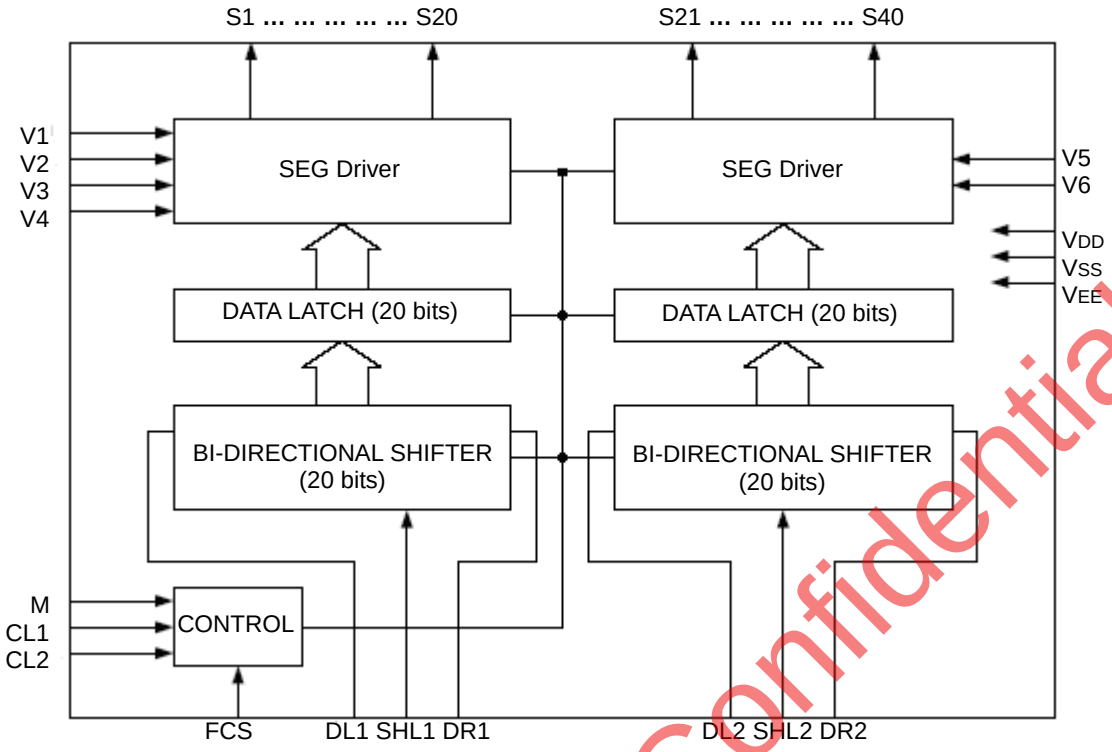
MAIN APPLICATIONS

-
-

FEATURE HIGHLIGHTS

- Dot matric LCD driver with 2 (two) 40-channel outputs.
- Bias voltage (V1~V6)
- Input/Output signals
  - Input: Serial display data and control pulse from controller IC
  - Output: 40x2 channels waveform for LCD driving.
- Display driving bias: static to 1/5
- Power supply for logic: 2.7V ~ 5.5V
- Power supply for LCD voltage (V_{DD}-V_{EE}): 3V~18V
- Package: bare die

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Description
UCi7065cBXA-N1	Bare Die

General Notes

APPLICATION INFORMATION
For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER
All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS
These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER
UltraChip believes the information contained in this document to be accurate and reliable. However, it is subject to change without notice. No responsibility is assumed by UltraChip for its use, nor for infringement of patents or other rights of third parties. No part of this publication may be reproduced, or transmitted in any form or by any means without the prior consent of UltraChip Inc. UltraChip's terms and conditions of sale apply at all times.

CONTACT DETAILS
UltraChip Inc. (Headquarter)
4F, No. 618, Recom Road,
Neihu District, Taipei 114,
Taiwan, R. O. C.

Tel: +886 (2) 8797-8947
Fax: +886 (2) 8797-8910
Sales e-mail: sales@ultrachip.com
Web site: http://www.ultrachip.com

PIN DESCRIPTION

<table>
<tr><th>Pin</th><th>Type</th><th>Description</th></tr>
<tr><td>VDD</td><td>PWR</td><td>Logic Power Supply</td></tr>
<tr><td>VSS</td><td>GND</td><td>Ground.</td></tr>
<tr><td>VEE</td><td>PWR</td><td>LCD power. LCD driving voltage</td></tr>
<tr><td>V1, V2</td><td>I</td><td>Voltage level selection.</td></tr>
<tr><td>V3, V4</td><td>I</td><td>Used as non-select-voltage level for part 1.</td></tr>
<tr><td>V5, V6</td><td>I</td><td>Used as non-select-voltage level for part 2.</td></tr>
<tr><td>S[1]~S[20]</td><td>O</td><td>SEGs. LCD driver output for part 1</td></tr>
<tr><td>SHL1</td><td>I</td><td>Direction control for part 1 SEGs.</td></tr>
<tr><td>DL1, DR1</td><td>I/O</td><td><table><tr><td></td><td>DL1</td><td>DR1</td></tr><tr><td>SHL1=L</td><td>IN</td><td>OUT</td></tr><tr><td>SHL1=H</td><td>OUT</td><td>IN</td></tr></table></td></tr>
<tr><td>S[21]~S[40]</td><td>O</td><td>SEGs. LCD driver output for part 2</td></tr>
<tr><td>SHL2</td><td>I</td><td>Direction control for part 2 SEGs.</td></tr>
<tr><td>DL2, DR2</td><td>I/O</td><td><table><tr><td></td><td>DL2</td><td>DR2</td></tr><tr><td>SHL2=L</td><td>IN</td><td>OUT</td></tr><tr><td>SHL2=H</td><td>OUT</td><td>IN</td></tr></table></td></tr>
<tr><td>M</td><td>I</td><td>Alternate the LCD driving waveform.</td></tr>
<tr><td>CL1</td><td>I</td><td>Latch Clock. Latches data after shift is completed.</td></tr>
<tr><td>CL2</td><td>I</td><td>Shift Clock. Shifts data into SEGs.</td></tr>
<tr><td>FCS</td><td>I</td><td>Mode selection signal for part 2.</td></tr>
</table>

FUNCTIONAL DESCRIPTION

Shift Registers and Data I/O

The UCi7065c supplies two sets of shift register, which controls the shift direction by SHL1 & SHL2. The DL1, DR1, DL2 and DR2 are data input or output option function.

Shift Direction of Channel 1			
SHL1	Sifht Direction	DL1	DR1
L	S[0] → S[20]	In	Out
H	S[20] → S[1]	Out	In

Shift Direction of Channel 2			
SHL2	Sifht Direction	DL2	DR2
L	S[21] → S[40]	In	Out
H	S[40] → S[21]	Out	In

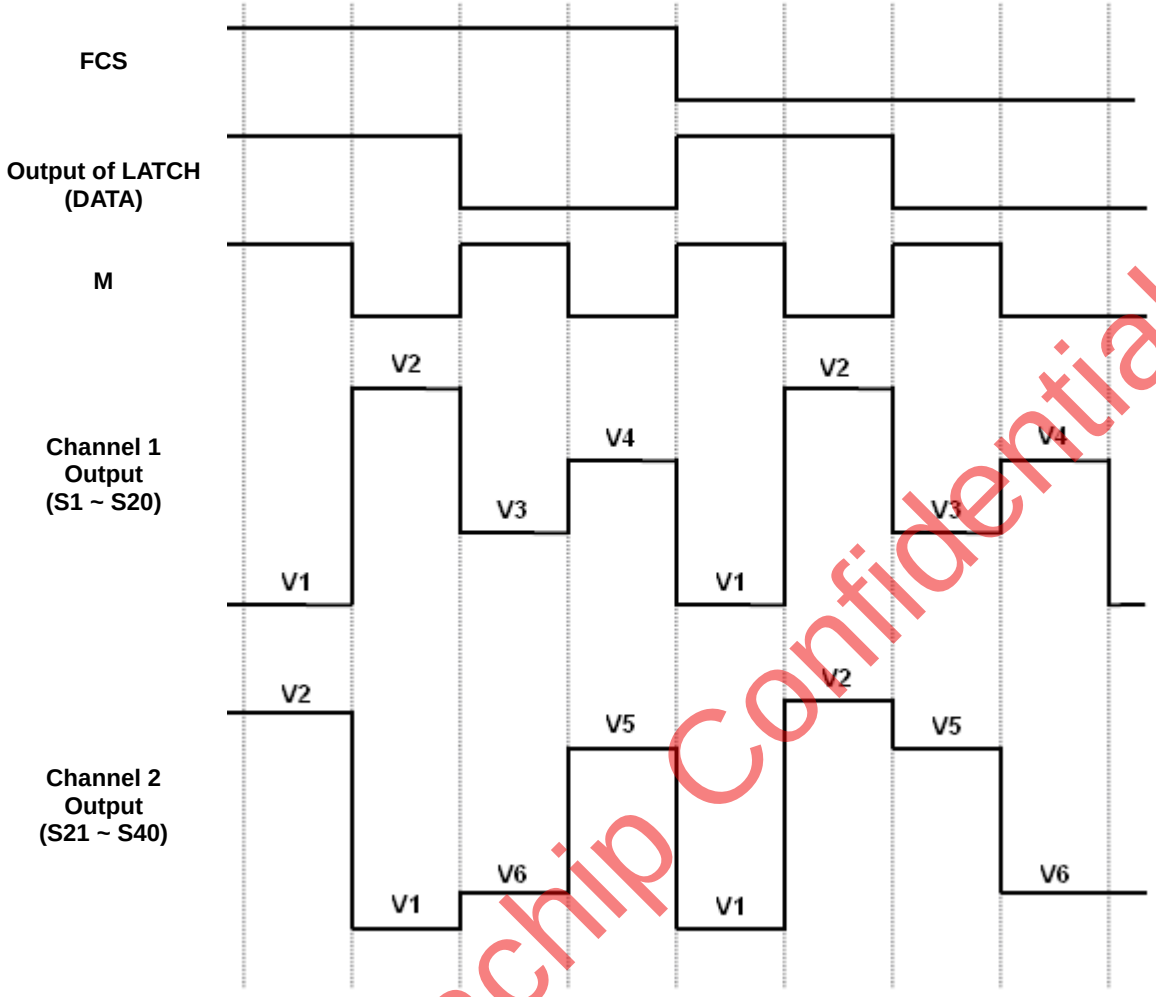
Clock and Mode Selection

In channel 1 part, the CL1 is the clock to latch data on the falling edge. It latches the data input from the bi-directional shift register at the falling edge of CL1 and transfers its outputs to the LCD driver circuit. The CL2 is the clock to shift data on the falling edge. It shifts the serial data at the falling of CL2 and transfers the output of each bit of the register to the latch circuit.

In channel 2 part, the CL1 and CL2 is the clock to latch or shift data on the falling or rising edge which is depend on FCS value. When FCS is low, the channel 2 function is the same as channel 1 as a segment driver. When FCS is high, the channel 2 function will become a common driver. Detail functions are show in the following table:

FCS	Clock Edge		Channel 1	Channel 2
L	CL1	↓	Latch data	Latch data
		↑	–	–
	CL2	↓	Shift data	Shift data
		↑	–	–
H	CL1	↓	Latch data	–
		↑	–	Shift data
	CL2	↓	Shift data	–
		↑	–	Latch data

LCD OUTPUT WAVEFORMS



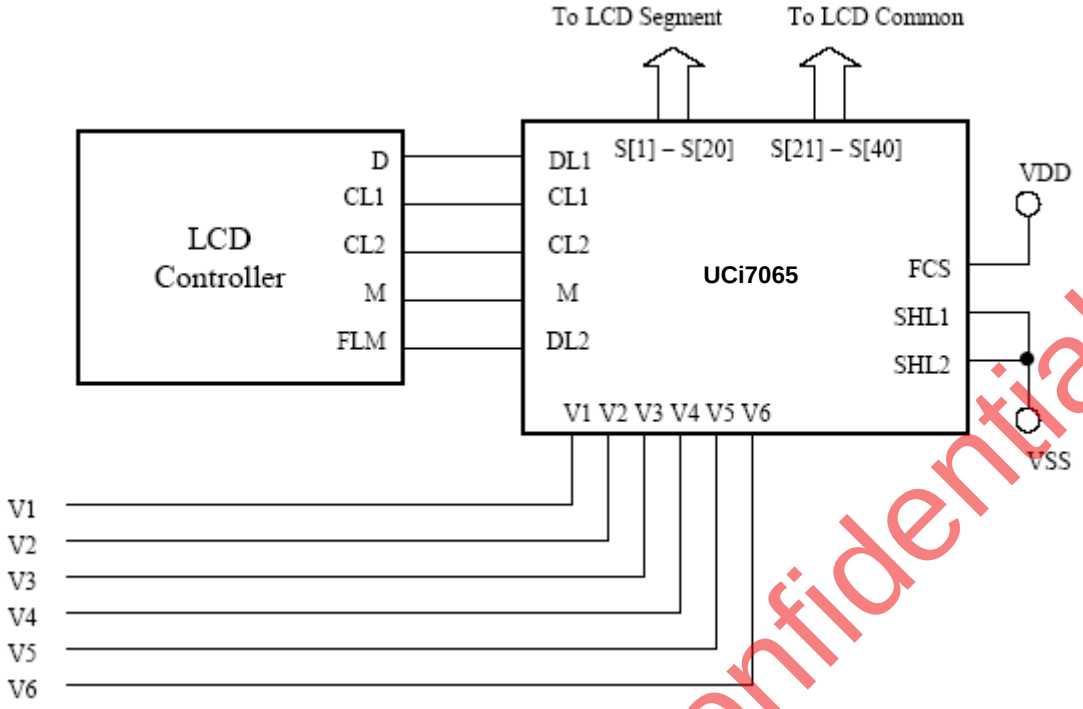
The output levels of channel1 and channel2 are decided by the combination of FCS, M, and latched data. Refer to the following table:

FCS	Latched Data	M	Channel 1	Channel 2
L	L	L	V4	V6
		H	V3	V5
	H	L	V2	V2
		H	V1	V1
H	L	L	V4	V5
		H	V3	V6
	H	L	V2	V1
		H	V1	V2

Note: To use the same function of channel 1/ 2 as a SEG driver, (V3 and V5) / (V4 and V6) need to short-circuit, respectivly.

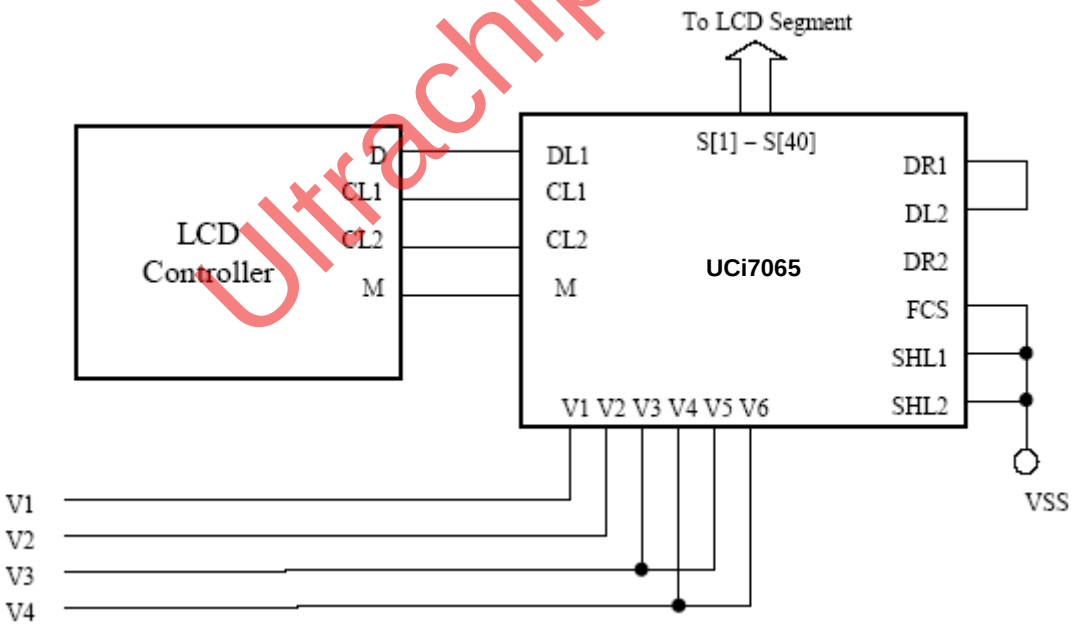
Channel 1 used as a segment driver and channel 2 as a common driver (FCS=H)

When channel 2 is used as a common driver, FCS is connected to VDD. Channel 2 will shift data on the rising edge of CL1 and latch data on the rising edge of CL2.



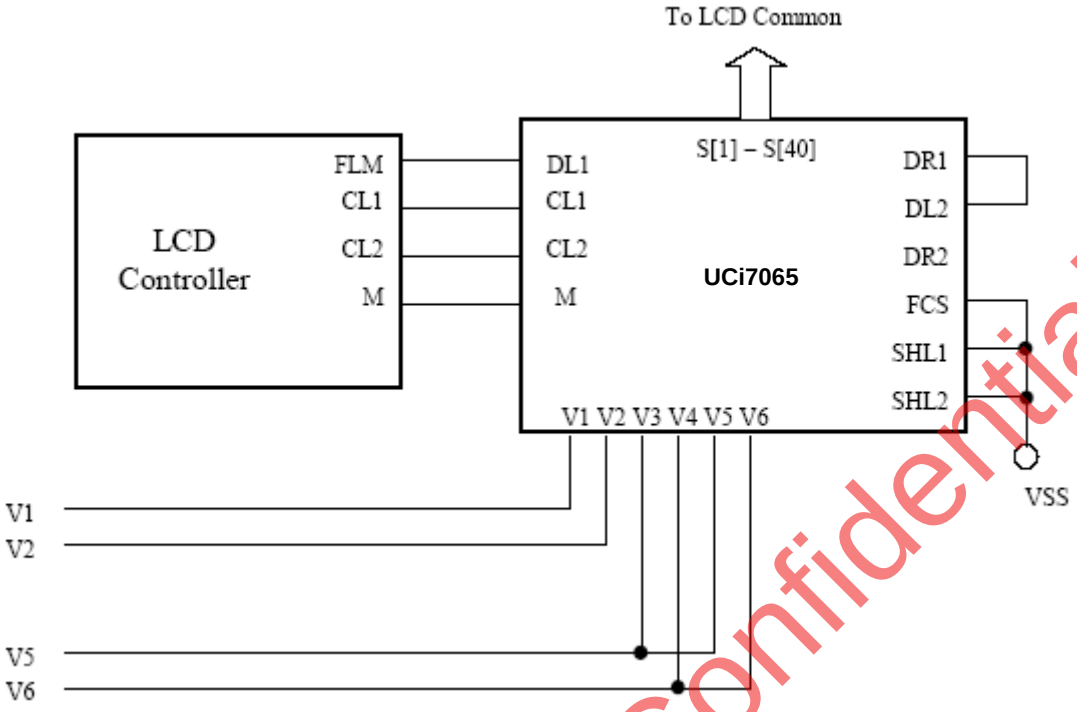
Both Channels 1 and 2 used as segment drivers (FCS=L)

When both channels 1 and 2 of the UCi7065c are used as segment drivers, they will shift data on the falling edge of CL2 and latch data on the falling edge of CL1. V3&V5, V4&V6 are shorted in the application circuit as shown in the following figure.



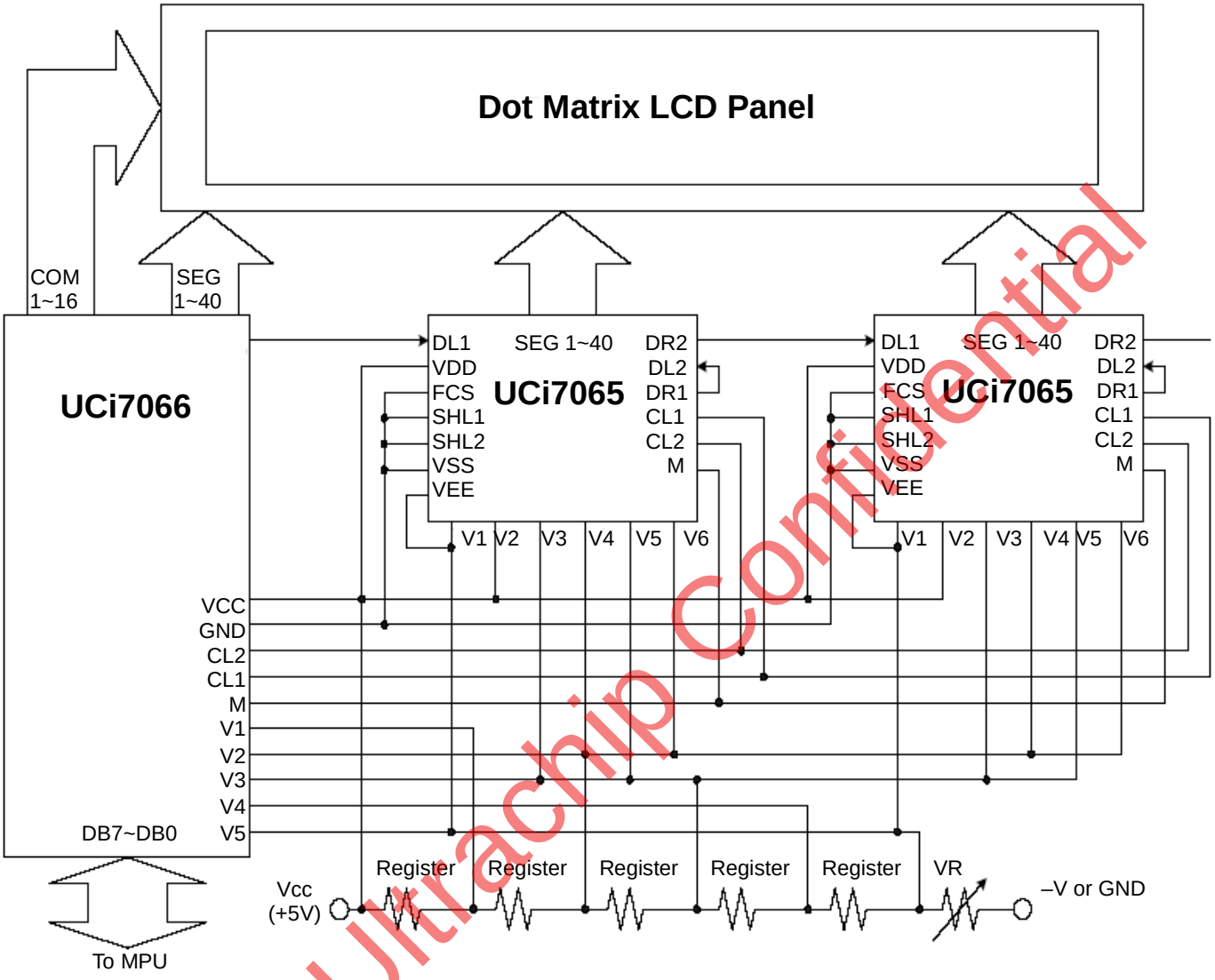
Both Channels 1 and 2 used as common drivers (FCS=L)

When both channels 1 and 2 of the UCi7065c are used as common drivers, the FCS is set low and the signals (CL1, CL2, M) from the controller are connected as shown in the following figure.



APPLICATION CIRCUIT

2-Line x 24-Word



Note:

Register = 2.2K ~ 10KΩ

V_R = 10K~30KΩ

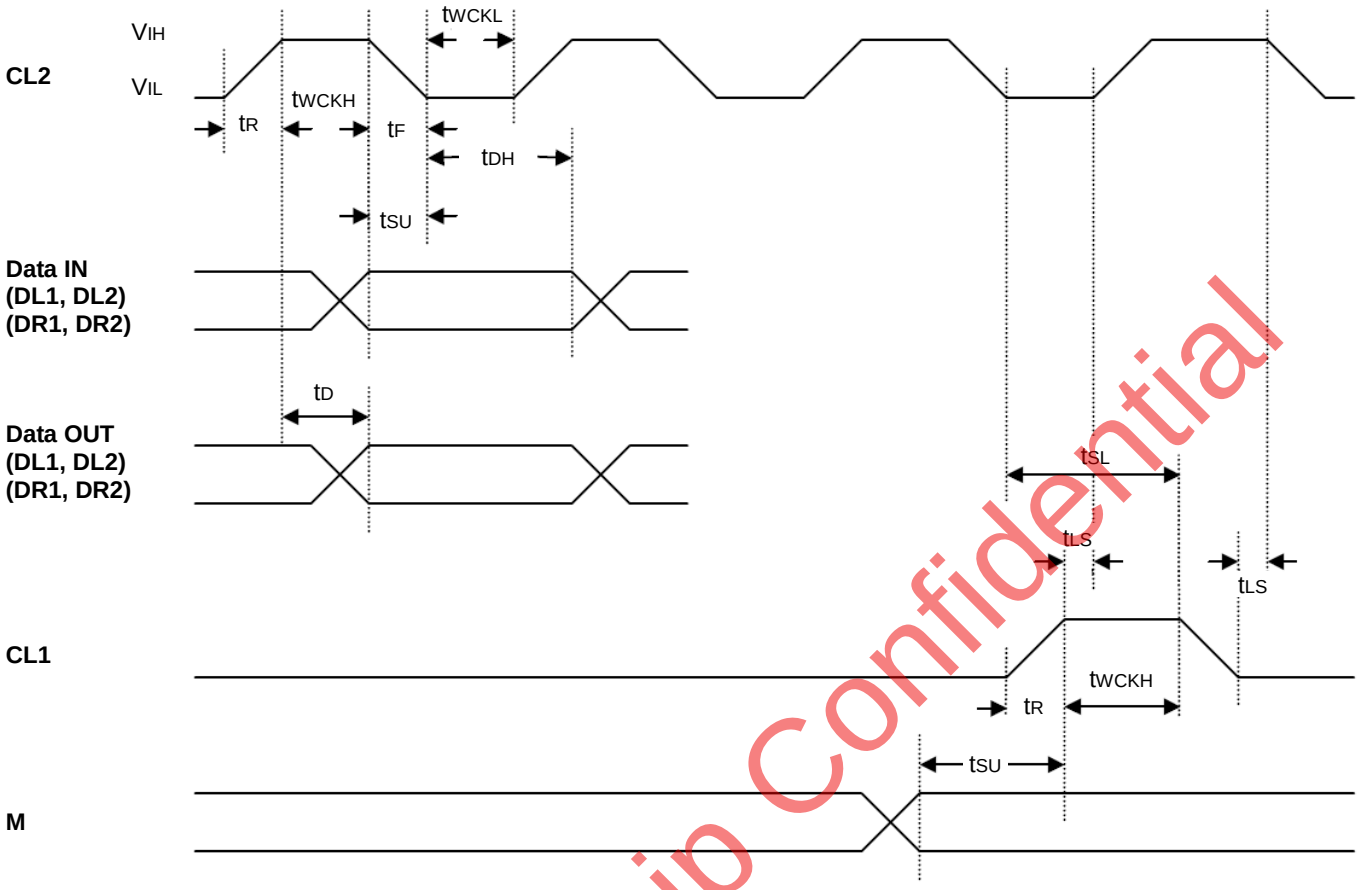
MAXIMUM RATING

Symbol	Parameter	Range	Unit
V_{DD}	Supply Voltage	–0.3 ~ +7.0	V
t_{OPR}	Operating Temperature	–40 ~ +90	°C
t_{STG}	Storage Temperature	–55 ~ +125	°C

DC CHARACTERISTICS

Symbol	Characteristics	Condition	Min.	Typical	Max.	Unit	Applicable Pins
V_{DD}	Operating Voltage		2.7	–	5.5	V	
V_{LCD}	Driver Supply Voltage	V_{DD}-V_{EE}	3	–	18	V	
V_{IH}	Input High Voltage		0.7V_{DD}	–	V_{DD}	V	CL1, CL2, M, SHL1, SHL2, DL1, DL2, DR1, DR2
V_{IL}	Input Low Voltage		0	–	0.3V_{DD}	V	
I_{LKG}	Input Leakage Current	Vin=0~V_{DD}	–5	–	5	uA	
V_{OH}	Output High Voltage	IOH=–0.4mA	V_{DD}–0.4	–	–	V	DL1, DL2, DR1, DR2, V1~V6, S[1]~S[40]
V_{OL}	Output Low Voltage	IOL=+0.4mA	–	–	0.4	V	
I_{DD}	Operating Current	FLC2=400kHz	–	100	300	uA	V_{DD}, V_{EE}
I_V	Leakage Current	V_{IN}=V_{DD}~V_{EE}	–10	–	10	uA	V1~V6

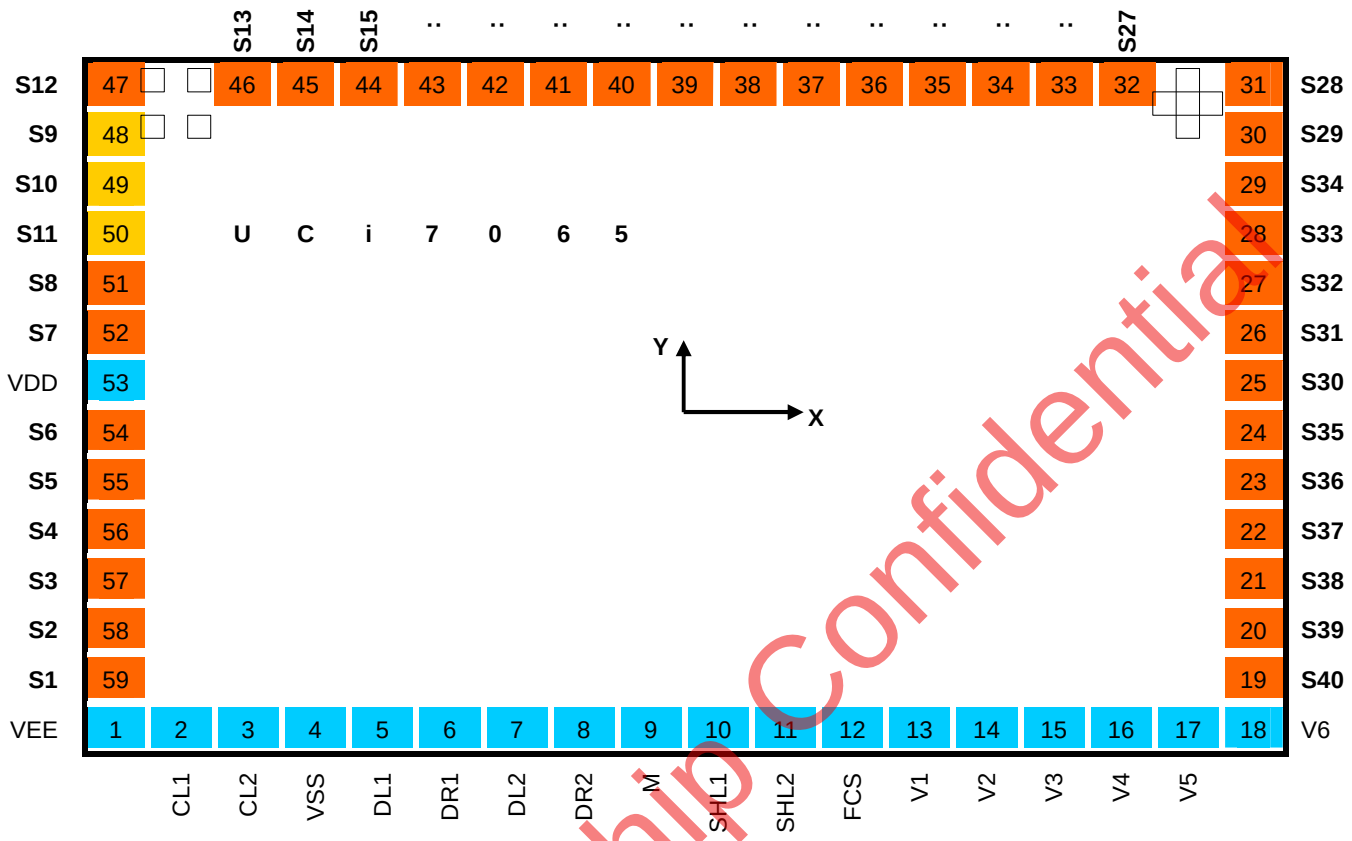
AC CHARACTERISTICS



Symbol	Signal	Condition	Min.	Max.	Unit	Applicable Pins
FCL	Data Shift Frequency		–	400	kHz	CL2
twckh	Clock High level Width		800	–	nS	CL1, CL2
twckl	Clock Low level Width		800	–	nS	CL2
tsl	Clock Set-up Time, CL2→CL1		500	–	nS	CL1, CL2
tls	Clock Set-up Time, CL1→CL2		500	–	nS	CL1, CL2
tr/tf	Clock Rise/Fall Time		–	200	nS	CL1, CL2
tsu	Data Set-up Time		300	–	nS	DL1, DL2, DR1, DR2
tdh	Data Hold Time		300	–	nS	DL1, DL2, DR1, DR2
td	Data Delay Time	CL=15pF	–	500	nS	DL1, DL2, DR1, DR2

PHYSICAL DIMENSION

Pad Location :



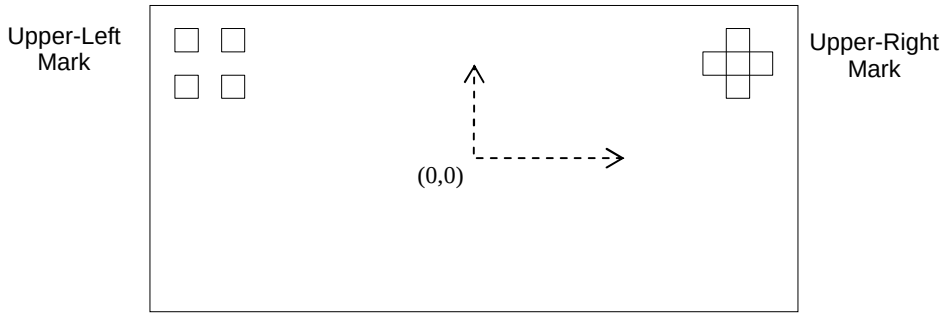
Note: Connect the substrate to VDD.

Die / Bump Information:

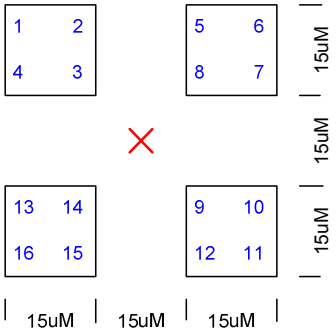
Die Size:	(1850μM ± 40μM) x (1440μM ± 40μM)
Die Thickness:	400μM ± 20μM
Die TTV:	DMAX – DMIN ≤ 2μM
Pad Size:	75μM x 80μM
Bump Pitch:	100μM
Coordinate origin:	Chip center
Pad reference:	Pad center

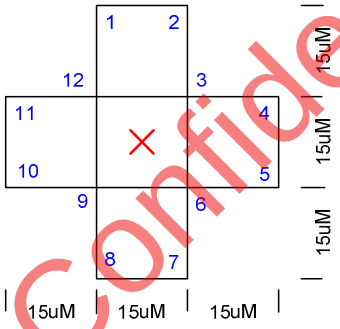
ALIGNMENT MARK

MARK LOCATION :



SHAPE :





COORDINATES :

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center (X)	-779	677.5	779.5	677.5
1	-801.5	700	772	700
2	-786.5	700	787	700
3	-786.5	685	787	685
4	-801.5	685	802	685
5	-771.5	700	802	670
6	-756.5	700	787	670
7	-756.5	685	787	655
8	-771.5	685	772	655
9	-771.5	670	772	670
10	-756.5	670	757	670
11	-756.5	655	757	685
12	-771.5	655	772	685
13	-801.5	670	–	–
14	-786.5	670	–	–
15	-786.5	655	–	–
16	-801.5	655	–	–

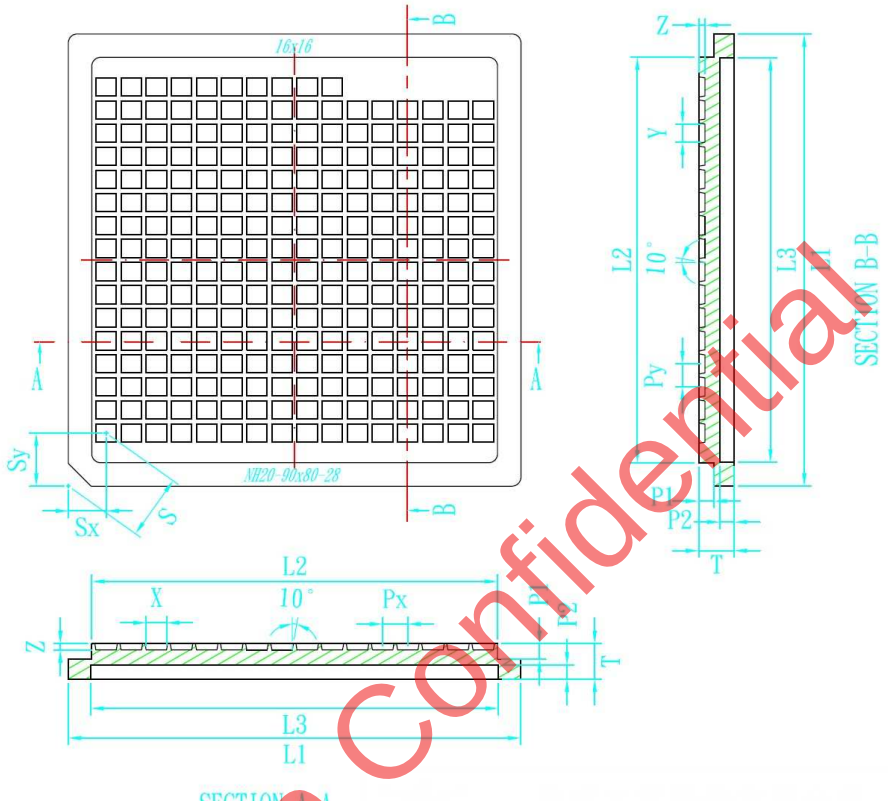
PAD COORDINATES

No	Pad	X	Y	W	H
1	VEE	-863	-639.5	80	75
2	CL1	-750	-658	75	80
3	CL2	-650	-658	75	80
4	VSS	-550	-658	75	80
5	DL1	-450	-658	75	80
6	DR1	-350	-658	75	80
7	DL2	-250	-658	75	80
8	DR2	-150	-658	75	80
9	M	-50	-658	75	80
10	SHL1	50	-658	75	80
11	SHL2	150	-658	75	80
12	FCS	250	-658	75	80
13	V1	350	-658	75	80
14	V2	450	-658	75	80
15	V3	550	-658	75	80
16	V4	650	-658	75	80
17	V5	750	-658	75	80
18	V6	863	-639.5	80	75
19	S40	863	-539.5	80	75
20	S39	863	-439.5	80	75
21	S38	863	-339.5	80	75
22	S37	863	-239.5	80	75
23	S36	863	-139.5	80	75
24	S35	863	-39.5	80	75
25	S30	863	60.5	80	75
26	S31	863	160.5	80	75
27	S32	863	260.5	80	75
28	S33	863	360.5	80	75
29	S34	863	460.5	80	75
30	S29	863	560.5	80	75

No	Pad	X	Y	W	H
31	S28	863	660.5	80	75
32	S27	702.5	658	75	80
33	S26	602.5	658	75	80
34	S25	502.5	658	75	80
35	S24	402.5	658	75	80
36	S23	302.5	658	75	80
37	S22	202.5	658	75	80
38	S21	102.5	658	75	80
39	S20	2.5	658	75	80
40	S19	-97.5	658	75	80
41	S18	-197.5	658	75	80
42	S17	-297.5	658	75	80
43	S16	-397.5	658	75	80
44	S15	-497.5	658	75	80
45	S14	-597.5	658	75	80
46	S13	-697.5	658	75	80
47	S12	-863	660.5	80	75
48	S9	-863	560.5	80	75
49	S10	-863	460.5	80	75
50	S11	-863	360.5	80	75
51	S8	-863	260.5	80	75
52	S7	-863	160.5	80	75
53	VDD	-863	60.5	80	75
54	S6	-863	-39.5	80	75
55	S5	-863	-139.5	80	75
56	S4	-863	-239.5	80	75
57	S3	-863	-339.5	80	75
58	S2	-863	-439.5	80	75
59	S1	-863	-539.5	80	75

TRAY INFORMATION

晶粒盤規格	90X80-28(橫)	
1	晶粒盤外圍尺寸 (L1)	50.75
2	晶粒盤外圍尺寸 (L2)	45.50
3	晶粒盤底部尺寸 (L3)	45.70
4	晶粒盤全高 (T)	4.00
5	第一晶穴中心X軸 (SX)	4.23
6	第一晶穴中心Y軸 (SY)	5.95
7	第一晶穴基準中心 (S)	7.30
8	晶穴寬度X軸 (X)	2.29
9	晶穴長度Y軸 (Y)	2.03
10	晶穴深度Z軸 (Z)	0.71
11	晶穴間距X軸 (Px)	2.82
12	晶穴間距Y軸 (Py)	2.59
13	晶穴數X軸 (Nx)	16
14	晶穴數Y軸 (Ny)	16
15	晶穴總數 (N)	250
16	晶粒盤內圍高 (P1)	1.76
17	晶粒盤底部深 (P2)	1.60



REVISION HISTORY

Revision	Description	Date
0.6	(First Release)	Nov. 29, 2013
0.8	Tray drawing is added.	Dec. 24, 2013