# Memristor

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A **memristor** (/ˈmɛmrɪstər/; a portmanteau of *memory resistor*) is a hypothetical non-linear passive two-terminal electrical component relating electric charge and magnetic flux linkage. It was envisioned, and its name coined, in 1971 by circuit theorist Leon Chua.[1] According to the characterizing mathematical relations, the memristor would hypothetically operate in the following way: The memristor's electrical resistance is not constant but depends on the history of current that had previously flowed through the device, i.e., its present resistance depends on how much electric charge has flowed in what direction through it in the past; the device remembers its history — the so-called *non-volatility property*.[2] When the electric power supply is turned off, the memristor remembers its most recent resistance until it is turned on again.[3][4]

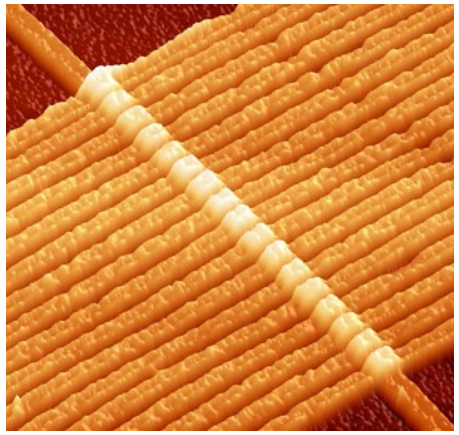
**Memristor**

| | |
|---|---|
| **Type** | Passive |
| **Working principle** | Memristance |
| **Invented** | Leon Chua (1971) |
| **Electronic symbol** | |

In 2008, a team at HP Labs claimed to have found Chua's missing memristor based on an analysis of a thin film of titanium dioxide thus connecting the operation of RRAM devices to the memristor concept; the HP result was published in *Nature*.[3] Following this claim, Leon Chua has argued that the memristor definition could be generalized to cover all forms of two-terminal non-volatile memory devices based on resistance switching effects.[2] There are, however, some serious doubts as to whether the memristor can actually exist in physical reality.[5][6][7] Additionally, some experimental evidence contradicts Chua's generalization since a non-passive nanobattery effect is observable in resistance switching memory.[8] Chua also argued that the memristor is the oldest known circuit element, with its effects predating the resistor, capacitor and inductor.[9]

These devices are intended for applications in nanoelectronic memories, computer logic and neuromorphic/neuromemristive computer architectures.[10] Commercial availability of memristor memory has been estimated as 2018.[11] In March 2012, a team of researchers from HRL Laboratories and the University of Michigan announced the first functioning memristor array built on a CMOS chip.[12]

## Contents



An array of 17 purpose-built oxygen-depleted titanium dioxide memristors built at HP Labs, imaged by an atomic force microscope. The wires are about 50 nm, or 150 atoms, wide.[13] Electric current through the memristors shifts the oxygen vacancies, causing a gradual and persistent change in electrical resistance.[14]

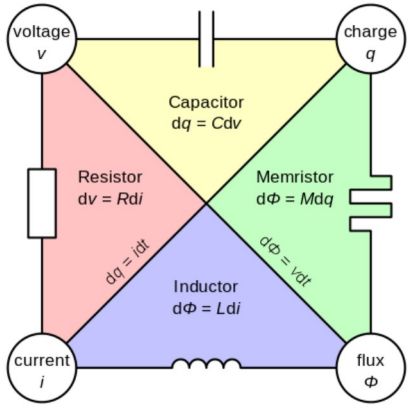
# Background

In his 1971 paper, Chua extrapolated a conceptual symmetry between the nonlinear resistor (voltage vs. current), nonlinear capacitor (voltage vs. charge) and nonlinear inductor (magnetic flux linkage vs. current). He then inferred the possibility of a memristor as another fundamental nonlinear circuit element linking magnetic flux and charge. In contrast to a linear (or nonlinear) resistor the memristor has a dynamic relationship between current and voltage including a memory of past voltages or currents. Other scientists had proposed dynamic memory resistors such as the memistor of Bernard Widrow, but Chua attempted to introduce mathematical generality.

Memristor resistance depends on the integral of the input applied to the terminals (rather than on the instantaneous value of the input as in a varistor).[3] Since the element "remembers" the amount of current that last passed through, it was tagged by Chua with the name "memristor". Another way of describing a memristor is as any passive two-terminal circuit element that maintains a functional relationship between the time integral of

current (called charge) and the time integral of voltage (often called flux, as it is related to magnetic flux). The slope of this function is called the *memristance M* and is similar to variable resistance.

The memristor definition is based solely on the fundamental circuit variables of current and voltage and their time-integrals, just like the resistor, capacitor and inductor. Unlike those three elements however, which are allowed in linear time-invariant or LTI system theory, memristors of interest have a dynamic function with memory and may be described as some function of net charge. There is no such thing as a standard memristor. Instead, each device implements a particular function, wherein the integral of voltage determines the integral of current, and vice versa. A linear time-invariant memristor, with a constant value for *M*, is simply a conventional resistor.[1] Manufactured devices are never purely memristors (*ideal memristor*), but also exhibit some capacitance and resistance.




Conceptual symmetries of resistor, capacitor, inductor, and memristor.

# Memristor definition and criticism

According to the original 1971 definition, the memristor was the fourth fundamental circuit element, forming a non-linear relationship between electric charge and magnetic flux linkage. In 2011 Chua argued for a broader definition that included all 2-terminal non-volatile memory devices based on resistance switching.[2] Williams argued that MRAM, phase change memory and RRAM were memristor technologies.[15] Some researchers argued that biological structures such as blood[16] and skin[17][18] fit the definition. Others argued that the memory device under development by HP Labs and other forms of RRAM were not memristors but rather part of a broader class of variable resistance systems[19] and that a broader definition of memristor is a scientifically unjustifiable land grab that favored HP's memristor patents.[20]

In 2011, Meuffels and Schroeder noted that one of the early memristor papers included a mistaken assumption regarding ionic conduction.[21] In 2012, Meuffels and Soni discussed some fundamental issues and problems in the realization of memristors.[5] They indicated inadequacies in the electrochemical modelling presented in the *Nature* paper "The missing memristor found"[3] because the impact of concentration polarization effects on the behavior of metal−$TiO_{2-x}$−metal structures under voltage or current stress was not considered. This critique was referred to by Valov *et al.*[8] in 2013.

In a kind of thought experiment, Meuffels and Soni[5] furthermore revealed a severe inconsistency: If a current-controlled memristor with the so-called *non-volatility property*[2] exists in physical reality, its behavior would violate Landauer's principle of the minimum amount of energy required to change "information" states of a system. This critique was finally adopted by Di Ventra and Pershin[6] in 2013.

Within this context, Meuffels and Soni[5] pointed to a fundamental thermodynamic principle: Non-volatile information storage requires the existence of free energy barriers that separate the distinct internal memory states of a system from each other; otherwise, one would be faced with an "indifferent" situation and the system would arbitrarily fluctuate from one memory state to another just under the influence of thermal fluctuations. When unprotected against thermal fluctuations, the internal memory states exhibit some diffusive dynamics which causes state degradation.[6] The free energy barriers must therefore be high enough to ensure a low bit-error probability of bit operation.[22] Consequently, there is always a lower

limit of energy requirement – depending on the required bit-error probability – for intentionally changing a bit value in any memory device.[22][23]

In the general concept of memristive system the defining equations are (see: #Theory):

$$y(t) = g(\mathbf{x}, u, t)u(t),$$
$$\dot{\mathbf{x}} = f(\mathbf{x}, u, t)$$

Here, *u(t)* is an input signal and *y(t)* an output signal. The vector **x** represents a set of *n* state variables describing the different internal memory states of the device. $\dot{\mathbf{x}}$ is the time-dependent rate of change of the state vector **x** with time.

When one wants to go beyond mere curve fitting and aims at a real physical modeling of non-volatile memory elements, e.g., resistive random-access memory devices, one has to keep an eye on the aforementioned physical correlations. To check the adequacy of the proposed model and its resulting state equations, the input signal *u(t)* can be superposed with a stochastic term $\xi(t)$ which takes into account the existence of inevitable thermal fluctuations. The dynamic state equation in its general form then finally reads:

$$\dot{\mathbf{x}} = f(\mathbf{x}, u(t) + \xi(t), t)$$

Here, $\xi(t)$ is, e.g., white Gaussian current or voltage noise. On base of an analytical or numerical analysis of the time-dependent response of the system towards noise, a decision on the physical validity of the modeling approach can be made, e.g., would the system be able to retain its memory states in power-off mode?

Such an analysis was performed by Di Ventra and Pershin[6] with regard to the genuine current-controlled memristor. As the proposed dynamic state equation provides no physical mechanism enabling such a memristor to cope with inevitable thermal fluctuations, a current-controlled memristor would erratically change its state in course of time just under the influence of current noise.[6][24] Di Ventra and Pershin[6] thus concluded that memristors whose resistance (memory) states depend solely on the current or voltage history would be unable to protect their memory states against unavoidable Johnson–Nyquist noise and permanently suffer from information loss, a so-called "stochastic catastrophe". A current-controlled memristor can thus not exist as a solid state device in physical reality.

The above-mentioned thermodynamic principle furthermore implies that the operation of 2-terminal, non-volatile memory devices (e.g. "resistance switching" memory devices (RRAM)) cannot be associated with the memristor concept, i.e., such devices cannot per se remember their current or voltage history. Transitions between distinct internal memory or resistance states are of probabilistic nature. The probability for a transition from state {**i**} to state {**j**} depends on the height of the free energy barrier between both states. The transition probability can thus be influenced by suitably driving the memory device, i.e., by "lowering" the free energy barrier for the transition {**i**} → {**j**} by means of, for example, an externally applied bias.

A "resistance switching" event can simply be enforced by setting the external bias to a value above a certain threshold value. This is the trivial case, i.e., the free energy barrier for the transition {**i**} → {**j**} is reduced to zero. In case one applies biases below the threshold value, there is still a finite probability that the device will switch in course of time (triggered by a random thermal fluctuation), but – as one is dealing with probabilistic

processes – it is impossible to predict when the switching event will occur. That is the basic reason for the stochastic nature of all observed resistance switching (RRAM) processes. If the free energy barriers are not high enough, the memory device can even switch without having to do anything.

When a 2-terminal, non-volatile memory device is found to be in a distinct resistance state {**j**}, there exists therefore no physical one-to-one relationship between its present state and its foregoing voltage history. The switching behavior of individual non-volatile memory devices can thus per se not be described within the mathematical framework proposed for memristor/memristive systems.

An extra thermodynamic curiosity arises from the definition that memristors/memristive devices should energetically act like resistors. The instantaneous electrical power entering such a device is completely dissipated as Joule heat to the surrounding, viz. no extra energy remains in the system after it has been brought from one resistance state $\mathbf{x_i}$ to another one $\mathbf{x_j}$. Thus, the internal energy of the memristor device in state $\mathbf{x_i}$, U(V, T, $\mathbf{x_i}$), would be the same as in state $\mathbf{x_j}$, U(V, T, $\mathbf{x_j}$), even though these different states would give rise to different device's resistances which itself must be caused by physical alterations of the device's material.

Other researchers noted that memristor models based on the assumption of linear ionic drift do not account for asymmetry between set time (high-to-low resistance switching) and reset time (low-to-high resistance switching) and do not provide ionic mobility values consistent with experimental data. Non-linear ionic drift models have been proposed to compensate for this deficiency.[25]

A 2014 article from researchers of ReRAM concluded that Strukov's (HP's) initial/basic memristor modelling equations do not reflect the actual device physics well, whereas subsequent (physics-based) models such as Pickett's model or Menzel's ECM model (Menzel is a co-author of that paper) have adequate predictability but are computationally prohibitive. As of 2014, the search continues for a model that balances these issues; the article identifies Chang's and Yakopcic's models as potentially good compromises.[26]

Martin Reynolds, an electrical engineering analyst with research outfit Gartner, commented that while HP was being sloppy in calling their device a memristor, critics were being pedantic in saying it was not a memristor.[27]

In the article "The Missing Memristor has Not been Found", published in *Scientific Reports* in 2015 by Vongehr and Meng,[7] it was shown that the real memristor defined in 1971 is not possible without using magnetic induction. This was illustrated by constructing a mechanical analog of the memristor and then analytically showing that the mechanical memristor cannot be constructed without using an inertial mass. As it is well known that the mechanical equivalent of an electrical inductor is mass, it proves that memristors are not possible without using magnetic induction. Thus, it can be argued that the variable resistance devices, such as the RRAMs, and the conceptual memristors may have no equivalence at all.[7][28]

# Experimental tests for memristors

Chua suggested experimental tests to determine if a device may properly be categorized as a memristor:[29]

- The Lissajous curve in the voltage-current plane is a pinched hysteresis loop when driven by any bipolar periodic voltage or current without respect to initial conditions.

- The area of each lobe of the pinched hysteresis loop shrinks as the frequency of the forcing signal increases.
- As the frequency tends to infinity, the hysteresis loop degenerates to a straight line through the origin, whose slope depends on the amplitude and shape of the forcing signal.

According to Chua[30][31] all resistive switching memories including ReRAM, MRAM and phase change memory meet these criteria and are memristors. However, the lack of data for the Lissajous curves over a range of initial conditions or over a range of frequencies, complicates assessments of this claim.

Experimental evidence shows that redox-based resistance memory (ReRAM) includes a nanobattery effect that is contrary to Chua's memristor model. This indicates that the memristor theory needs to be extended or corrected to enable accurate ReRAM modeling.[8]

# Theory

The memristor was originally defined in terms of a non-linear functional relationship between magnetic flux linkage $\Phi_{\mathrm{m}}(t)$ and the amount of electric charge that has flowed, *q(t)*:[1]

$$f(\Phi_{\mathrm{m}}(t), q(t)) = 0$$

The *magnetic flux linkage*, $\Phi_{\mathrm{m}}$, is generalized from the circuit characteristic of an inductor. It *does not* represent a magnetic field here. Its physical meaning is discussed below. The symbol $\Phi_{\mathrm{m}}$ may be regarded as the integral of voltage over time.[32]

In the relationship between $\Phi_{\mathrm{m}}$ and q, the derivative of one with respect to the other depends on the value of one or the other, and so each memristor is characterized by its memristance function describing the charge-dependent rate of change of flux with charge.

$$M(q) = \frac{\mathrm{d}\Phi_m}{\mathrm{d}q}$$

Substituting the flux as the time integral of the voltage, and charge as the time integral of current, the more convenient form is

$$M(q(t)) = \frac{\mathrm{d}\Phi_m/\mathrm{d}t}{\mathrm{d}q/\mathrm{d}t} = \frac{V(t)}{I(t)}$$

To relate the memristor to the resistor, capacitor, and inductor, it is helpful to isolate the term $M(q)$, which characterizes the device, and write it as a differential equation.

| Device | Characteristic property (units) | Differential equation |
|---|---|---|
| Resistor (R) | Resistance (V / A, or ohm, Ω) | $R = dV / dI$ |
| Capacitor (C) | Capacitance (C / V, or farad) | $C = dq / dV$ |
| Inductor (L) | Inductance (Wb / A, or henry) | $L = d\Phi_m / dI$ |
| Memristor (M) | Memristance (Wb / C, or ohm) | $M = d\Phi_m / dq$ |

The above table covers all meaningful ratios of differentials of $I$, $Q$, $\Phi_m$, and $V$. No device can relate $dI$ to $dq$, or $d\Phi_m$ to $dV$, because $I$ is the derivative of $Q$ and $\Phi_m$ is the integral of $V$.

It can be inferred from this that memristance is charge-dependent resistance. If $M(q(t))$ is a constant, then we obtain Ohm's Law $R(t) = V(t)/ I(t)$. If $M(q(t))$ is nontrivial, however, the equation is not equivalent because $q(t)$ and $M(q(t))$ can vary with time. Solving for voltage as a function of time produces

$$V(t) = M(q(t))I(t)$$

This equation reveals that memristance defines a linear relationship between current and voltage, as long as $M$ does not vary with charge. Nonzero current implies time varying charge. Alternating current, however, may reveal the linear dependence in circuit operation by inducing a measurable voltage without net charge movement—as long as the maximum change in $q$ does not cause much change in $M$.

Furthermore, the memristor is static if no current is applied. If $I(t) = 0$, we find $V(t) = 0$ and $M(t)$ is constant. This is the essence of the memory effect.

The power consumption characteristic recalls that of a resistor, $I^2R$.

$$P(t) = I(t)V(t) = I^2(t)M(q(t))$$

As long as $M(q(t))$ varies little, such as under alternating current, the memristor will appear as a constant resistor. If $M(q(t))$ increases rapidly, however, current and power consumption will quickly stop.

$M(q)$ is physically restricted to be positive for all values of $q$ (assuming the device is passive and does not become superconductive at some $q$). A negative value would mean that it would perpetually supply energy when operated with alternating current.

In 2008 researchers from HP Labs introduced a model for a memristance function based on thin films of titanium dioxide.[3] For $R_{ON} \ll R_{OFF}$ the memristance function was determined to be

$$M(q(t)) = R_{\mathrm{OFF}} \cdot \left(1 - \frac{\mu_v R_{\mathrm{ON}}}{D^2} q(t)\right)$$

where $R_{OFF}$ represents the high resistance state, $R_{ON}$ represents the low resistance state, $\mu_v$ represents the mobility of dopants in the thin film, and D represents the film thickness. The HP Labs group noted that "window functions" were necessary to compensate for differences between experimental measurements and their memristor model due to nonlinear ionic drift and boundary effects.

## Operation as a switch

For some memristors, applied current or voltage causes substantial change in resistance. Such devices may be characterized as switches by investigating the time and energy that must be spent to achieve a desired change in resistance. This assumes that the applied voltage remains constant. Solving for energy dissipation during a single switching event reveals that for a memristor to switch from $R_{on}$ to $R_{off}$ in time $T_{on}$ to $T_{off}$, the charge must change by $\Delta Q = Q_{on} - Q_{off}$.

$$E_{\mathrm{switch}} = V^2 \int_{T_{\mathrm{off}}}^{T_{\mathrm{on}}} \frac{\mathrm{d}t}{M(q(t))} = V^2 \int_{Q_{\mathrm{off}}}^{Q_{\mathrm{on}}} \frac{\mathrm{d}q}{I(q)M(q)} = V^2 \int_{Q_{\mathrm{off}}}^{Q_{\mathrm{on}}} \frac{\mathrm{d}q}{V(q)} = V\Delta Q$$

Substituting $V=I(q)M(q)$, and then $\int \mathrm{d}q/V = \Delta Q/V$ for constant $V$To produces the final expression. This power characteristic differs fundamentally from that of a metal oxide semiconductor transistor, which is capacitor-based. Unlike the transistor, the final state of the memristor in terms of charge does not depend on bias voltage.

The type of memristor described by Williams ceases to be ideal after switching over its entire resistance range, creating hysteresis, also called the "hard-switching regime".[3] Another kind of switch would have a cyclic $M(q)$ so that each *off-on* event would be followed by an *on-off* event under constant bias. Such a device would act as a memristor under all conditions, but would be less practical.

## Memristive systems

The memristor was generalized to memristive systems in Chua's 1976 paper.[29] Whereas a memristor has mathematically scalar state, a system has vector state. The number of state variables is independent of the number of terminals.

Chua applied this model to empirically-observed phenomena, including the Hodgkin–Huxley model of the axon and a thermistor at constant ambient temperature. He also described memristive systems in terms of energy storage and easily observed electrical characteristics. These characteristics might match resistive random-access memory relating the theory to active areas of research.

In the more general concept of an *n*-th order memristive system the defining equations are

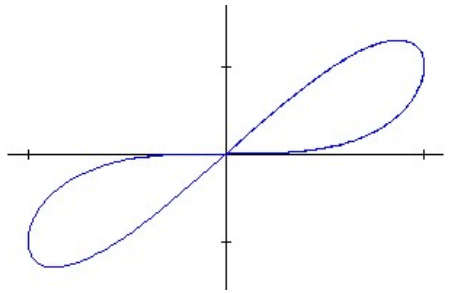
$$y(t) = g(\mathbf{x}, u, t)u(t),$$
$$\dot{\mathbf{x}} = f(\mathbf{x}, u, t)$$

where *u(t)* is an input signal, *y(t)* is an output signal, the vector **x** represents a set of *n* state variables describing the device, and *g* and *f* are continuous functions. For a current-controlled memristive system the signal *u(t)* represents the current signal *i(t)* and the signal *y(t)* represents the voltage signal *v(t)*. For a voltage-controlled memristive system the signal *u(t)* represents the voltage signal *v(t)* and the signal *y(t)* represents the current signal *i(t)*.

The *pure* memristor is a particular case of these equations, namely when *x* depends only on charge (**x**=*q*) and since the charge is related to the current via the time derivative d*q*/d*t*=*i(t)*. Thus for *pure* memristors *f* (i.e. the rate of change of the state) must be equal or proportional to the current *i(t)* .

## Pinched hysteresis

One of the resulting properties of memristors and memristive systems is the existence of a pinched hysteresis effect.[33] For a current-controlled memristive system, the input *u(t)* is the current *i(t)*, the output *y(t)* is the voltage *v(t)*, and the slope of the curve represents the electrical resistance. The change in slope of the pinched hysteresis curves demonstrates switching between different resistance states which is a phenomenon central to ReRAM and other forms of two-terminal resistance memory. At high frequencies, memristive theory predicts the pinched hysteresis effect will degenerate, resulting in a straight line representative of a linear resistor. It has been proven that some types of non-crossing pinched hysteresis curves (denoted Type-II) cannot be described by memristors.[34]



Example of pinched hysteresis curve, V versus I

## Extended memristive systems

Some researchers have raised the question of the scientific legitimacy of HP's memristor models in explaining the behavior of ReRAM.[19][20] and have suggested extended memristive models to remedy perceived deficiencies.[8]

One example[35] attempts to extend the memristive systems framework by including dynamic systems incorporating higher-order derivatives of the input signal *u(t)* as a series expansion

$$y(t) = g_0(\mathbf{x}, u)u(t) + g_1(\mathbf{x}, u)\frac{\mathrm{d}^2 u}{\mathrm{d}t^2} + g_2(\mathbf{x}, u)\frac{\mathrm{d}^4 u}{\mathrm{d}t^4} + \ldots + g_m(\mathbf{x}, u)\frac{\mathrm{d}^{2m} u}{\mathrm{d}t^{2m}},$$
$$\dot{\mathbf{x}} = f(\mathbf{x}, u)$$

where *m* is a positive integer, *u(t)* is an input signal, *y(t)* is an output signal, the vector **x** represents a set of *n* state variables describing the device, and the functions *g* and *f* are continuous functions. This equation produces the same zero-crossing hysteresis curves as memristive systems but with a different frequency response than that predicted by memristive systems.

Another example suggests including an offset value *a* to account for an observed nanobattery effect which violates the predicted zero-crossing pinched hysteresis effect.[8]

$$y(t) = g_0(\mathbf{x}, u)(u(t) - a),$$
$$\dot{\mathbf{x}} = f(\mathbf{x}, u)$$

# Implementations

## Self Directed Channel Memristor

In 2017, Campbell formally introduced the Self-Directed Channel (SDC) memristor.[36] The SDC device is the first memristive device available commercially to researchers, students and electronics enthusiast worldwide.[37] The SDC device is operational immediately after fabrication. Switching occurs in the Ge2Se3 active layer, where a key feature of the device, Ge-Ge homopolar bonds, are found. The three layers consisting of Ge2Se3/Ag/Ge2Se3, directly below the top tungsten electrode, mix together during deposition and jointly form the silver-source layer. This silver-source layer is not in direct contact with the active layer. This allows the device to have significantly higher processing and operating temperatures (above 250 °C and at least 150 °C, respectively) since silver does not migrate into the active layer at high temperatures, and the active layer maintains a high glass transition temperature (~350 °C). These processing and operating temperatures are higher than most ion-conducting chalcogenide device types, including the S-based glasses (e.g. GeS) that need to be photodoped or thermally annealed. It is a combination of these factors that allow the SDC device to operate over a wide range of temperatures, including long-term continuous operation at 150 °C.

## Titanium dioxide memristor

Interest in the memristor revived when an experimental solid state version was reported by R. Stanley Williams of Hewlett Packard in 2007.[38][39][40] The article was the first to demonstrate that a solid-state device could have the characteristics of a memristor based on the behavior of nanoscale thin films. The device neither uses magnetic flux as the theoretical memristor suggested, nor stores charge as a capacitor does, but instead achieves a resistance dependent on the history of current.

Although not cited in HP's initial reports on their $TiO_2$ memristor, the resistance switching characteristics of titanium dioxide were originally described in the 1960s.[41]

The HP device is composed of a thin (50 nm) titanium dioxide film between two 5 nm thick electrodes, one titanium, the other platinum. Initially, there are two layers to the titanium dioxide film, one of which has a slight depletion of oxygen atoms. The oxygen vacancies act as charge carriers, meaning that the depleted layer has a much lower resistance than the non-depleted layer. When an electric field is applied, the oxygen vacancies drift (see *Fast ion conductor*), changing the boundary between the high-resistance and low-resistance layers. Thus the resistance of the film as a whole is dependent on how much charge has been passed through it in a particular direction, which is reversible by changing the direction of current.[3] Since the HP device displays fast ion conduction at nanoscale, it is considered a nanoionic device.[42]

Memristance is displayed only when both the doped layer and depleted layer contribute to resistance. When enough charge has passed through the memristor that the ions can no longer move, the device enters hysteresis. It ceases to integrate $q=\int I\mathrm{d}t$, but rather keeps $q$ at an upper bound and $M$ fixed, thus acting as a constant resistor until current is reversed.

Memory applications of thin-film oxides had been an area of active investigation for some time. IBM published an article in 2000 regarding structures similar to that described by Williams.[43] Samsung has a U.S. patent for oxide-vacancy based switches similar to that described by Williams.[44] Williams also has a U.S. patent application related to the memristor construction.[45]

In April 2010, HP labs announced that they had practical memristors working at 1 ns (~1 GHz) switching times and 3 nm by 3 nm sizes,[46] which bodes well for the future of the technology.[47] At these densities it could easily rival the current sub-25 nm flash memory technology.

## Polymeric memristor

In 2004, Krieger and Spitzer described dynamic doping of polymer and inorganic dielectric-like materials that improved the switching characteristics and retention required to create functioning nonvolatile memory cells.[48] They used a passive layer between electrode and active thin films, which enhanced the extraction of ions from the electrode. It is possible to use fast ion conductor as this passive layer, which allows a significant reduction of the ionic extraction field.

In July 2008, Erokhin and Fontana claimed to have developed a polymeric memristor before the more recently announced titanium dioxide memristor.[49]

In 2010, Alibart, Gamrat, Vuillaume et al.[50] introduced a new hybrid organic/nanoparticle device (the NOMFET : Nanoparticle Organic Memory Field Effect Transistor), which behaves as a memristor [51] and which exhibits the main behavior of a biological spiking synapse.This device, also called synapstor (synapse transistor), was used to demonstrate a neuro-inspired circuit (associative memory showing a pavlovian learning) [52]

In 2012, Crupi, Pradhan and Tozer described a proof of concept design to create neural synaptic memory circuits using organic ion-based memristors.[53] The synapse circuit demonstrated long-term potentiation for learning as well as inactivity based forgetting. Using a grid of circuits, a pattern of light was stored and later recalled. This mimics the behavior of the V1 neurons in the primary visual cortex that act as spatiotemporal filters that process visual signals such as edges and moving lines.

## Layered memristor

In 2014, Bessonov et al. reported a flexible memristive device comprising a $MoO_x/MoS_2$ heterostructure sandwiched between silver electrodes on a plastic foil.[54] The fabrication method is entirely based on printing and solution-processing technologies using two-dimensional layered transition metal dichalcogenides (TMDs). The memristors are mechanically flexible, optically transparent and produced at low cost. The memristive behaviour of switches was found to be accompanied by a prominent memcapacitive effect. High switching performance, demonstrated synaptic plasticity and sustainability to mechanical deformations promise to emulate the appealing characteristics of biological neural systems in novel computing technologies.

## Ferroelectric memristor

The ferroelectric memristor[55] is based on a thin ferroelectric barrier sandwiched between two metallic electrodes. Switching the polarization of the ferroelectric material by applying a positive or negative voltage across the junction can lead to a two order of magnitude resistance variation: $R_{OFF} \gg R_{ON}$ (an effect called Tunnel Electro-Resistance). In general, the polarization does not switch abruptly. The reversal occurs gradually through the nucleation and growth of ferroelectric domains with opposite polarization. During this process, the resistance is neither $R_{ON}$ or $R_{OFF}$, but in between. When the voltage is cycled, the ferroelectric domain configuration evolves, allowing a fine tuning of the resistance value. The ferroelectric memristor's main advantages are that ferroelectric domain dynamics can be tuned, offering a way to engineer the memristor response, and that the resistance variations are due to purely electronic phenomena, aiding device reliability, as no deep change to the material structure is involved.

## Carbon nanotube memristor

In 2013, Ageev, Blinov et al.[56] reported observing memristor effect in structure based on vertically aligned carbon nanotubes studying bundles of CNT by scanning tunneling microscope.

## Spin memristive systems

### Spintronic memristor

Chen and Wang, researchers at disk-drive manufacturer Seagate Technology described three examples of possible magnetic memristors.[57] In one device resistance occurs when the spin of electrons in one section of the device points in a different direction from those in another section, creating a "domain wall", a boundary between the two sections. Electrons flowing into the device have a certain spin, which alters the device's magnetization state. Changing the magnetization, in turn, moves the domain wall and changes the resistance. The work's significance led to an interview by IEEE Spectrum.[58] A first experimental proof of the spintronic memristor based on domain wall motion by spin currents in a magnetic tunnel junction was given in 2011.[59]

### Memristance in a magnetic tunnel junction

The magnetic tunnel junction has been proposed to act as a memristor through several potentially complementary mechanisms, both extrinsic (redox reactions, charge trapping/detrapping and electromigration within the barrier) and intrinsic (spin-transfer torque).

#### Extrinsic Mechanism

Based on research performed between 1999 and 2003, Bowen et al. published experiments in 2006 on a magnetic tunnel junction (MTJ) endowed with bi-stable spin-dependent states[60](resistive switching). The MTJ consists in a SrTiO3 (STO) tunnel barrier that separates half-metallic oxide LSMO and ferromagnetic metal CoCr electrodes. The MTJ's usual two device resistance states, characterized by a parallel or antiparallel alignment of

electrode magnetization, are altered by applying an electric field. When the electric field is applied from the CoCr to the LSMO electrode, the tunnel magnetoresistance (TMR) ratio is positive. When the direction of electric field is reversed, the TMR is negative. In both cases, large amplitudes of TMR on the order of 30% are found. Since a fully spin-polarized current flows from the half-metallic LSMO electrode, within the Julliere model, this sign change suggests a sign change in the effective spin polarization of the STO/CoCr interface. The origin to this multistate effect lies with the observed migration of Cr into the barrier and its state of oxidation. The sign change of TMR can originate from modifications to the STO/CoCr interface density of states, as well as from changes to the tunneling landscape at the STO/CoCr interface induced by CrOx redox reactions.

Reports on MgO-based memristive switching within MgO-based MTJs appeared starting in 2008[61] and 2009.[62] While the drift of oxygen vacancies within the insulating MgO layer has been proposed to describe the observed memristive effects,[62] another explanation could be charge trapping/detrapping on the localized states of oxygen vacancies[63] and its impact[64] on spintronics. This highlights the importance of understanding what role oxygen vacancies play in the memristive operation of devices that deploy complex oxides with an intrinsic property such as ferroelectricity[65] or multiferroicity.[66]

#### Intrinsic Mechanism

The magnetization state of a MTJ can be controlled by Spin-transfer torque, and can thus, through this intrinsic physical mechanism, exhibit memristive behavior. This spin torque is induced by current flowing through the junction, and leads to an efficient means of achieving a MRAM. However, the length of time the current flows through the junction determines the amount of current needed, i.e., charge is the key variable.[67]

The combination of intrinsic (spin-transfer torque) and extrinsic (resistive switching) mechanisms naturally leads to a second-order memristive system described by the state vector $\mathbf{x} = (x_1,x_2)$, where $x_1$ describes the magnetic state of the electrodes and $x_2$ denotes the resistive state of the MgO barrier. In this case the change of $x_1$ is current-controlled (spin torque is due to a high current density) whereas the change of $x_2$ is voltage-controlled (the drift of oxygen vacancies is due to high electric fields). The presence of both effects in a memristive magnetic tunnel junction led to the idea of a nanoscopic synapse-neuron system.[68]

### Spin memristive system

A fundamentally different mechanism for memristive behavior has been proposed by Pershin[69] and Di Ventra.[70][71] The authors show that certain types of semiconductor spintronic structures belong to a broad class of memristive systems as defined by Chua and Kang.[29] The mechanism of memristive behavior in such structures is based entirely on the electron spin degree of freedom which allows for a more convenient control than the ionic transport in nanostructures. When an external control parameter (such as voltage) is changed, the adjustment of electron spin polarization is delayed because of the diffusion and relaxation processes causing hysteresis. This result was anticipated in the study of spin extraction at semiconductor/ferromagnet interfaces,[72] but was not described in terms of memristive behavior. On a short time scale, these structures behave almost as an ideal memristor.[1] This result broadens the possible range of applications of semiconductor spintronics and makes a step forward in future practical applications.

# Applications

Williams' solid-state memristors can be combined into devices called crossbar latches, which could replace transistors in future computers, given their much higher circuit density.

They can potentially be fashioned into non-volatile solid-state memory, which would allow greater data density than hard drives with access times similar to DRAM, replacing both components.[14] HP prototyped a crossbar latch memory that can fit 100 gigabits in a square centimeter,[73] and proposed a scalable 3D design (consisting of up to 1000 layers or 1 petabit per $cm^3$).[74] In May 2008 HP reported that its device reaches currently about one-tenth the speed of DRAM.[75] The devices' resistance would be read with alternating current so that the stored value would not be affected.[76] In May 2012 it was reported that access time had been improved to 90 nanoseconds if not faster, approximately one hundred times faster than contemporaneous flash memory, while using one percent as much energy.[77]

Memristor patents include applications in programmable logic,[78] signal processing,[79] neural networks,[80] control systems,[81] reconfigurable computing,[82] brain-computer interfaces[83] and RFID.[84] Memristive devices are potentially used for stateful logic implication, allowing a replacement for CMOS-based logic computation. Several early works in this direction are reported.[85] [86]

In 2009, a simple electronic circuit[87] consisting of an LC network and a memristor was used to model experiments on adaptive behavior of unicellular organisms.[88] It was shown that subjected to a train of periodic pulses, the circuit learns and anticipates the next pulse similar to the behavior of slime molds *Physarum polycephalum* where the viscosity of channels in the cytoplasm responds to periodic environment changes.[88] Applications of such circuits may include, e.g., pattern recognition. The DARPA SyNAPSE project funded HP Labs, in collaboration with the Boston University Neuromorphics Lab, has been developing neuromorphic architectures which may be based on memristive systems. In 2010, Versace and Chandler described the MoNETA (Modular Neural Exploring Traveling Agent) model.[89] MoNETA is the first large-scale neural network model to implement whole-brain circuits to power a virtual and robotic agent using memristive hardware.[90] Application of the memristor crossbar structure in the construction of an analog soft computing system was demonstrated by Merrikh-Bayat and Shouraki.[91] In 2011 they showed[92] how memristor crossbars can be combined with fuzzy logic to create an analog memristive neuro-fuzzy computing system with fuzzy input and output terminals. Learning is based on the creation of fuzzy relations inspired from Hebbian learning rule.

In 2013 Leon Chua published a tutorial underlining the broad span of complex phenomena and applications that memristors span and how they can be used as non-volatile analog memories and can mimic classic habituation and learning phenomena.[93]

According to Allied Market Research memristor market was worth $3.2 million in 2015 and will be worth $79.0 million by 2022.[94]

# Memcapacitors and meminductors

In 2009, Di Ventra, Pershin and Chua extended[95] the notion of memristive systems to capacitive and inductive elements in the form of memcapacitors and meminductors, whose properties depend on the state and history of the system, further extended in 2013 by Di Ventra and Pershin.[6]

## Memfractance and memfractor, 2nd and 3rd order memristor, memcapacitor and meminductor

In September 2014, Mohamed-Salah Abdelouahab, Rene Lozi and Leon Chua, published a general theory of 1st, 2nd, 3rd order and nth order memristive element using fractional derivatives.[96]

# Timeline

### 1971

Leon Chua postulated a new two-terminal circuit element characterized by a relationship between charge and flux linkage as a fourth fundamental circuit element.[1]

### 1976

Chua and his student Sung Mo Kang generalized the theory of memristors and memristive systems including a property of zero crossing in the Lissajous curve characterizing current vs. voltage behavior.[29]

### 2008

On May 1 Strukov, Snider, Stewart and Williams published an article in Nature identifying a link between the 2-terminal resistance switching behavior found in nanoscale systems and memristors.[3]

### 2009

On January 23 Di Ventra, Pershin and Chua extended the notion of memristive systems to capacitive and inductive elements, namely capacitors and inductors whose properties depend on the state and history of the system.[95]

### 2015

On July 7, 2015 Knowm Inc announced Self Directed Channel (SDC) memristors commercially.[97]

# See also

- Hybrid Memory Cube
- 3D XPoint
- Memistor
- Electrical element
- List of emerging technologies
- Physical neural network
- RRAM

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- Andrew Adamatzky and Leon Chua, eds. (2013). *Memristor Networks*. Springer. ISBN 978-3-319-02630-5.
- Keith Atkin (2013), "An introduction to the memristor", *Phys. Educ.* **48** 317 doi:10.1088/0031-9120/48/3/317 (https://dx.doi.org/10.1088%2F0031-9120%2F48%2F3%2F317). One of the relatively simple experiments described in this paper has been reproduced by Chris Winstead (https://www.bawker.net/display/73b88af777174bb18de3b26e8519da1c2607e91306ce386cf31d0920c2b3a165@www.bawker.net).
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# External links

- Finding the missing memristor (https://www.youtube.com/watch?v=n3XzuBt54ig) on YouTube
- Interactive database of memristor papers (2013) (http://memlinks.eu)
- Simonite, Tom (April 21, 2015). "Machine Dreams" (http://www.technologyreview.com/featuredstory/536786/machine-dreams). Technology Review. Retrieved April 2015. Check date values in: `|access-date=` (help)

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