FET AMPLIFIERS AND SWITCHING CIRCUITS

Lecture 6

OVERVIEW

- JFET Amplifier Operation
- DC Analysis
- AC Analysis
- D-MOSFET Amplifier
- E-MOSFET Amplifier
- MOSFET Analog Switching
- MOSFET Digital Switching
- MOSFET in Power Switching

JFET AMPLIFIER OPERATION

- A *common-source* JFET Amplifier is one in which the AC input signal is applied to the gate and the AC output signal is taken from the drain.
- The source terminal is common to both the input and output signal.
- A common-source amplifier either has no source resistor or has a bypassed source resistor, so the source is connected to AC ground.

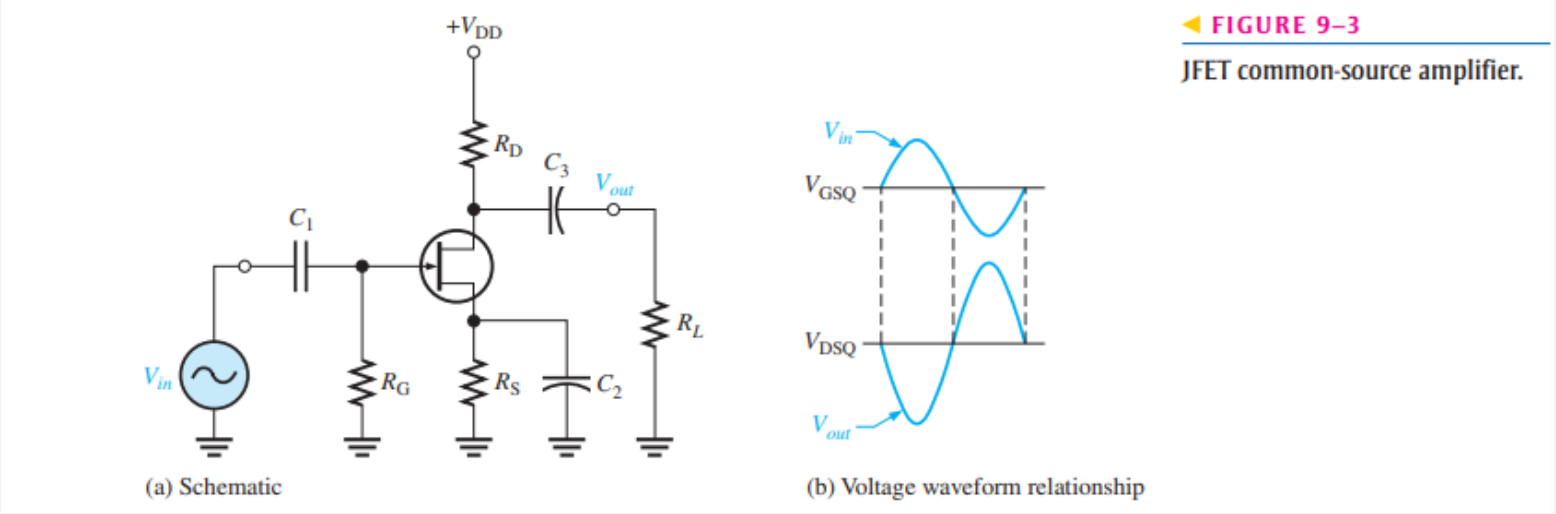
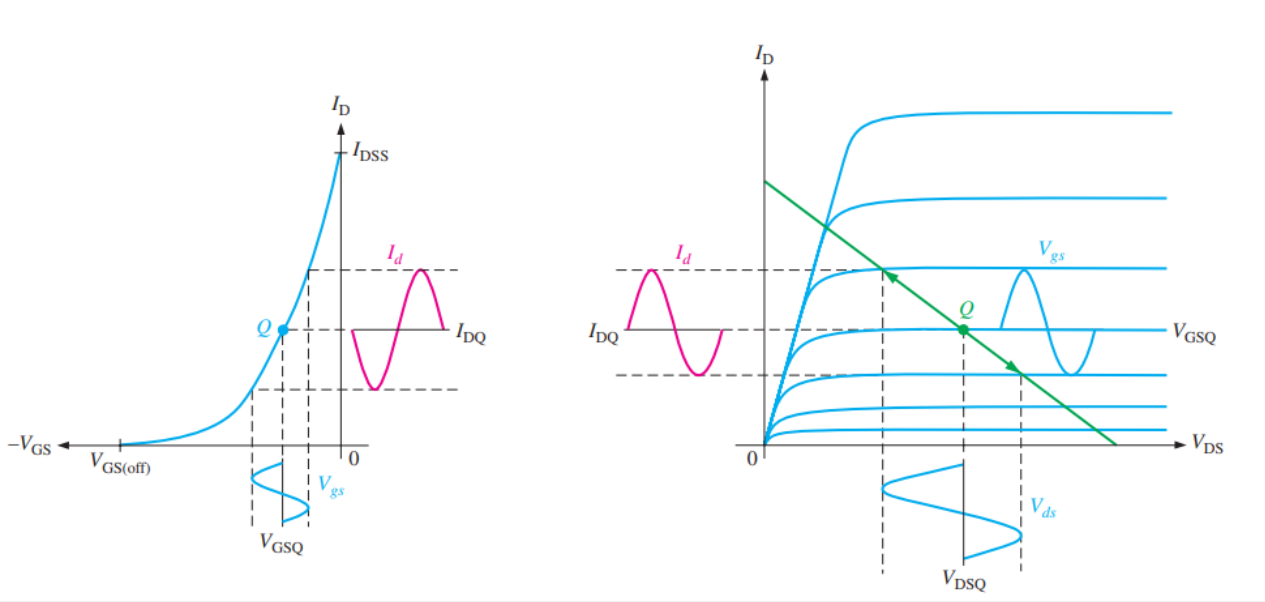


FIGURE 9–3

JFET common-source amplifier.

JFET AMPLIFIER. AC ANALYSIS

- The input signal voltage causes the gate-to-source voltage to swing above and below its **Q-point** value (V_{GSQ}), causing a corresponding swing in drain current.
- As the drain current increases, the voltage drop across R_D also increases, causing the drain voltage to decrease.
- The drain current swings above and below its **Q-point** value in phase with the gate-to-source voltage.
- The drain-to-source voltage swings above and below its **Q-point** value (V_{DSQ}) and is 180° out of phase with the gate-to-source voltage.

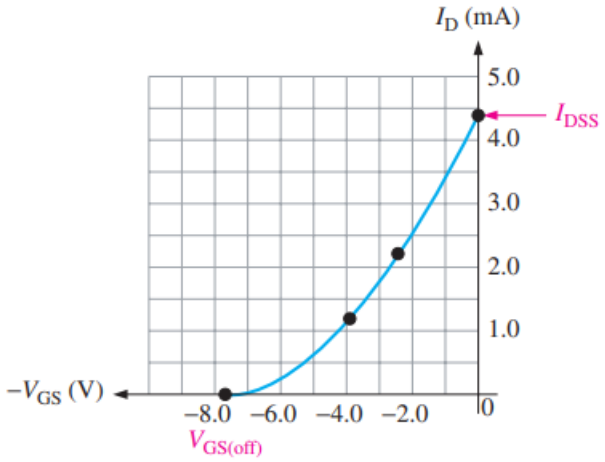


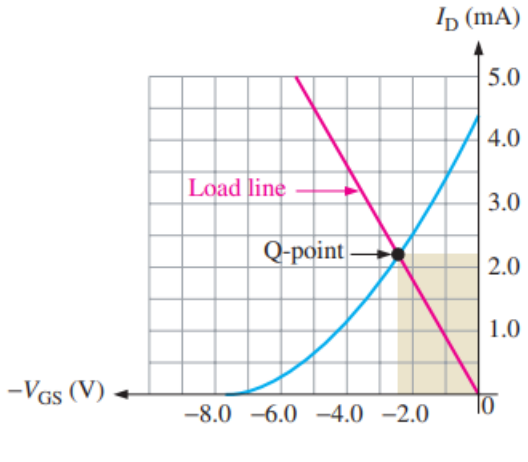
JFET AMPLIFIER. DC ANALYSIS

- I_D determines the **Q-point** for an amplifier and enables you to calculate V_D, so it is useful to determine its value. It can be found either graphically or mathematically:

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_{GS(off)}})^2$$

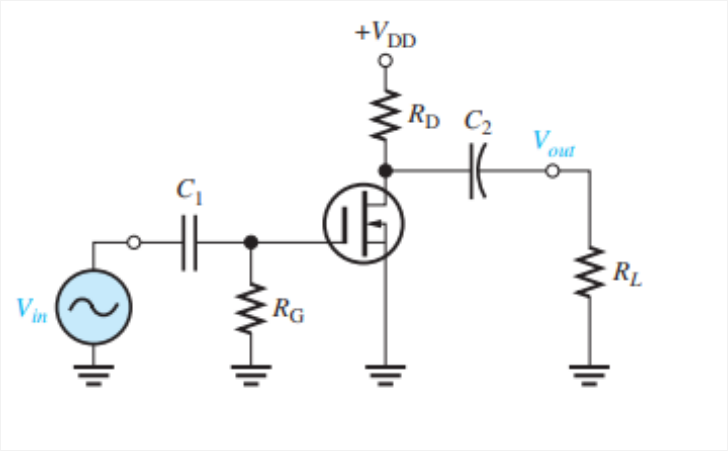
- The endpoints of the transconductance curve are at I_{DSS} and $V_{GS(off)}$.
- A DC graphical solution is done by plotting the load line on the same plot and reading the values of V_{GS} and I_D at the intersection of these plots (**Q-point**)

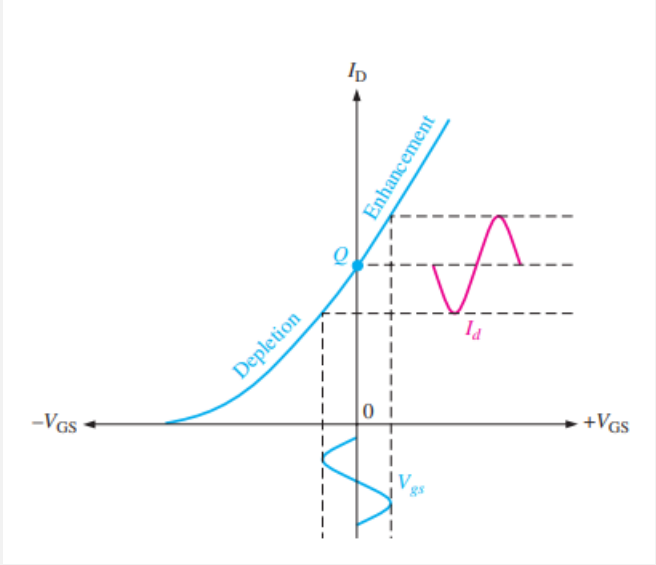


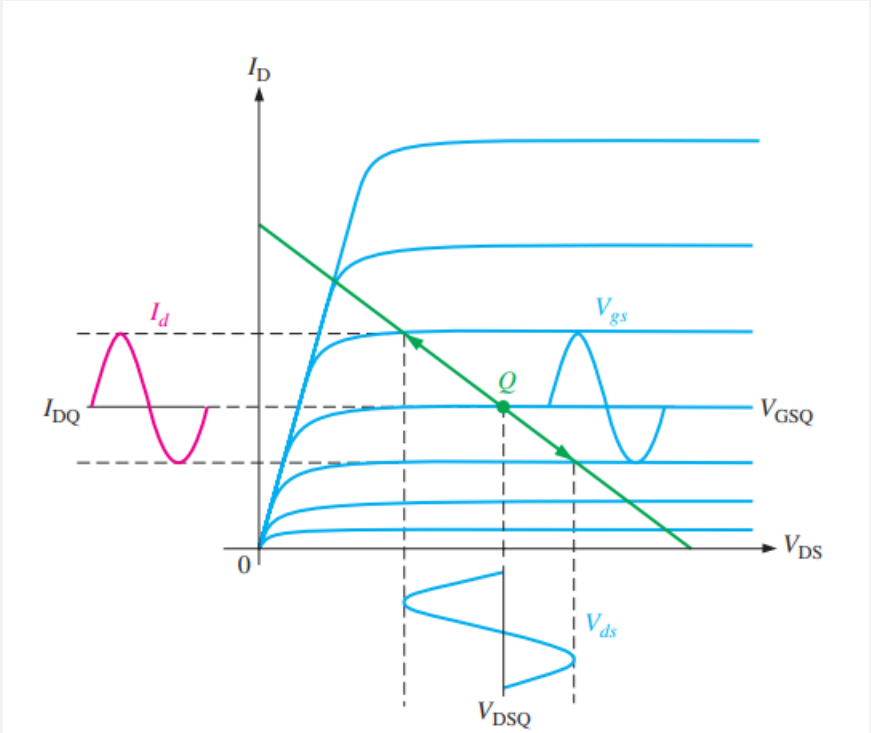


D-MOSFET AMPLIFIER

- The gate is at approximately 0 V DC and the source terminal is at ground, thus making $V_{GS} = 0\ V$
- The signal voltage causes V_{GS} to swing above and below its zero value, producing a swing in I_d.
- The negative swing in V_{GS} produces the depletion mode, and I_d decreases.
- The positive swing in V_{GS} produces the enhancement mode, and I_d increases.

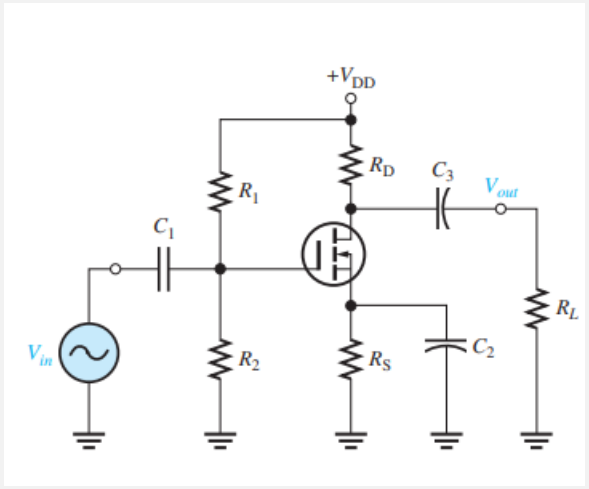


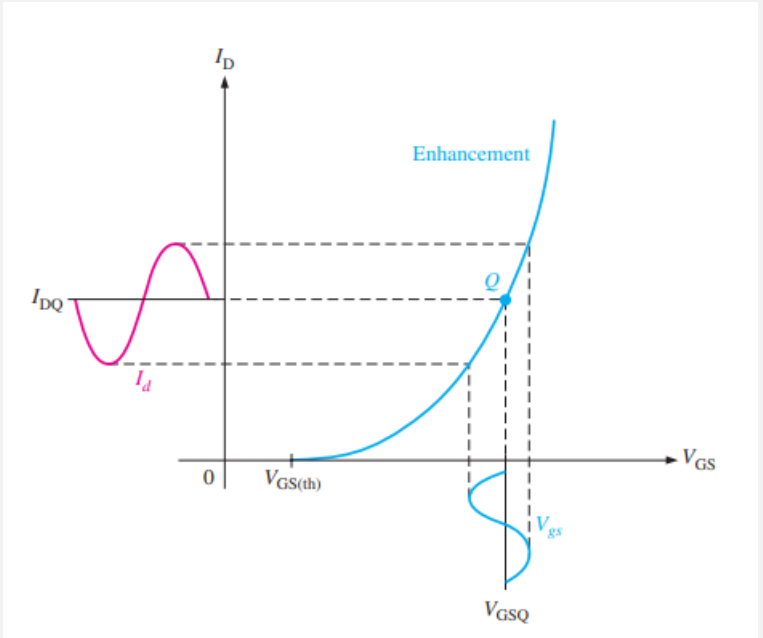


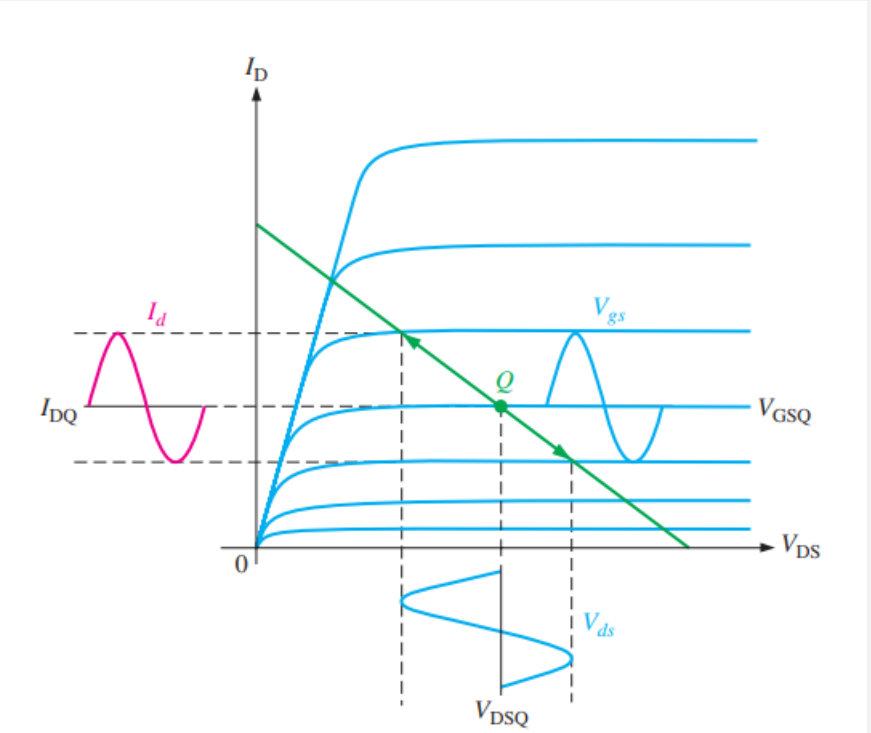


E-MOSFET AMPLIFIER

- The gate is biased with a positive voltage such that $V_{GS} > V_{GS(th)}$
- As with the JFET and D-MOSFET, the signal voltage produces a swing in V_{GS} above and below its Q-point value, V_{GSQ}. This causes a swing in I_d above and below its Q-point value, I_{DQ}.
- Operation is entirely in the enhancement mode.







MOSFET ANALOG SWITCHING

- E-MOSFETs are generally used for switching applications because of their threshold characteristic, $V_{GS(th)}$.
- When the gate-to-source voltage is less than the threshold value, the MOSFET is off.
- When the gate-to-source voltage is greater than the threshold value, the MOSFET is on.
- In the **off** state, when the device is operating at the lower end of the load line and acts like an open switch (very high R_{DS}).
- When V_{GS} is sufficiently greater than $V_{GS(th)}$, the device is operating at the upper end of the load line in the ohmic region and acts like a closed switch (very low R_{DS})

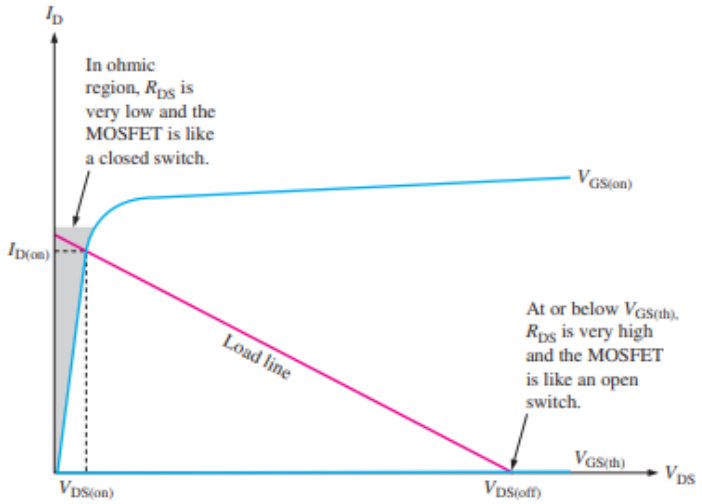
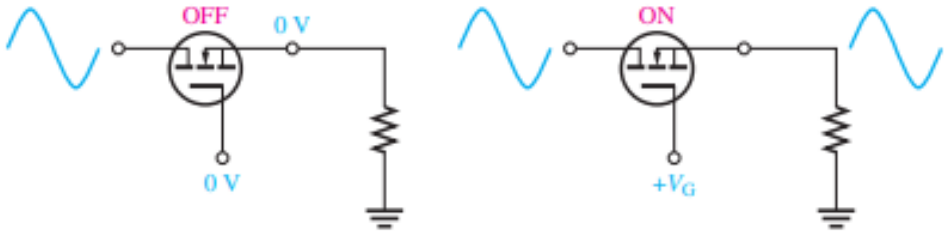


FIGURE 9–32

Switching operation on the load line.

ANALOG SWITCH

- A signal applied to the drain can be switched through to the source by a voltage on the gate.
- A major restriction is that the signal level at the source must not cause the gate-to-source voltage to drop below $V_{GS(th)}$.
- When the MOSFET is turned on, the signal at the drain is connected to the source by a positive V_{GS}.
- When the MOSFET is turned off ($V_{GS} = 0$), the drain signal is disconnected from the source and is equal to zero.



◀ FIGURE 9–34

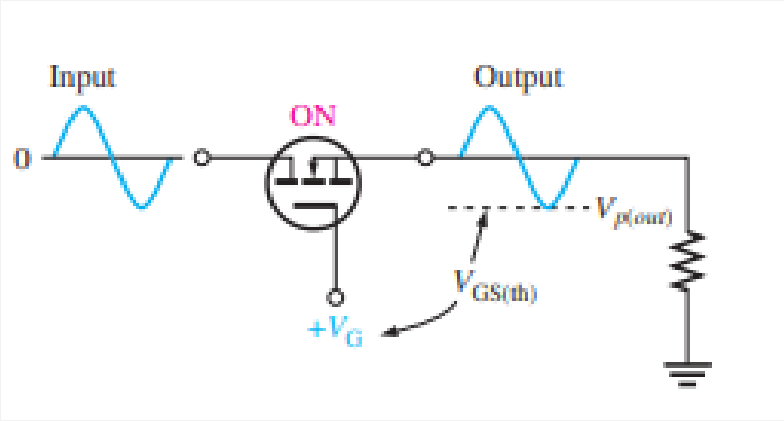
Operation of an *n*-channel MOSFET analog switch.

ANALOG SWITCH

- When the analog switch is on, the minimum gate-to-source voltage occurs at the negative peak of the signal.
- The difference in V_G and $-V_{p(out)}$ is the gate-to-source voltage at the instant of the negative peak and must be equal to or greater than $V_{GS(th)}$ to keep the MOSFET in conduction.

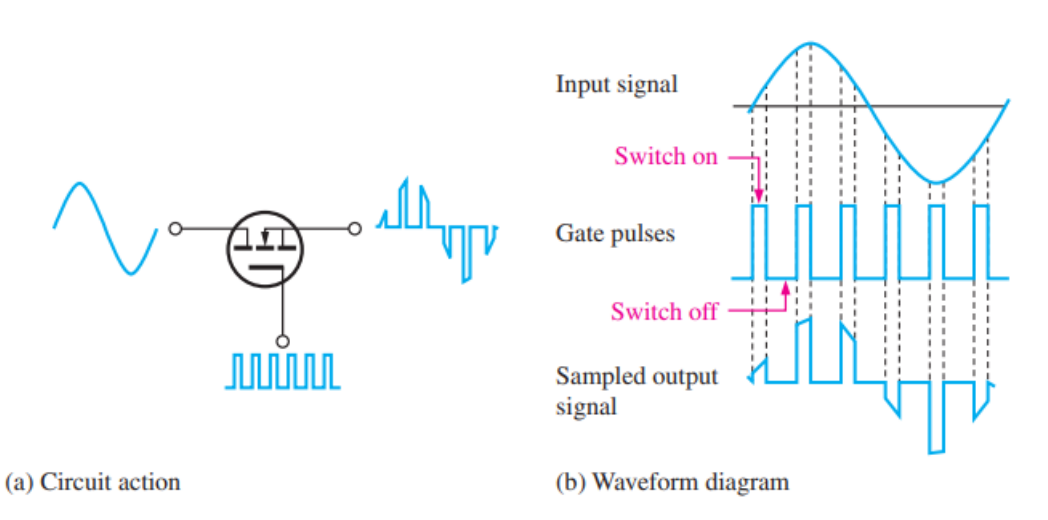
$$V_{GS} = V_G - V_{p(out)} \geq V_{GS(th)}$$

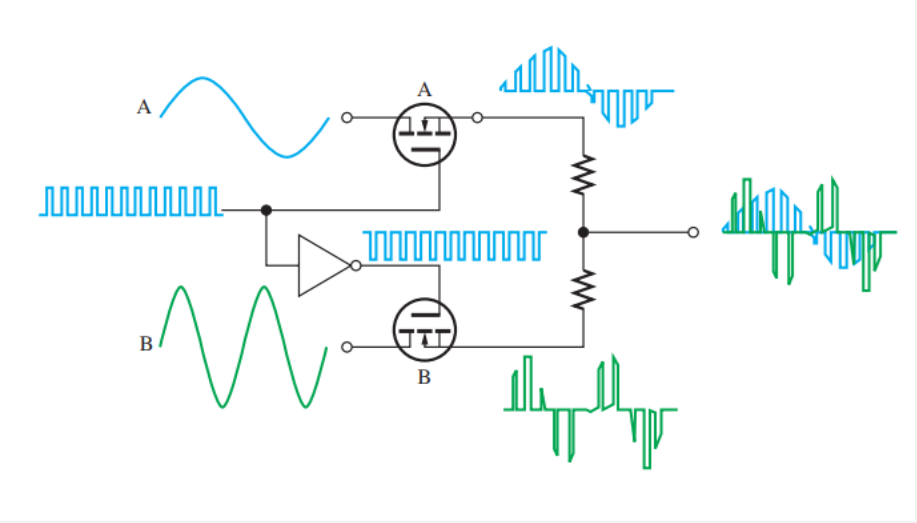
- Output signal amplitude is limited by $V_{GS(th)}$



ANALOG SWITCH APPLICATIONS

- Sampling Circuit (Analog-to-Digital Conversion)
  - Sample-and-hold circuit to sample the input signal at a certain rate.
- Analog Multiplexer
  - Where two or more signals are to be routed to the same destination
- Switched-Capacitor Circuit
  - Commonly used in integrated circuit programmable analog devices known as *analog signal processors.*

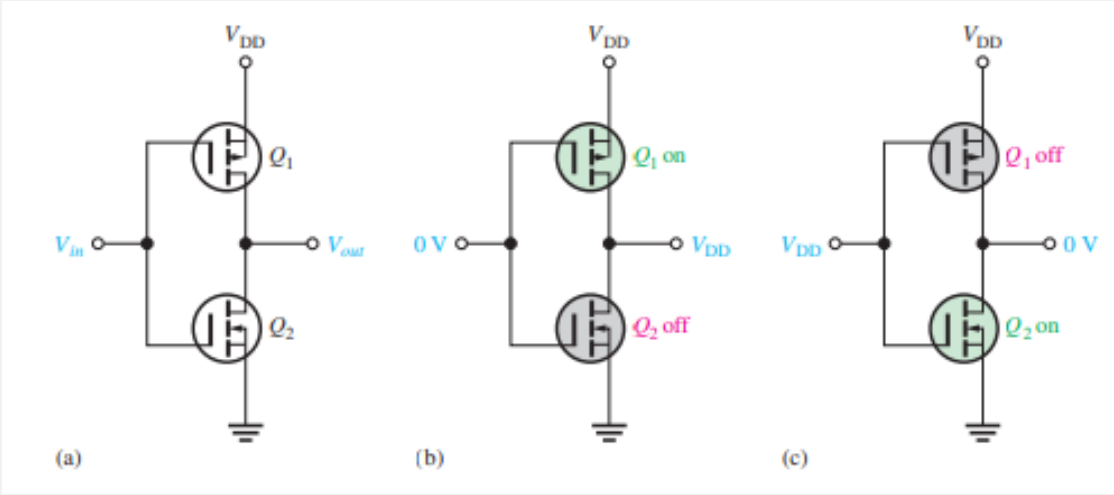




MOSFET DIGITAL SWITCHING

CMOS (Complementary MOS)

- CMOS combines **n-channel** and **p-channel** E-MOSFETs in a series arrangement.
- The input voltage at the gates is either 0 V or V_{DD}.
- V_{DD} and ground are both connected to source terminals of the transistors.
- When $V_{in} = 0\,V$, Q_1 is **ON** and Q_2 is **OFF**. The output is approximately V_{DD}.
- When $V_{in} = V_{DD}$, Q_2 is **ON** and Q_1 is **OFF**. The output is essentially connected to ground (0 V).



MOSFET DIGITAL SWITCHING

- **Inverter**. When the input is 0 V or low, the output is V_{DD} or high. When the input is V_{DD} or high, the output is 0 V or low. For this reason, this circuit is called an inverter in digital electronics.
- **NAND Gate**. Two additional MOSFETs and a second input are added to the CMOS pair to create a digital circuit known as a NAND gate. Q_4 is connected in parallel with Q_1, and Q_3 is connected in series with Q_2. When both inputs, V_A and V_B, are 0, Q_1 and Q_4 are **ON** while Q_2 and Q_3 are **OFF**, making V_{out}= V_{DD}. When both inputs are equal to V_{DD}, Q_1 and Q_4 are **OFF** while Q_2 and Q_3 are **ON**, making $V_{out} = 0$. You can verify that when the inputs are different, one at V_{DD} and the other at 0, the output is equal to V_{DD}.

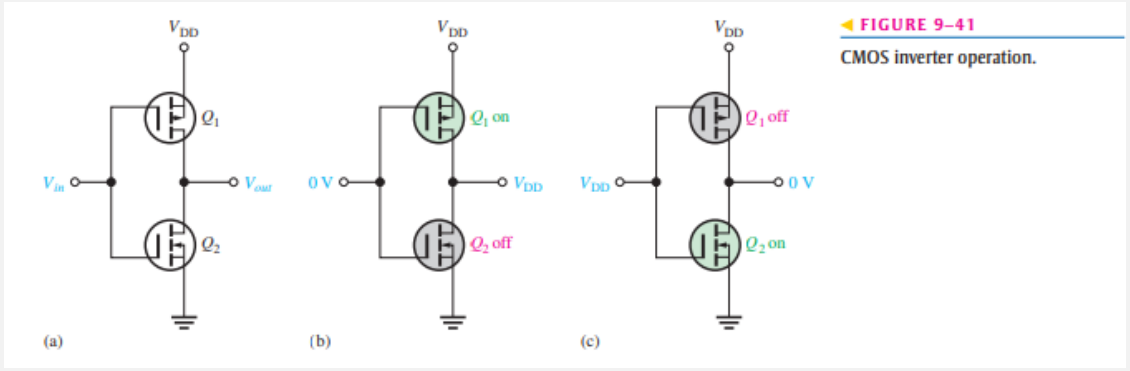
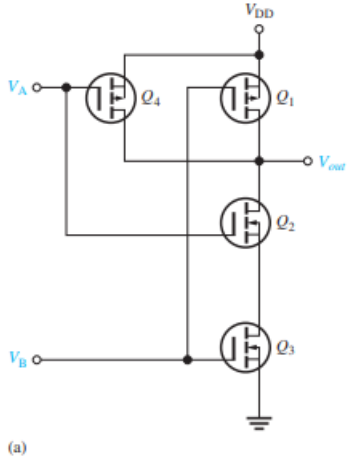


FIGURE 9–41
CMOS inverter operation.

FIGURE 9–42
CMOS NAND gate operation.



V_A	V_B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0	on	off	off	on	V_{DD}
0	V_{DD}	off	off	off	on	V_{DD}
V_{DD}	0	on	off	off	off	V_{DD}
V_{DD}	V_{DD}	off	on	on	off	0

(b)

MOSFET DIGITAL SWITCHING

NOR Gate. Two additional MOSFETs and a second input are added to the CMOS pair to create a digital circuit known as a NOR gate. Q_4 is connected in parallel with Q_2, and Q_3 is connected in series with Q_1. When both inputs, V_A and V_B, are 0, Q_1 and Q_3 are on while Q_2 and Q_4 are off, making $V_{out} = V_{DD}$. When both inputs are equal to V_{DD}, Q_1 and Q_3 are off while Q_2 and Q_4 are on, making $V_{out} = 0$. You can verify that when the inputs are different, one at V_{DD} and the other at 0, the output is equal to 0.

To summarize, when V_A **OR** V_B **OR** BOTH are high, the output is low; otherwise, the output is high.

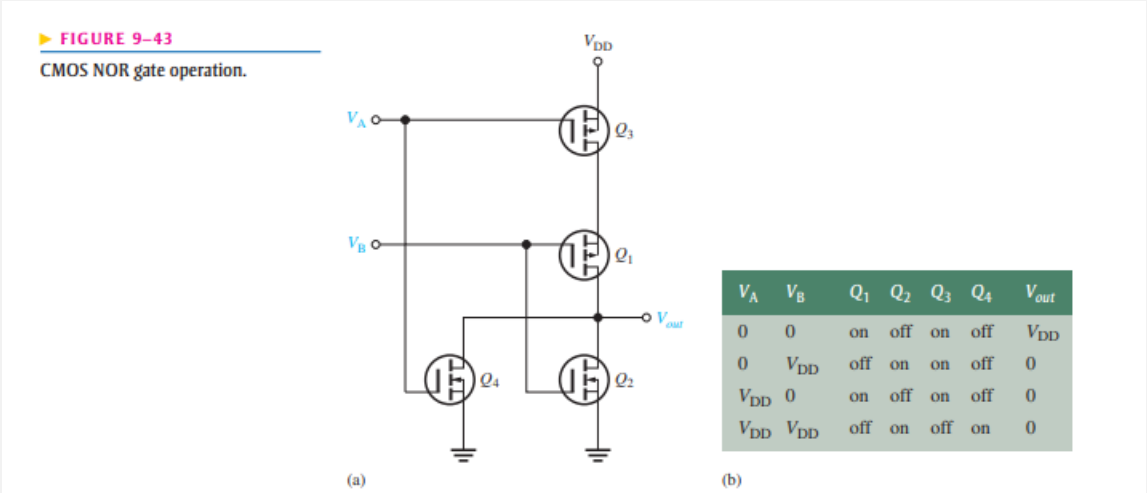


FIGURE 9–43
CMOS NOR gate operation.

V_A	V_B	Q_1	Q_2	Q_3	Q_4	V_{out}
0	0	on	off	on	off	V_{DD}
0	V_{DD}	off	on	on	off	0
V_{DD}	0	on	off	on	off	0
V_{DD}	V_{DD}	off	on	off	on	0

(b)

THYRISTORS

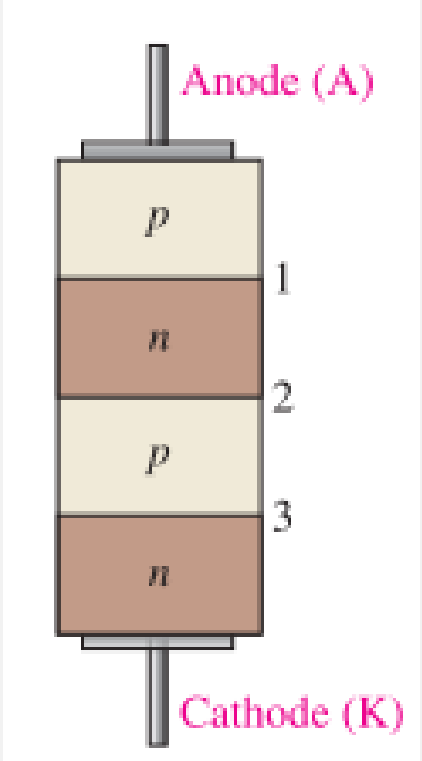
Lecture 7

OVERVIEW

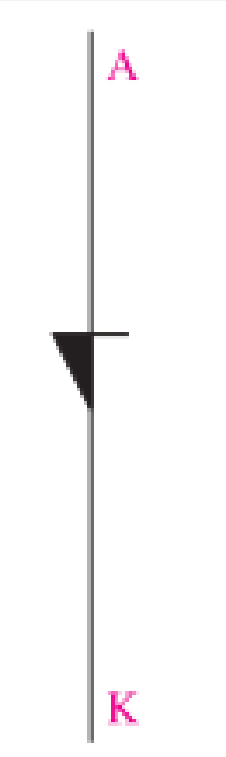
- Basic structure of Thyristor
- Working principles of Thyristor
- Forward Breakover Voltage
- Holding and switching current
- The Silicon-Controlled Rectifier (SCR).
- SCR Characteristics and Rating
- SCR Applications

BASIC STRUCTURE

- **Definition**: The device acts as a switch and remains off until the forward voltage reaches a certain value; then it turns on and conducts. Conduction continues until the current is reduced below a specified value.
- **Basics**:
  - Two terminals: Anode & Cathode
  - 4-layer device (4 semiconductor layers)
  - ***pnpn*** structure
  - Three ***pn*** junction
  - Known as **Shokley** diode & SUS (Silicon Unilateral Switch)



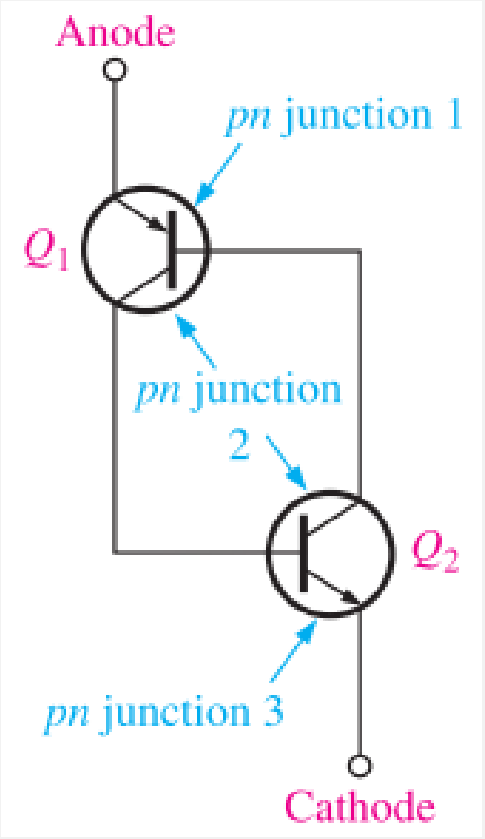
Schematic symbol

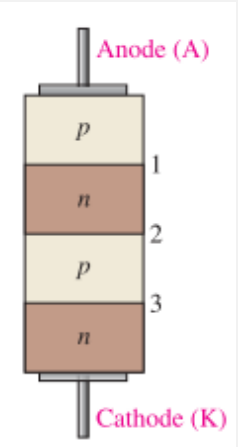


Schematic symbol

BASIC STRUCTURE

- Tyristor equivalent circuit::
  - ***pnp*** and ***npn*** transistors
  - Upper ***pnp*** layer as Q_1 and lower ***npn*** layer from Q_2
  - Middle layer shared by both transistors

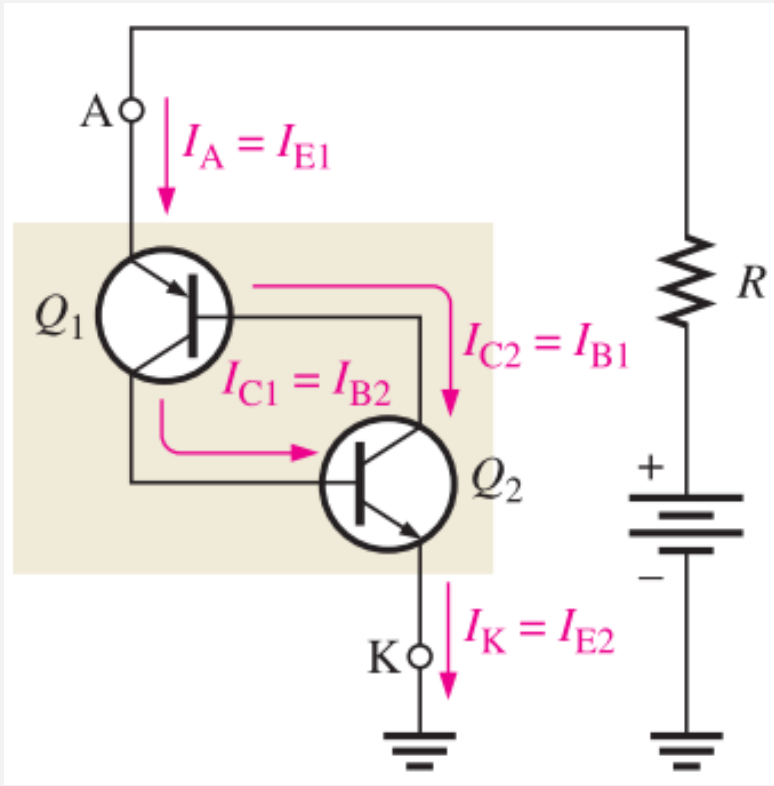


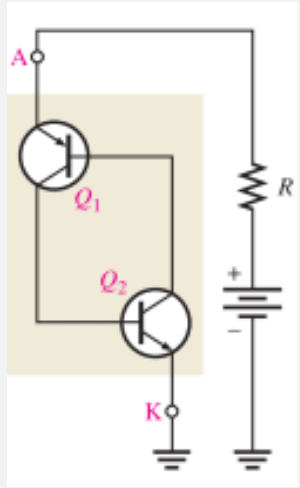


WORKING PRINCIPLE

Positive bias voltage applied to the anode with respect to cathode

- The base-emitter junction Q_1 & Q_2 are forward-biased
- Common base-collector junction (***pn***) is reverse-biased
- At low-bias level → Anode current is little → It is in the **OFF** state or forward-blocking region

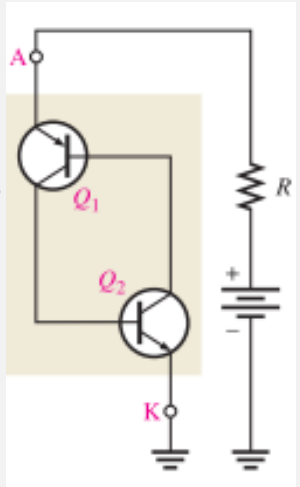


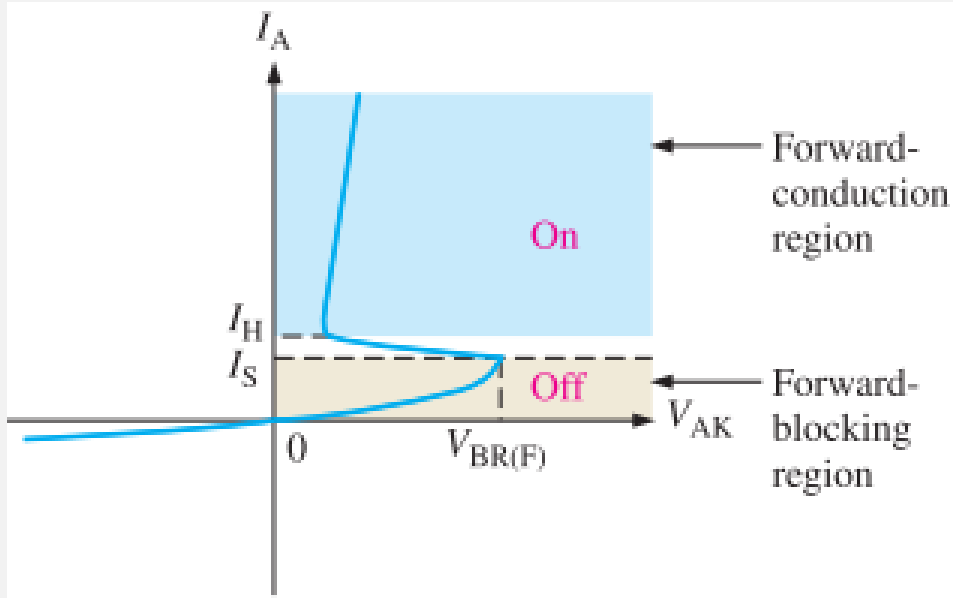


FORWARD-BREAKOVER VOLTAGE

- Forward-blocking region (forward bias):
  - Device has a very high forward resistance (ideally an open)
  - Device is in **OFF** state, acts as an open switch
  - Exist from: $V_{AK} = 0\ V$ to value $V_{AK} = V_{BR(F)}$ (*called forward-breakover voltage*)
  - As V_{AK} is increased → Anode current I_A gradually increases.
  - When I_A reaches I_S (Switching current) → $V_{AK} = V_{BR(F)}$

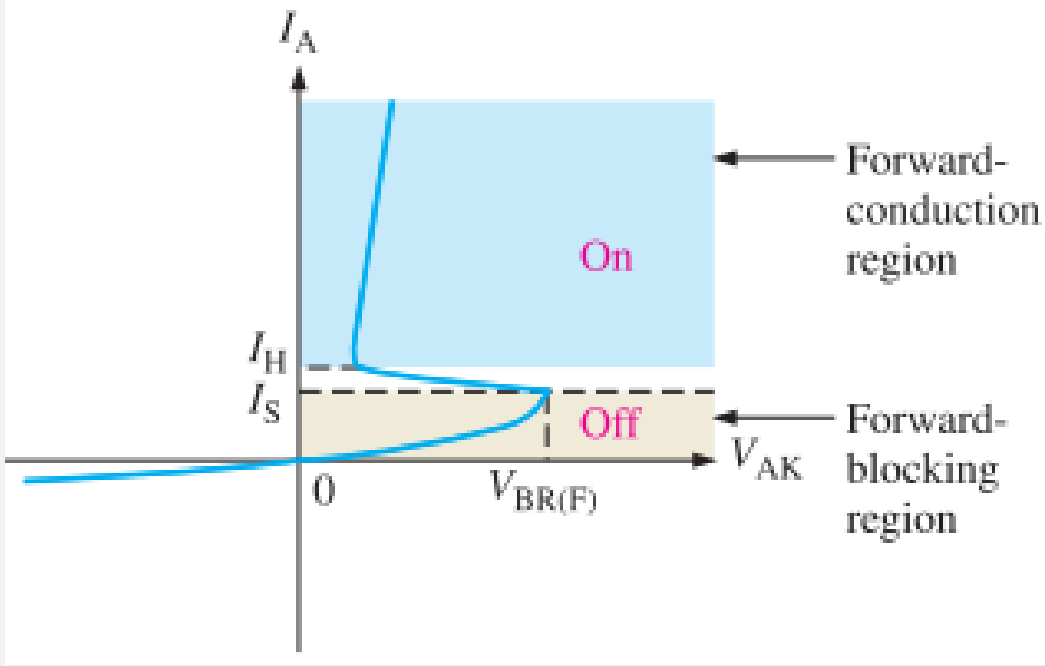
- Forward-conduction region:
  - When internal transistor structures become saturated, V_{AK} suddenly decreases to low value
  - The device is **ON** state and acts as a closed switch





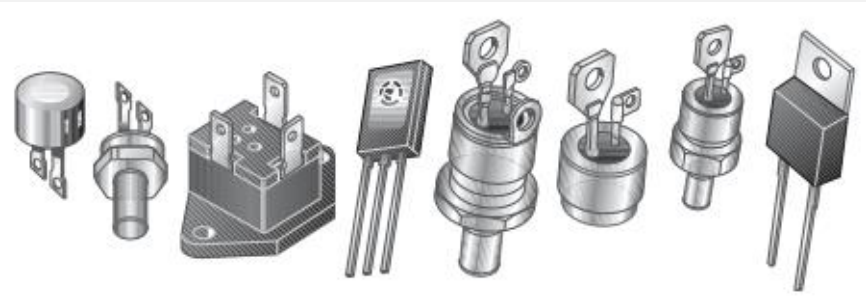
HOLDING AND SWITCHING CURRENT

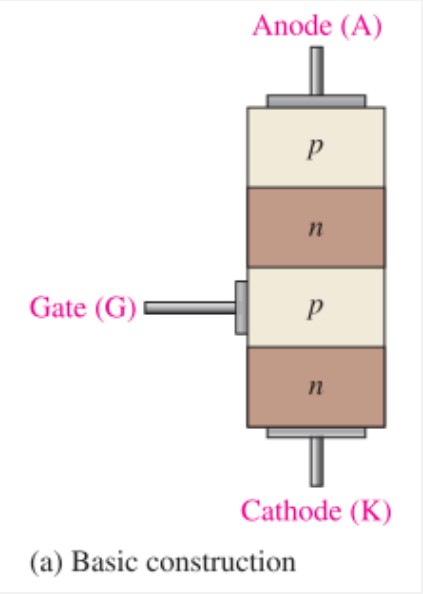
- Holding Current (I_H)
  - When the 4-layer diode (Thyristor) in in the ***ON*** state, conduction continues till anode current is reduced below a specified level, called holding current "$\boldsymbol{I_H}$"
  - Device switches to ***OFF*** state and enters the forward-blocking region, once I_A falls below I_H.
- Switching current (I_S)
  - Anode current value where the device switches from the forward-blocking-region (***OFF***) to the forward-conduction region (***ON***)
  - The value is always less than the holding current (I_H)



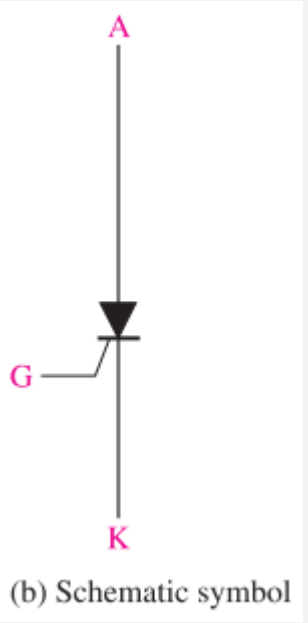
SCR (SILICON-CONTROLLED RECTIFIER)

- Three terminals:
  - Anode, Cathode, Gate
- Has two possible states of operation:
  - ***OFF*** state:
    - Acts as open circuit between anode & cathode
    - High resistance
  - ***ON*** state:
    - Acts ideally as a short from the anode to the cathode
    - Small on (forward) resistance





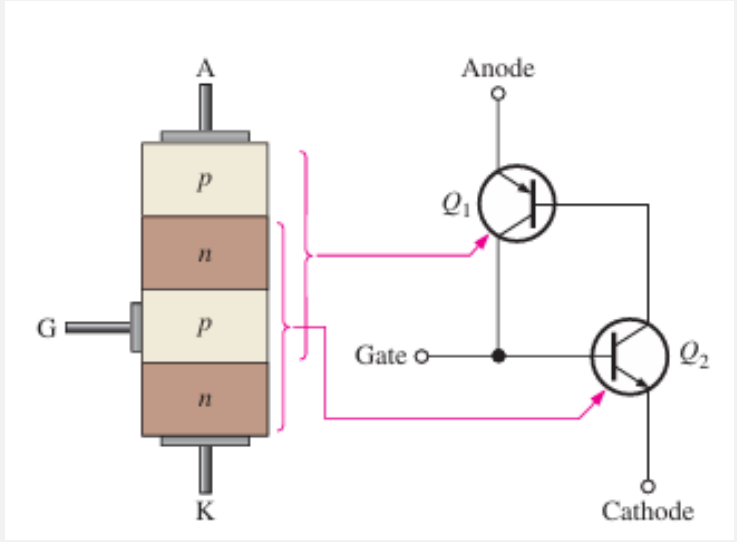
(a) Basic construction



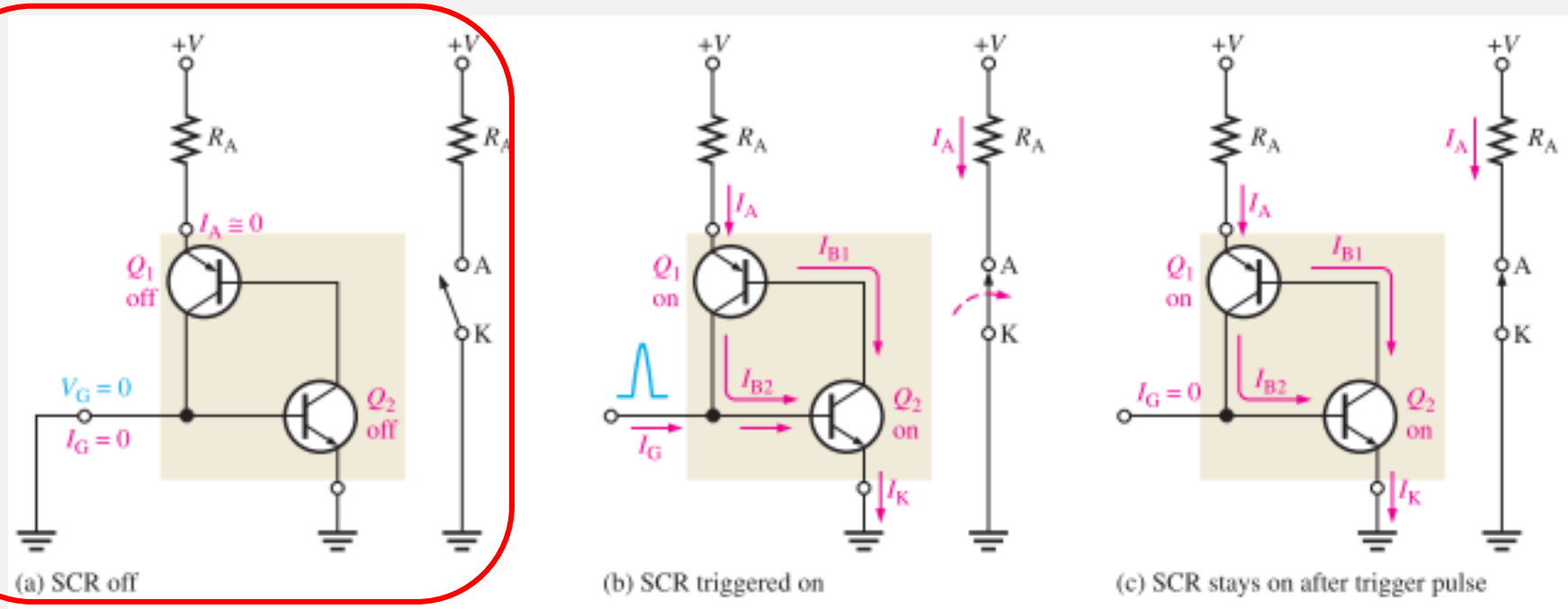
(b) Schematic symbol

SCR EQUIVALENT CIRCUIT

- 4-layer diode except for the gate connection
- The upper ***pnp*** layers act as a transistor, Q_1
- The lower ***npn*** layers act as a transistor, Q_2
- Two middle layers are “shared”

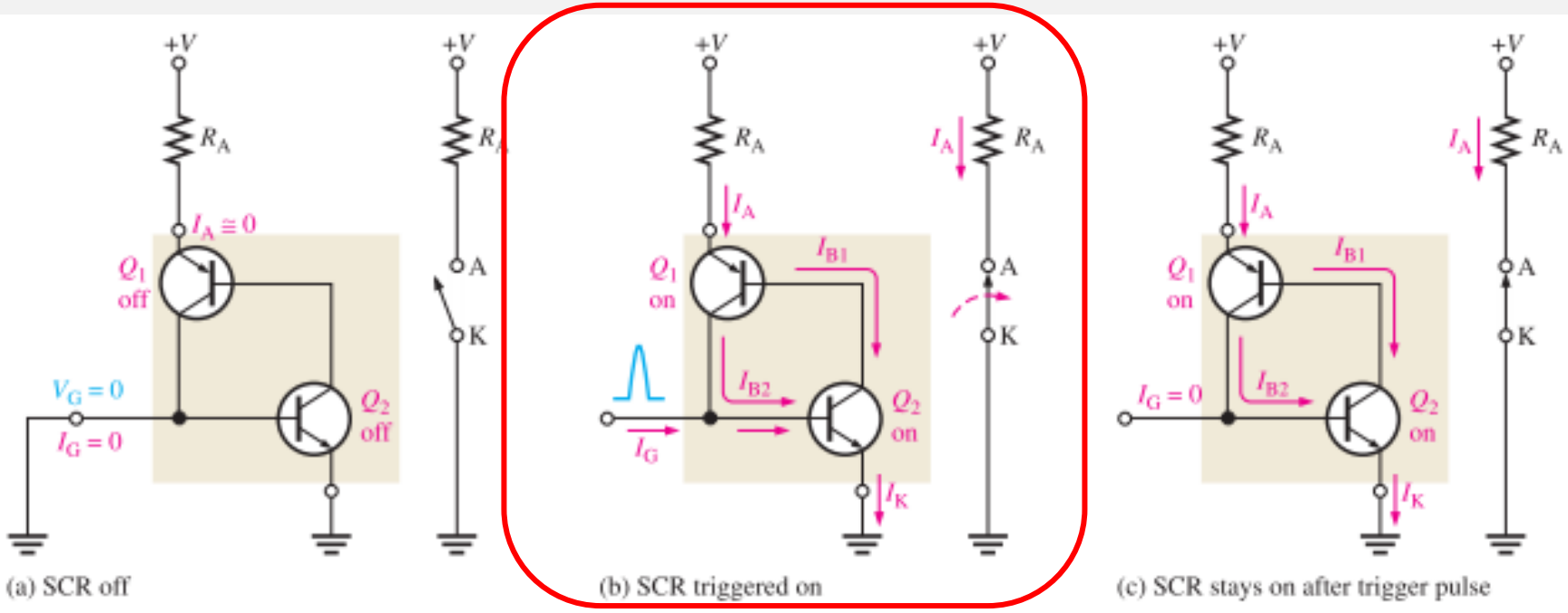


SCR "OFF" STATE



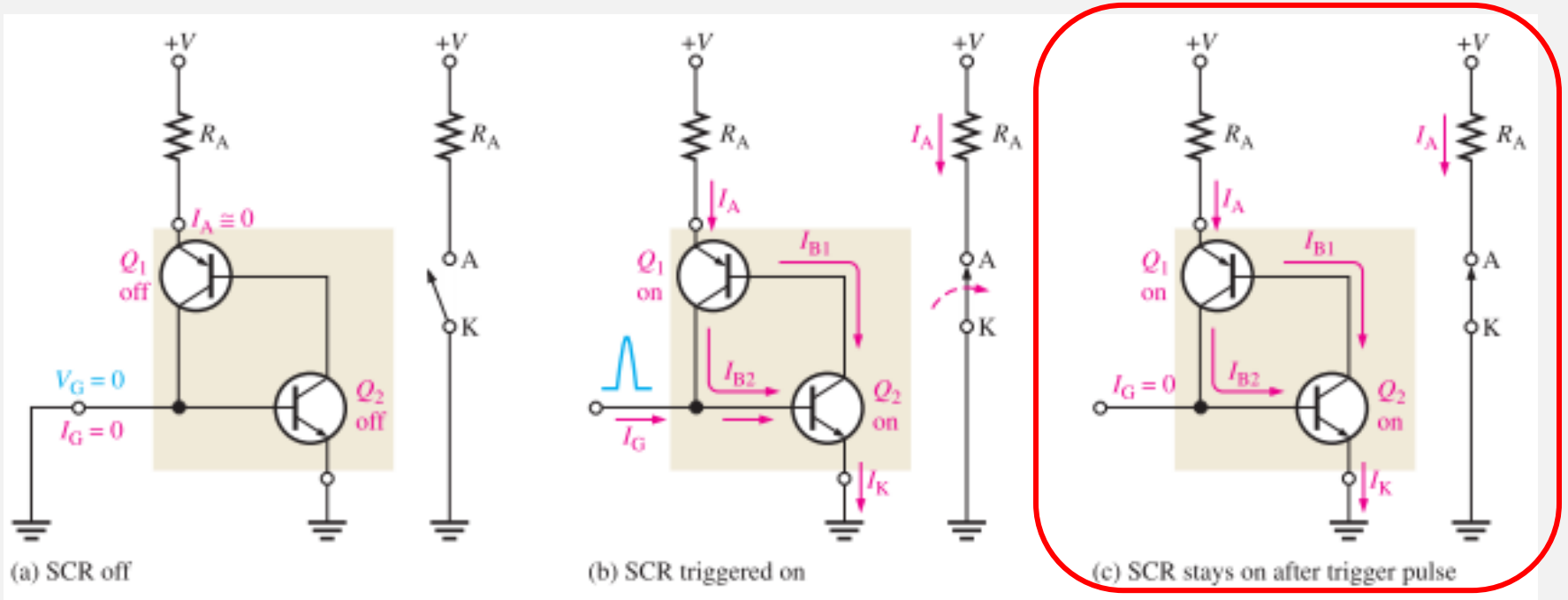
- Gate current, I_G, is zero.
- The device acts as a 4-layer diode in the ***OFF*** state
- Very high resistance between anode and cathode

SCR "ON" STATE



- Positive pulse of current (trigger) is applied to the gate
- Both transistors, Q_1 and Q_2 are ***ON***
- I_{B2} turns on Q_2 → provides path for I_{B1}, thus turning on Q_1
- Q_1 collector's current provides additional base current for Q_2

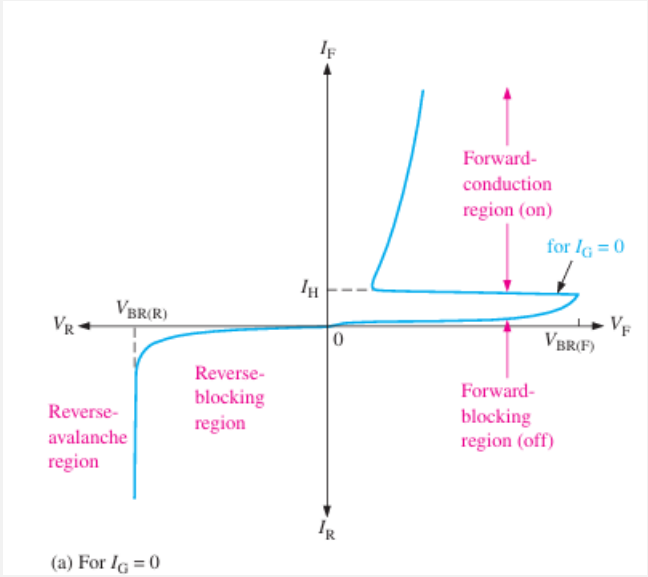
SCR AFTER TRIGGER PULSE



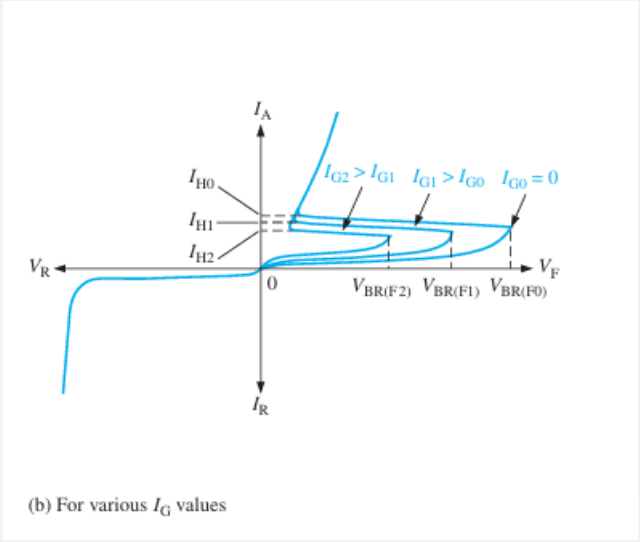
- Q_2 stays in conduction after trigger pulse is removed from the gate
- Low resistance between Anode and Cathode
- Q_2 sustains the saturated conduction of Q_1 by providing path for I_{B1}
- Q_1sustains the saturated conduction of Q_2 by providing path for I_{B2}
- Thus, the device stays on (latches) once it is triggered on

SCR CHARACTERISTIC CURVES

- An SCR can also be turned on without gate triggering by increasing the anode-to-cathode voltage to a value exceeding the forward-breakover voltage $V_{BR(F)}$.
- The forward-breakover voltage decreases as I_G is increased above 0 A.
- Eventually, a value of I_G is reached at which the SCR turns on at a very low anode-to-cathode voltage.
- The gate current controls the value of forward breakover voltage, $V_{BR(F)}$, required for turn-on.



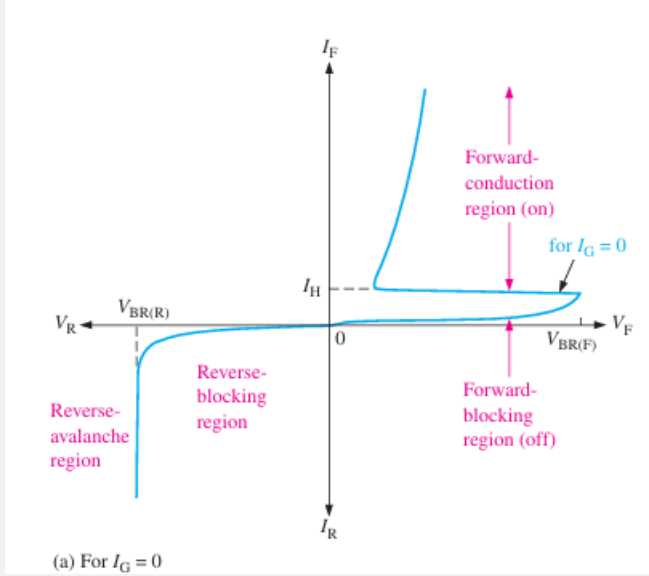
(a) For $I_G = 0$



(b) For various I_G values

TURNING THE SCR OFF

- Turning SCR off → Dropping the Anode current below the holding current (I_H)
- When the gate returns to 0V after the trigger pulse is removed, the SCR cannot turn off; it stays in the forward-conduction region.
- Two basic methods for turning off the SCR:
  1. Anode current interruption
  2. Forced commutation

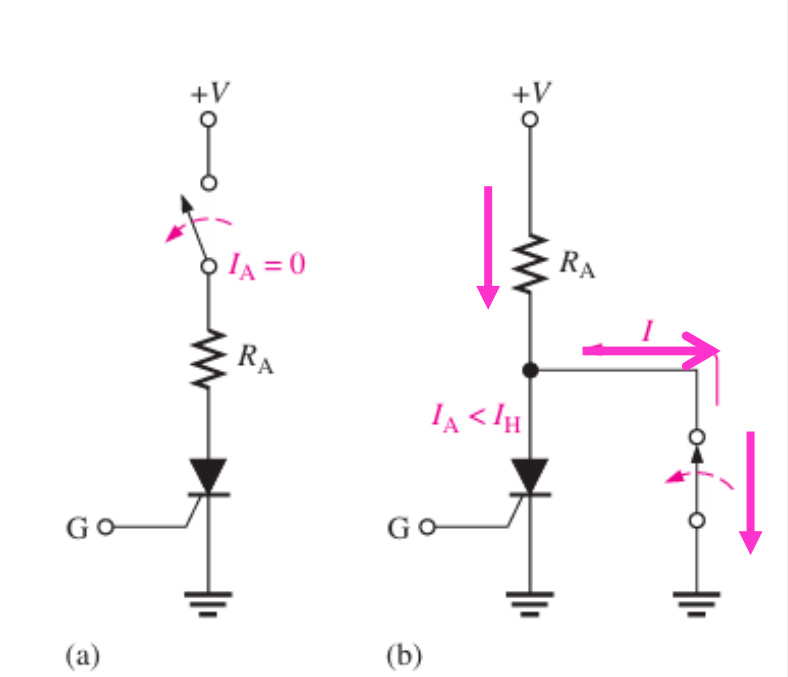


(a) For $I_G = 0$

TURNING THE SCR OFF

Anode current interruption:

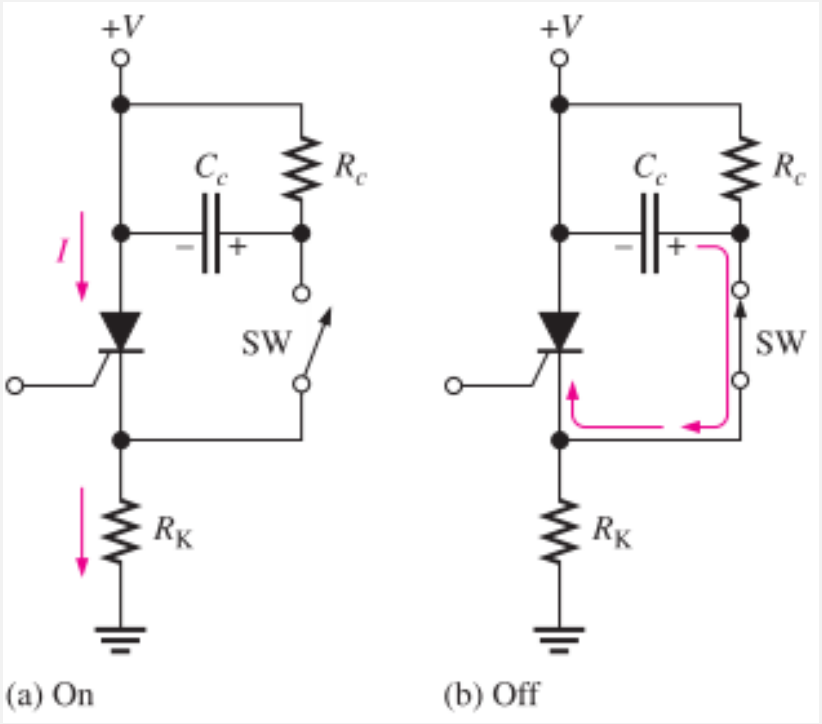
- Momentary series arrangement (**a**) – simply reduces the anode current to zero and causes the SCR to turn off
- Parallel switching arrangement (**b**) – routes part of the total current away from the SCR, thereby reducing the anode current to a value less than I_H.



TURNING THE SCR OFF

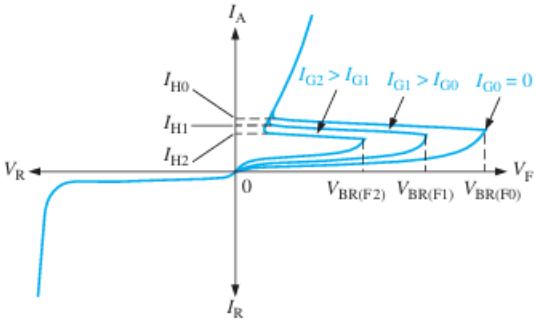
Forced Commutation

- Momentarily forcing current through SCR in the direction opposite to the forward-conduction → Net forward current is reduced below the holding value (I_H)
- The basic circuit consist of:
  - Transistor switch
  - Capacitor
- While SCR conducting the switch is open and C_c is charged to supply voltage through R_c (**a**)
- To turn off the SCR
  - Switch is closed
  - Placing the capacitor across the SCR and forcing current through it opposite to the forward current (**b**)
  - Takes few microseconds up to 30 μs



SCR CHARACTERISTICS AND RATING

- **Forward-breakover voltage $V_{BR(F)}$**
  - Voltage at which the SCR enters the forward-conduction region
  - $V_{BR(F)}$ is maximum when $I_G = 0$ and is designated $V_{BR(F0)}$
  - When the gate current is increased, $V_{BR(F)}$ decreases and is designed $V_{BR(F1)}$, $V_{BR(F2)}$ and so on, for increasing steps in gate current (I_{G1}, I_{G2} and so on)
- **Holding current I_H**
  - The value of anode current below which the SCR switches from forward-conduction region to the forward-blocking region
  - The value increases with decreasing values of I_G and is maximum for $I_G = 0$



(b) For various I_G values

SCR CHARACTERISTICS AND RATING

- **Gate trigger current I_{GT}**
  - The value of gate current necessary to switch the SCR from the forward-blocking region to the forward-conduction region under specified conditions.
- **Average Forward current $I_{F(AVG)}$**
  - The maximum continuous anode current (DC) that the device can withstand in the conduction state under specified conditions.

SCR CHARACTERISTICS AND RATING

- **Forward-blocking and reverse-blocking region**
  - These regions correspond to the *off* condition of the SCR where the forward current from anode to cathode is blocked by the effective open circuit of the SCR
- **Reverse breakdown voltage ($V_{BR(F)}$)**
  - This parameter specifies the value of reverse voltage from cathode to anode at which the device breaks into the avalanche region and begins to conduct heavily (the same as in a ***pn*** junction diode).
- **Forward-conduction region**
  - This region corresponds to the *on* condition of the SCR where there is forward current from anode to cathode through the very low resistance (approximate short) of the SCR.

THE OPERATIONAL AMPLIFIER

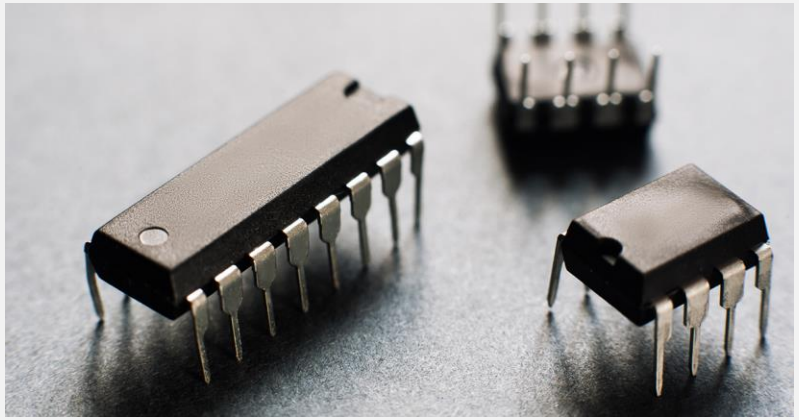
Lecture 8

OVERVIEW

- Introduction to Operational Amplifiers
- Op-Amp Input Modes
- Op-Amp Parameters
- Negative feedback
- Op-Amps with Negative Feedback
- Basic Op-Amp Circuits

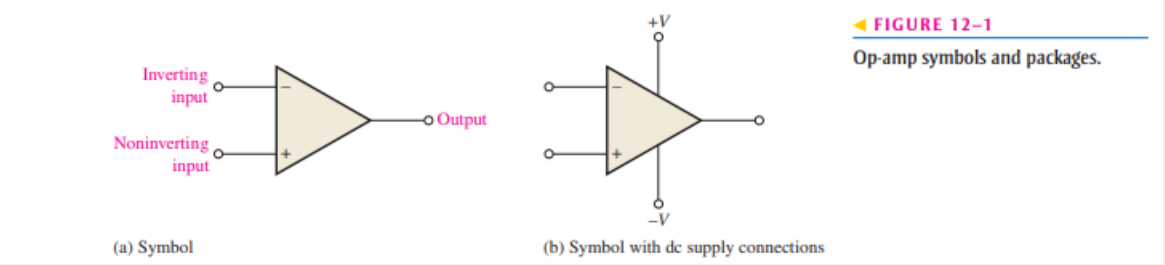
THE OPERATIONAL AMPLIFIER

- Early operational amplifiers (op-amps) were used primarily to perform mathematical operations such as addition, subtraction, integration, and differentiation—thus the term operational. These early devices were constructed with vacuum tubes and worked with high voltages. Today's op-amps are linear integrated circuits (ICs) that use relatively low DC supply voltages and are reliable and inexpensive.



THE OPERATIONAL AMPLIFIER

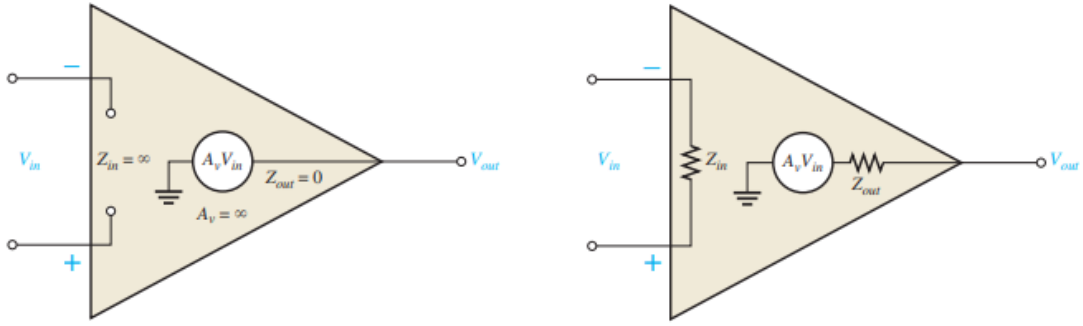
- Op-Amp has two input terminals, the inverting (−) input and the noninverting (+) input, and one output terminal.
- Most op-amps operate with two DC supply voltages, one positive and the other negative, although some have a single DC supply.
- Usually, DC voltage terminals are left off the schematic symbol for simplicity but are understood to be there



◀ FIGURE 12–1
Op-amp symbols and packages.

THE IDEAL OP-AMP

- The ideal op-amp has infinite voltage gain and infinite bandwidth.
- It has an infinite input impedance (open), so that it does not load the driving source.
- It has zero output impedance.
- The input voltage, V_{in}, appears between the two input terminals
- The output voltage is $A_v V_{in}$



(a) Ideal op-amp representation

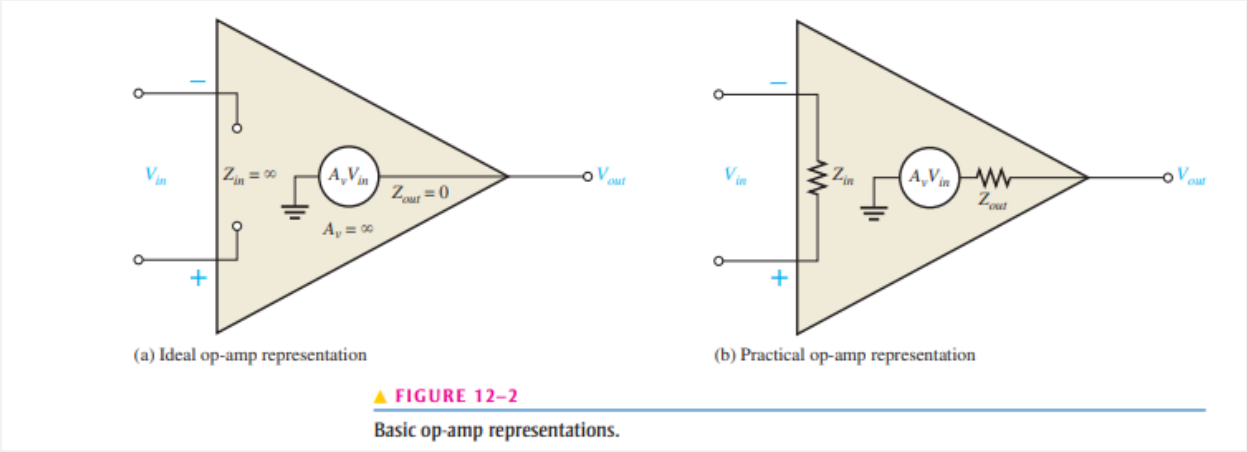
(b) Practical op-amp representation

▲ FIGURE 12–2

Basic op-amp representations.

THE PRACTICAL OP-AMP

- Op-amps have both voltage and current limitations.
- Peak-to-peak output voltage is usually limited to slightly less than the two supply voltages.
- Output current is also limited by internal restrictions such as power dissipation and component ratings.
- Practical op-amps have:
  - Very high voltage gain
  - Very high input impedance
  - Very low output impedance

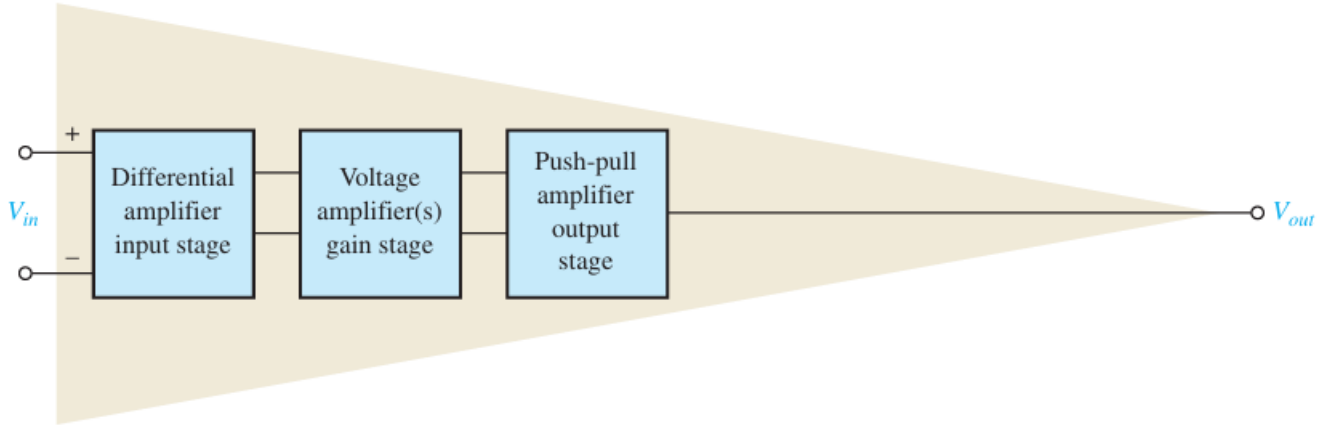


▲ FIGURE 12–2
Basic op-amp representations.

- There is always noise generated within the op-amp.
- Noise is an undesired signal that affects the quality of a desired signal.
- Circuit designers are using smaller voltages that require high accuracy, so low-noise components are in greater demand.

OP-AMP
INTERNAL BLOCK DIAGRAM

- A typical Op-amp is made up of 3 types of amplifier circuits:
  - **A differential amplifier** – provides amplification of the difference voltage between two inputs
  - **A voltage amplifier** – provides additional gain
  - **A push-pull amplifier** – used for output stage, additional voltage amplifier stage.



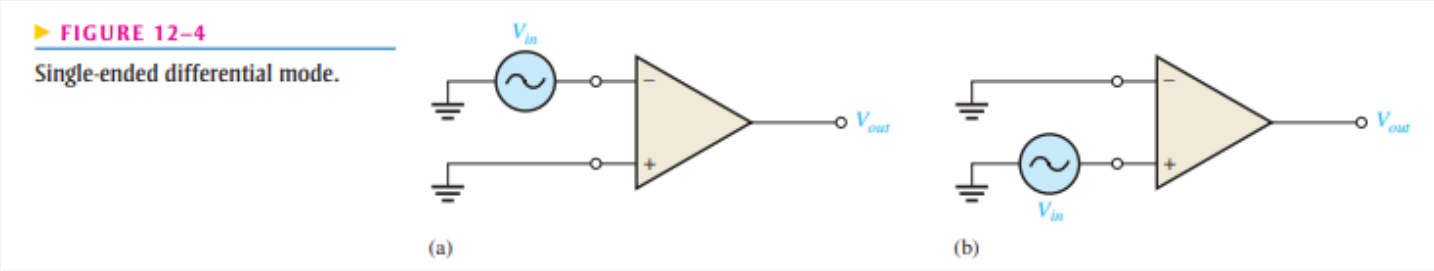
▲ FIGURE 12–3

Basic internal arrangement of an op-amp.

OP-AMP INPUT MODES

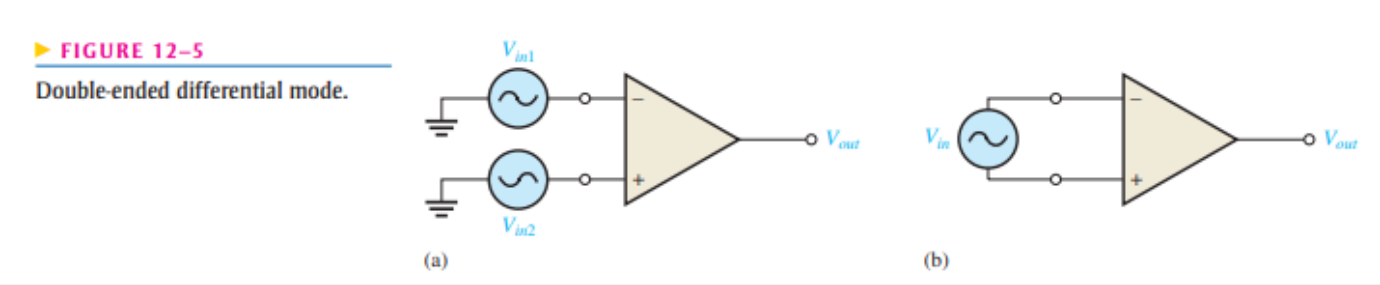
Differential mode

- One signal is applied to an input with the other input grounded:
  - In the case where the signal voltage is applied to the inverting input as in (**a**), an inverted, amplified signal voltage appears at the output.
  - In the case where the signal is applied to the non-inverting input with the inverting input grounded, as in (**b**), a noninverted, amplified signal voltage appears at the output.



OP-AMP INPUT MODES

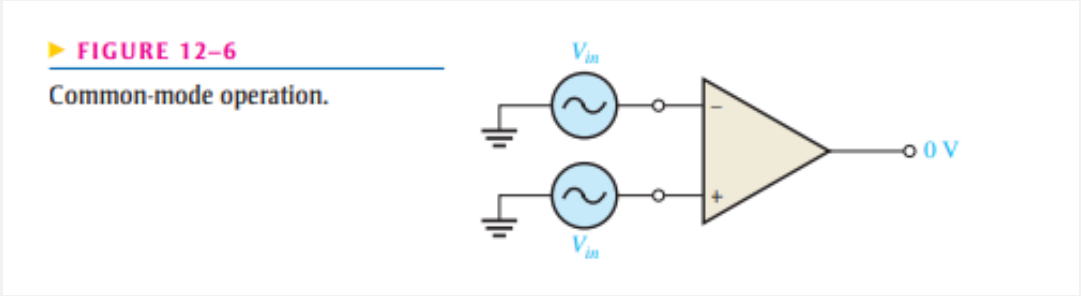
- **Differential mode**
  - Two opposite-polarity signals are applied to the inputs:
    - The amplified difference between the two inputs appears on the output. Equivalently, the double-ended differential mode can be represented by a single source connected between the two inputs.



OP-AMP INPUT MODES

❑ Common mode

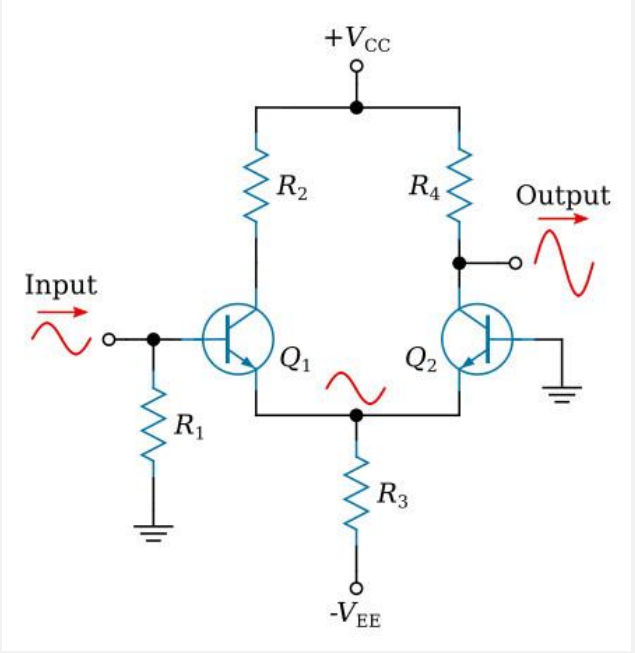
- Two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs
- When equal input signals are applied to both inputs, they tend to cancel, resulting in a zero output voltage. This action is called *common-mode rejection*.
- **Common-mode rejection:**
  - ✓ Important where an unwanted signal appears commonly on both op-amp inputs.
  - ✓ It means that this unwanted signal will not appear on the output and distort the desired signal.
- Common-mode signals (noise) generally are the result of the pick-up of radiated energy on the input lines, from adjacent lines, the 60 Hz power line, or other sources



SINGLE-INPUT SINGLE-OUTPUT DIFFERENTIAL AMPLIFIER

- When the input signal developed by R_1 goes positive, the current through Q_1 increases. This increased current causes a positive-going signal at the top of R_3. This signal is felt on the emitter of Q_2. Since the base of Q_2 is grounded, the current through Q_2 decreases with a positive-going signal on the emitter. This decreased current causes less voltage drop across R_4. Therefore, the voltage at the bottom of R_4 increases and a positive-going signal is felt at the output.

- When the input signal developed by R_1 goes negative, the current through Q_1 decreases. This decreased current causes a negative-going signal at the top of R_3. This signal is felt on the emitter of Q_2. When the emitter of Q_2 goes negative, the current through Q_2 increases. This increased current causes more of a voltage drop across R_4. Therefore, the voltage at the bottom of R_4 decreases and a negative- going signal is felt at the output



OP-AMP PARAMETERS

- Common-Mode Rejection Ratio (CMRR)
- Open-Loop Voltage Gain
- Maximum Output Voltage Swing
- Input Offset Voltage
- Input Bias Current
- Input Impedance
- Input Offset Current
- Output Impedance
- Slew Rate
- Noise Specification

NEGATIVE FEEDBACK

- **Negative feedback** is the process whereby a portion of the output voltage of an amplifier is returned to the input with a phase angle that opposes (or subtracts from) the input signal.
- The inverting input effectively makes the feedback signal 180° out of phase with the input signal.
- Without negative feedback, a small input voltage drives the op-amp to its saturated output states (limits) and it becomes nonlinear.
- Provides a controlled, stable voltage gain, controlled input and output impedance, amplifier bandwidth.

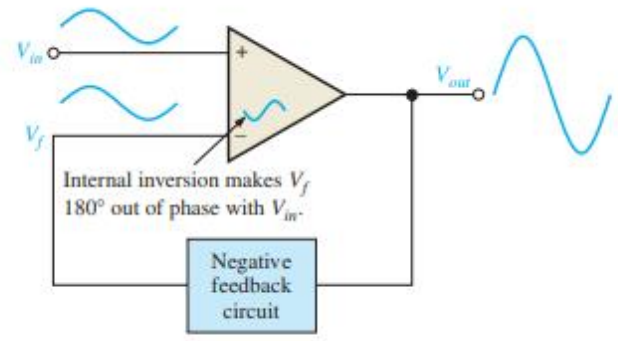


FIGURE 12–14
Illustration of negative feedback.

OP-AMPS WITH NEGATIVE FEEDBACK

An op-amp can be connected using negative feedback to stabilize the gain and increase frequency response. Negative feedback takes a portion of the output and applies it back out of phase with the input, creating an effective reduction in gain. This closed loop gain is usually much less than the open-loop gain and independent of it.

Closed-Loop Voltage Gain, A_{cl} The closed-loop voltage gain is the voltage gain of an op-amp with external feedback. The amplifier configuration consists of the op-amp and an external negative feedback circuit that connects the output to the inverting input. The closed-loop voltage gain is determined by the external component values and can be precisely controlled by them.

Noninverting Amplifier The input signal is applied to the noninverting (+) input. The output is applied back to the inverting input through the feedback circuit (closed loop) formed by the input resistor R_i and the feedback resistor R_f. Resistors R_i and R_f form a voltage-divider circuit, which reduces V_{out} and connects the reduced voltage V_f to the inverting input. The feedback voltage is expressed as

$$V_f = \left(\frac{Ri}{Ri + Rf}\right) V_{out}$$

$$A_{cl(NI)} = \frac{R_i + R_f}{R_i}$$

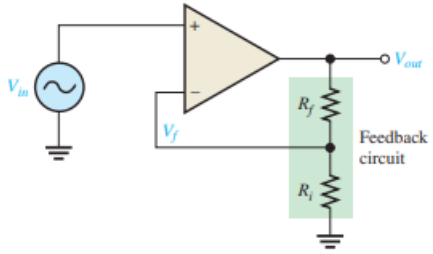


FIGURE 12–16
Noninverting amplifier.

OP-AMPS WITH NEGATIVE FEEDBACK

- **Voltage-Follower** The voltage-follower configuration is a special case of the noninverting amplifier where all of the output voltage is fed back to the inverting (−) input by a straight connection. The straight feedback connection has a voltage gain of 1 (which means there is no gain).
- **Inverting Amplifier** An op-amp connected as an inverting amplifier with a controlled amount of voltage gain. The input signal is applied through a series input resistor R_i to the inverting (−) input. Also, the output is fed back through R_f to the same input. The non-inverting (+) input is grounded. The closed loop gain is independent of the op-amp's internal open-loop gain. Thus, the negative feed back stabilizes the voltage gain.

$$A_{cl(I)} = -\frac{R_f}{R_i}$$

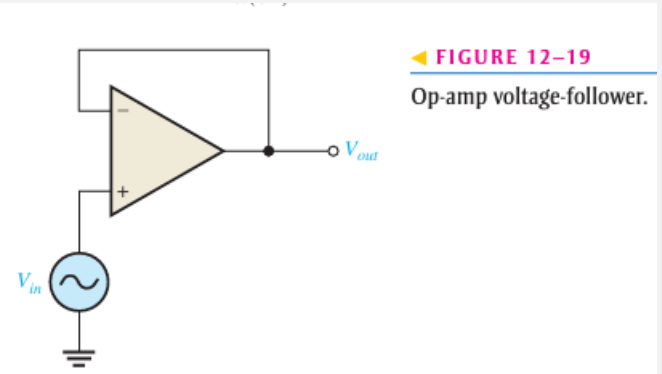


FIGURE 12–19
Op-amp voltage-follower.

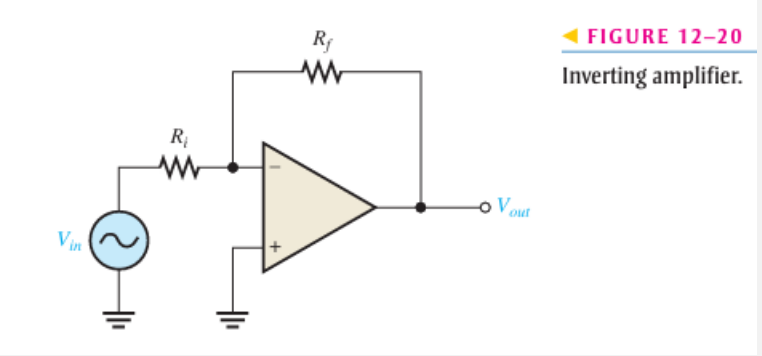


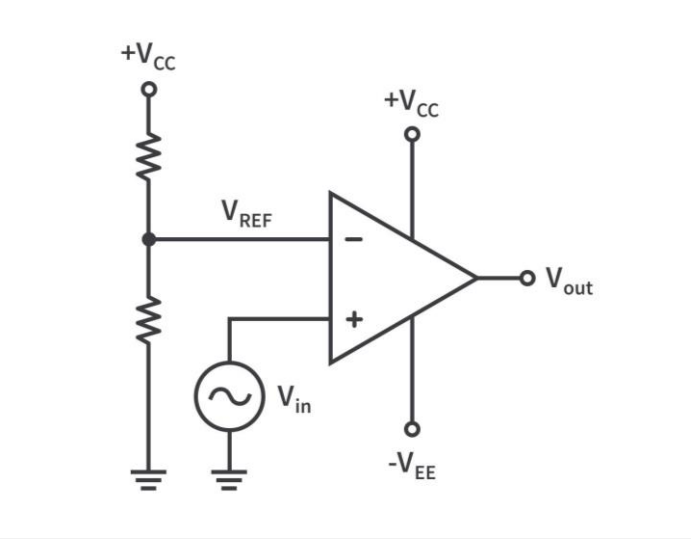
FIGURE 12–20
Inverting amplifier.

BASIC OP-AMP CIRCUITS

- Comparators
- Summing Amplifiers
- Integrators and Differentiators

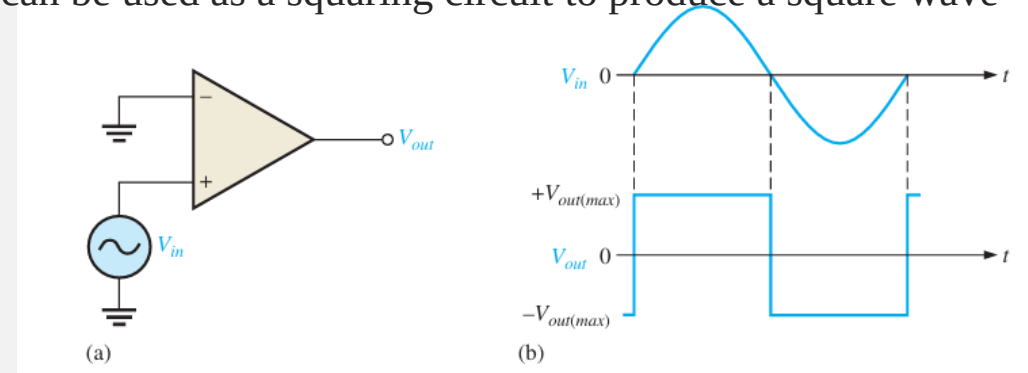
COMPARATORS

- A specialized op-amp circuit that compares two input voltages and produces an output that is always at either one of the two states , indicating the greater or less than relationship between the inputs.
- Provide very fast switching times
- For less critical applications, an op-amp running without negative feedback (open-loop) is often used as a comparator → enables to detect very tiny differences in the inputs as it has very high open-loop gain
- In general, comparators cannot be used as op-amps, but op-amps can be used as comparators in noncritical applications.



COMPARATORS
ZERO-LEVEL DETECTION

- Determine when an input voltage exceeds a certain level.
- As Figure (a) represents, the inverting (−) input is grounded to produce a zero level and that the input signal voltage is applied to the noninverting (+) input.
- Because of the high open-loop voltage gain, a very small difference voltage between the two inputs drives the amplifier into saturation, causing the output voltage to go to its limit.
- Figure (b) shows the result of a sinusoidal input voltage applied to the noninverting input of the zero-level detector.
- When the sine wave is positive, the output is at its maximum positive level.
- When the sine wave crosses 0, the amplifier is driven to its opposite state and the output goes to its maximum negative level.
- As you can see, the zero-level detector can be used as a squaring circuit to produce a square wave from a sine wave.



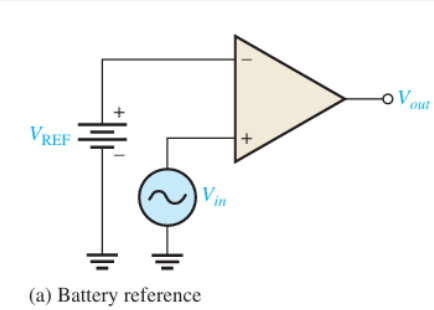
COMPARATORS
NONZERO-LEVEL DETECTION

- Detect positive and negative voltages by connecting a fixed reference voltage source to the inverting (−) input.
- A more practical arrangement is shown in Figure (b) using a voltage divider to set the reference voltage, V_{REF}, as follows:

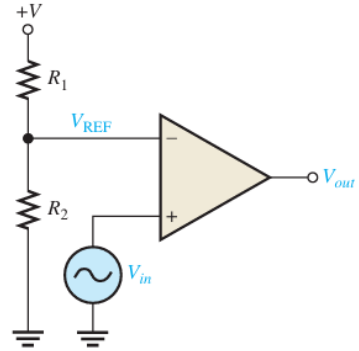
$$V_{REF} = \frac{R_2}{R_1 + R_2}\ (+V)$$

where +V is the positive op-amp dc supply voltage.

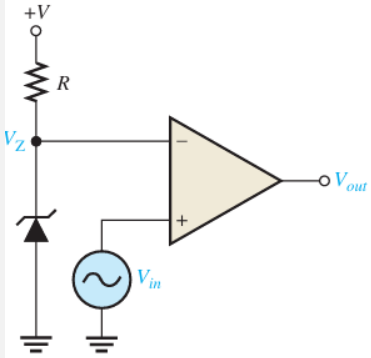
- The circuit in Figure (c) uses a Zener diode to set the reference voltage ($V_{REF} = V_Z$).
- As long as V_{in} is less than V_{REF}, the output remains at the maximum negative level. When the input voltage exceeds the reference voltage, the output goes to its maximum positive voltage, as shown in Figure (d) with a sinusoidal input voltage.



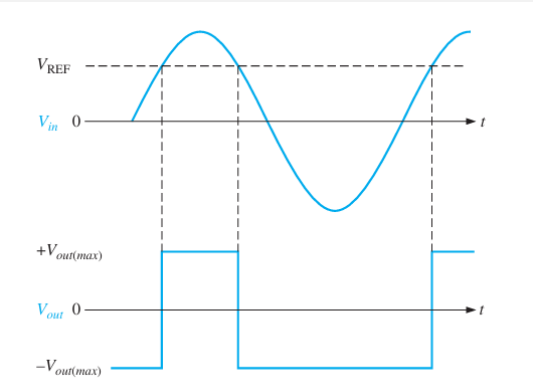
(a) Battery reference



(b) Voltage-divider reference



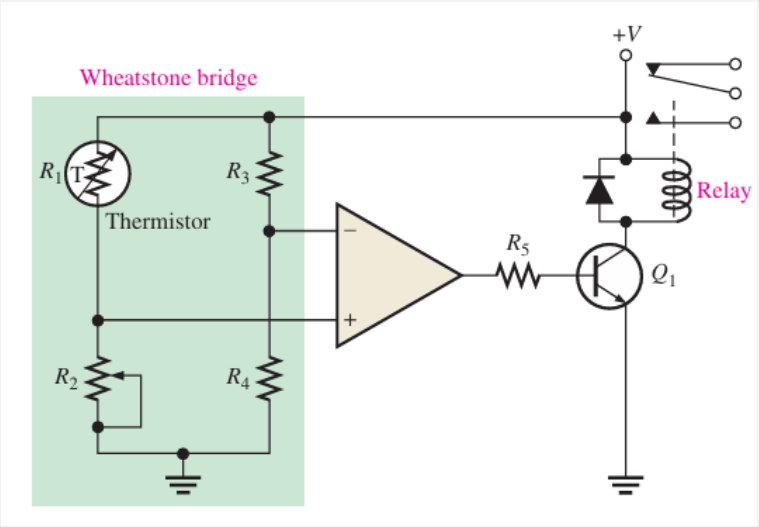
(c) Zener diode sets reference voltage



(d) Waveforms

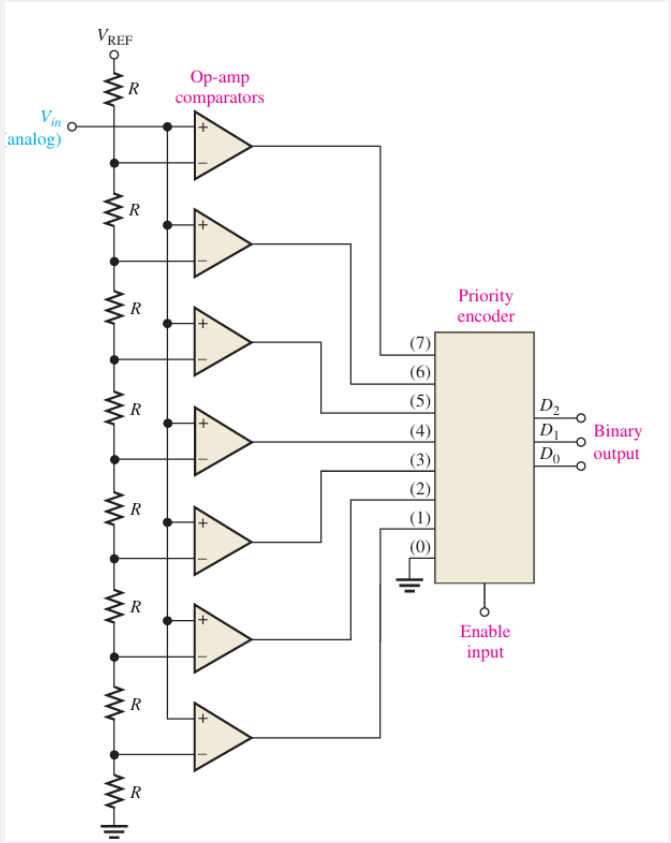
COMPARATOR APPLICATIONS

- Over-Temperature Sensing Circuit
  - A precision over-temperature sensing circuit to determine when the temperature reaches a certain critical value.
  - At normal temperatures (below critical), R_1 is greater than R_2, thus creating an unbalanced condition that drives the op-amp to its low saturated output level and keeps transistor Q_1 off.
  - As the temperature increases, the resistance of the thermistor decreases. When the temperature reaches the critical value, $R_1 = R_2$, and the bridge becomes balanced (since $R_3 = R_4$). At this point the op-amp switches to its high saturated output level, turning Q_1 on. This energizes the relay, which can be used to activate an alarm or initiate an appropriate response to the over-temperature condition.



COMPARATOR APPLICATIONS

- Analog-to-Digital (A/D) Conversion
  - Figure shows an analog-to-digital converter (ADC) that produces three-digit binary numbers on its output, which represent the values of the analog input voltage as it changes.
  - When the input voltage exceeds the reference voltage for a given comparator, a high level is produced on that comparator's output.
  - The output of each comparator is connected to an input of the *priority encoder*.
  - The *priority encoder* is a digital device that produces a binary number on its output representing the highest value input. The encoder samples its input when a pulse occurs on the enable line (sampling pulse), and a three-digit binary number proportional to the value of the analog input signal appears on the comparators' outputs.



ACTIVE FILTERS

Lecture 9

OVERVIEW

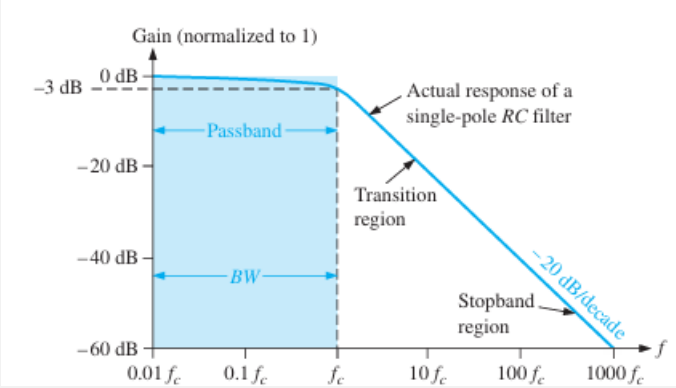
- Basic Filter Reponses
- Filter Response Characteristics
- Active Low-Pass Filters
- Active High-Pass Filters
- Active Band-Pass Filters
- Active Band-Stop Filters

BASIC FILTER RESPONSES

A **filter** is a circuit that passes certain frequencies and attenuates or rejects all other frequencies. Filters are usually categorized by the manner in which the output voltage varies with the frequency of the input voltage. The categories of active filters:

- Low-pass
- High pass
- Band-pass
- Band-stop

The **passband** of a filter is the range of frequencies that are allowed to pass through the filter with minimum attenuation (usually defined as less than $-3dB$ of attenuation). The **critical frequency**, (also called the *cutoff frequency*) defines the end of the passband and is normally specified at the point where the response drops $-3dB$ (70.7%) from the passband response. Following the *passband* is a region called the *transition* region that leads into a region called the *stopband*. There is no precise point between the *transition region* and the *stopband*.



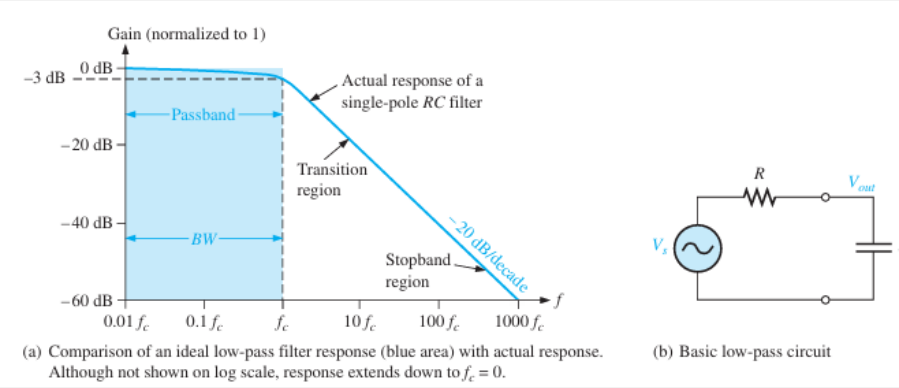
LOW-PASS FILTER RESPONSE

- Passes frequencies from DC (0 Hz) to f_c and significantly attenuates all other frequencies. The response drops to zero at frequencies beyond the pass band. The bandwidth of an ideal low-pass filter is equal to f_c.

$$BW = f_c$$

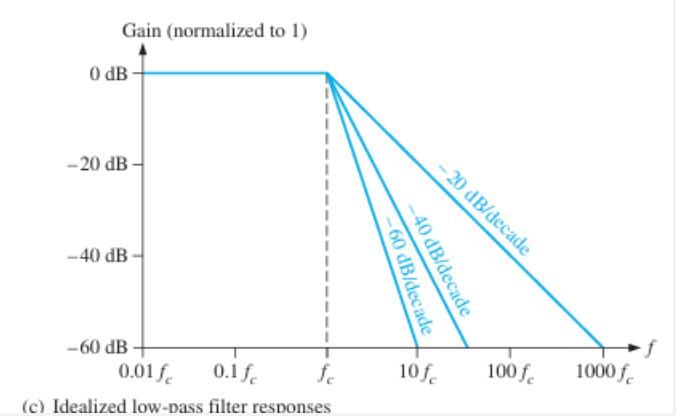
- Actual filter responses depend on the number of poles, a term used with filters to describe the number of RC circuits contained in the filter.
- The most basic low-pass filter is a simple RC circuit consisting of just one resistor and one capacitor; the output is taken across the capacitor. This basic RC filter has a single pole, and it rolls off at $-20db/decade$ beyond the critical frequency.
- The $-20dB/decade$ ***roll-off*** rate for the gain of a basic RC filter means that at a frequency of 10 f_c, the output will be $-20dB$ (10%) of the input.
- The gain drops off slowly until the frequency is at the critical frequency; after this, the gain drops rapidly.
- The critical frequency of a low-pass RC filter occurs when $X_C = R$, where

$$f_c = \frac{1}{2\pi RC}$$



(a) Comparison of an ideal low-pass filter response (blue area) with actual response. Although not shown on log scale, response extends down to $f_c = 0$.

(b) Basic low-pass circuit

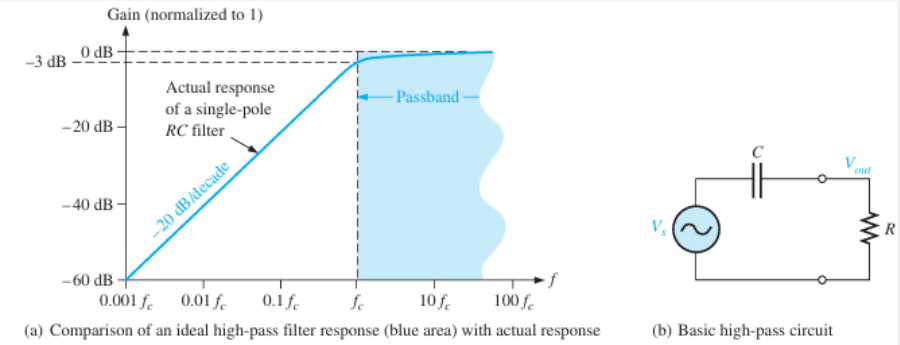


(c) Idealized low-pass filter responses

HIGH-PASS FILTER RESPONSE

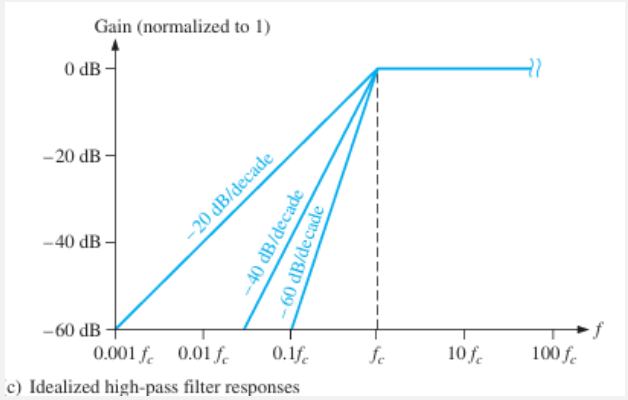
- Significantly attenuates or rejects all frequencies below and passes all frequencies above $\boldsymbol{f_c}$.
- The critical frequency is, again, the frequency at which the output is 70.7% of the input (or $-3dB$)
- The ideal response, indicated by the blue-shaded area, has an instantaneous drop at which, of course, is not achievable.
- Ideally, the passband of a high-pass filter is all frequencies above the *critical frequency*. The high-frequency response of practical circuits is limited by the op-amp or other components that make up the filter.
- A simple RC circuit consisting of a single resistor and capacitor can be configured as a high-pass filter by taking the output across the resistor as shown in Figure below. The critical frequency for the basic high pass filter occurs when $X_C = R$, where

$$f_c = \frac{1}{2\pi RC}$$



(a) Comparison of an ideal high-pass filter response (blue area) with actual response

(b) Basic high-pass circuit



c) Idealized high-pass filter responses

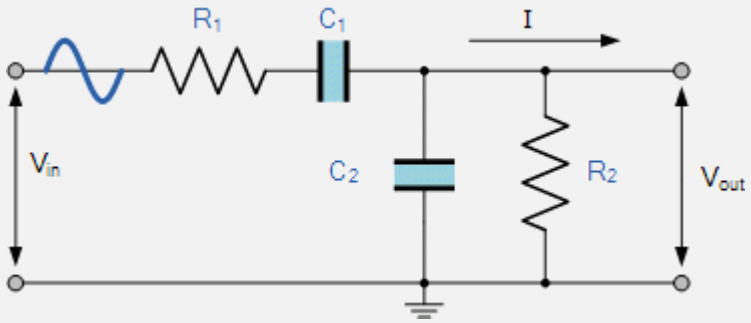
BAND-PASS FILTER RESPONSE

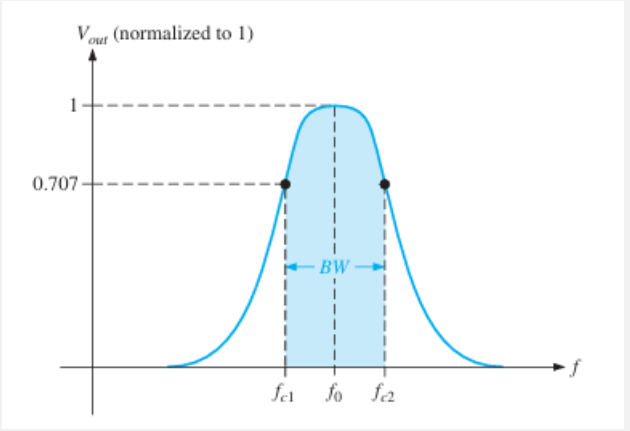
- Passes all signals lying within a band between a lower-frequency limit and an upper-frequency limit and essentially rejects all other frequencies that are outside this specified band.
- The bandwidth (BW) is defined as the difference between the upper critical frequency (f_{c2}) the lower critical frequency (f_{c1}).

$$BW = f_{c2} - f_{c1}$$

- The critical frequencies are the points at which the response curve is 70.7% of its maximum. The frequency about which the passband is centered is called the *center frequency*, f_0, defined as the geometric mean of the critical frequencies.

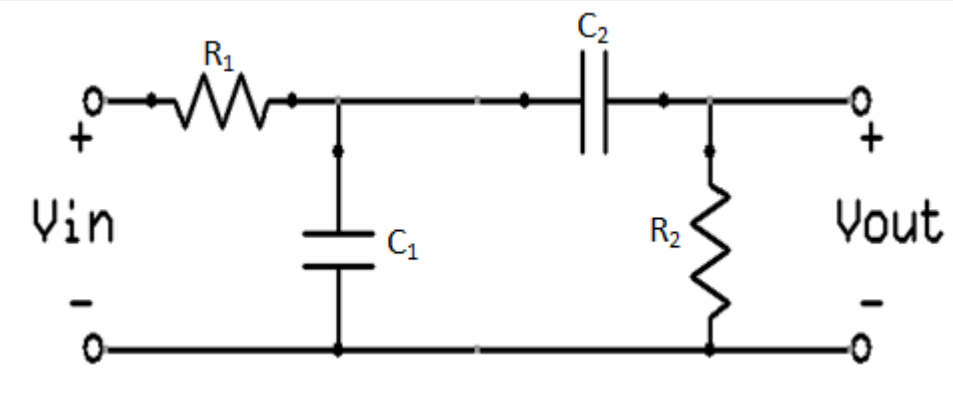
$$f_0 = \sqrt{f_{c1} f_{c2}}$$

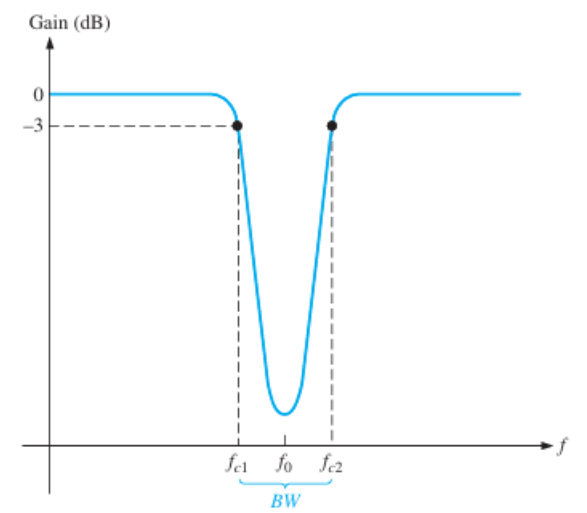




BAND-STOP FILTER RESPONSE

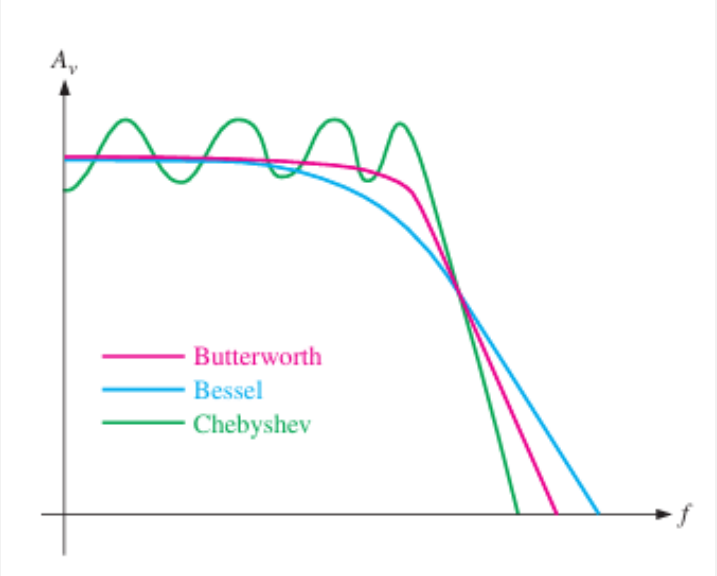
- Also known as *notch*, *band-reject*, or *band-elimination* filter.
- The operation is opposite to that of the band pass filter because frequencies within a certain bandwidth are rejected, and frequencies outside the bandwidth are passed.
- The bandwidth is the band of frequencies between the 3 dB points, just as in the case of the band-pass filter response.





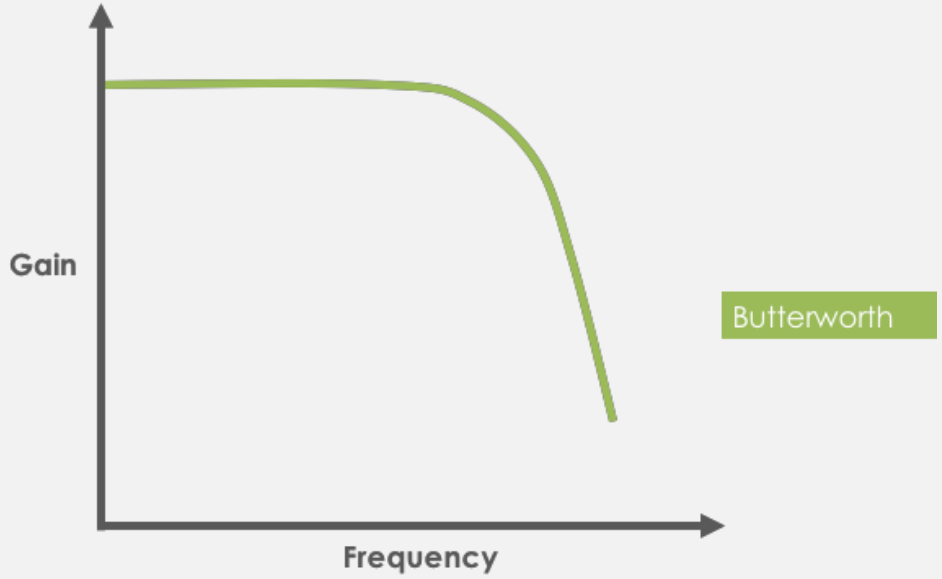
FILTER RESPONSE CHARACTERISTICS

- Each type of filter response (low-pass, high-pass, band-pass, or band-stop) can be tailored by circuit component values to have either a *Butterworth*, *Chebyshev*, or *Bessel* characteristic. Each of these characteristics is identified by the shape of the response curve, and each has an advantage in certain applications.
- *Butterworth*, *Chebyshev*, or *Bessel* response characteristics can be realized with most active filter circuit configurations by proper selection of certain component values.



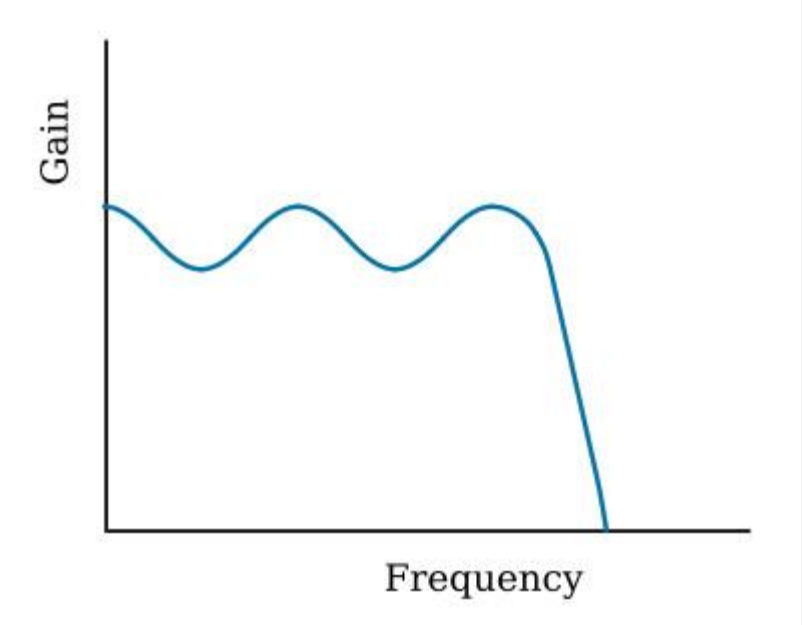
BUTTERWORTH CHARACTERISTICS

- The ***Butterworth*** characteristic provides a very flat amplitude response in the passband and a roll-off rate of -20 dB/decade/pole. The phase response is not linear, however, and the phase shift (thus, time delay) of signals passing through the filter varies nonlinearly with frequency. Therefore, a pulse applied to a filter with a Butterworth response will cause overshoots on the output because each frequency component of the pulse's rising and falling edges experiences a different time delay. Filters with the Butterworth response are normally used when all frequencies in the passband must have the same gain. The Butterworth response is often referred to as a maximally flat response.



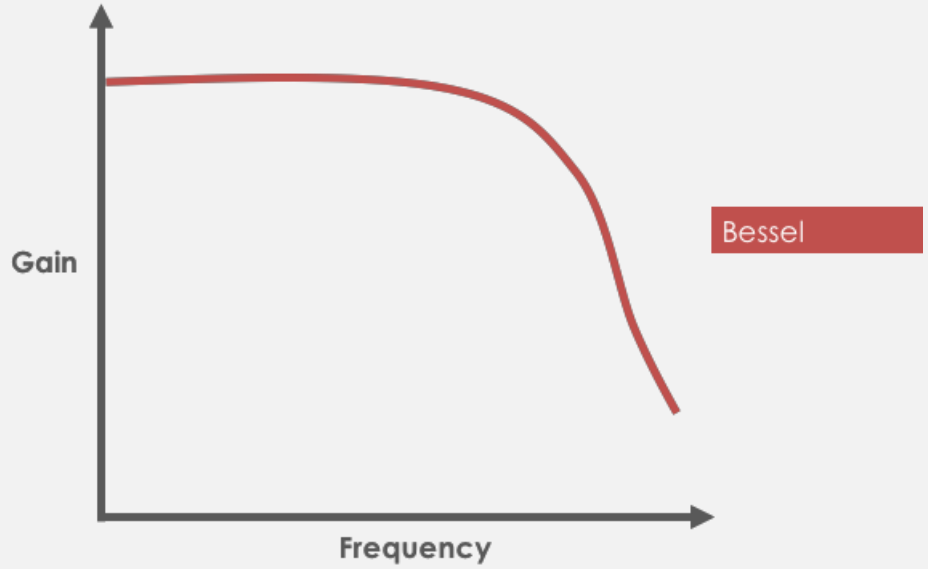
CHEBYSHEV CHARACTERISTICS

- Filters with the ***Chebyshev*** response characteristic are useful when a rapid roll-off is required because it provides a roll-off rate greater than -20 dB/decade/pole. This is a greater rate than that of the Butterworth, so filters can be implemented with the Chebyshev response with fewer poles and less complex circuitry for a given roll-off rate. This type of filter response is characterized by overshoot or ripples in the passband (depending on the number of poles) and an even less linear phase response than the Butterworth.



BESSEL CHARACTERISTICS

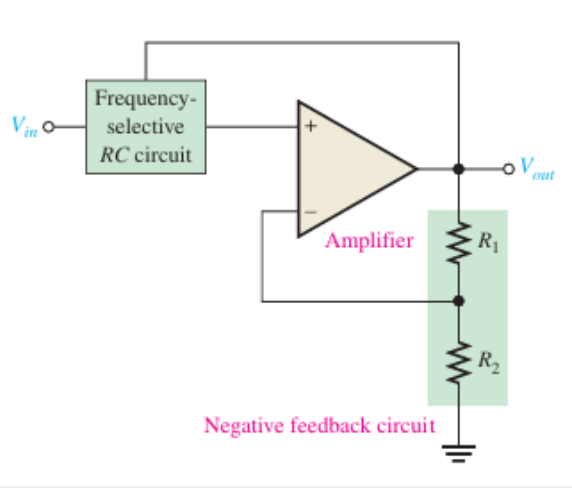
- The ***Bessel*** response exhibits a linear phase characteristic, meaning that the phase shift increases linearly with frequency. The result is almost no overshoot on the output with a pulse input. For this reason, filters with the Bessel response are used for filtering pulse waveforms without distorting the shape of the waveform.



DAMPING FACTOR

- An active filter can be designed to have either a Butterworth, Chebyshev, or Bessel response characteristic regardless of whether it is a low-pass, high-pass, band-pass, or band-stop type. The ***damping factor*** (**DF**) of an active filter circuit determines which response characteristic the filter exhibits. The value of the damping factor required to produce a desired response characteristic depends on the **order** (*number of poles*) of the filter.
- A generalized active filter includes an amplifier, a negative feedback circuit, and a filter section. The amplifier and feedback are connected in a noninverting configuration.
- The damping factor is determined by the negative feedback circuit and is defined by the following equation:

$$DF = 2 - \frac{R_1}{R_2}$$



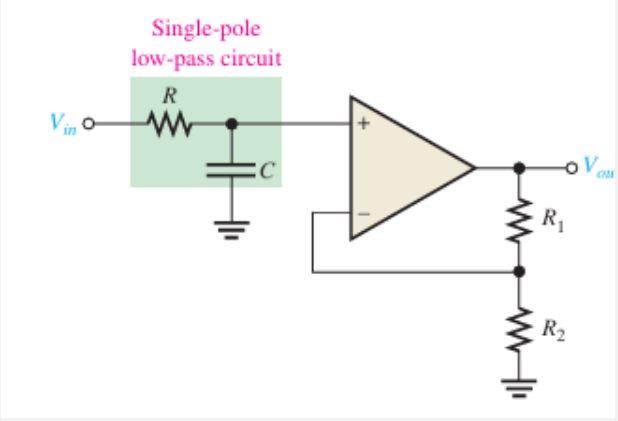
- Any attempted increase or decrease in the output voltage is offset by the opposing effect of the negative feedback. This tends to make the response curve flat in the passband of the filter if the value for the damping factor is precisely set.

CRITICAL FREQUENCY AND ROLL-OFF RATE

- The critical frequency is determined by the values of the resistors and capacitors in the frequency-selective RC circuit. For a single-pole (first-order) filter, the critical frequency is

$$f_c = \frac{1}{2\pi RC}$$

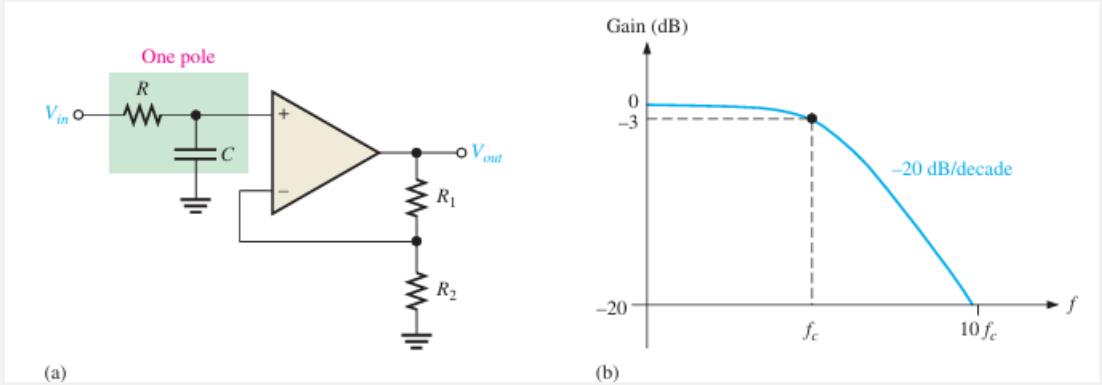
- The number of poles determines the ***roll-off rate*** of the filter. A Butterworth response produces $-20dB/decade/pole$. So, a first-order (one-pole) filter has a roll-off of $-\ 20\ dB/decade$; a second-order (two-pole) filter has a roll-off rate of $-40\ dB/decade$, a third-order (three-pole) filter has a roll-off rate of -60 $dB/decade$; so on.



ACTIVE LOW-PASS FILTER

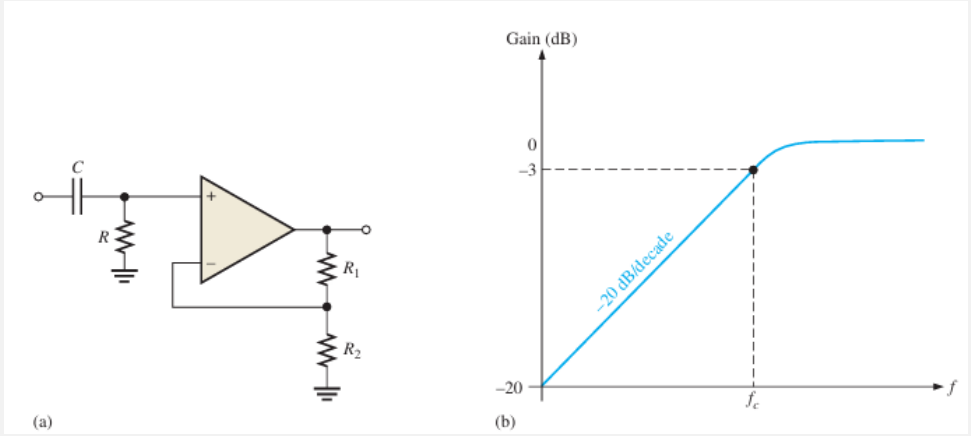
- Filters that include one or more op-amps in the design are called ***active*** filters.
- Filters that use op-amps as the active element provide several advantages over passive filters (R, L, and C elements only). The op-amp provides gain, so the signal is not attenuated as it passes through the filter. The high input impedance of the op-amp prevents excessive loading of the driving source, and the low output impedance of the op-amp prevents the filter from being affected by the load that it is driving. Active filters are also easy to adjust over a wide frequency range without altering the desired response.
- Figure below shows an active filter with a single low-pass RC frequency-selective circuit that provides a roll-off of $-20dB/decade$ above the critical frequency, as indicated by the response curve. The critical frequency of the single-pole filter is $f_c = 1/(2\pi RC)$.
- The op-amp in this filter is connected as a noninverting amplifier with the closed-loop voltage gain in the passband set by the values of R_1 and R_2:

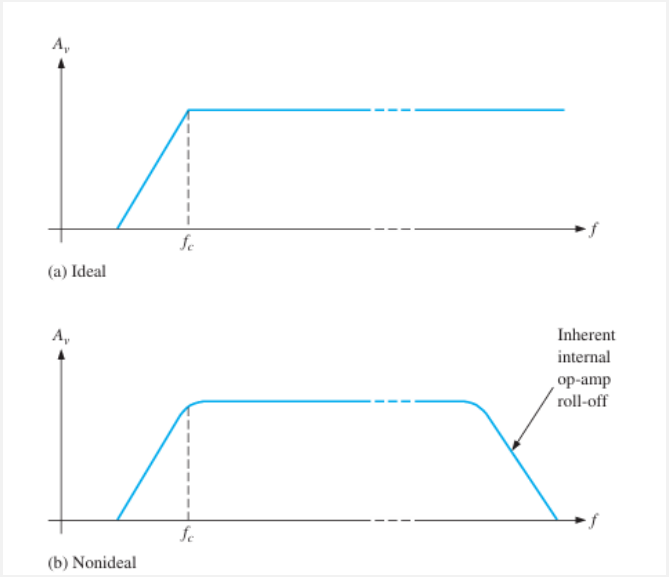
$$A_{cl(NI)} = \frac{R_1}{R_2} + 1$$



ACTIVE HIGH-PASS FILTER

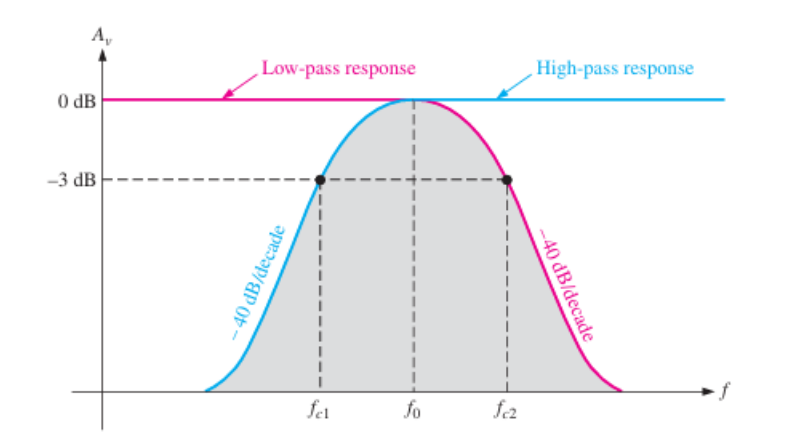
- The input circuit is a single high-pass RC circuit. The negative feedback circuit is the same as for the low-pass filters previously discussed.
- Ideally, a high-pass filter passes all frequencies above f_c without limit, although in practice, this is not the case.
- All op-amps inherently have internal RC circuits that limit the amplifier's response at high frequencies.
- Therefore, there is an upper-frequency limit on the high-pass filter's response which, in effect, makes it a band-pass filter with a very wide bandwidth.





ACTIVE BAND-PASS FILTER

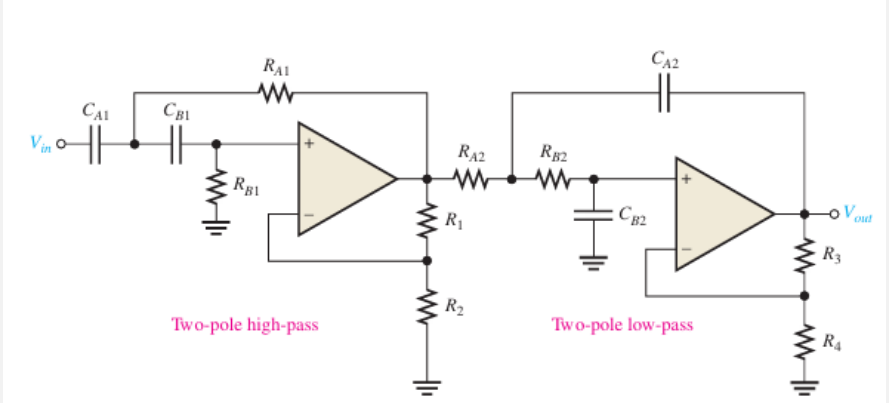
- Band-pass filters pass all frequencies bounded by a lower-frequency limit and an upper-frequency limit and reject all others lying outside this specified band. A band-pass response can be thought of as the overlapping of a low-frequency response curve and a high-frequency response curve.
- One way to implement a band-pass filter is a cascaded arrangement of a high-pass filter and a low-pass filter, as long as the critical frequencies are sufficiently separated.
- The critical frequency of each filter is chosen so that the response curves overlap sufficiently, as indicated. The critical frequency of the high-pass filter must be sufficiently lower than that of the low-pass stage. This filter is generally limited to wide bandwidth applications.
- The lower frequency of the passband is the critical frequency of the high-pass filter. The upper frequency is the critical frequency of the low-pass filter. Ideally, as discussed earlier, the center frequency of the passband is the geometric mean of f_{c1} and f_{c2}



$$f_{c1} = \frac{1}{2\pi\sqrt{R_{A1}R_{B1}C_{A1}C_{B1}}}$$

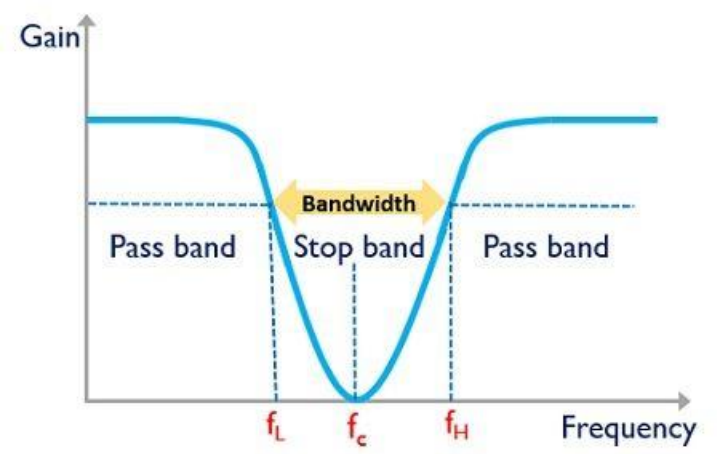
$$f_{c2} = \frac{1}{2\pi\sqrt{R_{A2}R_{B2}C_{A2}C_{B2}}}$$

$$f_0 = \sqrt{f_{c1}f_{c2}}$$

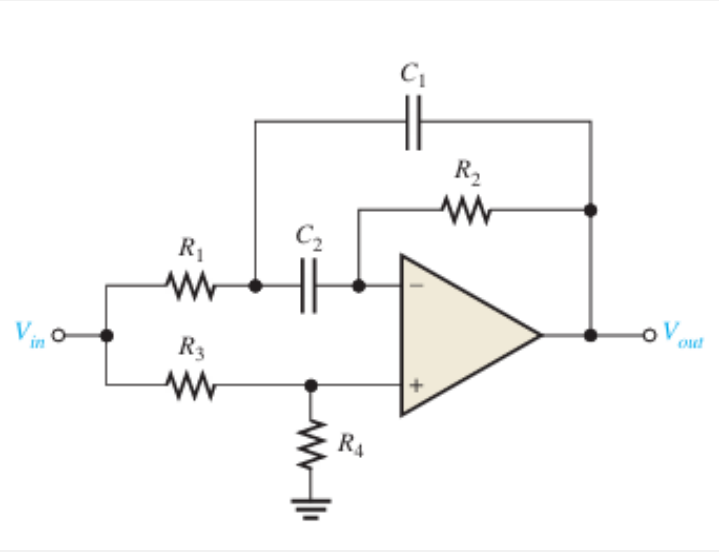


ACTIVE BAND-STOP FILTER

- Band-stop filters reject a specified band of frequencies and pass all others. The response is opposite to that of a band-pass filter.
- Band-stop filters are sometimes referred to as *notch filters*.
- Figure below shows a multiple-feedback band-stop filter.



Frequency Response



VOLTAGE REGULATOR

Lecture 11

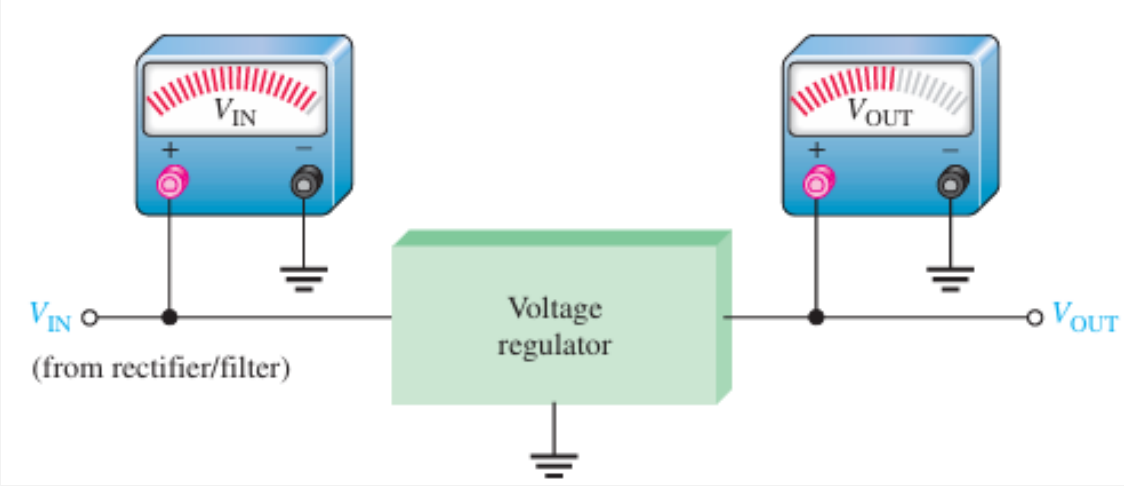
OVERVIEW

- Voltage Regulation
- Basic Linear Series Regulators
- Basic Linear Shunt Regulators
- Basic Switching Regulators
- Integrated Circuit Voltage Regulators

VOLTAGE REGULATION

Two basic categories of voltage regulation:

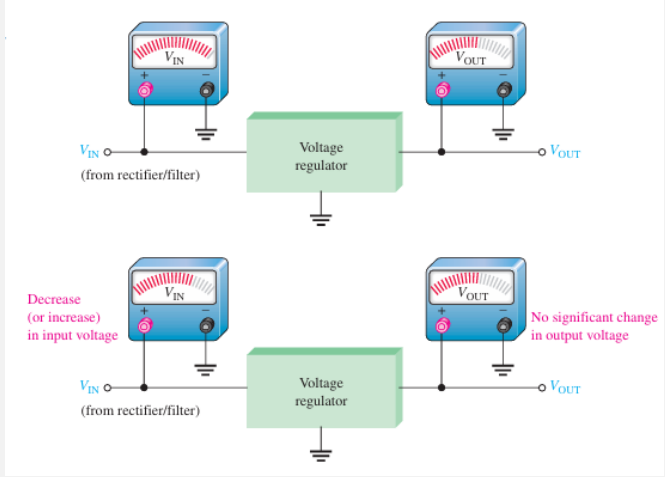
- **Line Regulation** – maintain a nearly constant output voltage when the input voltage varies.
- **Load Regulation** – maintain a nearly constant output voltage when the load varies.



LINE REGULATION

- When the AC input (line) voltage of a power supply changes, an electronic circuit called a regulator maintains a nearly constant output voltage. Line regulation can be defined as the percentage change in the output voltage for a given change in the input voltage. When taken over a range of input voltage values, line regulation is expressed as a percentage by the following formula:

$$Line\ regulation = \left(\frac{\Delta V_{OUT}}{\Delta V_{in}}\right) 100\%$$



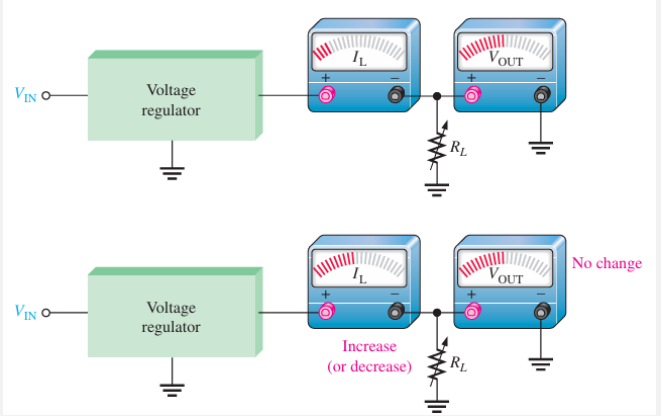
- Line regulation can also be expressed in units of %/V. For example, a line regulation of 0.05%/V means that the output voltage changes 0.05 percent when the input voltage in increases or decreases by one Volt. Line regulation can be calculated using the following formula:

$$Line\ regulation = \left(\frac{\Delta V_{OUT}/V_{OUT}}{\Delta V_{in}}\right) 100\%$$

LOAD REGULATION

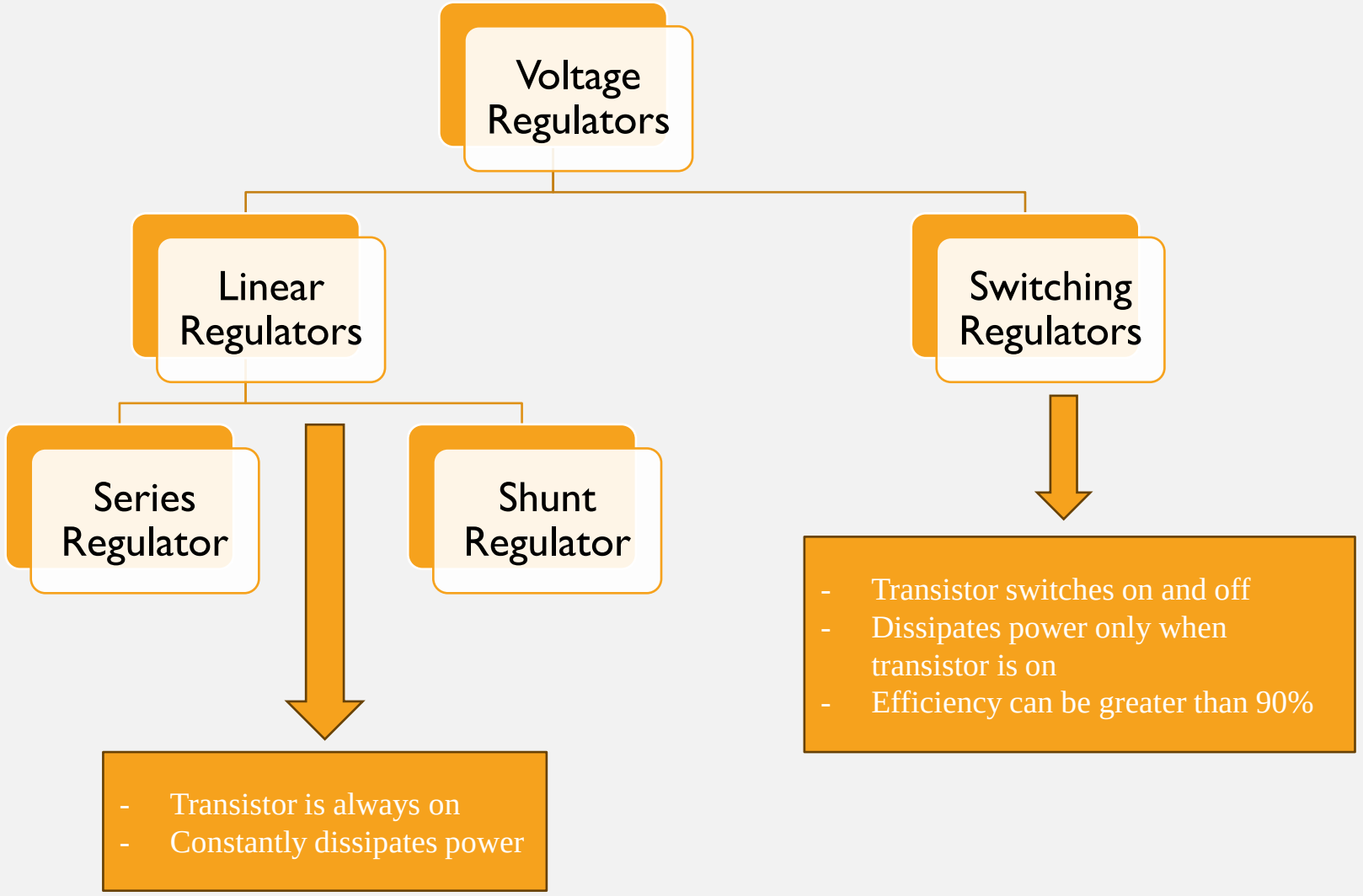
- When the amount of current through a load changes due to a varying load resistance, the voltage regulator must maintain a nearly constant output voltage across the load.
- A change in load current has practically no effect on the output voltage of a regulator (within certain limits).
- **Load regulation** can be defined as the percentage change in output voltage for a given change in load current. One way to express load regulation is as a percentage change in output voltage from no-load (NL) to full-load (FL):

$$Load\ regulation = \left(\frac{V_{NL} - V_{FL}}{V_{FL}}\right) 100\%$$



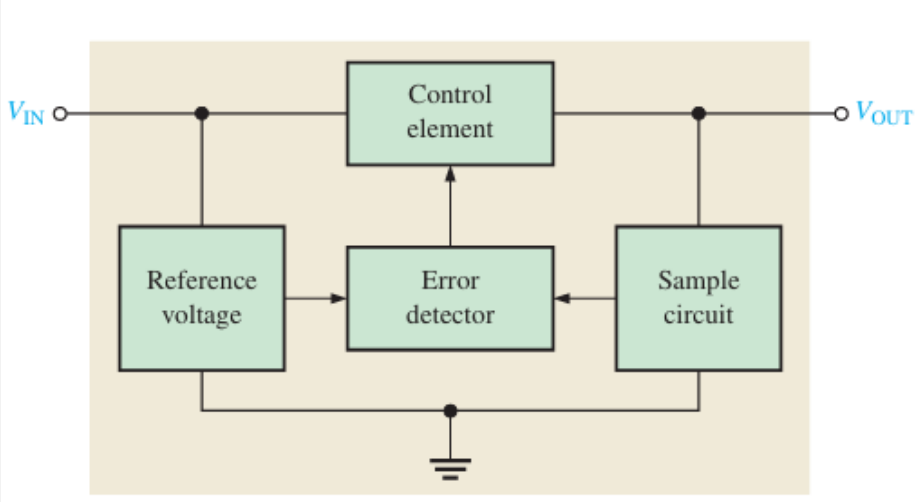
- Alternately, the load regulation can be expressed as a percentage change in output voltage for each mA change in load current. For example, a load regulation of $0.01\%/mA$ means that the output voltage changes 0.01 percent when the load current increases or decreases 1 mA.

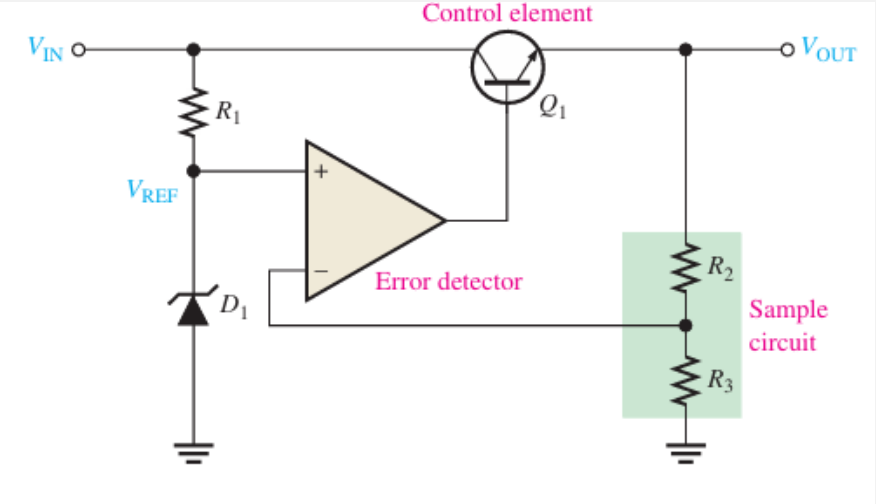
BASIC LINEAR SERIES REGULATORS



SERIES REGULATOR

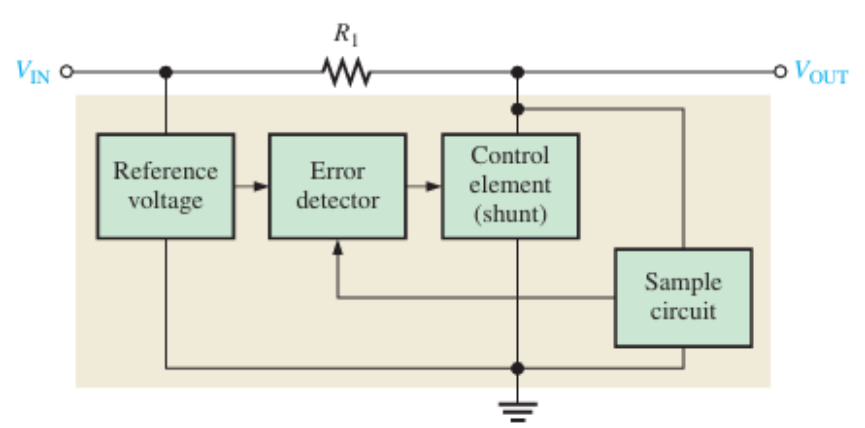
- The control element is a pass transistor in series with the load between the input and output.
- The output sample circuit senses a change in the output voltage.
- The error detector compares the sample voltage with a reference voltage and causes the control element to compensate in order to maintain a constant output voltage.

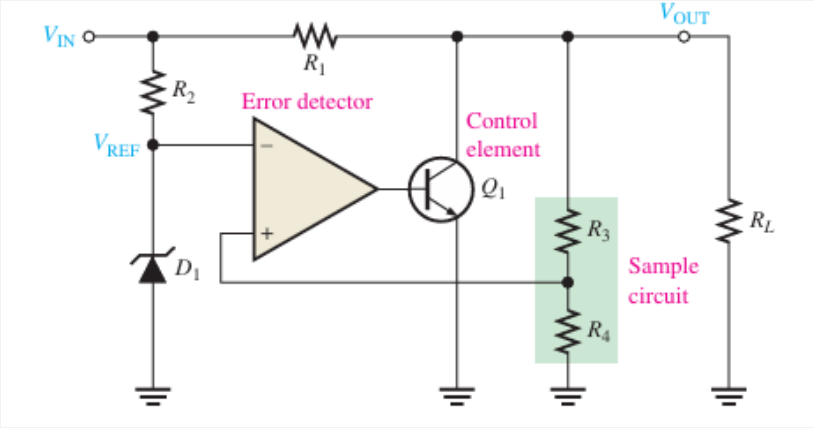




SHUNT REGULATORS

- The control element is a transistor, Q_1, in parallel with the load.
- A resistor, R_1, is in series with the load.





BASIC SWITCHING REGULATORS

- Switching regulators are designed for various power levels.
- They range in power levels from less than one watt for some battery-operated portable equipment to hundreds and thousands of watts in major applications.
- The requirements for the application determine the particular design, but all switching regulators require feedback to control the on-off time for the switch.

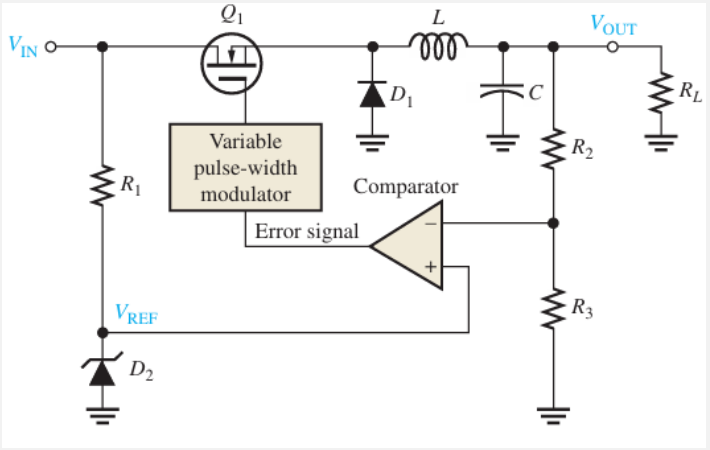
- Three basic configurations of switching regulators are
  - Step-down,
  - Step-up
  - Inverting

- In some cases, such as a laptop computer, all three types may be employed for various parts of the system; for example, the display typically will use an inverting type, the microprocessor would use a step-down type, and the disk drive may use a step-up type.

STEP-DOWN CONFIGURATION

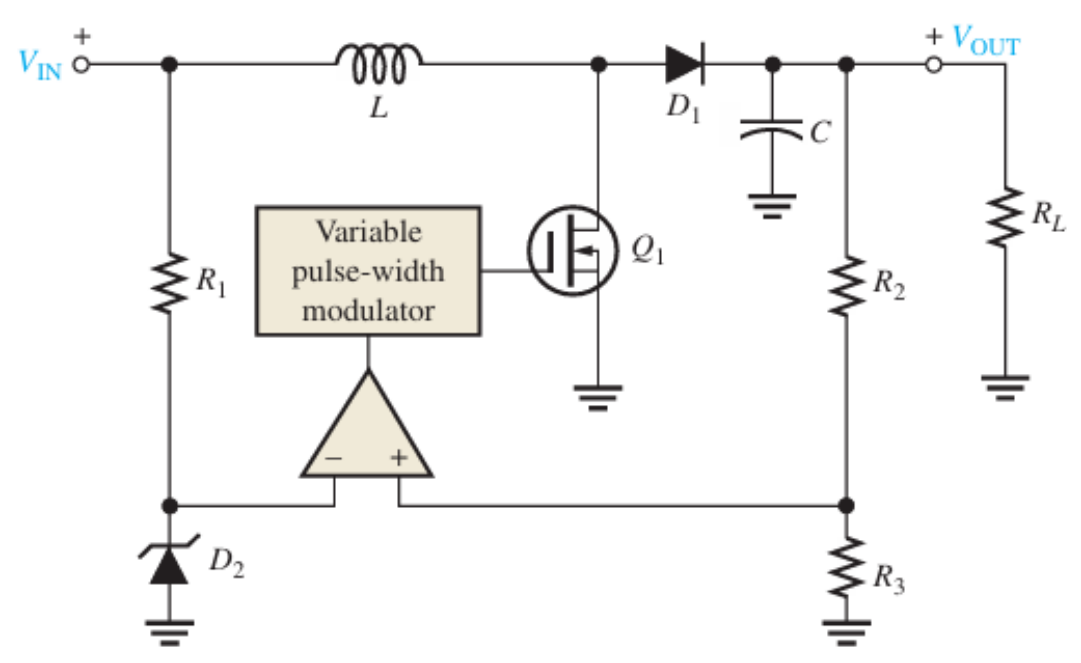
- In the step-down configuration (also called a *buck converter*), the output voltage is always less than the input voltage.
- The basic control element is a high-speed switch, which opens and closes rapidly from a control circuit that senses the output, and it adjusts the on-time and the off-time to keep the desired output.
- When the switch is closed, the diode is off and the magnetic field of the inductor builds, storing energy.
- When the switch opens, the magnetic field collapses, keeping nearly constant current in the load.
- A path for the load current is provided through the forward-biased diode (as long as the load resistance is not too large).
- The capacitor smoothes the DC to a nearly constant level.

- Figure shows a basic step-down switching regulator using a D-MOSFET switching transistor.
- MOSFET transistors can switch faster than BJTs and have been improved in recent years, so they have become the preferred type of switching device, provided that the off-state voltage is not too high.



STEP-UP CONFIGURATION

- A basic step-up type of switching regulator (sometimes called a *boost converter*) is shown in Figure below, where transistor Q_1 operates as a switch to ground.



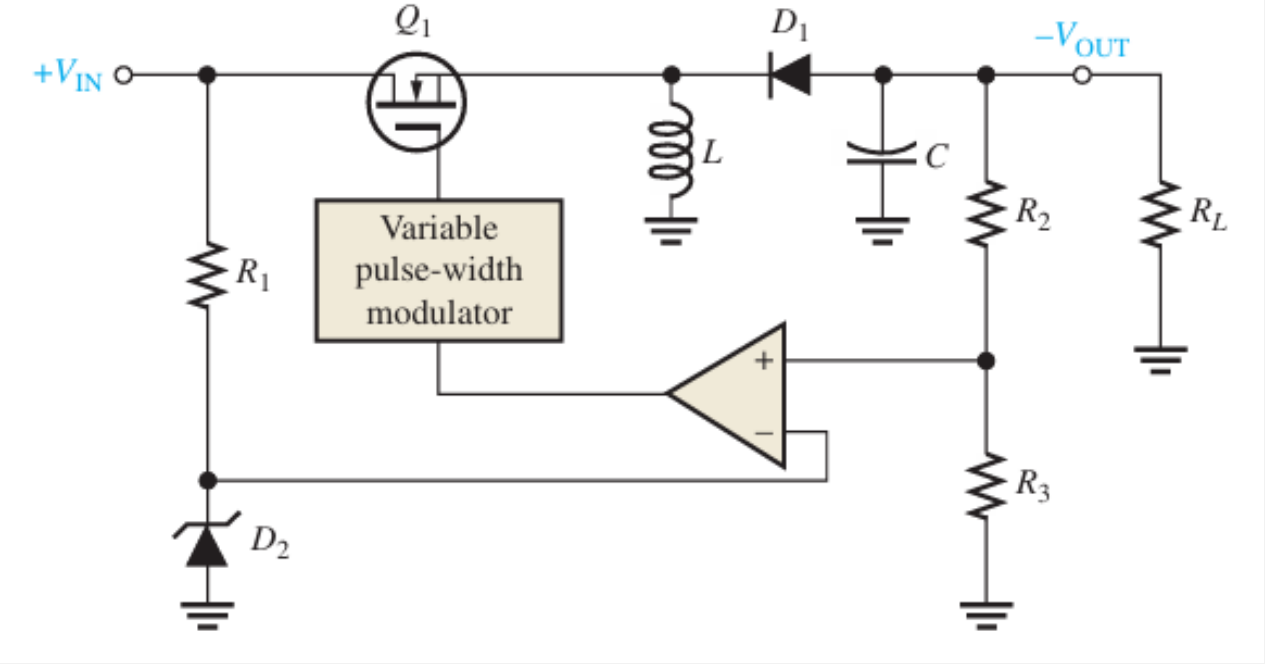
STEP-UP CONFIGURATION

- When Q_1 turns on, a voltage equal to approximately V_{IN} is induced across the inductor with a polarity.
- During the on-time (t_{on}) of Q_1, the inductor voltage, V_L, decreases from its initial maximum and diode D_1 is reverse-biased.
- The longer Q_1 is on, the smaller V_L becomes.
- During the on-time, the capacitor only discharges an extremely small amount through the load.
- When Q_1 turns off, the inductor voltage suddenly reverses polarity and adds to V_{IN}, forward-biasing diode D_1 and allowing the capacitor to charge.
- The output voltage is equal to the capacitor voltage and can be larger than V_{IN} because the capacitor is charged to V_{IN} plus the voltage induced across the inductor during the off-time of Q_1.
- The output voltage is dependent on both the inductor's magnetic field action (determined by t_{on}) and the charging of the capacitor (determined by t_{off}).
- Voltage regulation is achieved by the variation of the on-time of Q_1 (within certain limits) as related to changes in V_{OUT} due to changing load or input voltage.
- If V_{OUT} tries to increase, the on-time of Q_1 will decrease, resulting in a decrease in the amount that C will charge.
- If V_{OUT} tries to decrease, the on-time of Q_1 will increase, resulting in an increase in the amount that C will charge. This regulating action maintains V_{OUT} at an essentially constant level.

VOLTAGE-INVERTER CONFIGURATION

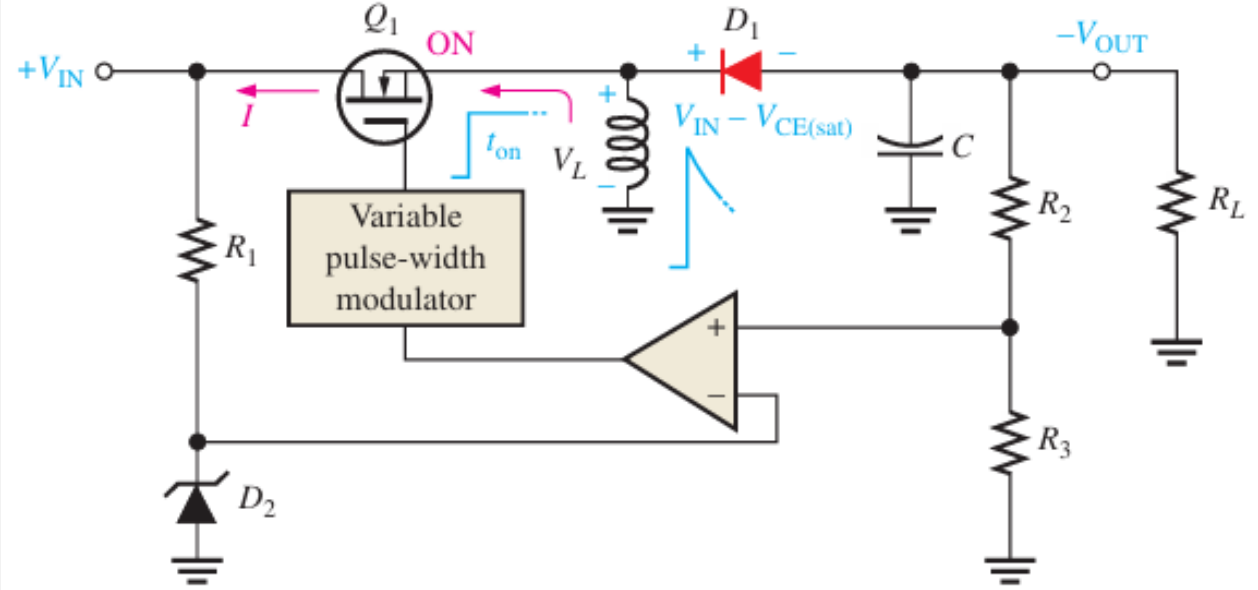
- Produces an output voltage that is opposite in polarity to the input.

- Sometimes called a *buck-boost* converter.



VOLTAGE-INVERTER CONFIGURATION

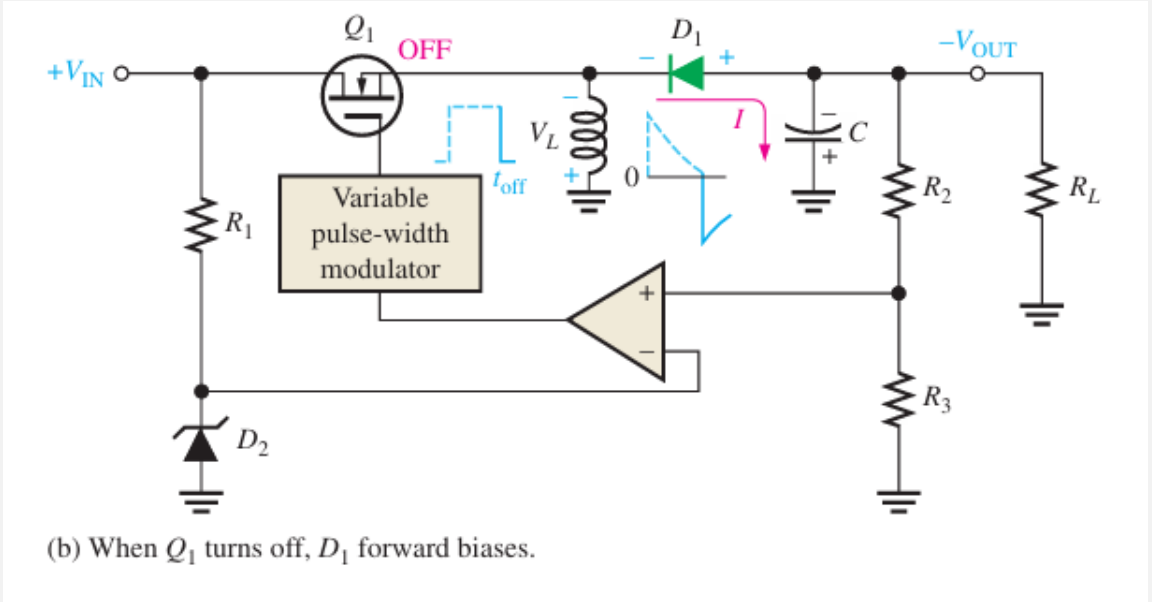
- When Q_1 turns on, the inductor voltage jumps to approximately $V_{IN} - V_{CE(sat)}$ and the magnetic field rapidly expands, as shown.
- While Q_1 is on, the diode is reverse-biased and the inductor voltage decreases from its initial maximum.



(a) When Q_1 is on, D_1 is reverse-biased.

VOLTAGE-INVERTER CONFIGURATION

- When Q_1 turns off, the magnetic field collapses and the inductor's polarity reverses.
- This forward-biases the diode, charges C, and produces a negative output voltage, as indicated.
- The repetitive on-off action of Q_1 produces a repetitive charging and discharging that is smoothed by the LC filter action.



(b) When Q_1 turns off, D_1 forward biases.