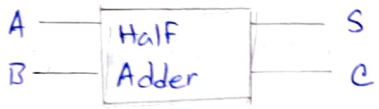
Experiment No. 2a

Aim: - Implementation of half adder using logic gates.

Theory: A combinational logic circuit that performs the addition of two data bits A and B called a half adder. Addition will result in two output bits one of which is Sum(S) and the other is Carry bit (C). The Boolean functions describing the half adder are:

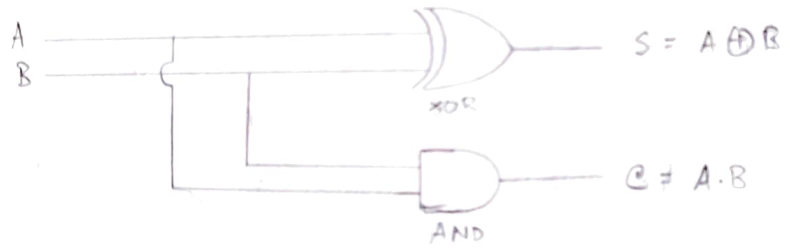
$$S = A'B + AB' = A \oplus B$$

$$C = A \cdot B$$



Apparatus Required: IC 4081, IC4070, digital trainer kit

Half Adder Using Basic Gates:



TRUTH TABLE:

INPUT		OUTPUT	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Adder K-map:

For Sum (S): $S = A \oplus B$

A \ B	0	1
0	0	1
1	1	0

For Carry (C): $C = A \cdot B$

A \ B	0	1
0	0	0
1	0	1

Result: Half adder is constructed and truth table is verified.

Experiment No: (2 b)

Aim: Implementation of Full Adder using logic gates.

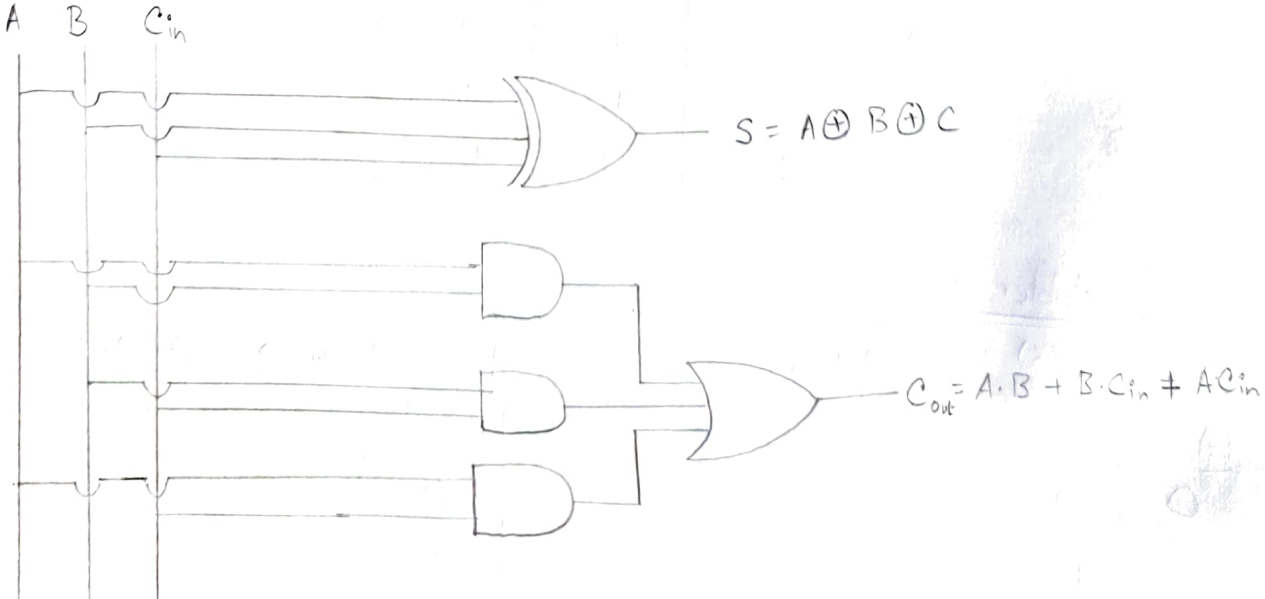
Theory: The half adder does not take the carry bit from its previous stage into account. This carry bits from its previous stage is called carry-in- bit. A full adder adds three one bit binary numbers - two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit

The boolean functions for describing full adder are:

$$S = A \oplus B \oplus C$$

$$C_{out} = A \cdot B + B \cdot C_{in} + A \cdot C_{in}$$

Full Adder using Basic Gates:



Truth Table:

Input			Output	
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map for Full Adder:

For $S = A \oplus B \oplus C$

A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	1	0

For $C_{out} = A \cdot B + B \cdot C_{in} + C_{in} \cdot A$

A \ BC	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Result:

Full Adder is constructed and it's truth table is verified.

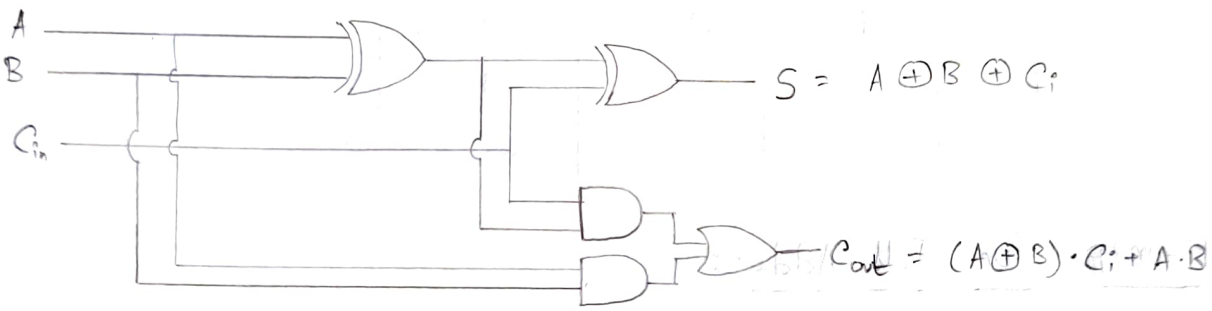
Experiment No. 2c

Aim: Implementation of a full adder using two half adders and an OR Gate.

Apparatus Required: IC 4081, IC 4070, IC 4071, Digital trainer kit, wires

Theory: A full adder is a digital circuit that performs addition. A full adder can be constructed from two half adders by connecting A and B input of one half adder, connecting the sum from that to an input to the second adder, connecting the carry in C_{in} to the other input and OR-ing the two half adders carry outputs to give the final carry output.

Circuit Diagram:



Truth table:

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Result:

Full adder using two half adders and OR gate is constructed and its truth table is verified.

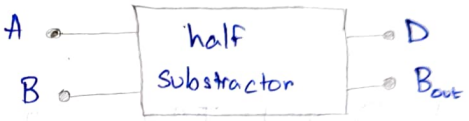
Experiment No. 2d

Aim: Implementation of half substractor using logic gates

Theory: Substracting a single bit binary value B from another A produces a difference bit D and a borrow bit B_{out}. The operation is called half Subtraction and the circuit to realize it is called half substractor. The Boolean functions describing the half substractor are:

$$D = A \oplus B$$

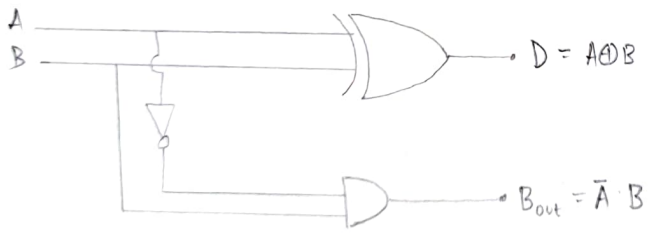
$$B_{out} = \bar{A} \cdot B$$



Apparatus Required:

IC 4070, IC 4069, IC 4081, Digital Trainer's kit, wires.

Circuit Diagram:



Truth Table:

A	B	D	B_{out}
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

K-map:

Difference (D): $D = A \oplus B$

A \ B	0	1
0	0	1
1	1	0

For Borrow (B_0): $B_{out} = \bar{A} \cdot B$

A \ B	0	1
0	0	1
1	0	0

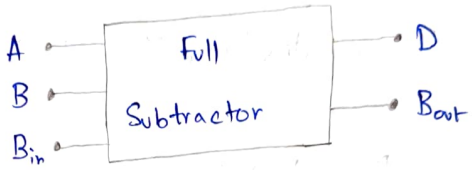
Result: Half Substractor is constructed and truth table is verified.

Aim: Implementation of Full Substractor using logic gates.

Theory: Subtracting two binary values (single bit), B and B_{in} from a single bit value A produces a difference bit D and a B_{out} borrow out bit. This is called full substraction. The Boolean functions describing the full Subtrater are:

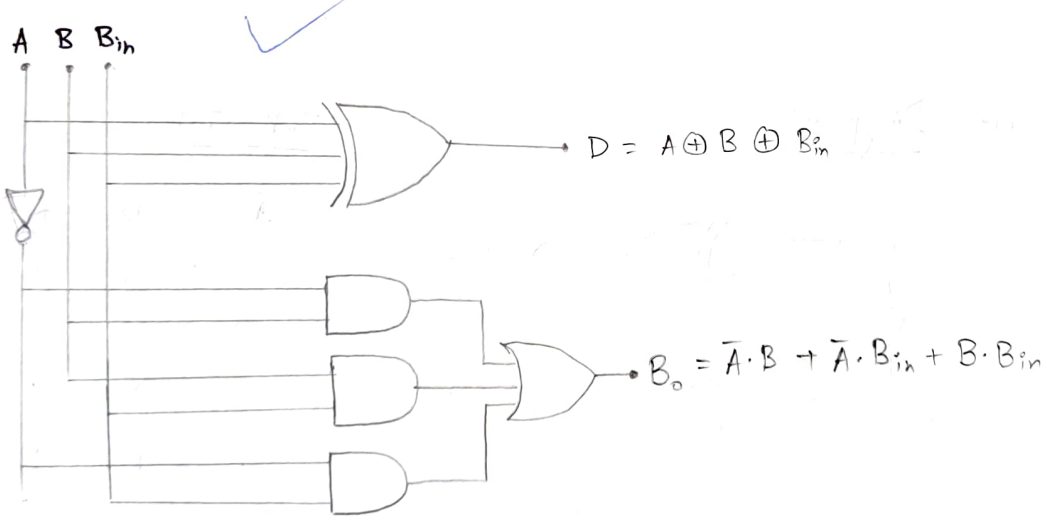
$$D = A \oplus B \oplus B_{in}$$

$$B_{out} = \bar{A} \cdot B + \bar{A} \cdot B_{in} + B \cdot B_{in}$$



Apparatus Required: IC 4081, IC 4070, IC 4069, IC 4071, Digital Trainer kit, Wires

Circuit Diagrams:



Truth Table:

INPUT			OUTPUT	
A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-map:

For Difference

A \ BBin	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$D = A'B'B_{in} + A'B\cdot B_{in}' + AB'\cdot B_{in}' + ABB_{in}$

$= A \oplus B \oplus B_{in}$

For Borrow out

A \ BBin	00	01	11	10
0	0	1	1	1
1	0	0	1	0

$B_o = A'B_{in} + A'B + BB_{in}$

Result:

Full subtractor is constructed and truth table is verified

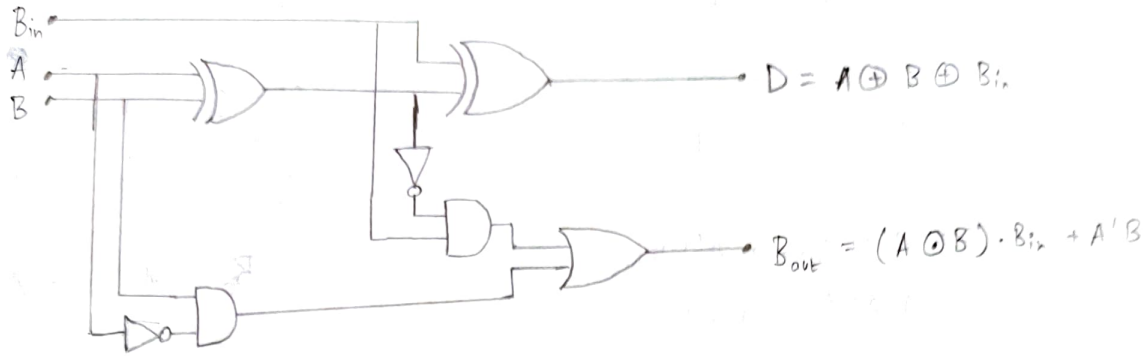
Experiment: 2f

Aim: Implementation of a full substractor using two half subtractors and OR Gate.

Theory: The full subtractor is a combinational circuit which is used to perform subtraction of three input bits, the minuted, subtracted, and borrow in. The difference output from the second half subtrator is the XOR of B_{in} and the output of the first half subtracter which is same as variance output of full subtracter. This circuit has three inputs and two outputs:

Apparatus Required: IC4081, IC4070, IC4071, IC4069, Digital Trainer kit, wires

Circuit Diagram:



Expression for difference:-

$$D = A'B'B_{in} + A'BB_{in}' + AB'B_{in}' + ABB_{in}$$
$$= B_{in}(A'B' + AB) + B_{in}'(AB' + A'B)$$
$$= B_{in}(A \oplus B)' + B_{in}'(A \oplus B)$$
$$= A \oplus B \oplus B_{in}$$

Expression for Borrow Out (B_o)

$$B_o = A'B'B_{in} + A'B \cdot B_{in}' + A'BB_{in} + ABB_{in}$$
$$= A'B'B_{in} + A'BB_{in} + A'BB_{in} + A'BB_{in} + A'BB_{in}$$
$$= A'B_{in}(B + B') + A'B(B_{in} + B_{in}') + BB_{in}(A + A')$$
$$= A'B_{in} + A'B + BB_{in}$$

OR,

$$B_o = A'B'B_{in} + A'BB_{in}' + A'BB_{in} + ABB_{in}$$
$$= B_{in}(AB + A'B') + A'B(B_{in} + B_{in}')$$
$$= B_{in}(A \odot B) + A'B$$

Result:

Full substractor using two subtractors and OR gate is constructed and thus the table is verified.

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