Experiment No. 10(A)

Experiment Name: Truth Table verification of SR flip-flop.

Theory:- The SET-RESET flip-flop is designed with the help of two NOR Gates and also two NAND Gates. These flipflop are also called SR Latch. The design of such a flip-flop includes two inputs called the SET [S] and RESET [R]. There are also two outputs Q and Q'

S = 1, R = 0, Q = 1, Q' = 0

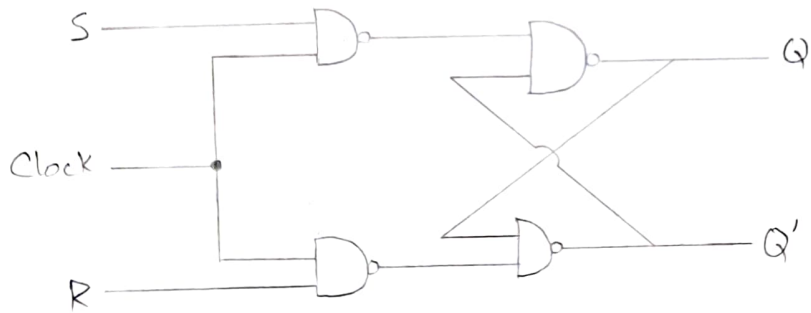
This state is also called the SET state

S = 0, R = 1, Q = 0, Q' = 1

This state is known as the RESET state

Apparatus Required: Digital Trainer kit, NAND Gate - IC 4011, Wires

Circuit Diagram:



Truth Table:

Clock	S	R	Q
Not Trigger	x	x	Q
Trigger	0	0	Hold
Trigger	0	1	0
Trigger	1	0	1
Trigger	1	1	Invalid

Conclusion :

Hence from this experiment, we were able to verify the truth table of SR flipflop.

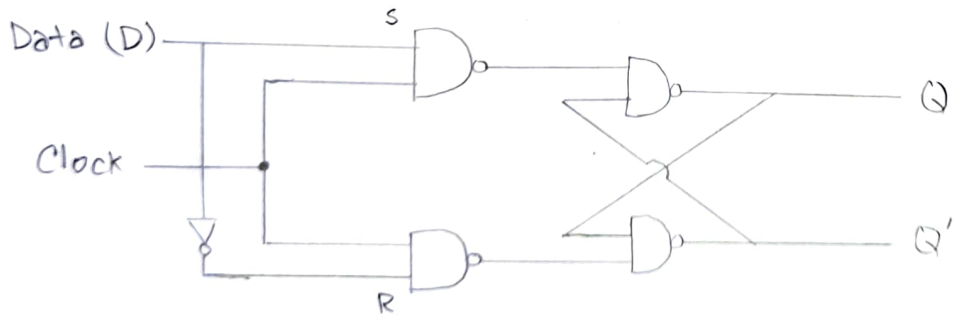
● Experiment No: 10(B)

Experiment Name :- Truth table verification of D flipflop.

Theory: The D flip-flop has one data input 'D' and a clock input. The circuit ldge triggers on the clock input. The flipflop has two outputs Q and Q'. The D flipflop is the most imported of the clocked flipflops as it ensures that input S and R are never equal to one at the same time.

Apparatus Required: IC Trainer kit, NAND Gate - IC 4011, NOT Gate - IC 4069, Connecting wires.

Circuit Diagram :



Truth Table :

Clock	D	Q	$\bar{Q}$
↓ 0	x	Q	$\bar{Q}$
↑ 1	0	0	1
↑ 1	1	1	0

Conclusion: Hence from this experiment we were able to verify the truth table of D flipflop.

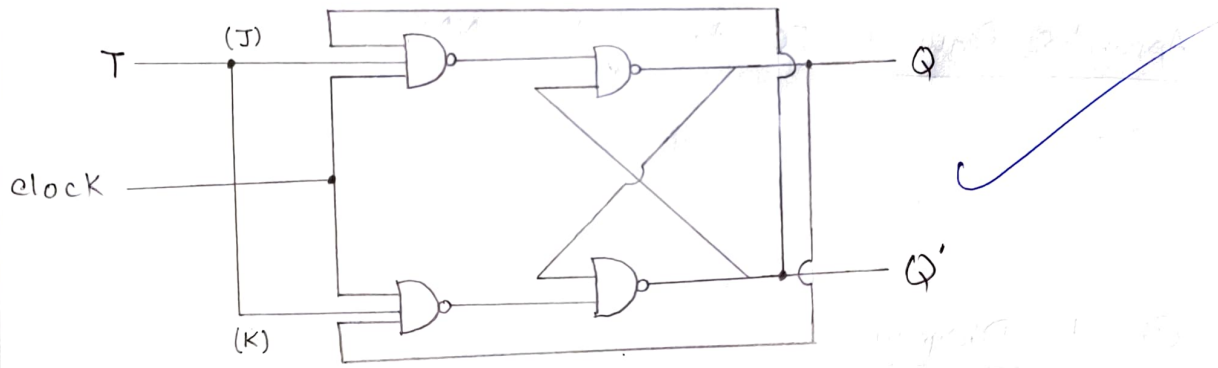
Experiment No. - 10 (C)

Experiment Name: Truth table verification of T flipflop.

Theory: T flipflip is known as toggle flipflop. In this flipflop we need just one input T and gives us two output Q and $\bar{Q}$. The T flipflop is the modification of the JK flipflop. Both the JK flipflop input are held at logic 1 and clock signal continious to change.

Apparatus Required: IC Trainer kit, NAND Gate - IC4011, wire

Circuit Diagram:



Truth Table:

T	Previous		Next	
	Q_{prev}	Q'_{prev}	Q_{next}	Q'_{next}
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	0	1

Conclusion: Hence, from this experiment we were able to verify the truth table of T flipflop.

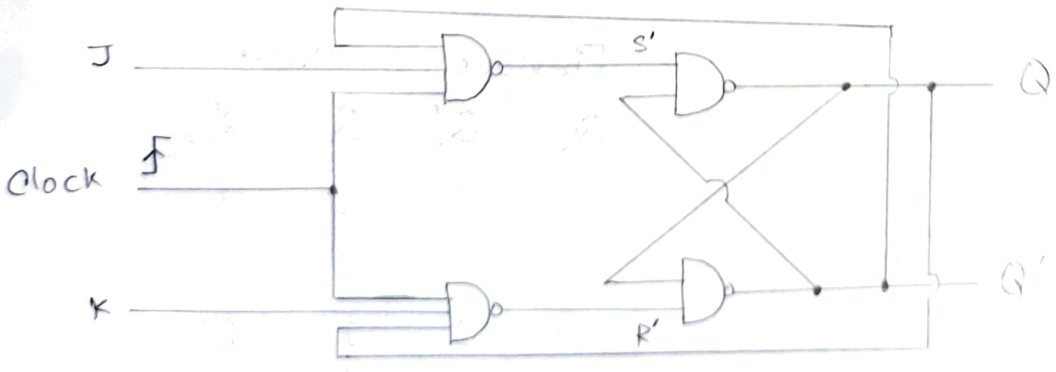
Experiment No. 10(D)

Experiment Name: Truth table verification of JK flipflop

Theory: The JK flipflop is basically a SR flipflop with the addition of a clock input circuitly that prevents the invalid output condition that can occur when both input S and R are equal to logic level "1" Due to this additional clocked input, a JK flipflop has four possible input combinations "logic 1", "logic 0", "no change" and "toggle". JK flipflop needs two inputs "J" and "K" and it gives two outputs 'Q' and 'Q'.

Apparatus Required: IC trainer kit, NAND Gates - IC4011, Connecting wires.

Circuit Diagram:



Truth Table:

	J	K	Q	$\overline{Q}$
Same As SR Latch	0	0	0	0
	0	0	0	1
	0	1	1	0
	0	1	0	1
	1	0	0	1
	1	0	1	0
Toggle Action	1	1	0	1
	1	1	1	0

Conclusion:

Hence from this experiment we were able to verify the truth table of JK flipflop.