Experiment NO. - 7

Aim: Building a 2bit comparator using logic gates.

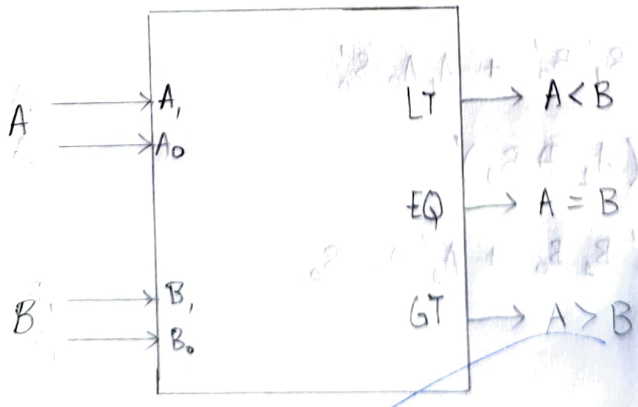
Component Required: Digital trainer kit, XOR Gate, OR Gate, AND Gate, NOT Gate and Copper Wires.

Theory: A comparator is a combinational logic circuit which compares 2 binary numbers (N1 and N2) and determines if N1 is lesser than (LT)/ equals to (EQ) /greater than (GT) N2.

A 2bit comparator has two input lines for each of the 2-bit binary numbers, with three distinct output lines, which denotes LT, EQ and GT respectively. If one of three outputs is 1, then rest are 0.

Because two numbers can attain only one state from the following - i) $A < B$, ii) $A = B$, iii) $A > B$. Here Binary numbers are represented as $N1 = A_1A_0$ and $N2 = B_1B_0$ (A_1, A_0 and B_1, B_0 being the bit of the two numbers respectively.

Block Diagram:



Truth Table:

INPUTS				OUTPUTS		
A_1	A_0	B_1	B_0	GT (A>B)	EQ (A=B)	LT (A<B)
0	0	0	0	0	1	0
		0	1	0	0	1
		1	0	0	0	1
		1	1	0	0	1
0	1	0	0	1	0	0
		0	1	0	1	0
		1	0	0	0	1
		1	1	0	0	1
1	0	0	0	1	0	0
		0	1	1	0	0
		1	0	0	1	0
		1	1	0	0	1
1	1	0	0	1	0	0
		0	1	1	0	0
		1	0	1	0	0
		1	1	0	1	0

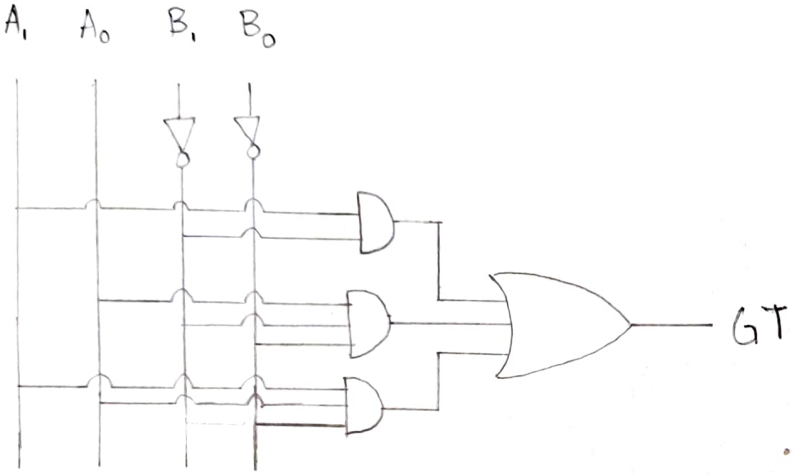
Equation for GT, EQ, LT obtained from the truth table are

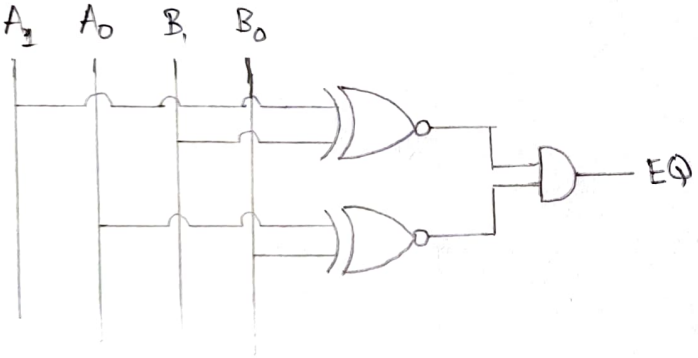
GT – $A_1 B_1' + A_0 B_1' B_0' + A_1 A_0 B_0'$

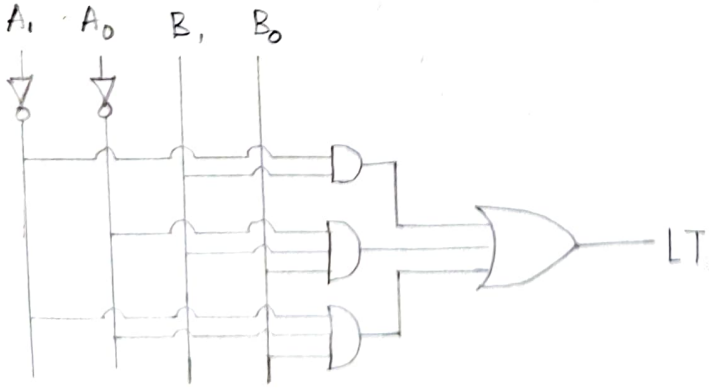
EQ – $(A_0 \oplus B_0)' (A_1 \oplus B_1)'$

LT – $A_1' B_1 + A_0' B_1 B_0 + A_1' A_0' B_0$

Circuit Diagrams:







Result: 2 bit comparator circuit was made and its truth table is verified.

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