Experiment NO. 8(a)

Aim: Implementation of 4×1 Multiplexer circuit using logic gates.

Apparatus Required: Digital Trainer kit, wires, 3 input AND Gate, OR Gate

Theory: Multiplexer generally means many into one. A multiplexer is a circuit with many Inputs but only one output. By applying control signals we can steer any input to the output. The fig(1) shows the general idea. The circuit has n-input signal, control signal & one output signal. Where $2^n = m$. One of the popular multiplexer is the 16 to 1 multiplexer, which has 16 input bits, 4 control bits & 1 output bit.

Block Diagram for 4:1 MULTIPLEXER:

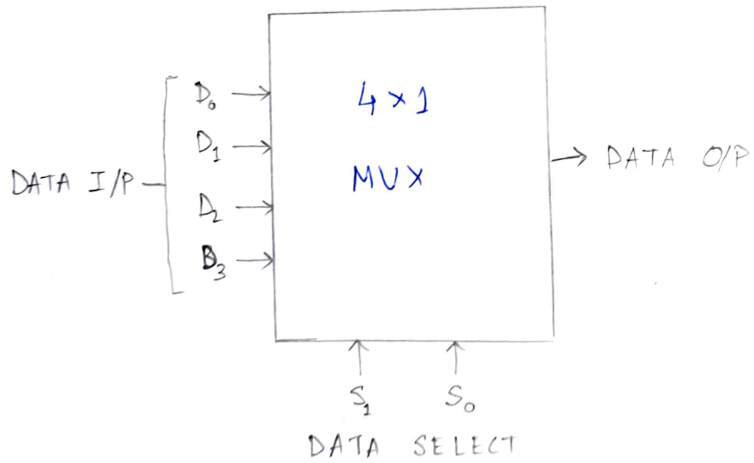


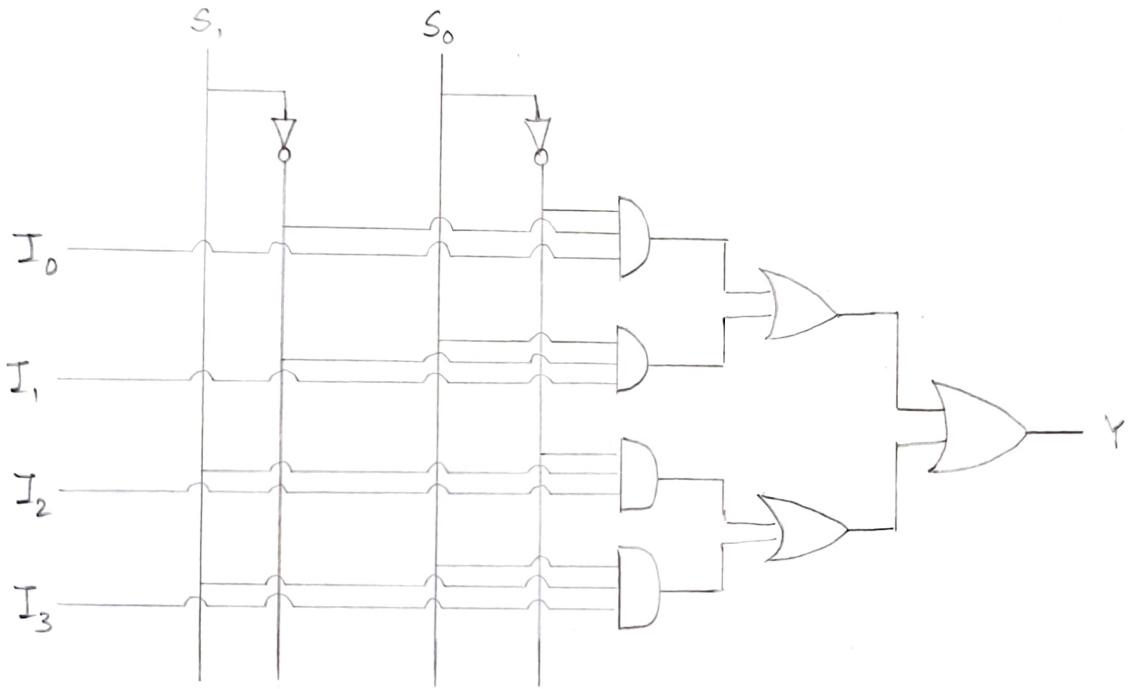
Fig 1

Truth Table:

S_1	S_0	I_3	I_2	I_1	I_0	Y
0	0				I_0	I_0
0	1			I_1		I_1
1	0		I_2			I_2
1	1	I_3				I_3

$$Y = S_1' S_0' I_0 + S_1' S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3$$

Circuit Diagram:



Conclusion:

4×1 MUX was formed and truth table is verified.

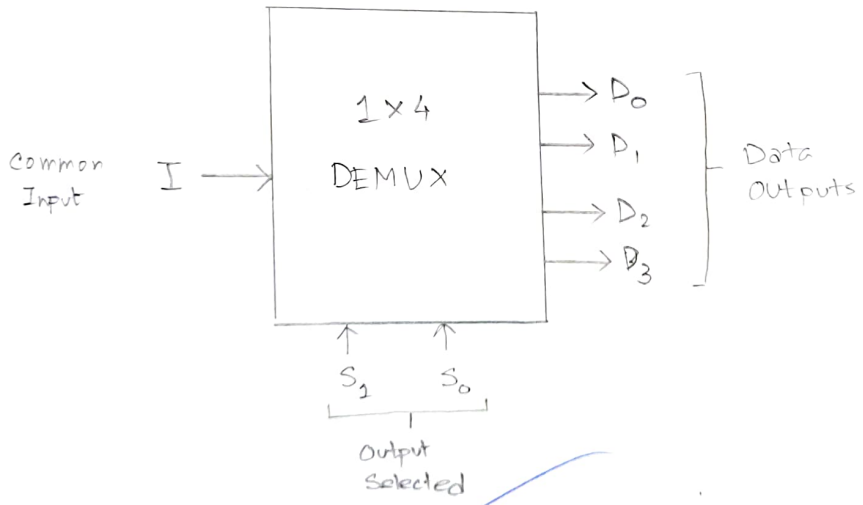
Experiment No. 8(b)

Aim: Implementation of 1×4 Demultiplexer circuit using logic gates.

Apparatus Required: Digital trainer kit, 3 input AND Gates, wires

Theory: The demultiplexer is a combinational logic circuit designed to switch one common input line to one of several seperate output line. The demultiplexer takes one single input data line and then switches it to any one of a number of individual output lines one at a time. The demultiplexer converts a serial data signal at the input to a paralled data at its output lines.

Block Diagram of 1:4 DEMULTIPLEXER:



Truth Table:

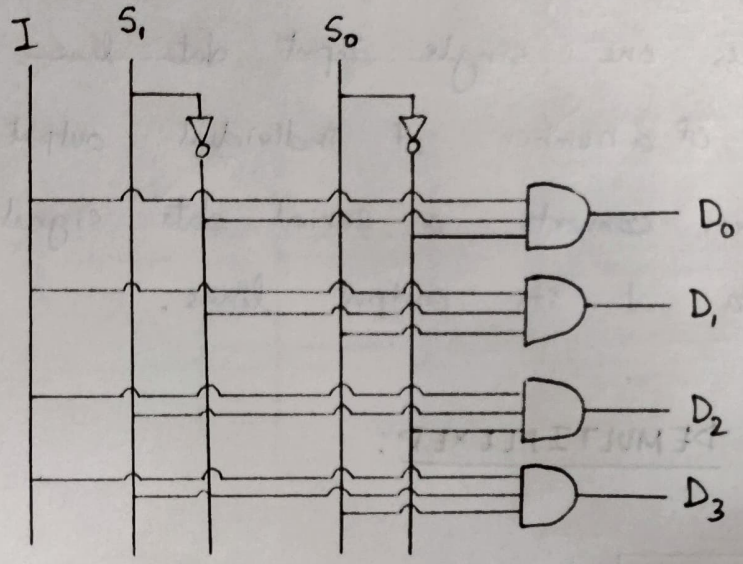
Input	Select Lines		Output Lines			
I	S_1	S_0	D_0	D_1	D_2	D_3
I	0	0	I	0	0	0
I	0	1	0	I	0	0
I	1	0	0	0	I	0
I	1	1	0	0	0	I

The output expression for each output bit is –

$D_0 = S_1' S_0' I$ $\quad$ $D_1 = S_1' S_0 I$

$D_2 = S_1 S_0' I$ $\quad$ $D_3 = S_1 S_0 I$

Circuit Diagram:



Conclusion:

1×4 DEMUX was formed and it's truth table is verified.