Experiment NO. - 6(a)

Aim - Realisation of even parity generator and even parity checker service.

Component Required - Digital Trainer kit, XOR Gate, Copper wires

Theory - Let us assume that a 3-bit message is to be transmitted with on even parity bit. Let the three input A, B, C, are applied to the circuit and output bit is the parity bit P. The total number of 1's must be even to generate the even parity bit P. The figure 1 shows the truth table of even parity generator in which 1 is placed as parity bit in order to make all 1's as even when the number of 1s in the truth table is odd.

Even parity checker is present in the signal recieving device. It checks corruption in parity.

Truth Table: (Even Parity Generator)

3 bit message			Even bit parity (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Figure 1

From the above truth table, the simplified expression of the parity bit can be written as-

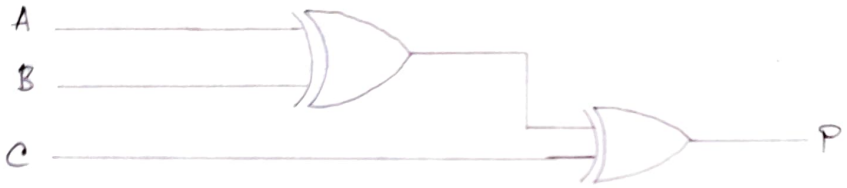
$$P = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$

$$= \bar{A}(B \oplus C) + A\overline{(B \oplus C)}$$

$$= A \oplus B \oplus C$$

Circuit Diagram (Even parity Generator):



Truth Table (Even parity checker):

4 bit recieved message				Parity error check (C_p)
A	B	C	D	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Figure 2

The output expression for even parity checker is -

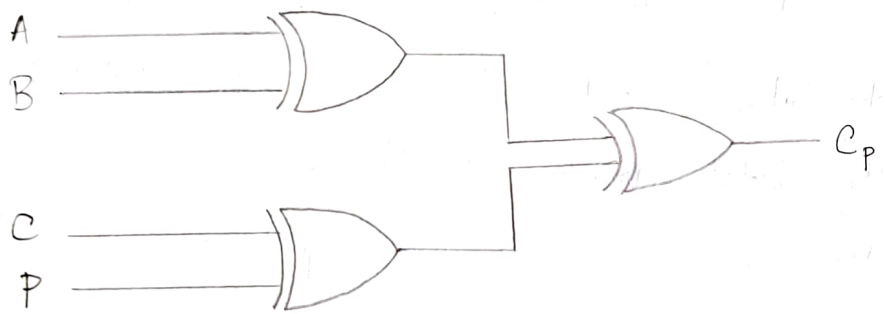
$$PEC = \bar{A}\bar{B}(\bar{C}P + C\bar{P}) + \bar{A}B(\bar{C}\bar{P} + CP) + AB(\bar{C}P + C\bar{P}) + A\bar{B}(\bar{C}\bar{P} + CP)$$

$$PEC = \bar{A}\bar{B}(C \oplus P) + \bar{A}B(\overline{C \oplus P}) + AB(C \oplus P) + A\bar{B}(\overline{C \oplus P})$$

$$PEC = (\bar{A}\bar{B} + AB)(C \oplus P) + (\bar{A}B + A\bar{B})(\overline{C \oplus P})$$

$$PEC = (A \oplus B) \oplus (C \oplus P)$$

Circuit diagram (even parity checker)-



Conclusion

Even parity generator and checker circuit was formed and their truth table is verified.

Experiment No. - 6 (b)

Aim - Realisation of an odd parity generator and odd parity checker service.

Componant Required: Digital Trainer kit, NOT Gate, XOR gate and wires.

Theory: Let us consider that the 3 bit data in to be transmitted with an odd parity bit. The three input are A, B and C and P is the output parity bit. The total number of bits must be odd in order to generate the odd parity bit. In the given truth table 1 is placed in the parity bit, in order to make the total number of bit odd when the total number of 1's in the truth table is even. Odd parity checker is present in the signal recieving device. It checks corruption in parity.

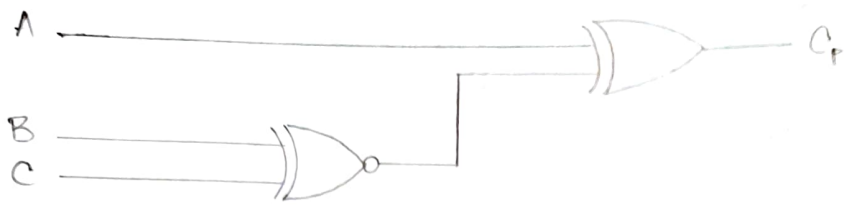
Truth Table (odd parity generator):

3 bit message			Odd Parity bit Generator (P)
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

The output parity bit expression for this generator circuit is -

$$P = A \oplus (\overline{B \oplus C})$$

Circuit Diagram (Odd parity Generator):



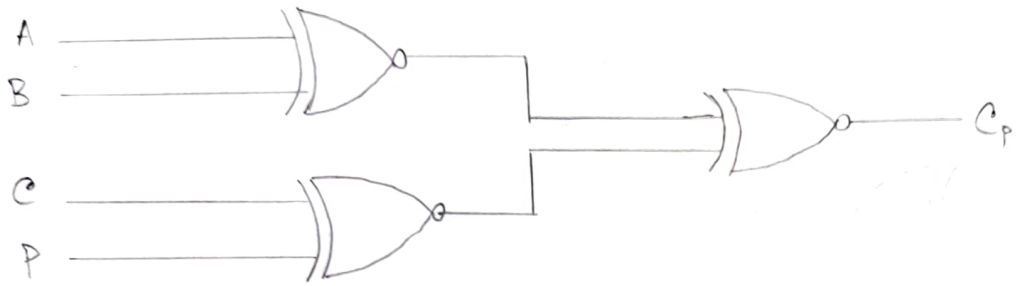
Truth Table (odd parity checker):

4 bit recieved message				Parity error
A	B	C	P	Check C_p
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

The output expression for odd parity checker is -

$$PE\,C = (A \odot B) \odot (C \odot P)$$

Circuit Diagram (odd parity check)



Result:

Odd parity generator and checker circuit was formed and then truth table is verified