

## University of Engineering & Management, Kolkata End Semester Examination, November - December, 2022 Programme Name: B.Tech in CSE/CSE(AIML)/CSE(IOT)/CSBS

Semester: 3rd

Course Name: Digital Electronics

Course Code: ESCE302

Time: 3 Hours Full Marks: 100

Answer 10 questions. Each question carries 2 marks. (2 × 10)		
1.A.		2,CO2,Understand
1.B.	Or	2,CO2,Understand
2.A.		2,CO2,Understand
2.B.	Convert 23D916 to binary, decimal and octal.	2,CO2,Understand
3.A.	Explain the difference between asynchronous and synchronous counters.	2,CO2,Understand
3.B.	Convert Decimal (432) <sub>10</sub> to BCD code.	2,CO2,Understand
4.A.	If J=K=1 and CLEAR=0, what will be the output of the JK flip flop?	
4.B.	Write 4 properties of TTL.	2,CO1,Remember
5.A.	What is toggle?	2,CO1,Remember
5.B.	What is meant by edge triggering?	2,CO1,Remember
5.A.	If J=K=0 and PRESET=0, what will be the output of the JK flip flop?	2,CO1,Remember
6.B.	Or State 2 advantages and 2 disadvantages of MOS.	2,CO1,Remember

7.A.	Why is Gray code called a unit distance code? Explain with the help of an example	2,CO1,Remember		
7.B.	the help of an example.  Or  Define excess 3 code? Why it is known as self- complementing code?	2,CO1,Remember		
8.A.	What is the difference between a latch and a flip-flop?	2,CO1,Remember		
8.B.	What is the primary disadvantage of asynchronous counter?	2,CO1,Remember		
9.A.	Draw the state diagram of a 4 bit Ring counter.	2,CO3,Apply		
9.B.	Solve for the 2's complement of 1001001.	2,CO3,Apply		
10.A.	Construct the basic block diagram of a 2 bit magnitude comparator.	2,CO3,Apply		
10.B.	Implement XOR gate using NAND gate.	2,CO3,Apply		
Group - B  Answer 8 questions. Each question carries 5 marks. (5 × 8)				
	Asses the logic circuit diagram for a 2:4 decoder with enable	5,CO5,Evaluate		
	Asses the logic circuit diagram for a 2:4 decoder with enable input. Explain its working.  Or	5,CO5,Evaluate		
	input. Explain its working.	5,CO5,Evaluate 5,CO5,Evaluate		
	Or  Reframe a combinational circuit for excess -3 code to BCD conversion using minimum number of logic gates.			
11.B.	Or  Reframe a combinational circuit for excess -3 code to BCD conversion using minimum number of logic gates.  Calculate canonical SOP for the following: f = ABC + BD' + AC'.  Or	5,CO5,Evaluate		
11.B. 12.A. 12.B.	Or  Reframe a combinational circuit for excess -3 code to BCD conversion using minimum number of logic gates.  Calculate canonical SOP for the following: f = ABC + BD' + AC'.  Or  Assess binary multiplication: 1101.1 * 1101	5,CO5,Evaluate 5,CO5,Evaluate		
11.B. 12.A. 12.B.	Or  Reframe a combinational circuit for excess -3 code to BCD conversion using minimum number of logic gates.  Calculate canonical SOP for the following: f = ABC + BD' + AC'.  Or  Assess binary multiplication: 1101.1 * 1101  Evaluate the circuit of ECL 2 input NOR gate.  Or  Judge the function using single 2.1 May and any other logic	5,CO5,Evaluate 5,CO5,Evaluate 5,CO5,Evaluate		
11.B. 12.A. 12.B. 13.A. 13.B.	Or  Reframe a combinational circuit for excess -3 code to BCD conversion using minimum number of logic gates.  Calculate canonical SOP for the following: f = ABC + BD' + AC'.  Or  Assess binary multiplication: 1101.1 * 1101  Evaluate the circuit of ECL 2 input NOR gate.	5,CO5,Evaluate  5,CO5,Evaluate  5,CO5,Evaluate  5,CO5,Evaluate  5,CO5,Evaluate		

15 A	Explain the operation of a 4-bit ring counter with the help of	5,CO4,Analyze
13.A.	suitable tables and diagrams.	
	O1	5 CO 4 A I
15.B.	Construct a code converter circuit to show BCD to excess-3 code conversion. Explain its working with suitable examples.	5,CO4,Analyze
16.A	Construct a code converter circuit to show excess-3 to BCD code conversion. Explain its working with suitable examples.  Or	5,CO4,Analyze
16.B	Construct a 3:8 decoder circuit and explain its working.	5,CO4,Analyze
17.A	Write the universal gates. Implement NOT, AND, OR and XOR using any one of the universal gates.	5,CO6,Create
17.B	Evaluate the following in 9's complement form: (245) and (7865).	5,CO6,Create
18.A	Evaluate a combinational circuit to identify whether an input number to the circuit is prime or not. Draw the circuit, truth table, derive expression (if any) and explain.	5,CO5,Evaluate
18.1	Or Construct binary division: (11111111/1001)	5,CO5,Evaluate
		a, o o o, z, wrante
	Group - C	
	Answer 4 questions. Each question carries 10 marks. (10	0 × 4)
19.A.	Write short note on TTL - include characteristics, circuit diagram, advantages and disadvantages.  Or	10,CO6,Create
19.B.	Write short note on CMOS - include characteristics, circuit diagram, advantages and disadvantages.	10,CO6,Create
20.A.	a) Evaluate the following Boolean function using 4 variable map: $F(w,x,y,z) = \Sigma(2,3,10,11,12,13,14,15)$ b) Formulate the expression for Odd Parity Or	10,CO5,Evaluate
20.B.	<ul> <li>a) Evaluate and implement a comparator that can compare between two 3-bit binary numbers.</li> <li>b) Judge the logic diagram of a full adder using only NAND gate</li> </ul>	10,CO5,Evaluate
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21.A. a) Compare the following: Asynchronous counter vs synchronous counter.
b) Compare the following: Ring counter vs Johnson counter
21.B. Using Quine-McCluskey (tabular minimization method) minimize F(a, b, c, d) = ∑m(1, 2, 3, 4, 5) + ∑d(12, 13, 14, 15)
22.A. Construct a 2-bit asynchronous up-down counter. Explain its working as UP & DOWN separately.
22.B. Construct a synchronous counter circuit with the specific count sequence as 0-> 2 -> 4 -> 7->0. Avoid the data lock out condition.
10,CO3,Apply
10,CO3,Apply

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