



**University of Engineering & Management, Kolkata**  
**Odd Semester Term- II Examination, October-November, 2021**  
**Programme Name: B.Tech in Computer Science      Semester: 3rd**  
**Course Name: Digital Electronics**  
**Course Code: ESC302**

**Full Marks: 100**

**Time: 3 Hours**

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**TERM - II QUESTION PAPER**

**GROUP – A (20 marks)**

**Answer the following questions. Each question is of 2 marks**

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|-----------|--|---|
| <b>1.</b> | <b>i)</b> If $J=K=0$ and $\text{PRESET}=0$ , what will be the output of the JK flip flop? Why?                 | 2 |
|           | <b>ii)</b> Draw the state diagram of a JK flip flop  | 2 |
|           | <b>iii)</b> State the difference between positive and negative edge triggering of clock in sequential circuit. | 2 |
|           | <b>iv)</b> Define duty cycle. What is the duty cycle for clock signal.   | 2 |
|           | <b>v)</b> Show how JK flip flop can be operated as a toggle flip flop.   | 2 |
|           | <b>vi)</b> What do you mean by modulus of a counter? Give example.   | 2 |
|           | <b>vii)</b> Draw the block diagram of a 4 bit SISO.  | 2 |
|           | <b>viii)</b> Prove that, $(A+B)(A'C'+C)(B'+AC)' = A'B$   | 2 |
|           | <b>ix)</b> Construct the block diagram of a 4:2 priority encoder.  | 2 |
|           | <b>x)</b> Write the logic family integration levels along with the number of gates per chip.                   | 2 |

**GROUP – B (30 marks)**

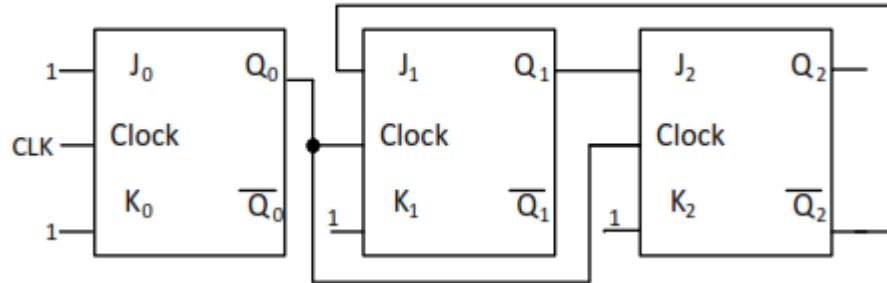
**Answer the following questions. Each question is of 5 marks**

- |           |  |   |
|-----------|--|---|
| <b>2.</b> | <b>i)</b> What do you mean by the race around condition?   | 2 |
|           | <b>ii)</b> How a race around condition in JK Flip flop can be resolved?  | 3 |
| <b>3.</b> | <b>i)</b> Implement and design a D flip flop from a JK flip flop given.  | 5 |
| <b>4.</b> | <b>i)</b> Explain, with the help of a neat diagram, the functionality of a MOD-8 asynchronous UP counter.                          | 5 |
| <b>5.</b> | <b>A. i)</b> What is the significance of parity checker circuit? Construct a 4-bit parity checker circuit and explain its working. | 5 |

OR

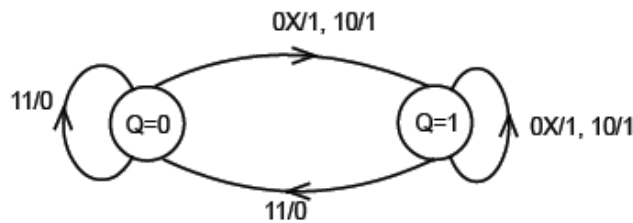
- B. i) Construct & explain the circuit of a 4:2 priority encoder. Explain how the problems of plain encoder are removed in a priority encoder. 5

6. A. i) Analyze the following sequential circuit with timing diagram



OR

- B. i) A state diagram of a logic gate that exhibits a delay in the output is shown in the figure, where X is the don't care condition, and Q is the output representing the state. Analyze which logic circuit is this?



7. A. i) Design a MOD-3 synchronous UP counter with all necessary steps involved. 5

OR

- B. i) Explain the operation of a 4-bit ring counter with the help of suitable tables and diagrams. 5

### GROUP - C (50 Marks)

Answer the following questions. Each question is of 10 marks

8. i) Obtain the minimal SOP for the Boolean expression,  $F(A,B,C,D) = \sum m(4,6,9,10,11,13) + \sum d(2,12,15)$  using Quine-McCluskey Method. 10
9. i) Design a synchronous counter with count sequence 4->6->7->3->1->4. Avoid data lockout conditions. [Use any Flip-flop of your choice] 10
10. A. i) Draw and explain the 3 to 8 line decoder using basic gates only. 5
- ii) Construct and implement a comparator that can compare between two 3-bit binary numbers. 5

**OR**

- B. i)** Construct a 3-to-8 decoder using two 2-to-4 decoders with enable inputs 5
- ii)** Implement a full subtractor using 4:1 MUX. 5

- 11. A. i)** Explain how a counter circuit can be treated as a frequency divider circuit. 3
- ii)** Design an asynchronous 4-bit up-down counter and it will count up when a signal line  $M = 0$  and count down when the signal line  $M = 1$ . Use only JK flip flop for the design. 7

**OR**

- B. i)** Can you design a MOD-6 counter using a MOD-8 counter? If yes, how the design is to be implemented, explain that with all necessary steps involved? 10

- 12. A. i)** Write short note on TTL - include characteristics, circuit diagram, advantages and disadvantages 10

**OR**

- B. i)** Write short note on CMOS - include characteristics, one circuit diagram using CMOS, advantages and disadvantages 10

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