University of Engineering & Management, Kolkata

Term - I Examination, August - September, 2021

Programme Name: B.Tech in Computer Science **Semester: 3rd**

Course Name: Digital Electronics

Course Code: ESC302

Full Marks: 100 **Time: 3 hours**

GROUP A (20 Marks)

Answer the following questions. Each question is of 2 marks.

1. i) Design a SR NAND Latch.

ii) Describe BCD? Find the BCD code of $(33)_{10}$.

iii) State the principle of Duality. Give an appropriate example.

iv) State the basic difference between Combinational and Sequential Circuits.

v) Convert 427_{10} to Excess-3 code.

vi) Why Gray code is called a unit distance code? Explain with the help of an example.

vii) Demonstrate the implementation of F= (XY'+ X'Y)(A+B') with only NOR gates.

viii) If $73_x = 54_{y,}$ solve for the possible values of x and y.

ix) $F(P, Q, R, S) = \Sigma m(0, 2, 5, 7, 9, 11) + \Sigma d(3, 8, 10, 12, 14)$
Consider the minterm list form of a Boolean function F given above. Here, m denotes a minterm and d denotes a don't care term. Identify the essential prime implicants of the function F.

x) 'Zone Bits' are used in which coding scheme ? State the zone bits for the digits and different sets of characters.

GROUP B (30 Marks)

Answer the following questions. Each question is of 5 marks.

2. Design the AND, OR, and XOR operations using NAND gates only.

3. Design the logic diagram of a full-subtractor using only NAND gates. Indicate the intermediate expressions too.

4. Design and explain the Full Adder circuit using two Half Adder circuits with an OR gate. Why we need the OR gate in the circuit?

5. A. Simplify the following Boolean function using a K-Map:
F = Σm(0,2,4,7,8,10,12,16,18,20,23,24,25,26,27,28)

OR

5. B. Prove the following using Boolean Algebra theorems:
A'BC + AB'C + ABC' + ABC = AB + BC + CA

6. A. Simplify the following Boolean function using a 4-variable K-Map:
F(w,x,y,z)= Σm(0,2,3,5,7,9,13)+ Σd(1,6,12)

OR

6. B. Infer the canonical form (POS/ SOP) of the following logic expressions:
   a. Y = AB+C'
   b. F = (A+B') . (C' + D') . (B' + C')

7. A. Design a 4:1 MUX - draw its the block diagram, write the truth table, and implement using only the Basic Gates. [1+2+2]

OR

7. B. Build a 16:1 MUX using 4:1 MUX.

GROUP C (50 Marks)

Answer the following questions. Each question is of 10 marks.

8. i) Design a combinational circuit that accepts a 4-bit Gray Code as input and converts it to its equivalent Binary number.
ii) Design a combinational circuit that converts a Binary Coded Decimal value to its equivalent Excess-3 code. **[5+5]**

9. i) Design a combinational circuit that acceptsa 4-bit input in Excess-3 format, and converts it to its equivalent Binary Coded Decimal format.
ii) Design a combinational circuit that accepts a 4-bit Binary number as input, and converts it to its equivalent Unit Distance Code. **[5+5]**

10. A. i) Simplify the expression Y = ∏ (0,1,4,5,6,8,9,12,13,14) Using K-Map method.
ii) Plot the logical expression ABCD + AB'C'D' + AB'C + AB on a K-Map; obtain the simplified expression from the map. **[5+5]**

OR

10. B. i). Illustrate the following conversions:
a. 'UEM' in ASCII to Binary
b. 111001001100010111010100 in EBCDIC to character

ii) a. 1101 in Binary to Gray Code
b. 1001 in Gray Code to Binary **[3+2+3+2]**

11. A. For the logic expression: Y = A'B'C+A'BC'+AB'C'+ABC
i) a. Infer the truth table
b. State the operation performed
ii) a. Illustrate this operation using basic gates
b. Illustrate this operation using only NAND gates **[3+1+3+3]**

OR

11. B. i) Find the prime implicants using Quine McCluskey method for:
$F(A,B,C,D) = \Sigma m(2,3,7,9,11,13) + \Sigma d(1,10,15)$. Construct the circuit for this expression using Basic gates only. **[7]**
ii) Use K-map to simplify and obtain the minimal expression of
$F(A,B,C,D,E)=\Sigma m(0,2,3,6,7,8,10,15) + \sum d(5,11,14)$. Construct the circuit for the minimized expression using NAND gates only. **[3]**

12. A. Infer the minimal SOP for the Boolean expression,
$F(A,B,C,D) = \sum m(4,6,9,10,11,13) + \sum d(2,12,15)$ using Quine McCluskey Method.

OR

12. B. For the Truth Table given below:

INPUTS				OUTPUT
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
1	0	0	0	1
1	1	0	0	1
1	1	1	0	1
1	1	1	1	1
0	1	1	1	0
0	0	1	1	0
0	0	1	0	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	1	0

a. Infer the logic expression in SOP form
b. Using k-maps, find the minimized expression.
c. Construct the circuit for the expression using
i. Basic, and
ii. Universal Gates **[3+3+2+2]**

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