University of Engineering & Management, Kolkata

End Semester Examination, January, 2022

Programme Name: B.Tech in CSE/CST/CSIT/CSBS/CSE(A.I.M.L)/CSE(I.O.T) **Semester: 3rd**

Course Name: Digital Electronics

Course Code: ESC302

Full Marks: 100 **Time: 3 Hours**

GROUP – A (20 marks)

Answer the following questions. Each question is of 2 marks. **10 x 2 = 20**

1. i) Solve for the 2's complement of 1001001.
ii) Prove Absorption Law.
iii) Implement AND and OR gate using NAND gate.
iv) Construct the basic block diagram of a 4:1 Multiplexer (with all notations available).
v) What is a magnitude Comparator?
vi) Construct the block diagram of a 4:2 priority encoder.
vii) What is the difference between a latch and flip - flop?
viii) What is toggle?
ix) Write 4 properties of TTL.
x) Draw the state diagram of a 4 bit Johnson counter.

GROUP – B (30 marks)

Answer the following questions. Each question is of 5 marks. **6 x 5 = 30**

2. Transform the following expression: (A + B) (C + D), Using only NOR gate.

3. Derive the characteristic equation of D flip flop and draw its state diagram.

4. Construct a combinational circuit for excess -3 code to BCD conversion using minimum number of logic gates.

5. A. Solve using K-map: Y (A,B,C,D) = C' (A'B'D'+D) + AB'C + D'

OR

B. Obtain the minimal SOP for the Boolean expression:
f = ∑(1,2,3,7,8,9,10,11,14,15) using the Quine-McClusky method.

6. A. Demonstrate how you can cascade two 2:4 decoders to make one 3:8 decoders.

OR

B. Implement the function using single 8:1 Mux and any other logic gates, if required: F(A,B,C,D)=∑m(0,1,2,5,9,11,13,15).

7. A. Derive the characteristic equation of JK flip flop and draw its state diagram.

OR

B. Construct and explain the working of a 4 bit SISO register circuit.

GROUP - C (50 Marks)

Answer the following questions. Each question is of 10 marks. **5 x 10 = 50**

8. Infer the minimal SOP for the Boolean expression:
f (A,B,C,D) = ∑m (4,6,9,10,11,13) + ∑d (2,12,15) using Quine-McClusky Method.

9. **i)** Draw the logic diagram of a Half Subtractor using only NAND gates. **5 + 5**

ii) Draw and explain the 3 to 8 line decoder using basic gates only.

10. A. Infer the minimized expression of the following canonical SOP expression using Quine McCluskey method and mention the redundant group(s), if any: Σ(3,4,5,7,9,13,14,15). Implement the minimized expression using NAND only.

OR

B. i) Draw a NAND logic diagram that implements the complement of the following function: F(A,B,C,D)= Σ(0,1,2,3,4,8,9,12) **5 + 5**

ii) Simplify the following Boolean function using 4 variable map: F(w,x,y,z)= Σ(2,3,10,11,12,13,14,15)

11. A. i) Construct a 2-bit asynchronous up-down counter. Explain its working as UP & DOWN separately. **6 + 4**

ii) Compare the input conditions for a SR flip flop vs JK flip flop. Is there any advantage of JK over the SR flip-flop?

OR

B. i) What do you mean by a modulus of a counter? **2 + 8**

ii) Construct a MOD-10 counter using a MOD-16 counter. Explain the behaviour of the circuit with proper diagram, logic expressions & Circuit excitation table.

12. A. Write short note on TTL - include characteristics, circuit diagram, advantages and disadvantages.

OR

B. Write short note on ECL – include characteristics, circuit diagram, advantages and disadvantages.

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