University of Engineering & Management, Kolkata

2nd Term Examination, November, 2022

Programme Name: B.Tech (CSE / CSE (AIML) / CSE (IOT, CYS, BCT))

Semester: 3rd

Course Name: Digital Electronics

Course Code: ESC302

Full Marks: 30 Date:3rd November, 2022 Time: 9.30am to 10.30am

---

GROUP – A (10 marks)

Answer any five of the following questions. Each question is of 2 marks 5 x 2 = 10

1. i) Obtain the logical expression for sum and carry for a half adder.

   ii) Explain why demultiplexer is also called as a data distributor.

   iii) What is meant by edge triggering?

   iv) What is Race Around Condition?

   v) If J=K=0 and PRESET=0, what will be the output of the JK flip flop?

   vi) Develop the complement of x + yz.

GROUP – B (10 marks)

Answer any two the following questions. Each question is of 5 marks 2 x 5 = 10

2. Simplify the following function using K map technique (W, X, Y, Z) = m (1,3,7,11,15) + d(0,2,5)

3. Illustrate a simplified logic circuit that has three inputs, A, B, and C, and whose output will be HIGH only when a majority of the inputs are HIGH.

4. Explain the functioning of a 3-bit asynchronous UP counter, with appropriate timing diagrams.

5. Construct and explain the working of a 4-bit SISO register circuit.

GROUP - C (10 Marks)

Answer any one of the following questions. Each question is of 10 marks **1 x 10 = 10**

6. Explain, with the help of timing diagram and truth table, the functioning of a MOD-8 asynchronous UP counter.
7. Construct a synchronous counter circuit with the specific count sequence as 0-> 2 -> 4 -> 7->0. Avoid the data lock out condition.
8. a) Design a full subtractor using 4:1 MUX.
   b) design and explain a 3 to 8 line decoder using NOT and NAND gates only.

****