University of Rajshahi
Department of Computer Science and Engineering
B. Sc. (Engg) Part-II Odd Semester Examination 2021
Course: CSE-2111 (Digital System Design)
Full Marks: 52.5 Duration: 3(Three) Hours
Answer 06(Six) questions taking any 03(Three) questions from each part

Part-A

1. a) Explain weighted, non-weighted, and unit-distance codes for representing decimal numbers with examples. 4.50
   b) Given two 8-bit 2's complement binary number A = $(00101101)_2$ and B = $(11011010)_2$. Compute C=A-B and verify the result by converting A, B, and C into decimal. 3
   c) How parity bit can be used for single-biterror detection? Explain with an example. 1.25

2. a) Draw a circuit diagram to implement an Exclusive-OR gate using four NAND gates. 1.25
   b) Design a circuit diagram for converting BCD code into 2-out-of-5 code. 3.50
   c) Prove i) $y + x\bar{y}\bar{z} + xz = x + y$and ii) $\overline{(x+y)}z + x\bar{y} = \bar{y}(x+z)$ using Boolean algebra properties. 4

3. a) i) Write down the truth table for a half adder. 3
      ii) Derive the logic circuit from the truth table of a half adder.
      iii) Draw a full adder circuit by using two half adders.
   b) What is the basic difference between a parallel adder and a serial adder? Draw the timing diagram of a 4-bit parallel adder. 3
   c) Implement a logic circuit for a 1-bit comparator and draw its truth tableState the truth table and circuit diagram of a 1-bit binary comparator. 2.75

4. a) Design the circuit diagram of a BCD to 7-segment decoder. 5
   b) Implement the following Boolean expressions using a 74LS138 3-to-8-line decoder. 2.75
      $Y_1 = \bar{A}\bar{B} + AC + \bar{A}\bar{C}$; $Y_2 = \bar{A}C + A\bar{C}$; $Y_3 = \bar{B}C + B\bar{C}$;
   c) Write some typical applications of multiplexer and demultiplexer. 1

Part-B

5. a) Differentiate between i) combinational and sequential logic circuits, ii) synchronous and asynchronous logic circuits. 3
   b) Define setup time and hold time with necessary diagram. 2
   c) ExplainDflip-flop with asynchronous Preset and Clear input signals with block diagram, truth table, and timing diagram. 3.75

6. a) Mention the different modes of operations of the shift register. Draw the block diagram of 4-bit serial input serial output shift register, discuss its operation, and draw the truth table and waveforms. Draw the circuit diagram of a 4-bit serial in/parallel out and parallel in/serial out shift registers. 4.75
   b) Classify counters in shift registers. Explain the operation of Johnson Counter in brief. 4

7. a) Draw the HDL design flow. 2.25
   b) State the Verilog HDL supported levels of abstraction for designing digital circuits. 2.50
   c) Write HDL code to implement a 4-to-2 line priority encoder. 4

8. a) Explain the port connection rules of Verilog HDL. 2
   b) Define rise, fall, and turn-off delays with necessary diagram. 2.25
   c) Draw the timing diagram of the following simulate module. 4.50

```
module comb_circuit(x, v);
input  [3:0]v;
output x;
nor  #5  (n,v[3],v[2]);
and  #10 (a,v[1],v[0]);
xor  #5  (x,n,a);
endmodule
```

```
module simulate;
reg [3:0]V; wire X;
comb_circuitct(X, V);
initial
begin
   V = 4'b0000;
#25 V = 4'b0110;
#25 V = 4'b0011;
#25 V = 4'b1011;
end
endmodule
```

University of Rajshahi

Department of Computer Science and Engineering

B. Sc. (Engg) Part-II Odd Semester Examination 2020

Course: CSE-2111 (Digital System Design)

Full Marks: 52.5 Duration: 3 (Three) Hours

Answer 06 (Six) questions taking any 03 (Three) questions from each part

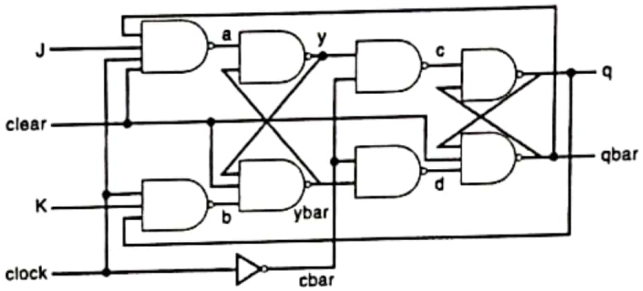
Part-A

1. a) Why do we use binary number system instead of decimal number system in the digital devices? 1
   b) Represent $(93)_{10}$ and $(-93)_{10}$ as 8-bit i) Sign-Magnitude, ii) 1's complement, and iii) 2's Complement binary number. 2.75
   c) State the purpose of Hamming code for digital communication devices. Compute the data word with hamming code for the original binary data word $(10110010110)_2$. 5

2. a) Why NAND gate and NOR gate are called universal gate? Explain with necessary diagram. 3
   b) Prove i) $xy + \bar{x}z + yz = xy + \bar{x}z$ and ii) $\bar{x}\bar{y}\bar{z} + \bar{x}y\bar{z} + xy\bar{z} = \bar{x}\bar{z} + y\bar{z}$ using Boolean algebra properties. 3
   c) Simplify the Boolean function $F(A,B,C,D) = \sum(1,3,7,8,11,15)$ which has the don't care conditions: $d(A,B,C,D) = (0,2,5,9)$. 2.75

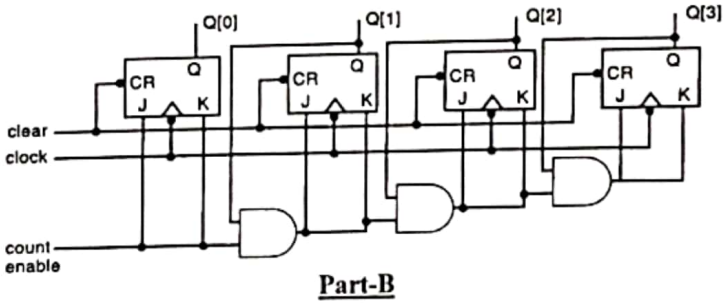
3. a) Write HDL codes for 2x2-bit combinational array multiplier. 3.75
   b) How to invoke a Verilog module from a VHDL module? Explain with an example of a mixed language description or a full adder using 2 half adders. 5

4.



The circuit diagram for the JK flip-flop is given above.

a) Implement the above circuit diagram of JK flip-flop as a Verilog HDL module. 4.75
b) Use the above JK flip-flop module to implement the following 4-bit synchronous counter. 4



Part-B

5. a) Implement a full adder circuit using a 3-to-8 decoder. 2.5
   b) How decoder can be used as de-multiplexer? 2
   c) How could we implement an 8-to-1 multiplexer using 2-to-1 multiplexer. 2
   d) Distinguish between combinational and sequential logic circuit. 2.25

6. a) Compare between D latch and D flip-flop with timing diagram. 2.25
   b) Show the implementation of T flip-flop from D flip-flop. 2
   c) Show the circuit and timing diagram of a 4-bit bidirectional shift register. 4.5

7. a) What are advantages of synchronous counter over asynchronous counter? 2
   b) Design a 4 bit synchronous counter for counting the following binary sequence: 6.75
   0000→0101→1010→0110→1001→0011→1100→1111→0000

8. a) How does the binary counter work as a frequency divider? 2
   b) What is the frequency of the output of 8th FF when the input clock frequency is 512 KHz? 1.75
   c) What is full adder? Design a full adder circuit. 5

University of Rajshahi
Depart of Computer Science and Engineering
B.Sc. Engg. Part-2 (Odd semester) Examination-2019

Course Title:: Digital System Design **Course ID: CSE 2111**

Total time: 3 hours **Total Marks: 52.5**

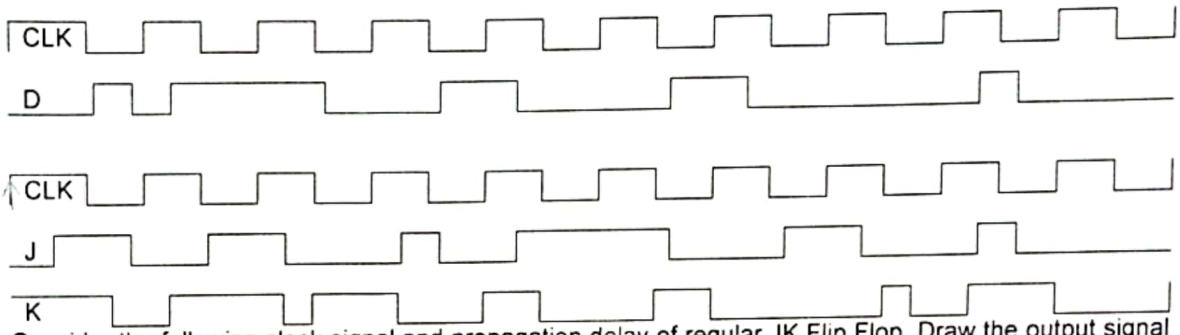
(Answer Any Six (06) questions taking Three from each section)

Section-A

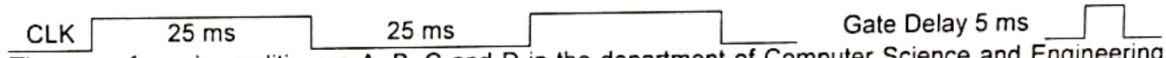
1(a) Is a 32-bit ALU as fast as a 1-bit ALU? Explain your answer. 1.75

(b) Explain, why carry look ahead adder is faster than a regular adder. 1

(c) Draw the output signal of (i) D Latch and (ii) Master-slave JK Flip Flop for the following clock signals and respective Inputs: 4



(d) Consider the following clock signal and propagation delay of regular JK Flip Flop. Draw the output signal of that JK Flip Flop with clock signal when both J and K are set to 1 (high). 2



2(a) There are four air conditioners A, B, C and D in the department of Computer Science and Engineering located in the office, seminar library, digital lab and chairman's room. However, unfortunately, due to power constraint only one air conditioner can be in use at a time. Therefore, it requires to set the priory of using those air conditioners, priority is as follows, digital lab> seminar library > office > chairman's room. Design a proper priority encoder and complete the following truth table where output (XY) gives the binary codes assigned to the inputs depends on priority from highest to lowest as follows (11)> (10) > (01) > (00). 5.75

A	B	C	D	X	Y
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		

A	B	C	D	X	Y
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

(b) An innovative student of the department of Computer Science developed a project where he recordsthe temperature of his class room in 16 different levels (0 ~15) and stores those values in a 4-bit Register. The chairman of the department becomes very interested to this project and has installed those devices in four different class rooms but unfortunately the chairman can watch only one data set from a room at a time. Design a multiplexer to help the chairman about what he wants. First draw the truth table for this problem and then draw the circuit diagram. 3

3(a) The chairman of the department becomes happy when he finds that his students can show numerical digits on a 7-segmnet display as an output of a 4-bit Binary counter. He wants to use it in his office to count his 9 staffs while entering into office. The chairman observes that the device displays digits perfectly when it counts from 0 and then increases. Suddenly, chairman founds that it displays something unknown character on 7-segment display when count is more than 9. What was the problem in that design of that Binary to 7-segment decoder? In order to fix the problem, design a decoder so that it can display character 'U' and 'E' for the respective additional count values given in the following table (Draw truth table for the whole 7-segmnet display but show design detail of any 4 segments of the 7-segmnet display): 7

Binary count				Letter to be displayed
1	0	1	0	U
1	0	1	1	E
1	1	0	0	E
1	1	0	1	E
1	1	1	0	E
1	1	1	1	E

(b) What is the frequency of the output of 8^{th} FF when the input clock frequency is 512 KHz? 1.75

4(a) The 8-bit data are stored in a Register A, we want to transfer it through serial lines, at the receiving end, the transmitted serial 8-bits will be again stored in another Register B. Draw a digital circuit using Register, Counter, Shift register, Multiplexer and Demultiplexer to implement the above problem and then explain its operation. 7

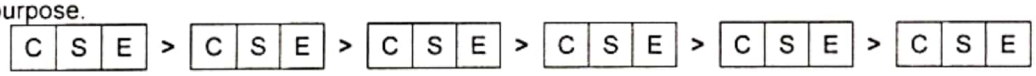
(b) Distinguish between asynchronous and synchronous counter. 1.75

Section-B

5(a) The electric power for the water pump of the department of Computer Science is controlled by four different switches S1, S2, S3 and S4 handled by the chairman, engineer, office staff and guard, respectively. For the proper use of the water pump, the chairman sets some rules. The electric power can be turned ON when either (i) chairman's switch is turned ONbut guard's switch is turned OFF, or (2) chairman's switch is turned OFF but both engineer's and staff's switch are turned ON. Draw the truth table for these problems, derive the switching function and use a 74LS151 to implement this switching function. 4.75

(b) Design a 4-input MUX (Multiplexer). How can you design an eight-input MUX by using two 4-input MUX? 4

6(a) On the occasion of CSE Grand Reunion 2019, students from the second year of this department designed different types of lighting patterns for the decoration purpose. One of the students designed a lighting pattern to display three letters of their department 'C', 'S' and 'E' but in a sequence given below (the shaded box means the light is turned ON). Now, today, you have to design some digital circuits for this purpose. 5.75



(b) The department of Computer Science has installed a Flash light to display the name of the department. However, unfortunately it flashes a bit faster that makes it difficult to differentiate between ON and OFF states. Therefore, the chairman wants to introduce some additional digital circuits to reduce the speed of supplied clock. Design necessary digital circuit to reduce clock's speed as given in following timing diagram (A is supplied clock signal, B is expected clock signal): 3

7(a) What are features of PALC22V10, PALCE22V10 and GAL22V10? 2

(b) What is "Programmable logic plane" and "Output logic" of a PAL device? What are output features of PAL16L8, PAL16R6, PAL16R4 and PAL22V10? 3

(c) Draw a circuit diagram of PAL device having two inputs, two product terms and one output. 2

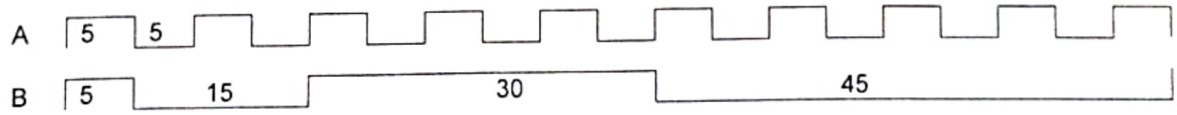
(d) What is Macrocell? Draw the circuit diagram of a typical Macrocell. 1.75

8(a) What are the "Design Block' and "Stimulus Block" used in Verilog HDL? 2

(b) Describe the "port connection rule" used in Verilog HDL. 2

(c) Write a program in Verilog HDL for a 4-to-1 Multiplexer. 2

(d) Write a program in Verilog HDL to produce the following two signals A and B. 2.75



University of Rajshahi
Department of Computer Science and Engineering
B.Sc. (Engg.) Part-2 (Odd Semester) Examination-2018
Course: CSE2111 (Digital System Design)
Marks: 52.50 Time: 3:00 Hours

[N.B. Answer any **Six** questions taking **Three** from each section.]

Section-A

1. a) Convert 01010010 (BCD) to Binary. You have a BCD number of two digit decimal values. Now design a BCD-to-binary converter with 4-bit parallel adder. Draw the logic circuit and explain its operation. 5

   b) Design a BCD to Excess-3 code converter and draw its logic diagram. 3.75

2. a) Why carry-look-ahead adder is faster than regular adder – explain with diagram. 3

   b) Distinguish between 1's complement and 2's complement system. Why this circuits are necessary? 2.75

   c) Design a logic circuit that has four inputs, A B, C and D and whose output will be high only when a majority of inputs are high. 3

3. a) Define decoder and demultiplexer. How decoder can be used as a demultiplexer? 2.25

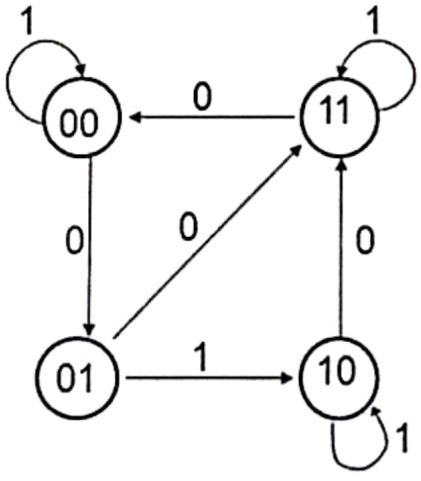
   b) Define Multiplexer. Implement the logic function $F(A,B,C,D) = \sum m(1,3,4,7,11,13,15)$ using 8x1 MUX. 4

   c) Implement the logic function $F(A,B,C) = \sum m(1,3,4,7)$ using a 3-to-8 line decoder with active low output. 2.5

4. a) What is parity bit? Implement a 4-bit even parity generator circuit and discuss the operation of the circuit with example. 2.75

   b) Define state table and state diagram with example. 2

   c) From the following state diagram, design the sequential circuit using JK flip-flops. 4



Section -B

5. a) Define asynchronous and synchronous counter. Write the advantages of synchronous counter over asynchronous counter. 2.25
   b) Construct a binary counter that will convert a 64-kHz pulse signal into a 8-kHz square wave. 2
   c) Draw the logic diagram of a Mod-8 synchronous up/down counter. Explain its operation with timing diagram. 4.5

6. a) Define Excitation table. Write the excitation table of SR, JK, D and T flip flop. 3
   b) Design a counter with JK flip flop that will count the sequence 0,1,5,4, 3, 2, 0. 5.75

7. a) Discuss FPGA architecture in brief. Distinguish between PLA and PAL in terms of design architecture. 3
   b) Implement the Boolean function using PAL 3

$$Y_1 = \sum m(1,2,4,7)$$

$$Y_2 = \sum m(3,6)$$

   c) Determine the size of the PROM required to implement a dual 8-to-1 multiplexer with common selection inputs 2.75

8. a) What is VHDL? Briefly describe the salient features of VHDL and Verilog. 2.75
   b) Explain an 8-to-1 line Multiplexer module in Verilog HDL. 3
   c) Write a VHDL code to implement XOR operation. 3

University of Rajshahi
Department of Computer Science and Engineering
B.Sc. Engg.(CSE) Part 2 Odd Semester Examination-2017
Course: CSE2111 (Digital System Design)
Full Marks: 52.5 Time: 3 Hours

[N.B. Answer SIX questions taking THREE from each Section.]

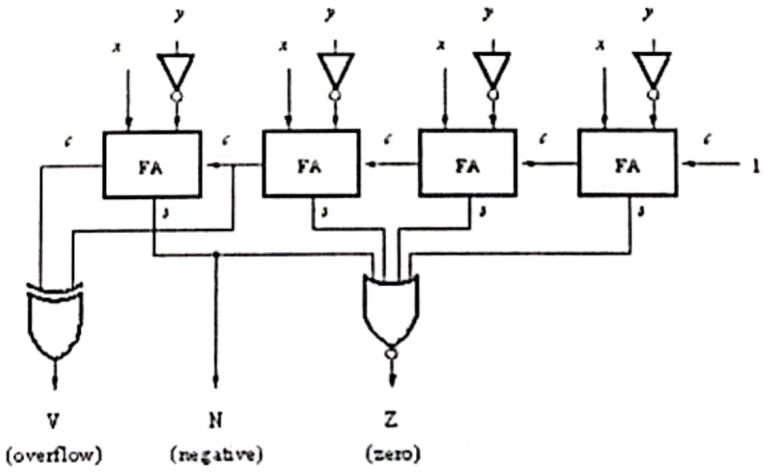
Part A

1. (a) Represent $(-200)_{10}$ and $(200)_{10}$ using sign-magnitude, 1's complement and 2's complement binary form. 2
   (b) Represent $(275)_{10}$ and $(641)_{10}$ in BCD and then perform BCD addition. Check your result by converting back to decimal. 2
   (c) Construct a BCD adder to add two 4-bit BCD code groups using 4-bit parallel adders and discuss its operation with suitable examples. 4.75

2. (a) Design a combinational logic circuit to compare two 4-bit binary numbers A and B and to generate the outputs A<B, A=B and A>B. 3
   (b) Design a combinational circuit to convert BCD code to 7-segment code. 3.75
   (c) Design a combinational logic using suitable multiplexer to realize the following boolean expression: $Y= AD'+B'C+BC'D'$. 2

3. (a) What is priority encoder? Design a 4-line to 2-line priority encoder with active HIGH inputs and outputs with priority assigned to the higher order data input lines. 4.75
   (b) Implement a full-adder circuit using a 3-to-8 decoder. 4

4. (a) What is code converter? Draw the combinational logic circuit for binary to gray code conversion. 1.75
   (b) Design and explain a 2-bit binary multiplier combinational logic circuit. 4
   (c) In computer computations it is often necessary to compare numbers. Two four-bit signed numbers, $X = x_3x_2x_1x_0$ and $Y = y_3y_2y_1y_0$, can be compared by using the subtractor circuit in Figure, which performs the operation $X - Y$. The three outputs denote the following: $Z = 1$ if the result is 0, otherwise $Z = 0$; $N = 1$ if the result is negative, otherwise $N = 0$; $V = 1$ if arithmetic overflow occurs, otherwise $V = 0$. Show how Z, N, and V can be used to determine the cases $X = Y$, $X<Y$, $X<=Y$, $X>Y$ and $X>=Y$. 3



Part B

5.(a)	What is shift register? Design a 4-bit right shift register with parallel load of data.	3
(b)	What is counter? Differentate between asynchronous and synchronous counter. List the applications of counter.	1.75
(c)	Draw the truth table and design a logic diagram of a MOD-10 ripple counter. Explain its operation with timing diagram.	4
6.(a)	Design a synchronous counter with JK flip-flop that will count the sequence as 0, 2, 4, 6, and repeat.	4
(b)	Design a MOD-8 synchronous up/down counter and explain its operation with timing diagram.	4
(c)	What is presettable counters?	0.75
7.(a)	Design a magnetic core RAM using 2x4 decoder (consider 2-bits input and 2-bits output). Discuss the read/write operation.	4
(b)	Distinguish between PLA and PAL in terms of design architecture.	1.75
(c)	Define the different hardware of FPGA. Draw the basic FPGA architecture. Give an example.	3
8.(a)	What is a hardware description language? What are the requirements of a good HDL?	3
(b)	Briefly describe the salient features of VHDL and Verilog.	4
(c)	What are the advantages of using JAVA HDL over Verilog?	1.75

University of Rajshahi

Department of Computer Science and Engineering

B. Sc. (Engg.) Part-2 Odd Semester Examination-2016

Course: CSE2111 (Digital System Design)

Full Marks: 52.5 Duration: 3(Three) Hours

Answer 06(Six) questions taking any 03(Three) questions from each part.

Part-A

1.(a) Design a 4-bit binary adder circuit with necessary figures. 2

(b) What do you mean by the terms 'carry generate' and 'carry propagate'? Define those terms with a full adder circuit and necessary equations. 2.75

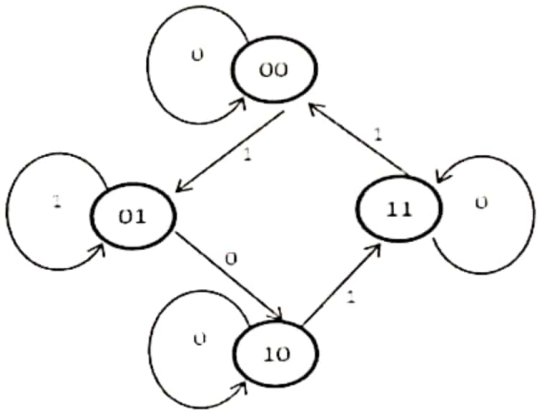
(c) Define lookahead carry-generator. Design a 4-bit carry-lookahead adder. 4

2.(a) Draw a 2-input AND gate and a 2-input OR gate using Transistor-Transistor logic 2.75

(b) There are **Four** switches to control a water pump. The water pump is turned on for the following conditions (i) if switch 1 is turned OFF but both switch 2 and 3 are turned ON, or, (ii) if switch-4 is turned ON but both switch 2 and 3 are turned OFF. Draw the truth table, derive the switching functions, minimize the switching functions by using K-map and draw the logic-gate diagram (circuit). 4

(c) What are the differences between '7400' and '74LS00'? 2

3.(a) Design a clocked sequential circuit that counts from 00 to 11 with JK flip-flops whose state diagram is given below: 4



(b) Define latch and flip-flop. Design a clocked master-slave JK flip-flop. 3

(c) Define state reduction problem. What is the benefit by considering **don't care** terms in designing a sequential circuit? 1.75

4.(a) Design the sequential circuit using register and ROM whose next state and outputs are defined by the following equations: 4

$A_1(t+1)=\Sigma(4,6)$

$A_2(t+1)=\Sigma(1,3,5,7)$

$y(A_1, A_2, x)=\Sigma(3,7)$

(b) Design a 2-input serial adder using a sequential logic procedure. 3

(c) Discuss the difference between serial and parallel modes of operation in a register. 1.75

Part-B

5.(a) Draw the logic diagram of a 4-bit Ripple counter and explain its operation. 3

(b) What do you mean by negative-edge triggered FF, positive edge triggered FF and level triggered FF. Explain with diagrams. 2

(c) Draw the logic diagram of a 4-bit **Johnson** counter and explain its operation. 3.75

6.(a) Design an integrated circuit memory using 2×4 decoder (consider 2-bit input and 2-bit output). 4

(b) A combinational circuits is defined by the following functions 4.75

$F_1(A,B,C)=\Sigma(3,4,6,7)$

$F_2(A,B,C)=\Sigma(0,2,5,8)$

Implement the circuit with a PLA having 3 inputs, 4 product terms and 2 outputs.

7.(a) Describe the abstraction levels of Verilog HDL. 3

(b) Write the input-output connection rules of Verilog HDL with example. 2.75

(c) What is the difference between the following two lines of Verilog code? 3

i. #5 a=5;

ii. a=#5 b;

8.(a) Write Verilog HDL programs including the design and stimulus blocks for 4.75 +4

(i) 4-1 multiplexer,

(ii) 4-bit full adder.

University of Rajshahi

Department of Computer Science & Engineering

B.Sc. (Engg.) Part-II Odd Semester Examination 2015

Course: CSE-2111 (Digital System Design)

Full Marks: 52.5 Duration: 3(Three) Hours

Answer 6(Six) questions taking any 3(Three) from each part

Part-A

1. a) Why combinational logic circuit is needed? Design a BCD to Excess-4 code converter and draw its logic diagram. 4

   b) Why carry-lookahead adder is faster then carry propagation adder. Draw the logic diagram of a 4-bit lookahead carry generator. Construct a 4-bit carry-lookahead adder with a lookahead carry generator. 4.75

2. a) What is the difference between a decoder and a de-multiplexer? Implement a full adder circuit with a decoder and two OR gate. 4

   b) Define multiplexer. Implement $F(A,B,C,D) = \Sigma(1,2,4,8,9,15)$ with a 8x1 MUX. 4.75

3. Consider a synchronous sequential binary logic circuit with one input A and one output Z. Suppose A denotes single bit binary number and the input sequence is divided per every three clock cycle. Here, each division is called an *interval*. We would like to design a sequential circuit which outputs 1 at the last clock period of the interval if and only if the interval contains one or more '1's. Table-1 illustrates an example of the action.

Clock	C	1	2	3	4	5	6
Input	A	0	0	0	1	0	1
Output	Z	0	0	0	0	0	1

Table- 1

   a) Draw the state transition diagram for the circuit. 2

   b) Draw the state transition table for the circuit. 2

   c) Draw the Karnaugh map for the circuit. 2

   d) Design the synchronous sequential circuit and draw it. You can only use the symbols for AND, OR, NOT, D flip-flop and JK flip-flop. 2.75

4. a) Distinguish between flip-flop and latch. Explain clocked SR flip-flop with logic diagram, function table and characteristics equation. 4

   b) Complete the diagram of the sequential circuit whose sequence is given below: 4.75

State	a	a	b	c	d	e	f	f	g	f	g
Input	0	1	0	1	0	1	1	0	1	0	0
Output	0	0	0	0	0	1	1	0	1	0	0

Draw the logic diagram using SR flipflops.

Part-B

5. a) What is shift register? Design a 4-bit bidirectional shift register with parallel load. 4.25
   b) Whet is ripple counter? Draw the logic diagram of a BCD ripple counter with timing diagram. 4.5

6. A circuit C1 shown in Fig-1 accepts n-bit unsigned binary numbers A and B as input and produce G and S as output, where G is the greater and S is the smaller between A and B respectively. When A=B, we have G=S=A=B. Fig-2 shows a circuit C2 processes numbers of one binary digit. Suppose that cascading n units of circuit C2 implement a circuit C1. The inputs *c* and *d* of circuit C2 represent that A<B and A>B respectively for more significant digits than processed by the circuit. The outputs *e* and *f* represent that A<B and A>B hold respectively including the digits being processed. G_i and S_i respectively represent i^{th} bit of greater and smaller number.

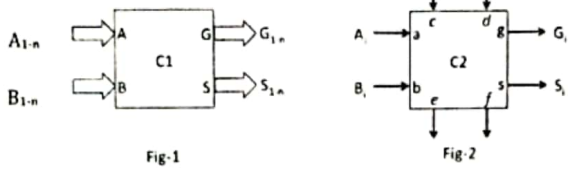


Fig-1

Fig-2

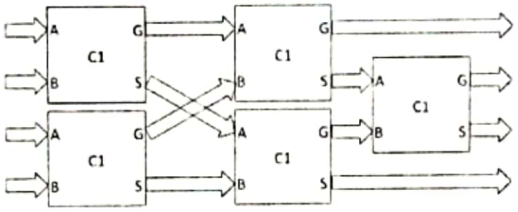


Fig-3

   a) Construct a truth table for circuit C2. Note that '1' represents *true* and '0' represents *false*. 2.5
   b) Draw a circuit diagram of C2 by using only AND, OR and NOT gate. 2.5
   c) Draw a block diagram of circuit C1 for comparing two 4-bit binary numbers by using four C2 circuit blocks. 1
   d) As shown in Fig-3, four input numbers are sorted by connecting several units of circuit C1. Following Fig-3, show an example circuit for sorting three inputs. 2.75

7. a) Distinguish between SRAM and DRAM. Briefly explain the internal organization of a 64x4 RAM. 4.25
   b) What are the major differences between CPLDs and FPGAs? Discuss FPGA architecture in brief. 4.5

8. a) State port connection rules in Verilog HDL. 2.75
   b) Explain min, max and typ delays in the gate-level design with respect to Verilog HDL. 3
   c) Describe a 8-to-1 line Multiplexer module in Verilog HDL. 3

5

Department of Computer Science & Engineering
B.Sc. Engineering Part-2, odd Semester Examination 2014

Course: CSE2111 (Digital System Design)
Time: 3 hours **Marks: 52.5**

(Answer SIX questions taking THREE from each part)

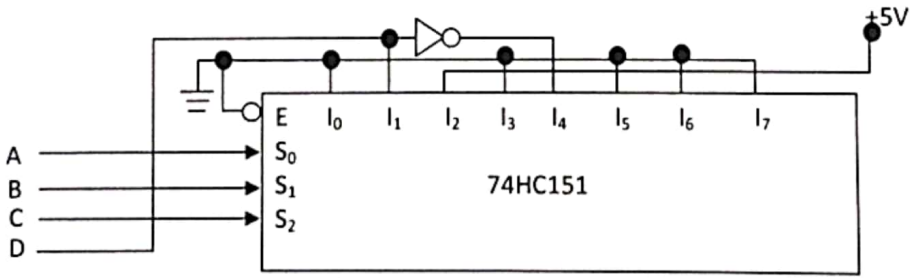
PART-A

1. a) Define code converter? Design 3 bit Gray Code to binary converter and explain the operation. 4.25
   b) Design an 8-bit magnitude comparator using 74HC85 4-bit magnitude comparator and hence describe the operation of the following eight-bit comparison A7….A0=10101111 and B7…..B0=10101001. 4.5

2. a) Design a 4-bit binary parallel adder/subtractor circuit and explain the operation with an example. 5.5
   b) There are two types of adder, one is ripple carry and other is carry look-ahead. What will be the good design of 32-bit adder? Explain your answer. 3.25

3. a) Design a binary multiplier of two numbers A and B (two bit each), C=AxB. Explain its operation. 4.5
   b) Explain an application of magnitude comparator with a digital circuit. 4.25

4. a) Design a 1–line–to-8 line demultiplexer and discuss the operation of the circuit. 4.25
   b) From the following figure 4.5
   Set up a truth table showing the output Z for the 16 possible combinations of input variables.
   Write the sum of product expression for Z and simplify it to verify
   $Z = \overline{C}B\overline{A} + D\overline{C}BA + \overline{D}C\overline{B}A$



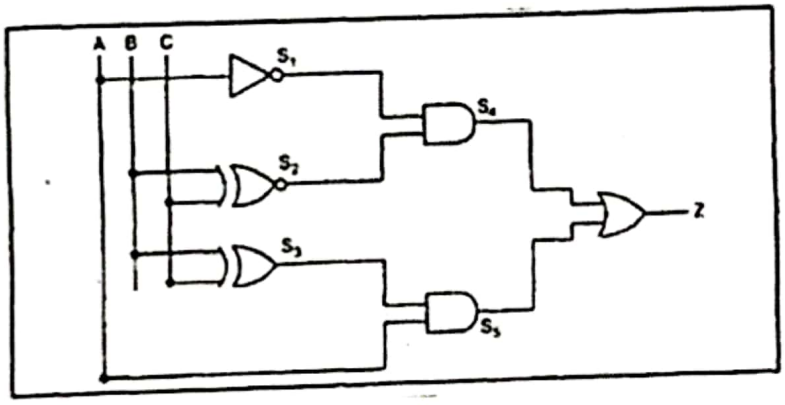
PART-B

5. a) Define asynchronous and synchronous counter. Discuss the problems of asynchronous counter? 3
   b) What is MOD number of a counter? Show how to wire the 74LS293 asynchronous counter IC as a MOD-10 counter and explain its operation. 5.75

6. a) Define excitation table. Write the excitation table of JK flip flop and D flip flop. 3
   b) Design a counter with JK flip flop that will count the sequence 0,1,3,7,5,2,0 5.75

7. a) A certain memory stores 8 k x 16 bit words. How many data input lines, data output lines and address lines does it have? What is its capacity in bytes? 3
   b) Define PAL and PLA. Implement the Boolean function using PAL. 5.75
   $Y_1 = \Sigma m\ (1, 3, 5, 7)$
   $Y_2 = \Sigma m\ (2, 4)$.

8. a) What is VHDL? What are the three levels of architecture description in VHDL? Briefly discuss. 4.75
   b) Write a VHDL code for the circuit diagram given below: 4



Rajshahi University

Department of Computer Science and Engineering

B.Sc. Engineering Part-II Examination: 2013 (Odd Semester)

Course: CSE-2111 (Digital System Design)

Full Marks: 52.5, Time: 4 Hours

[Answer any SIX (06) questions taking at least THREE (03) from each of the groups]

Part-A

1. a) What is code converter? Design a BCD to Excess-3 code converter and explain the operation. 4.25

   b) What is a magnitude comparator? Design a 2-bit magnitude comparator and explain the operation. 4.5

2. a) Design a 2-bit carry look-ahead adder. What are the advantages and disadvantages of carry look-ahead adder over ripple-carry adder? 4.25

   b) What is parity bit? Implement a 4-bit even parity generator and checker circuit and discuss the operation of the circuit with example. 4.5

3. a) Define 'minterm' and 'maxterm' with example. 2.75

   b) Define Multiplexer. Implement the following function using 4×1 MUX. 3

   $F=\sum m(0,3,4,7)$

   c) Define Decoder. Implement the following function using 74LS138 decoder. 3

   $f(A,B,C)=\sum m(0,1,4,5,7)$

4. a) What is priority encoder? Design a four-line to two-line priority encoder with active HIGH inputs and outputs, with priority assigned to the higher-order data input line. 4.75

   b) Implement a full adder circuit using a 3-to-8 line decoder. 4

Part-B

5. a) Define asynchronous and synchronous counter. What are the advantages and disadvantages of synchronous counter over asynchronous counter? 2.5

	b)	Draw a counter circuit that will convert a 64-KHz pulse signal into a 1-KHz square wave.	2
	c)	What is MOD number of a counter? Construct a decade counter and explain its operation.	4.25
6.	a)	Design a counter with J-K flip-flop that will count the sequence 0, 2, 3, 6, 5, 1, 0.	5.75
	b)	Explain the operation of Ring counter.	3
7.	a)	How does a programmable logic device differ from a fixed logic device? What are the primary advantages of using programmable logic devices?	3
	b)	Differentiate Programmable Logic Array (PLA) and Programmable Array Logic(PAL).	2
	c)	Determine the size of the PROM required for implementing the following logic circuits: (i) a binary multiplier that multiplies two four-bit numbers; (ii) a dual 8-to-1 multiplexer with common selection inputs; (iii) a single-digit BCD adder/subtractor with a control input for selection of operation.	3.75
8.	a)	What is a hardware description language? What are the requirements of a good HDL?	3
	b)	Briefly describe the salient features of VHDL and Verilog	4
	c)	What are the advantages of using Java HDL over Verilog?	1.75