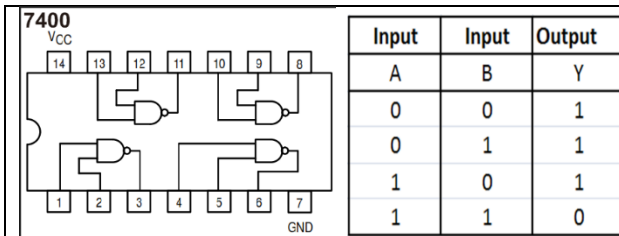
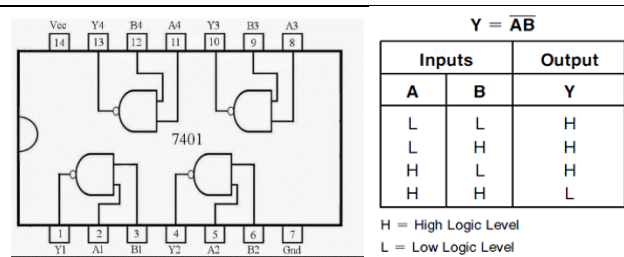


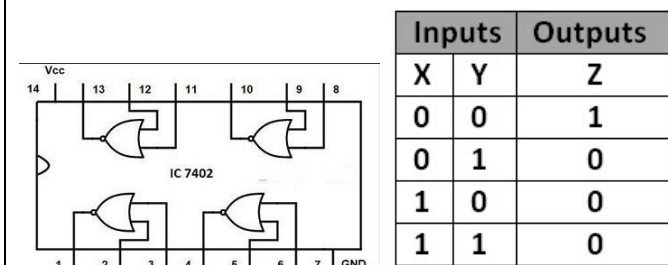
## Pin Configuration & Truth/Function Table:



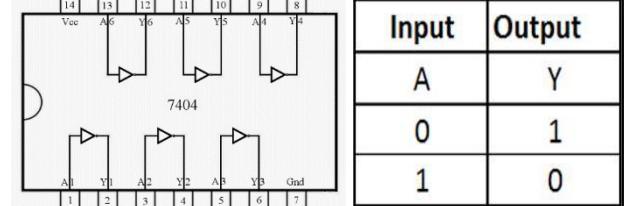
7400 - 2 input NAND Gate



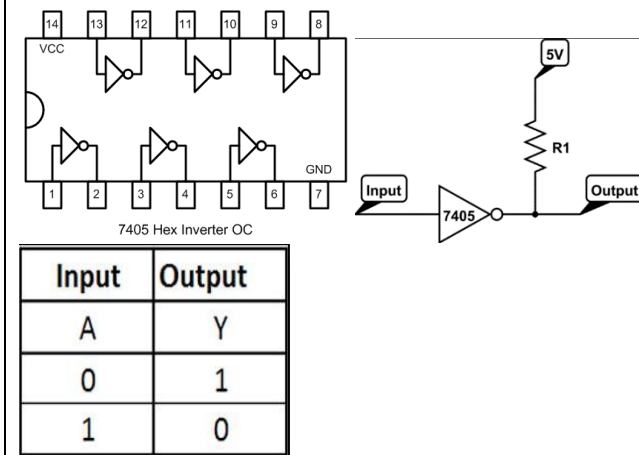
7401 - 2-input NAND gate; open collector outputs



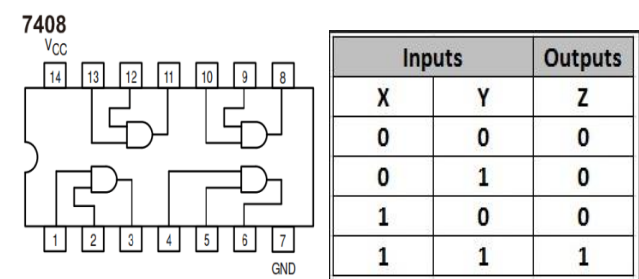
7402 - Quad 2-input NOR Gate



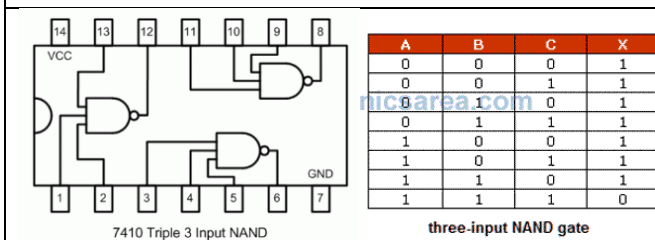
7404 - Hex inverter or NOT Gate



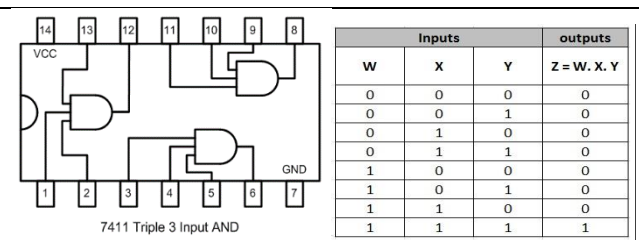
7405 - Hex inverter; open collector outputs



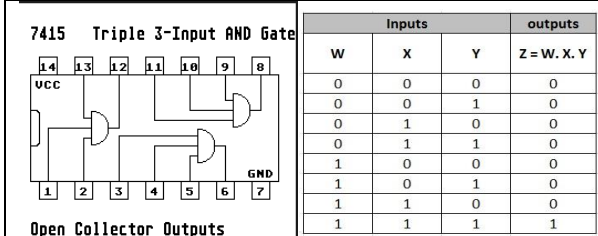
7408 - Quad 2-input AND gate



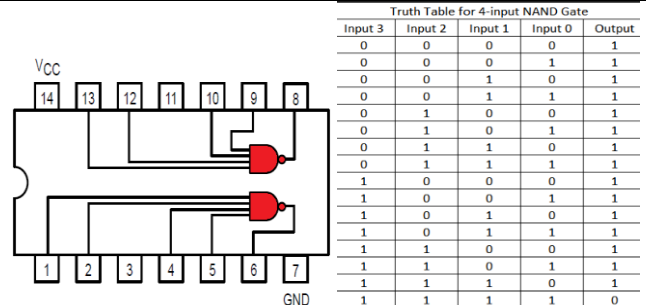
Triple 3-input NAND Gate - 7410



7411 - Triple 3-input AND Gate



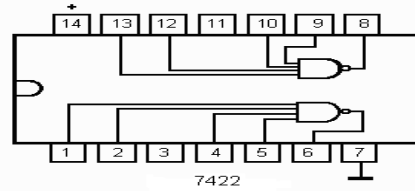
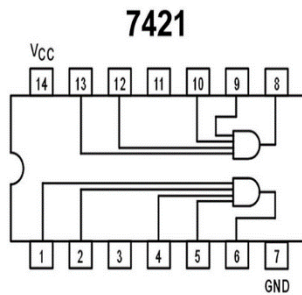
7415 - Triple 3-Input AND gate; open collector outputs



7420 - Dual 4-input NAND gate

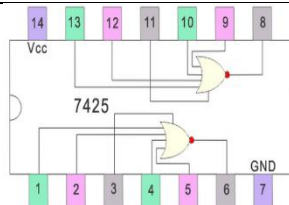
#### 4 Input AND gate

A	B	C	D	A.B.C.D
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



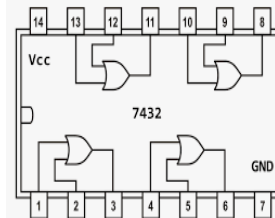
Input A	Input B	Input C	Input D	Output Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

#### Dual 4-Input AND Gates - 7421



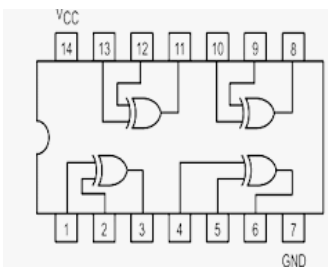
INPUT					OUTPUT
IN <sub>1</sub>	IN <sub>2</sub>	IN <sub>3</sub>	IN <sub>4</sub>	IN <sub>5</sub>	OUT
0	0	0	0	0	1
1	X	X	X	X	0
X	1	X	X	X	0
X	X	1	X	X	0
X	X	X	1	X	0
X	X	X	X	1	0

#### 4 Input NAND Gate (Open Collector) - 7422



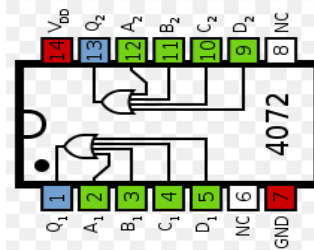
Inputs		Outputs
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

#### Dual 4-input NOR gate with strobe - 7425



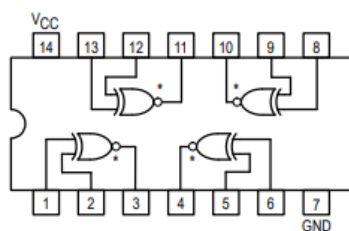
Inputs		Outputs
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

#### Quad 2-input OR gate - 7432



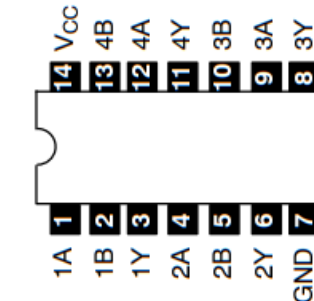
Input D	Input C	Input B	Input A	output
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

#### Quad 2-Input Exclusive-OR Gate - 7486



IN		OUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H

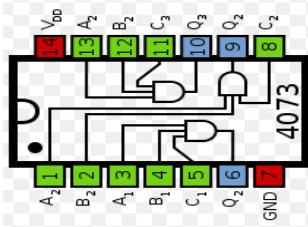
#### DUAL 4 INPUT OR GATE-4072



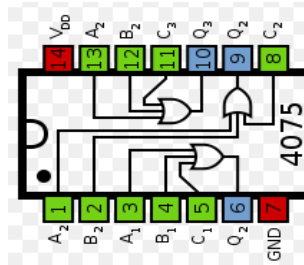
Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

#### 2-INPUT EXCLUSIVE NOR GATE - 74266

#### Quad 2-Input Positive AND Gate with Open Collector Outputs - 7409



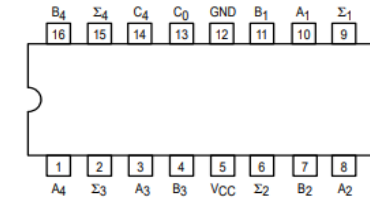
Inputs			outputs
W	X	Y	Z = W . X . Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

### 3 INPUT AND GATE - 4073

### 3 INPUT OR GATE-4075



C <sub>in</sub>	B	A	Σ	C <sub>out</sub>
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

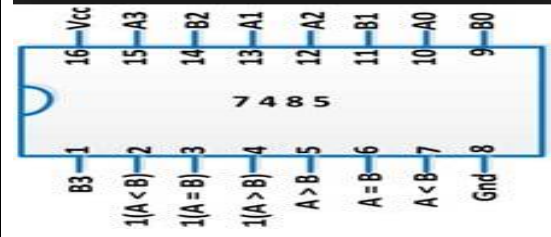
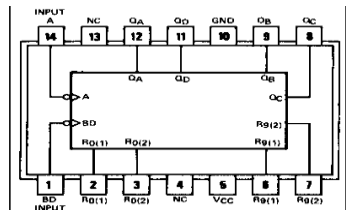


Table 10.1 Truth table of 7485

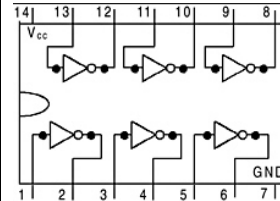
Comparing inputs						Cascading inputs			Outputs		
A <sub>3</sub>	B <sub>3</sub>	A <sub>2</sub>	B <sub>2</sub>	A <sub>1</sub>	B <sub>1</sub>	A <sub>0</sub>	B <sub>0</sub>	A > B	A < B	A = B	A > B
A <sub>3</sub> > B <sub>3</sub>	x	x	x	x	x	x	x	x	x	x	0
A <sub>3</sub> < B <sub>3</sub>	x	x	x	x	x	x	x	x	x	x	1
A <sub>3</sub> = B <sub>3</sub>	A <sub>2</sub> > B <sub>2</sub>	x	x	x	x	x	x	x	x	x	0
A <sub>3</sub> = B <sub>3</sub>	A <sub>2</sub> < B <sub>2</sub>	x	x	x	x	x	x	x	x	x	1
A <sub>3</sub> = B <sub>3</sub>	A <sub>2</sub> = B <sub>2</sub>	A <sub>1</sub> > B <sub>1</sub>	x	x	x	x	x	x	x	x	0
A <sub>3</sub> = B <sub>3</sub>	A <sub>2</sub> = B <sub>2</sub>	A <sub>1</sub> < B <sub>1</sub>	x	x	x	x	x	x	x	x	1
A <sub>3</sub> = B <sub>3</sub>	A <sub>2</sub> = B <sub>2</sub>	A <sub>1</sub> = B <sub>1</sub>	A <sub>0</sub> > B <sub>0</sub>	x	x	x	x	x	x	x	0
A <sub>3</sub> = B <sub>3</sub>	A <sub>2</sub> = B <sub>2</sub>	A <sub>1</sub> = B <sub>1</sub>	A <sub>0</sub> < B <sub>0</sub>	x	x	x	x	x	x	x	1
A <sub>3</sub> = B <sub>3</sub>	A <sub>2</sub> = B <sub>2</sub>	A <sub>1</sub> = B <sub>1</sub>	A <sub>0</sub> = B <sub>0</sub>	1	0	0	0	1	0	0	0
A <sub>3</sub> = B <sub>3</sub>	A <sub>2</sub> = B <sub>2</sub>	A <sub>1</sub> = B <sub>1</sub>	A <sub>0</sub> = B <sub>0</sub>	0	1	0	0	0	1	0	0
A <sub>3</sub> = B <sub>3</sub>	A <sub>2</sub> = B <sub>2</sub>	A <sub>1</sub> = B <sub>1</sub>	A <sub>0</sub> = B <sub>0</sub>	0	0	1	0	0	0	1	0
A <sub>3</sub> = B <sub>3</sub>	A <sub>2</sub> = B <sub>2</sub>	A <sub>1</sub> = B <sub>1</sub>	A <sub>0</sub> = B <sub>0</sub>	1	1	0	0	0	0	0	1
A <sub>3</sub> = B <sub>3</sub>	A <sub>2</sub> = B <sub>2</sub>	A <sub>1</sub> = B <sub>1</sub>	A <sub>0</sub> = B <sub>0</sub>	0	0	0	0	1	1	0	0

### 4-bit Binary Full Adder -7483

### 4-Bit Magnitude Comparator -7485



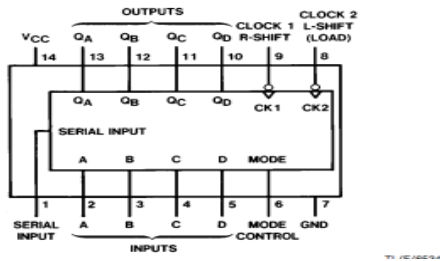
Input Pulses	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
0	0	0	0	0 (resets)



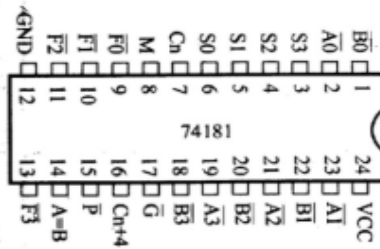
Clock Pulse	Q1	Q2	Q3	Q4
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1

### Decade and Binary Counter - 7490

### 8-BIT SHIFT REGISTERS-7491



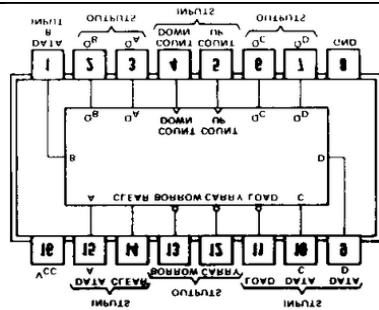
Mode Control	Inputs				Outputs			
	Clocks		Serial	Parallel	QA	QB	QC	QD
	2(L)	1(R)						
H	H	X	X	X X X X	QA0	QB0	QC0	QD0
H	↓	X	X	a b c d	a	b	c	d
H	↓	X	X	QB↑ QC↑ QD↑	QBn	QCn	QDn	d
L	L	H	X	X X X X	QA0	QB0	QC0	QD0
L	X	↓	H	X X X X	H	QA0	QB0	QC0
L	X	↓	L	X X X X	L	QA0	QB0	QC0
↑	L	L	X	X X X X	QA0	QB0	QC0	QD0
↑	L	L	X	X X X X	QA0	QB0	QC0	QD0
↑	L	H	X	X X X X	QA0	QB0	QC0	QD0
↑	H	L	X	X X X X	QA0	QB0	QC0	QD0
↑	H	H	X	X X X X	QA0	QB0	QC0	QD0



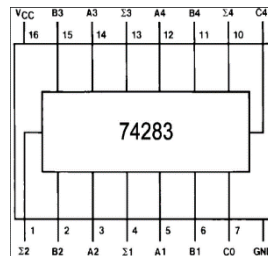
SELECTION				M = H LOGIC FUNCTIONS	ACTIVE-HIGH DATA	
S3	S2	S1	S0		Cn = H (no carry)	Cn = L (with carry)
L	L	L	L	F = A	F = A	F = A PLUS 1
L	L	L	H	F = A + B	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = AB	F = A + B	F = (A + B) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = AB	F = A PLUS AB	F = A PLUS AB PLUS 1
L	H	L	H	F = B	F = (A + B) PLUS AB	F = (A + B) PLUS AB PLUS 1
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = AB	F = AB MINUS 1	F = AB
H	L	L	L	F = A + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + B) PLUS AB	F = (A + B) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A	F = A PLUS A PLUS 1
H	H	L	H	F = A + B	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + B) PLUS 1	F = (A + B) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

#### 4-BIT PARALLEL-ACCESS SHIFT REGISTERS- 7495

#### 4-BIT ARITHMETIC LOGIC UNIT-74181



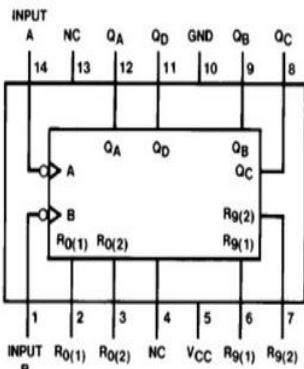
Input Pulses	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
0	0	0	0	0 (resets)



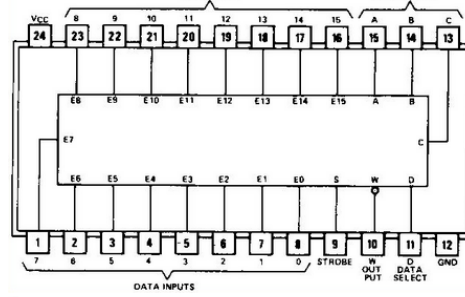
Inputs				Output
S3	S2	S1	S0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

#### SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)-74192

#### 4-BIT BINARY FULL ADDER WITH FAST CARRY-74283



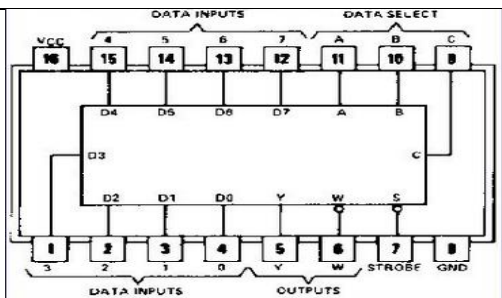
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H



Strobe input (Strobe)	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	Output Y
0	0	0	0	0	D <sub>0</sub> '
0	0	0	0	1	D <sub>1</sub> '
0	0	0	1	0	D <sub>2</sub> '
0	0	0	1	1	D <sub>3</sub> '
0	0	1	0	0	D <sub>4</sub> '
0	0	1	0	1	D <sub>5</sub> '
0	0	1	1	0	D <sub>6</sub> '
0	0	1	1	1	D <sub>7</sub> '
0	1	0	0	0	D <sub>8</sub> '
0	1	0	0	1	D <sub>9</sub> '
0	1	0	1	0	D <sub>10</sub> '
0	1	0	1	1	D <sub>11</sub> '
0	1	1	0	0	D <sub>12</sub> '
0	1	1	0	1	D <sub>13</sub> '
0	1	1	1	0	D <sub>14</sub> '
0	1	1	1	1	D <sub>15</sub> '
1	x	x	x	x	1

DECADE COUNTER 4-BIT BINARY COUNTER -74293

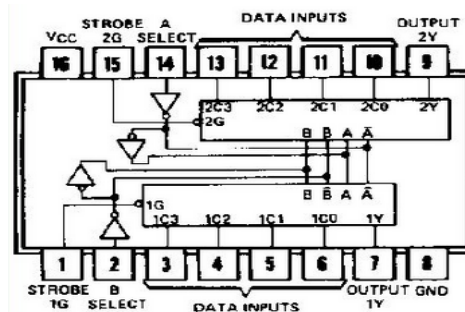
16:1 Multiplexers / Data Selectors -74150



TRUTH TABLE

E	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>	Z	Z
H	x	x	x	x	x	x	x	x	x	x	x	H	L
L	L	L	L	L	x	x	x	x	x	x	x	H	L
L	L	L	L	H	x	x	x	x	x	x	x	L	H
L	L	L	H	x	L	x	x	x	x	x	x	L	H
L	L	L	H	x	H	x	x	x	x	x	x	L	H
L	L	H	L	x	x	L	x	x	x	x	x	H	L
L	L	H	L	x	x	H	x	x	x	x	x	L	H
L	L	H	H	x	x	x	L	x	x	x	x	H	L
L	L	H	H	x	x	x	H	x	x	x	x	L	H
L	H	L	L	x	x	x	L	x	x	x	x	H	L
L	H	L	L	x	x	x	H	x	x	x	x	L	H
L	H	L	H	x	x	x	x	L	x	x	x	H	L
L	H	L	H	x	x	x	x	H	x	x	x	L	H
L	H	H	L	x	x	x	x	x	L	x	x	H	L
L	H	H	L	x	x	x	x	x	H	x	x	L	H
L	H	H	H	x	x	x	x	x	x	L	x	H	L
L	H	H	H	x	x	x	x	x	x	H	x	L	H

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

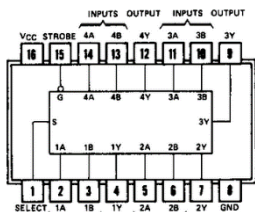


Entrées							Sortie
A	B	C0	C1	C2	C3	G	Y
x	x	x	x	x	x	1	0
0	0	0	x	x	x	0	0
0	0	1	x	x	x	0	1
0	1	x	0	x	x	0	0
0	1	x	1	x	x	0	1
1	0	x	x	0	x	0	0
1	0	x	x	1	x	0	1
1	1	x	x	x	0	0	0
1	1	x	x	x	1	0	1

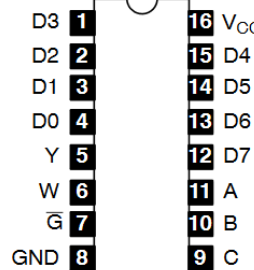
8-Line To 1-Line Data Selectors/Multiplexers-74151

Dual 4-Line To 1-Line Data Selectors/Multiplexers -74153





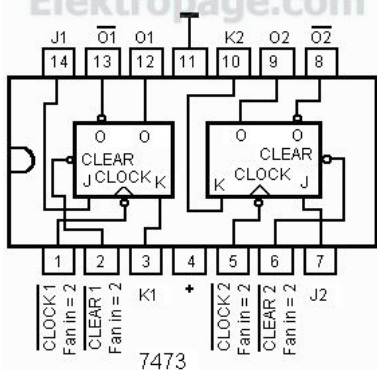
Select Data Inputs			Y = A ⊕ B ⊕ C
S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



Enable	Select Inputs			Output
E	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	Y
0	X	X	X	0
1	0	0	0	D <sub>0</sub>
1	0	0	1	D <sub>1</sub>
1	0	1	0	D <sub>2</sub>
1	0	1	1	D <sub>3</sub>
1	1	0	0	D <sub>4</sub>
1	1	0	1	D <sub>5</sub>
1	1	1	0	D <sub>6</sub>
1	1	1	1	D <sub>7</sub>

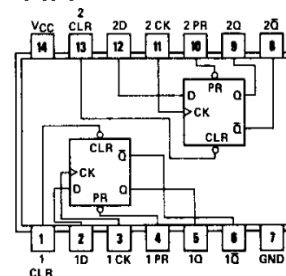
#### Quadruple 2-Line To 1-Line Data Selectors/Multiplexers-74157

#### 8:1 Data Selectors/multiplexers With 3-state Outputs-74251



J	K	CLK	Q	Q'
0	0	0	0	1
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

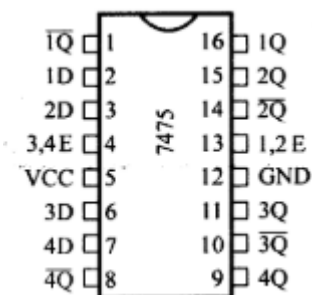
#### 7474



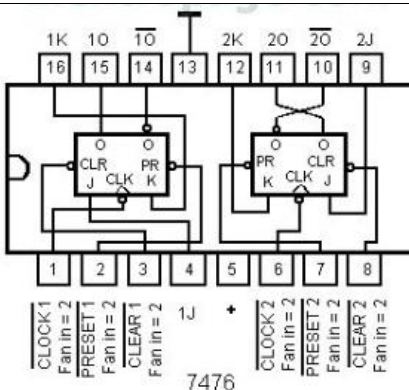
ENTREES				SORTIES	
PRESET	CLEAR	CLOCK	D	Q	Q'
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1	1
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q <sub>0</sub>	Q <sub>0</sub>
1	1	1	X	Q <sub>0</sub>	Q <sub>0</sub>

#### DUAL J-K FLIP-FLOPS WITH CLEAR-7473

#### Dual D-Type Positive-Edge-Triggered Flip-Flops With Preset And Clear-7474



ENTREES				SORTIES	
CLEAR	PRESET	CLOCK	J	K	Q
1	0	X	X	X	0
0	1	X	X	X	1
1	1	X	X	X	1
0	0	↑	0	0	Q <sub>0</sub>
0	0	↑	1	0	1
0	0	↑	0	1	0
0	0	↑	1	1	TOGGLE
0	0	0	X	X	Q <sub>0</sub>
0	0	1	X	X	Q <sub>0</sub>

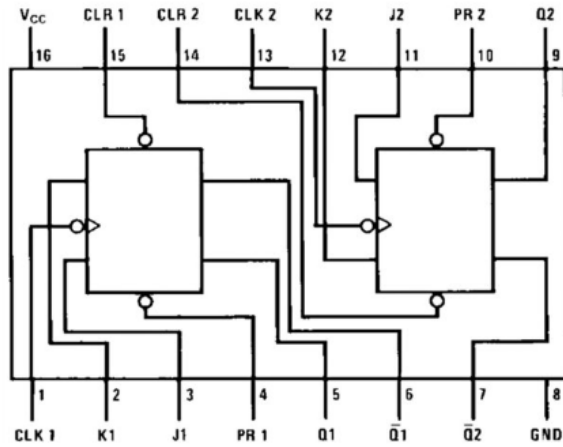


INPUTS			OUTPUTS	
Preset	Clear	Clock	T	Q
L	H	X	X	H
H	L	X	X	L
L	L	X	X	H
H	H	↓	H	TOGGLE
H	H	↓	L	H
H	H	L	X	TOGGLE

#### 4-BIT BI STABLE LATCHES -7475

#### DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR-7476

## 74112



INPUTS					OUTPUTS		FUNCTION
CLR	PR	J	K	CK	Q	Q̄	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	NO CHANGE
H	H	L	L	$\downarrow$	Q <sub>n</sub>	Q̄ <sub>n</sub>	
H	H	H	L	$\downarrow$	H	L	
H	H	L	H	$\downarrow$	L	H	TOGGLE
H	H	H	H	$\downarrow$	Q̄ <sub>n</sub>	Q <sub>n</sub>	
H	H	X	X	$\downarrow$	Q <sub>n</sub>	Q̄ <sub>n</sub>	

X: Don't Care

### Dual J-K Negative-Edge-Triggered Flip-Flops with Clear And Preset-74112

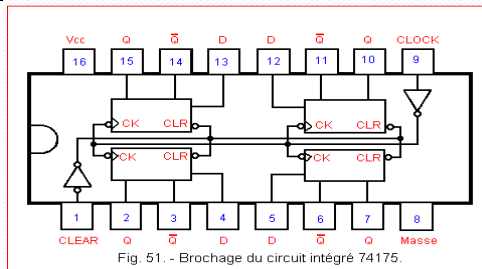
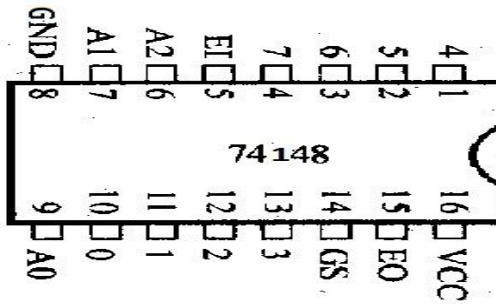


Fig. 51. - Brochage du circuit intégré 74175.

CLEAR	CLOCK	D	Q	Q̄
0	X	X	0	1
1	$\uparrow$	0	0	1
1	$\uparrow$	1	1	0
1	0	X	Q <sub>0</sub>	Q̄ <sub>0</sub>
1	1	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

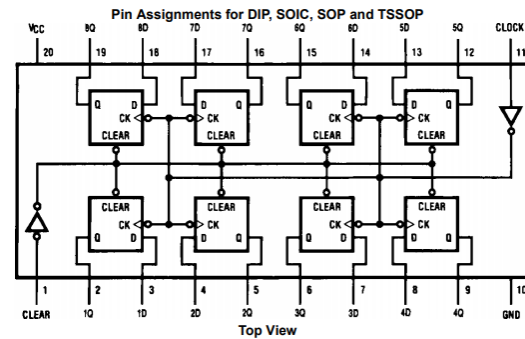
ia. 52. - Table de vérité de chaque bascule D du

### HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR -74175



Inputs									Outputs				
EI	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>	GS	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	L	H	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

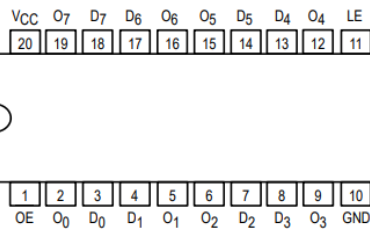
### 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS-74148



### Truth Table

(Each Flip-Flop)			
Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	$\uparrow$	H	H
H	$\uparrow$	L	L
H	L	X	Q <sub>0</sub>

### OCTAL D-TYPE FLIP-FLOP WITH CLEAR -74273

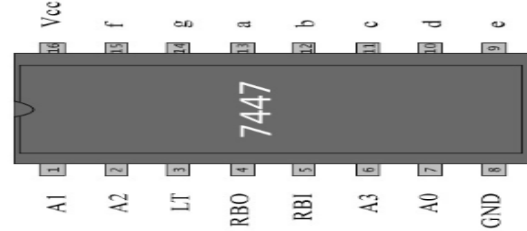


'LS373, 'S373  
(each latch)

INPUTS			OUTPUT Q
OC	C	D	
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

Output Control	Latch Enable	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

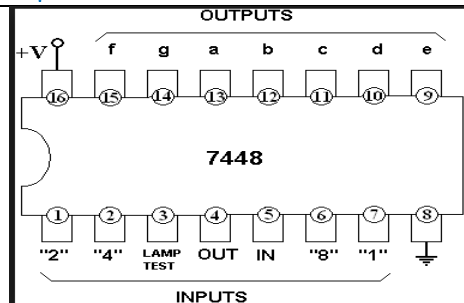
H = high level, L = low level  
Q<sub>0</sub> = level of output before steady-state input conditions were established.  
Z = high impedance



DECIMAL OR FUNCTION	INPUTS							OUTPUTS							NOTE
	LT	RBI	D	C	B	A	BIRBO	A	B	C	D	E	F	G	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	L	1
1	H	X	L	L	L	H	H	L	L	L	H	H	H	H	1
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	L	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	L	L	L	H	L	
11	H	X	H	L	H	H	H	H	L	L	H	H	L	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	L	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	2
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	3
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	4

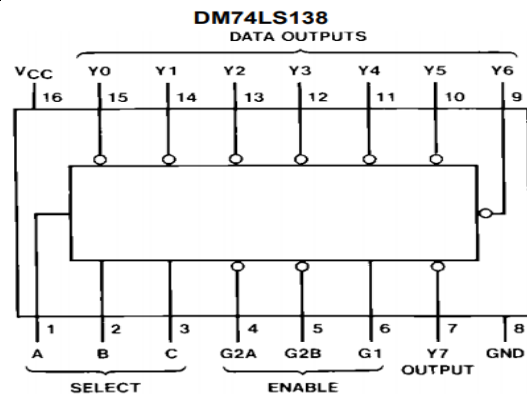
### 3-state Octal D-type Transparent Latches and Edge-triggered Flip-flops -74373

### BCD-TO-SEVEN-SEGMENT DECODERS / DRIVERS-7447



TRUTH TABLE  
SN54/74LS48

DECIMAL OR FUNCTION	INPUTS							OUTPUTS							NOTE
	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	L	L	1
1	H	X	L	L	L	H	H	L	H	L	L	L	L	L	1
2	H	X	L	L	H	L	H	H	L	H	H	L	L	H	
3	H	X	L	L	H	H	H	H	L	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	L	L	L	H	H	
5	H	X	L	H	L	H	H	L	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	L	L	L	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	L	L	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	L	L	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	L	L	L	L	H	H	
13	H	X	H	H	L	H	H	L	L	L	L	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	L	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

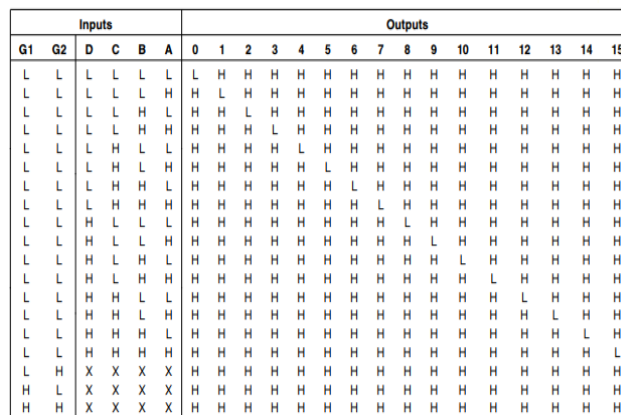
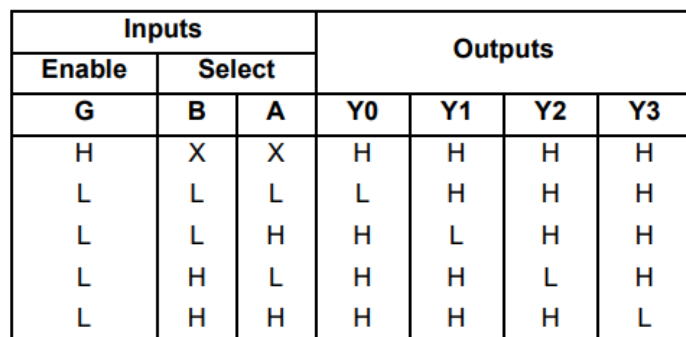


Inputs			Outputs									
Enable		Select										
G1	G2 (Note 1)	C B A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7		
X	H	X X X	H	H	H	H	H	H	H	H		
L	X	X X X	H	H	H	H	H	H	H	H		
H	L	L L L	L	H	H	H	H	H	H	H		
H	L	L L H	L	L	H	H	H	H	H	H		
H	L	L H L	L	L	L	H	H	H	H	H		
H	L	L H H	L	L	L	L	H	H	H	H		
H	L	H L L	L	L	L	L	L	H	H	H		
H	L	H L H	L	L	L	L	L	L	H	H		
H	L	H H L	L	L	L	L	L	L	L	H		
H	L	H H H	L	L	L	L	L	L	L	L		

### BCD to 7-Segment Decoder -7448

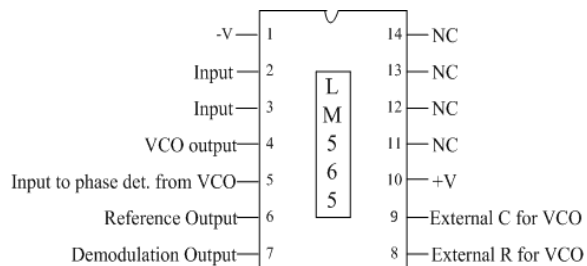
### 3-to-8-line decoders / Demultiplexer -74138



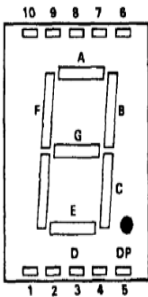
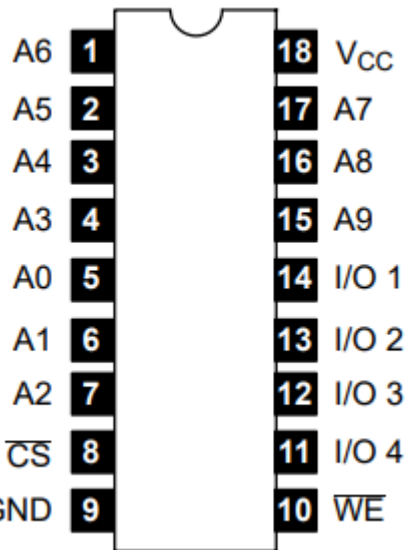


H = High Level L = Low Level X = Don't Care

## 4-Line to 16-Line Decoders/Demultiplexers -74154



## Phase Locked Loop- LM565

 <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>1 Segment E</p> <p>2 Segment D</p> <p>3 Common Anode</p> <p>4 Segment C</p> <p>5 Decimal Point</p> <p>6 Segment B</p> <p>7 Segment A</p> <p>8 Common Anode</p> <p>9 Segment F</p> <p>10 Segment G</p> </div> <div style="width: 45%;"> <p>Segment E</p> <p>Segment D</p> <p>Common Cathode</p> <p>Segment C</p> <p>Decimal Point</p> <p>Segment B</p> <p>Segment A</p> <p>Common Cathode</p> <p>Segment F</p> <p>Segment G</p> </div> </div>	
<a href="#">7 Segment display</a>	<a href="#">Static 4K RAM-2214</a>

N.B- If have any wrong pin diagram & truth/function table, please change those pins configurations & truth/ function table.  
(SAC-504 & 507)