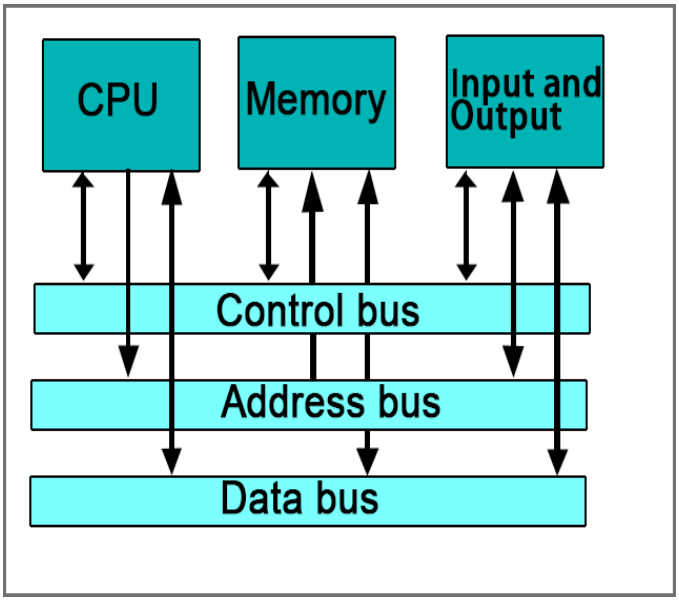
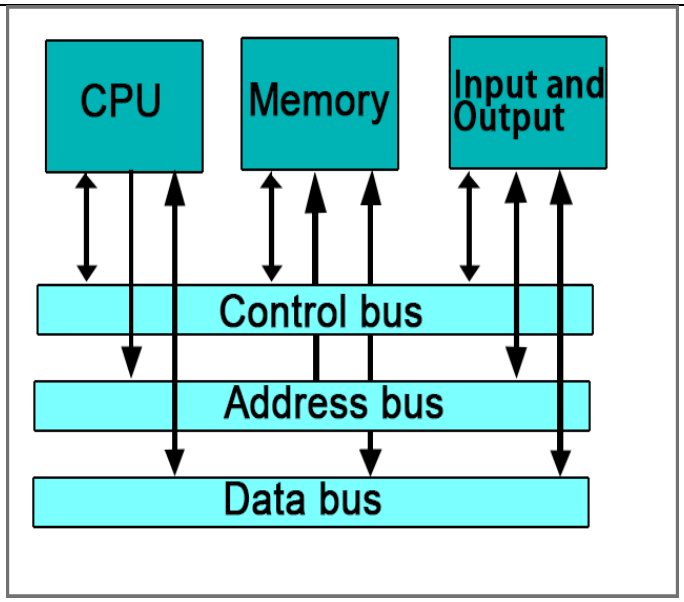
Questions: Lecture-3

	What is Bus System? Different components of a computer are connected through conducting wires, called bus system. Different components communicate through these lines; data transfer, address information and electronic commands are passed through these conducting pathways. 
	What are different types of buses? There are three types of buses, as discussed below: Data bus: transfers data from • CPU- to –Memory • Memory-to-CPU • CPU/Memory-to Output Devices • Input Devices- to-CPU/Memory Address Bus: carries address from CPU to Memory or Input/Output Devices. Control Bus: Carries different command (electronic from) from CPU to Memory and other components/functional units. CPU also receives some Control signals from Input/output devices and other functional units through some control lines of control bus.

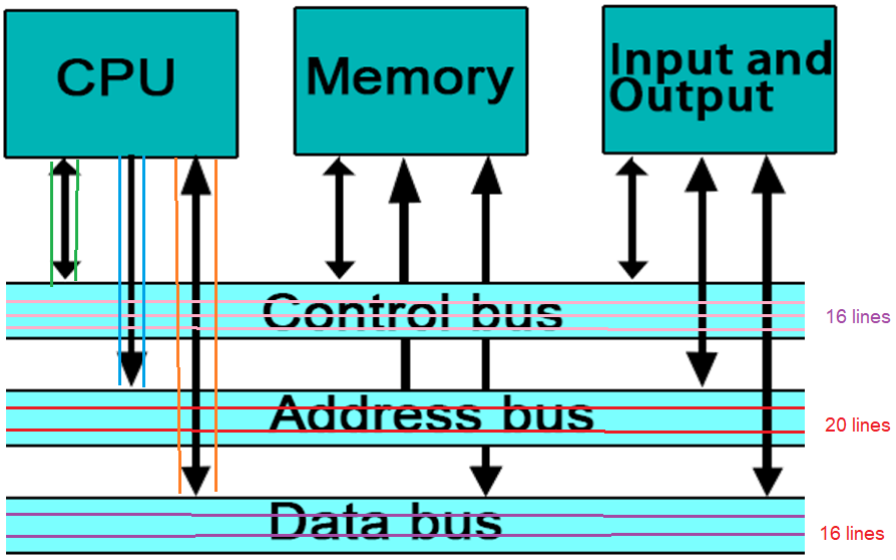


What is the size of bus?

Each bus is designed to carry/transfer a number of bits and there are number of lines/conducting wires in bus and a single conducting line can carry only one bit.

Sizes of different types of buses are defines by no of bits transferred at a time which is related to the number of conducting wires.

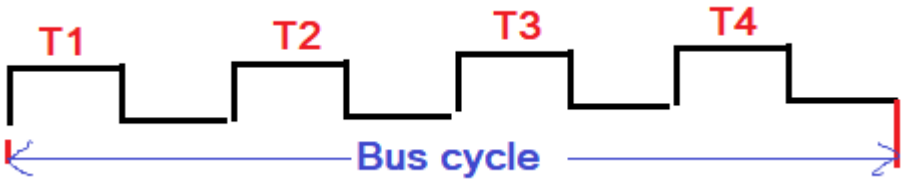
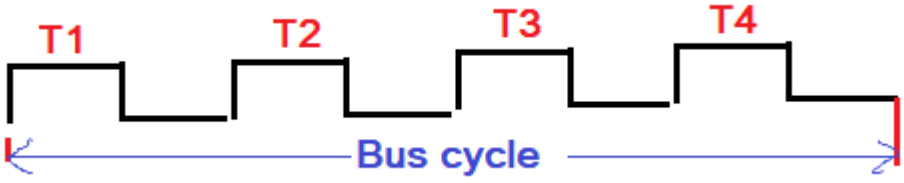
Example: For the following bus system, the size of data bus is 16 bits, size of address bus is 20 bits and size of control bus is 16 bits.



It is to be noted that for address and data buses, all lines are used at the same time to carry address and data information respectively. But in case of control bus, only one

	or few lines may be used at a time since the CPU is designed to perform only one or a few operation at a time. For example, the CPU cannot perform read and write operation at a time. So, either read or write control signal will be activated at a time.
	What do the sizes of three types of bus depend on? Sizes of three types of buses depend on CPU/processor used in the computer/system.
	What does the size of data bus depend on? Size of data bus depends on CPU/processor.
	What does the size of address bus depend on? Size of address bus depends on CPU/processor.
	What is the significance of size of data bus in processor? Give examples. The size of data bus will indicate how many bits the CPU can read/write from/to RAM at a time. If the data bus is 8-bits, the CPU can read 8-bits from RAM or save 8-bit to RAM at a time. Similarly, If the data bus is 16-bits, the CPU can read 16-bits from RAM or save 16-bit to RAM at a time.
	What do you understand by 8bit/16bit/32 bit data bus? There are 8/16/32 conducting wires or lines within bus system to transfer data between CPU-RAM, RAM-I/O devices. The CPU can read/write 8bit/16bit/32bit data/instruction in a single read/write operation. If the data bus is wider, the CPU can more bytes (instruction/data) from RAM in a single read operation and also stores more bytes in a single write operation.
	Mention one advantage and one disadvantage of a single bus system. Very simple but synchronized with the slowest unit connected to it. So the faster units have to remain in idle or wait state most of the time.
	What is the significance of size of address bus in processor? Give examples. The size of address bus will decide the size (capacity) of RAM can be used with the processor. For example, if the size of address bus is 10bits, The size of RAM to be used with the processor is limited to 1KB since 10 bits address can generate 2^{10} (=1024) addresses

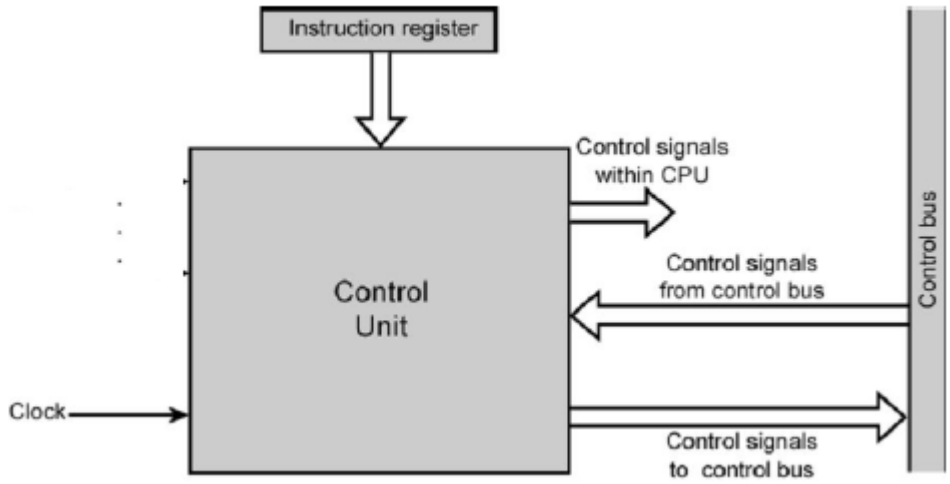
	which is 1K. If a byte addressable memory is used, then the maximum size(capacity) of memory would be 1KB. Similarly, if the size of address bus is 20bits, The size of RAM to be used with the processor is limited to 1MB since 20 bits address can generate 2^{20} (=1024x1024) addresses which is 1M. If a byte addressable memory is used, then the maximum size (capacity) of memory would be 1MB. Moreover, in early days computer, the maximum size of a program was limited by the size of RAM a computer could use. It means, in order to run a program, user program must fit into RAM. This limitation is no more in place now a days due to the development of virtual memory concepts that all modern processors support. In virtual memory concept, secondary storage (hard disk) is logically considered as primary memory. User program can be saved into Hard drive and then when it is run, operating system will transfer parts by parts of it to RAM.
	How does the size of the data bus affect system performance? CPU can read more bits from RAM, CPU can also save more bits to RAM at a time. For example, if instructions are 16bits (2Bytes) and data bus is 8-bits, then CPU needs to perform two read operations to read instructions from a byte addressable RAM. If instructions are 16bits (2Bytes) and data bus is 16-bits, then CPU needs to perform one read operation to read instructions from RAM.
	How does the size of the address bus affect system performance? Higher address bus means the CPU can generate more addresses and higher capacity RAM can be used with the CPU that will allow bigger programs to run on the computer.
	Give some examples of commonly found control signals in any general purpose processor? READ, WRITE, RESET, INTERRUPT etc. READ and WRITE control signals are output with respect to CPU whereas RESET and INTERRUPT control signals are input with respect to CPU.
	What is the direction of signal flow on data bus? The data bus is bidirectional, it means, signals can follow in both the direction although only a specific direction at a time. During read operation, the CPU receives data from RAM through data bus and signal flow is input with respect to the CPU whereas during write

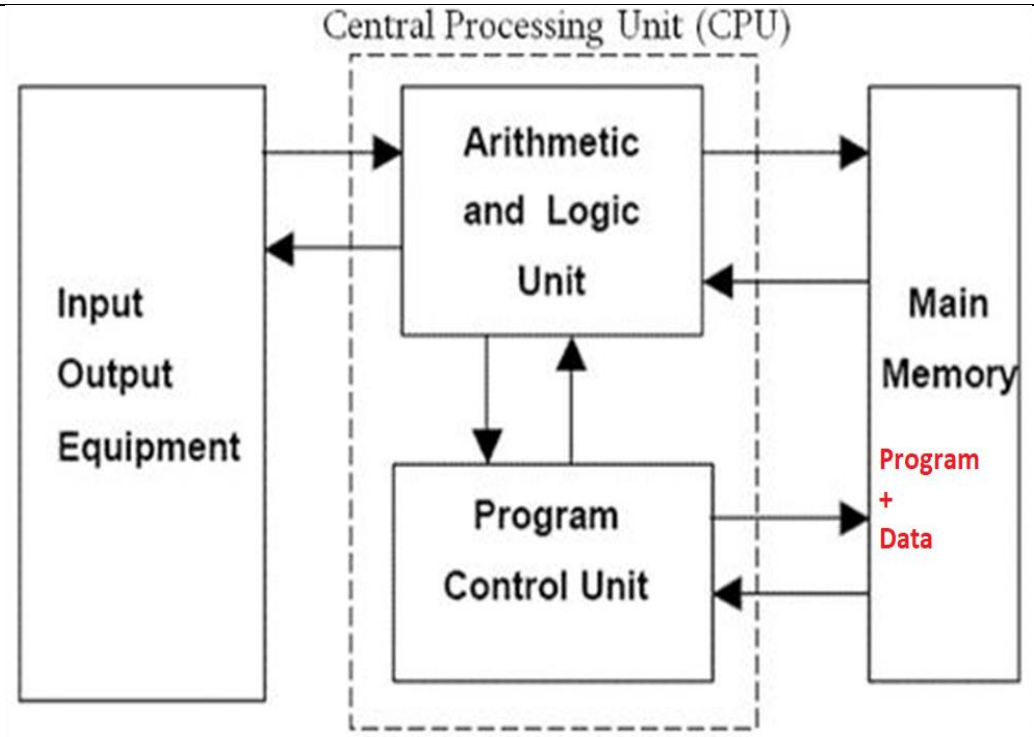
	operation CPU saves contents of register to RAM through data bus and signal flow is output with respect to CPU.
	What is the direction of signal flow on address bus? The address bus is unidirectional and output with respect to CPU. It means, CPU always sends address information to RAM and Input/output devices through address bus.
	What is the direction of signal flow on control bus? The signal flow on control bus is bidirectional although it is not like data bus. Some control signals are output with respect to CPU whereas some control signals are input to the CPU. Example: READ and WRITE control signals are output with respect to CPU whereas RESET and INTERRUPT control signals are input with respect to CPU.
	State the steps, the CPU is designed to follow in a READ operation. Read operation means that contents of a memory locations will be copied to a register within the CPU. A CPU is designed to follow following steps: a) CPU will send the address of memory location to RAM through address bus b) READ control signal is activated c) The contents of RAM will be available on data bus d) Contents of data bus will be copied to a register within CPU Each task, state above, would require at least a clock cycle of the CPU clock/timing signal. So four clock cycles are required for a READ operation. At time step,T1, task (a) is performed. In time steps T2, T3 and T4 tasks (b), (c) and (d) are performed respectively.  Time required for a READ operation, called access time to RAM. It is also called bus cycle.
	State the steps, the CPU is designed to follow in a WRITE operation. Write operation means that the CPU will store/save contents of a register to a specific memory location. It is also stated that the contents of a register will be copied to RAM. A CPU is designed to follow following steps: e) CPU will send the address of memory location to RAM through address bus f) CPU will send the contents of a register to data bus g) WRITE control signal is activated h) The contents of data bus will be saved/copied to RAM Each task, state above, would require at least a clock cycle of the CPU clock/timing signal. So four clock cycles are required for a WRITE operation. At time step,T1, task (a) is performed. In time steps T2, T3 and T4 tasks (b), (c) and (d) are performed respectively. 

	Time required for a WRITE operation is same as READ operation and called access time to RAM. It is also called bus cycle.

Short questions and MCQ

	The size of data bus depends on: a) CPU b) Memory c) Input/Output devices d) Program
	What is the direction of signal flow on data bus? Bi-directional
	What is the direction of signal flow on address bus? Unidirectional (output w.r.t CPU)
	The size of address bus decides: a) CPU speed b) Memory speed c) Memory capacity d) System throughput
	The size of address bus decides: e) CPU speed f) Memory speed g) Memory capacity h) System throughput
	The size of data bus depends on: e) CPU f) Memory g) Input/Output devices h) Program
	What is control unit? Control units is also called instruction decoder. It is the most important functional unit of the CPU to decode the machine codes of instructions into electronic signals. Each machine code is a command for a basic operation to the CPU. The machine code contains binary codes for operation to be performed, data or addresses of data and address or binary code of result field where CPU saves the result. Upon receiving the machine code of an instruction, the control unit generate a series of electronic signals, called control signals in a sequence which are used to activate/perform very basic/elementary operations within the CPU or external to the CPU, called microoperations. Examples of microoperations are as follows:

	Transfer contents of a register to internal bus of CPU Select/activate a specific circuit within ALU for the current operation being decoded Transfer contents of internal CPU bus to a register etc For each microoperation as stated above, one or a few control signals need to be generated/activated by the control unit and placed to appropriate sections. The control unit provides signals that activate the various microoperations within the CPU. The control unit also determines the sequence in which the actions are performed. Executing an instruction means activating the necessary sequence of microoperations in the CPU required to perform the operation specified by the instruction. Timing of all registers in a synchronous digital system in controlled by an electronic signal called clock. 
	What are design techniques of control unit? Control unit design techniques are either — hardwired — Or microprogrammed
	What is Von Neumann architecture? First **stored program computer model.** Both Instructions and Data are stored in RAM in binary Instructions (Program) are modified easily Single RAM holds both Instructions and Data Single BUS system was used to connect CPU to RAM



Key Features

- Data and instructions are both stored in a single primary storage
- Instructions are read from memory one at a time and in order (serially as it is stored/as it appears in a program).
- The processor decodes and executes one instruction at a time.
- Result is stored
- CPU reads next instruction from RAM
- This process continues till the end of the program.
- Parallel implementation of instructions is not allowed.
- Instructions can only be carried out one at a time and sequentially.
- CPU cannot read Instruction and data simultaneously due to a single bus system

Limitations: Von Neumann Bottleneck

An instruction read/fetch and a data operation cannot occur at the same time because they share a common bus.

CPU has to wait and remains idle for a certain amount of time while low speed memory is being accessed.

Von Neumann bottleneck limits the performance of the system.

Harvard Architecture

- Separate memory for program and data.
  - Instructions are stored in program memory and data are stored in data memory.
- Instruction and data accesses can be done in parallel.
- Some microcontrollers and pipelines with separate instruction and data caches follow this concept.
- The processor-memory bottleneck remains.