North South University
Term Final Assignment: Summer 2025
CSE332: Computer Organization and Architecture

Last date to submit: 10pm,September 2, 2025

This is not mandatory for all. Only students who got very low marks can submit.

1.	Show the binary multiplication 1101 and 1011 using left shift and right shift algorithms. Also draw schematic diagrams for the implementation of both algorithms
2.	Show the multiplication of 4 x (- 5) using Booth's algorithm. You need to show the flowchart, schematic of the hardware and contents of registers, adder and other units in a table.

3.	Identify data dependency, if any, show the processing of instruction on a MIPS (5-stage pipeline) processor. Assume there is only a datapath from EXE/MEM buffer to an input to EXE unit for data forwarding.
	LW $s0, 64($s1)
	SUB $t0, $s0, $s2
	SW $t0, 40($s3)
	NSU: Lw $s2, 40($s3)
	XOR $s7, $s2, $s2
	ANDI $s4, $s5, $zero
	BNE $s4, $s7, NSU
	ADDI $s1, $s0, 0xF

4.	Identify data dependency, if any, show the processing of instruction on a MIPS (5-stage pipeline) processor. If data forwarding is used, please specify the datapaths exist in the pipeline architecture.
	LW $s0, 64($s1)
	SUB $t0, $s0, $s2
	NEXT_inst: Lw $s2, 40($s3)
	XOR $s7, $s2, $s2
	ANDI $s4, $s5, $zero
	BNE $s4, $s7, NEXT_inst
	ADDI $s1, $s0, 0xF

5.	Design microarchitecture of a RISC processor that must support (i) ALU instructions in Register mode, (ii) ALU instructions in Immediate mode, (iii) LOAD instruction and (iv) STORE instruction
6.	What is cache memory? What do you understand by locality of reference? List the steps in sequential order, how does CPU fetch instructions and read data in a system having split caches.
7.	Draw the flowchart and schematic diagram for floating point adder and explain it.

8.	Draw the microarchitecture of an accumulator based CPU.
9.	For the following C statement, what is the corresponding MIPS assembly code? Assume that the variables f, g, h, and i are given and could be considered 32-bit integers as declared in a C program. Use a minimal number of MIPS assembly instructions. f = g + (h − 5) +q; i = f + 16;
10.	Show the instruction formats of MIPS R2000 processor.