Course Objective and Outcome Form
Department of Electrical and Computer Engineering
School of Engineering and Physical Sciences
North South University, Bashundhara, Dhaka-1229, Bangladesh

1.	Course Number and Title:	CSE 332 Computer Organization and Architecture
2.	Credits:	3
3.	Type:	Required, Engineering, Lecture + Lab
4.	Prerequisites:	CSE 231 Digital Logic Design
5.	Contact Hours:	Lecture – 3 Hours/week, Lab – 3 Hours/week

6. Course Summary

This course introduces students to the basic concepts of computers, their design and how they work. It encompasses the definition of the machine's instruction set architecture, its use in creating a program, and its implementation in hardware. The course addresses the bridge between gate logic and executable software, and includes programming both in assembly language (representing software) and HDL (representing hardware). It will cover modern computer principles using a typical processor and emphasize system-level issues, understanding process performance, and the use of abstraction as a tool to manage complexity. It will then explain how efficient memory systems are designed to work closely with the processor. Next, it will introduce micro-architecture, datapath design, pipeline architecture and hazards, superscalar architecture, multi-core processors, cache memory & mapping, ALU, Floating Point Numbers and Floating Point ALU design. Moreover, design of microprogrammed control unit will be discussed. Finally, we introduce systems with many processors.

7. Course Objective:

The objectives of this course are

a) to develop basic understanding of computer organization: roles of processors, main memory, and input/output devices.
b) to evaluate/measure the performance of a computing system for comparing with other similar systems
c) to familiar with architectural design concepts related to different building blocks of a processor. Also to introduce VHDL to design micro-architecture.
d) to employ specialized knowledge of subsystems like data-path, memory and control unit components to design a RISC processing element
e) to define processor specification and instruction set architecture.
f) to understand memory organization, including cache structures and virtual memory schemes.
g) to understand design of multiplier, floating point ALU, multi-core and superscalar processor

8. Course Outcomes (COs):

Upon Successful completion of this course, students will be able to:

SI	CO Description	Weightage (%)
CO1	Introduction to functional units and evaluate the performance of a computing system	10%
CO2	Analyze instruction set architecture and different building blocks of processor for designing more efficient processors	20%
CO3	Design an instruction set architecture and subsystems of central processing unit.	20%
CO4	Design pipeline architecture, cache memory, ALU, floating point ALU, superscalar and multi-core processor	20%

9. Mapping of CO-PO

SI	CO Description	POs	Bloom's taxonomy domain/level	Delivery methods and activities	Assessment tools
CO1	Introduction to functional units and evaluate the performance of a computing system	a-b	Cognitive/ Evaluate	Lectures, Notes	Mandatory Quiz/ Mid/Final
CO2	Analyze instruction set architecture and different building blocks of processor for designing more efficient processors, VHDL	c-e	Cognitive/ Analyze	Lectures, Notes, Lab	Lab-work
CO3	Design an instruction set architecture and subsystems of central processing unit.	c-g	Cognitive/ Create	Lectures, Notes,	Quiz/ Mid/Final
CO4	Design pipeline architecture, cache memory, integer ALU, floating point ALU, superscalar and multi-core processor	d-g	Cognitive/ Evaluate	Lectures, Notes	Quiz/ Mid/Final

10. Resources: Text Book

No	Name of Author(s)	Year of Publication	Title of Book	Edition	Publisher's Name	ISBN
1.	David A. Patterson, John L. Hennessy	2013	Computer Organization and Design, MIPS Edition: The Hardware/Software Interface	5th	Morgan Kaufmann	ISBN-13: 978-0124077263

Reference book

No	Name of Author(s)	Year of Publication	Title of Book	Edition	Publisher's Name	ISBN
1.	William Stallings	2015	Computer Organization and Architecture	10th Ed.	Pearson Publisher	ISBN-10. 0134101618

11. Weightage Distribution among Assessment Tools

Assessment Tools	Weightage (%)
Attendance	5
Assignment	5
Quiz	15
Mid Term-1	15
Mid Term-2	15
MCQ	10
Final Exam	25
Lab work	10

12. Grading Policy: NSU Standard