ID:	Name:

Brac University

Semester: Summer 2024
Course Code: CSE251
Electronic Devices and Circuits
Section: 01-27

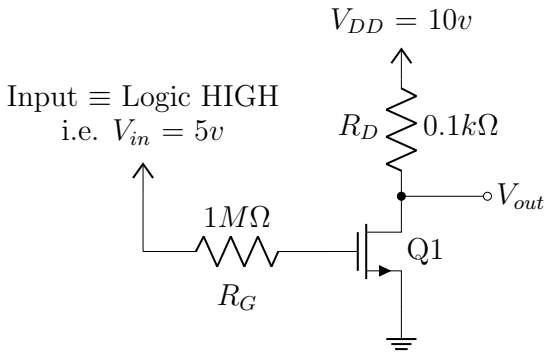
Set **A**

Assessment: *Final Examination*
Duration: 1 hour 40 minutes
Date: 28 September, 2024
Full Marks: 30

Instructions: Answer **any 3 out of 4** questions.

■ Question 1 of 4 *[CO1, CO2, CO3] [10 marks]*

Joy and Nirmol were designing an inverter circuit with MOSFET for their project. Joy designed the following circuit. However, Nirmol said that the designed inverter circuit would malfunction. When they tested the circuit, it malfunctioned. For logic HIGH input, the output was also logic HIGH instead of logic LOW. Nirmol modified the value of R_D to a larger value, and eventually it fixed the issue.



For Input	
Voltage Level	*Logic Level*
$V_{in} = 0v$	LOW i.e. '0'
$V_{in} = 5v$	HIGH i.e. '1'
For Output	
Voltage Level	*Logic Level*
V_{out} >5v	HIGH i.e. '1'
V_{out} <5v	LOW i.e. '0'

MOSFET Equations

Cut-off Mode

$I_{DS} = 0$

Triode Mode

$I_{DS} = k\left[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2\right]$

Saturation Mode

$I_{DS} = \frac{1}{2}kV_{OV}^2$

MOSFET Parameters

$V_T = 1v$, $K = 4mA/v^2$

Inverter Circuit of Joy and It's Corresponding Voltage Level, Logic Level

(a) [CO1] **State** the conditions to verify the assumptions regarding the Saturation Mode of a MOSFET. [1]

(b) [CO2] **Analyze** the circuit shown above and **calculate** the value of V_{out} using the method of assumed states. [3]
You must **validate** your assumption. **Determine** whether Nirmol was correct or not.

(c) [CO2] Nirmol changed the value of R_D to $1k\Omega$. Now, **Analyze** the modified circuit and **calculate** V_{out}. [3]
Determine whether the the inverter was working properly after the modification.

(d) [CO3] **Design** the inverter circuit by choosing a suitable value of R_D such that, the MOSFET operates at the edge of saturation. [Hint: At the edge of saturation, $V_{DS} = V_{OV}$] [3]

■ Question 2 of 4 *[CO1, CO2, CO3] [10 marks]*

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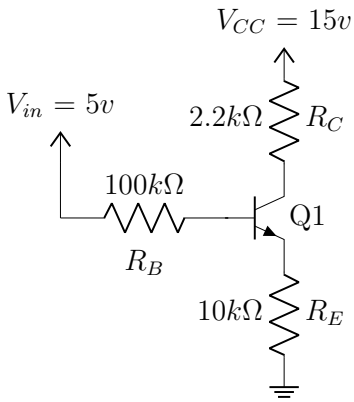
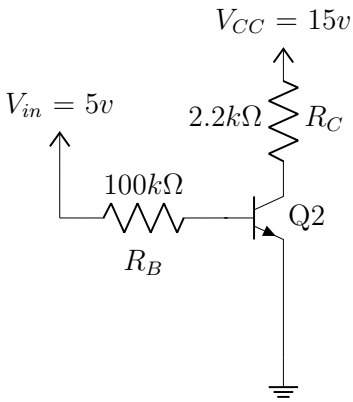


Karim's Circuit



Rahim's Circuit

For Both BJTs

$\beta = 100$

$V_{BE(Active)} = 0.7v$

$V_{BE(Saturation)} = 0.8v$

$V_{CE(Saturation)} = 0.2v$

Karim designed a BJT circuit. When his friend Rahim saw it, he claimed that the BJT would operate in the Active mode. Then Rahim built a circuit and asked Karim to figure out the operating mode the BJT.

(a) [CO1] What is the S-model of a BJT? **Explain** briefly with the I-V characteristics graph. [2]

(b) [CO2] **Calculate** I_B, I_C, I_E, V_{CE} in Karim's circuit and **determine** whether Rahim was correct or not. [4]

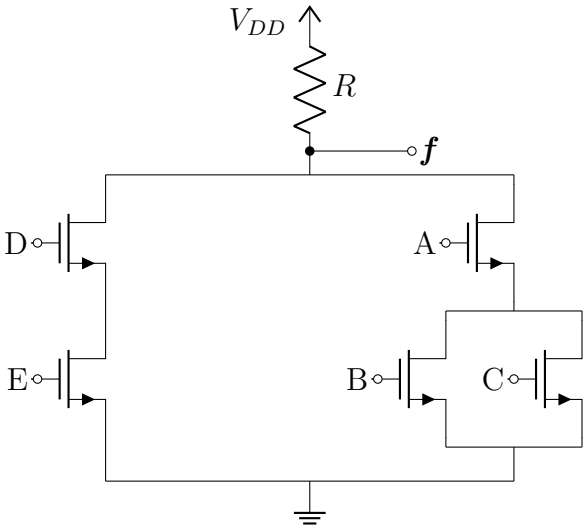
(c) [CO2] **Analyze** Rahim's circuit and **Calculate** I_B, I_C, I_E, V_{CE} to help Karim determine the operating state of the BJT. [4]

■ Question 3 of 4 *[CO1, CO2, CO3] [10 marks]*

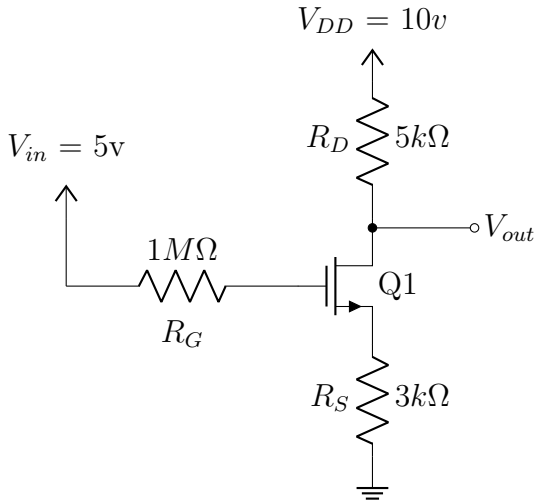
(a) [CO1] **Determine** the logic function, $\boldsymbol{f}$ in 'Circuit-A' for the boolean inputs A, B, C , D and E. [2]

(b) [CO2] **Analyze** 'Circuit-B' and **calculate** I_{DS} and V_{out} using method of assumed states. You must **validate** your assumptions. Here, $V_T = 1v$ and $K = 2mA/v^2$. [4]

(c) [CO3] **Implement** the following logic functions using MOSFETs where A, B, C, D, E are boolean inputs. [4]
(i) f = $\overline{A.B.C + D.E}$ (ii) g = $A.B.(C + D)$



Circuit-A



Circuit-B

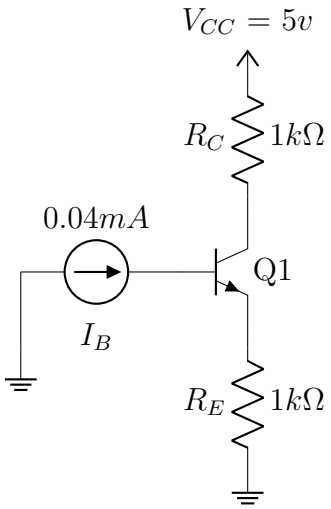
■ Question 4 of 4 *[CO1, CO2, CO3] [10 marks]*

(a) [CO1] **Draw** the I-V characteristics graph of a BJT. **Label** the graph properly. [2]

(b) [CO2] **Analyze** 'Circuit-C' and **calculate** I_B, I_C, I_E, V_{CE} using method of assumed states. You must **validate** your assumptions. [4]

(c) [CO3] For 'Circuit-C', the operating state of the BJT found in part-B can be changed by changing the value of V_{CC}. **Determine** how should you change the value of V_{CC} to change the operating state of the BJT found in part-B. **Show** necessary calculation. [2]

(d) [CO3] **Implement** the logic function, f = $\overline{A + B.C + D}$ using BJTs where A, B, C, D are boolean inputs. [2]



BJT Parameters
$\beta = 90$
$V_{BE(Active)} = 0.7v$
$V_{BE(Saturation)} = 0.8v$
$V_{CE(Saturation)} = 0.2v$

Circuit-C