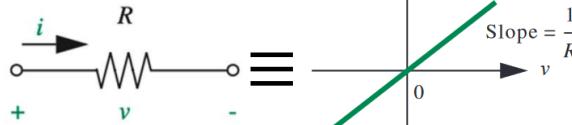


Lecture 6: MOSFETS

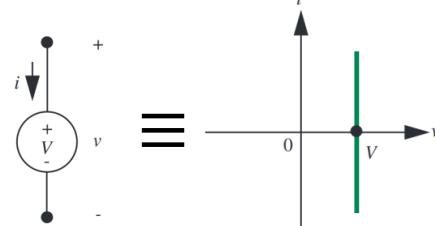
Two terminal Devices

Linear Devices

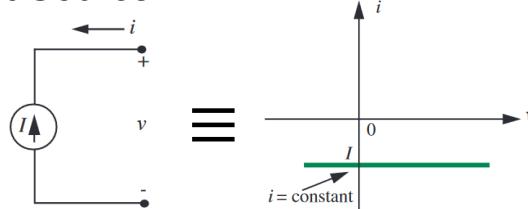
Resistor



Voltage Source



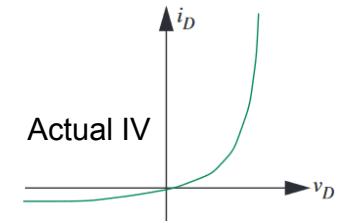
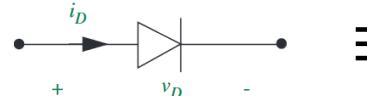
Current Source



IV characteristics of two terminal devices are fixed.

Non-linear Devices

Diode



PWL: Piecewise Linear



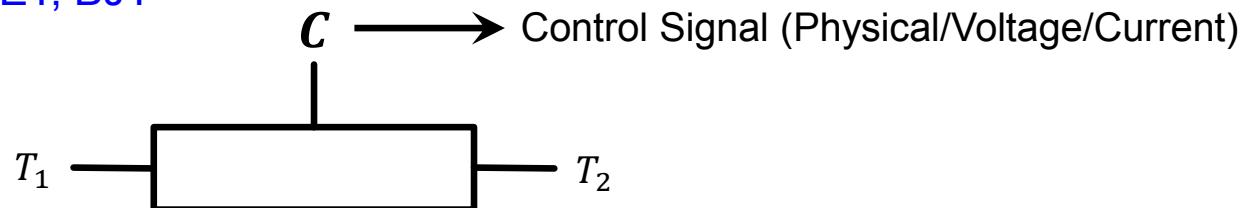
IV characteristics of **three terminal devices** can be changed

Three terminal Devices

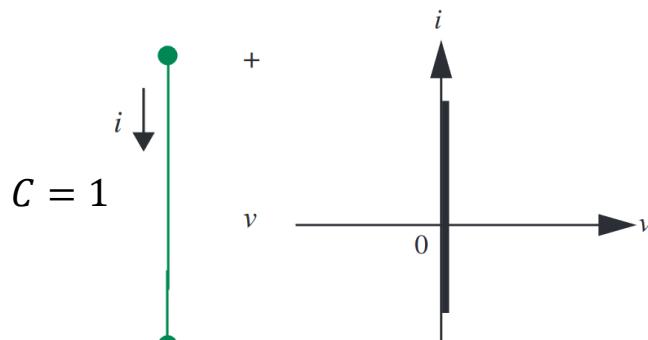
IV of two terminal can be controlled using a third terminal.

Example: Switch, MOSFET, BJT

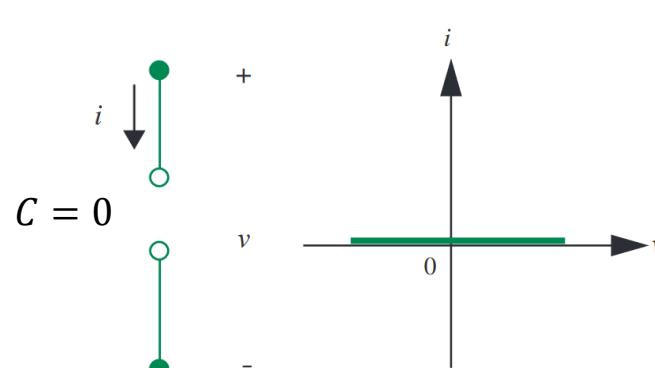
Switch



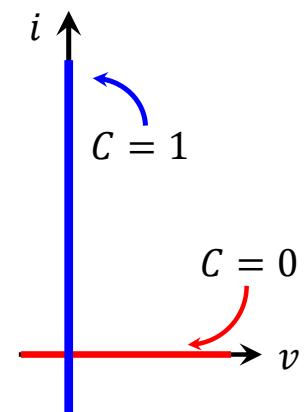
IV characteristics between T_1 and T_2 can be controlled by C



Switch **ON**

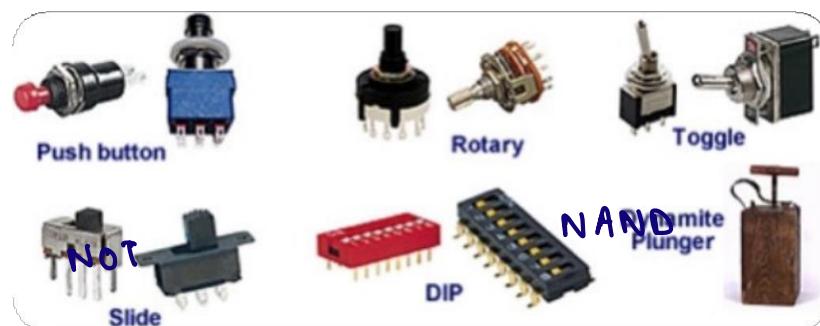


Switch **OFF**

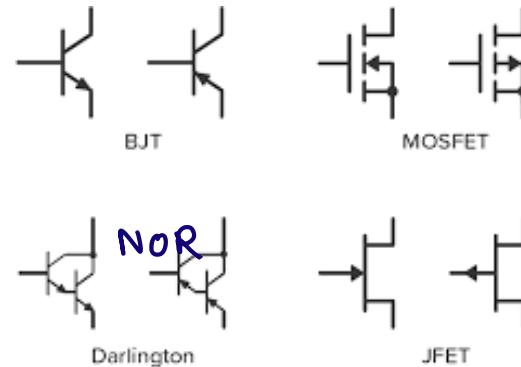


Switch – Types

- Depending on the control, the switch can be
 - **Analog:** Controlled using physical toggle/button
 - **Digital:** Controlled using voltage or current. Example – MOSFET (voltage controlled), BJT (current controlled)



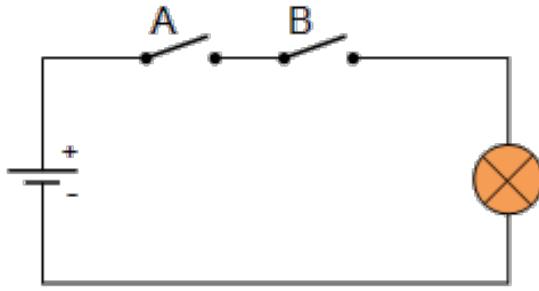
Analog switches



Digital switches (Transistors)

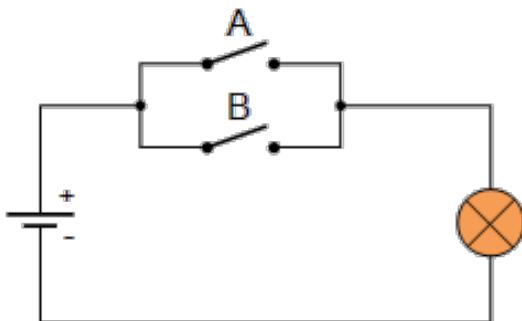
Switch Application – Logic Gates

- We can use switches to build logic gates



A	B	Bulb
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

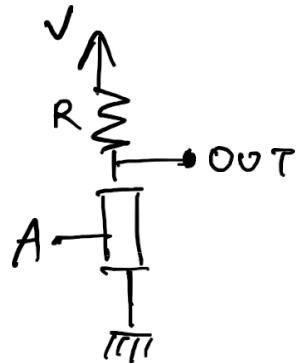
AND operation



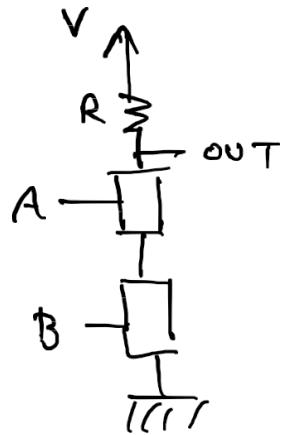
A	B	Bulb
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

OR operation

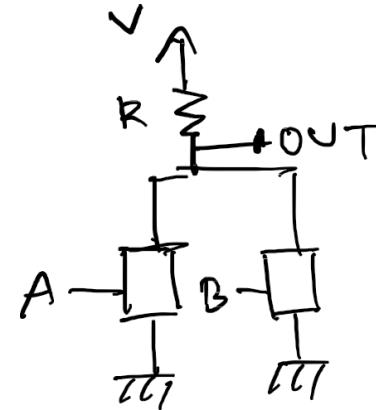
Switch Application – Logic Gates



$$OUT = \overline{A}$$



$$OUT = \overline{AB}$$



$$OUT = \overline{A+B}$$

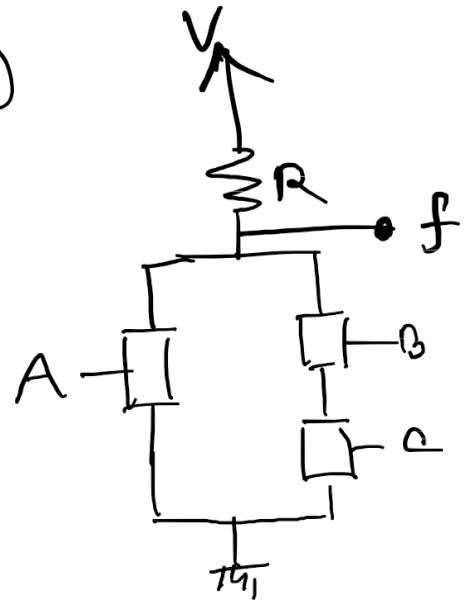
<i>A</i>	<i>V_{out}</i>
0	5V
1	0V

<i>A</i>	<i>B</i>	<i>V_{out}</i>
0	0	5V
0	1	5V
1	0	5V
1	1	0V

<i>A</i>	<i>B</i>	<i>V_{out}</i>
0	0	5V
0	1	0V
1	0	0V
1	1	0V

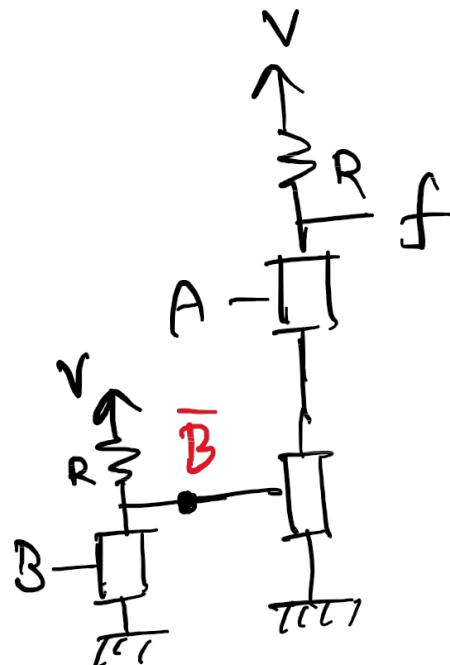
Examples

①



$$f = \overline{A + B.C}$$

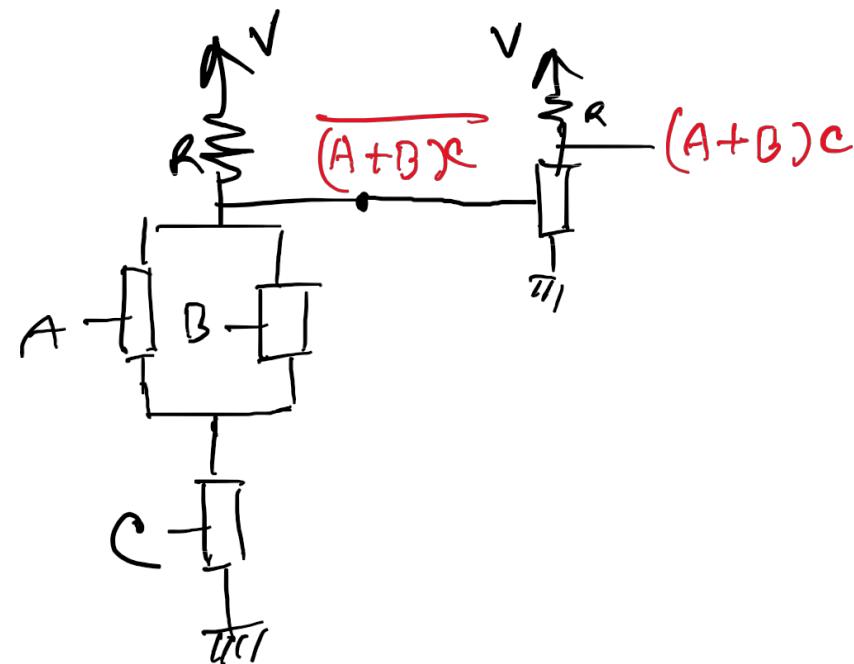
②



$$f = \overline{A\bar{B}}$$

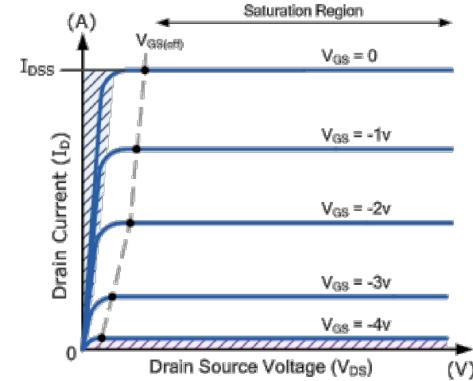
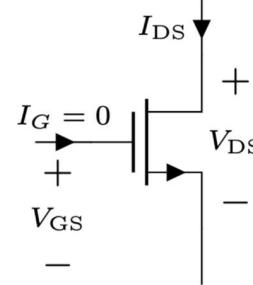
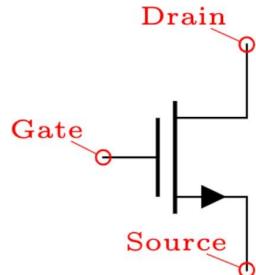
Example

Implement using switches: $f = (A + B)C$



Transistors as Digital Switch

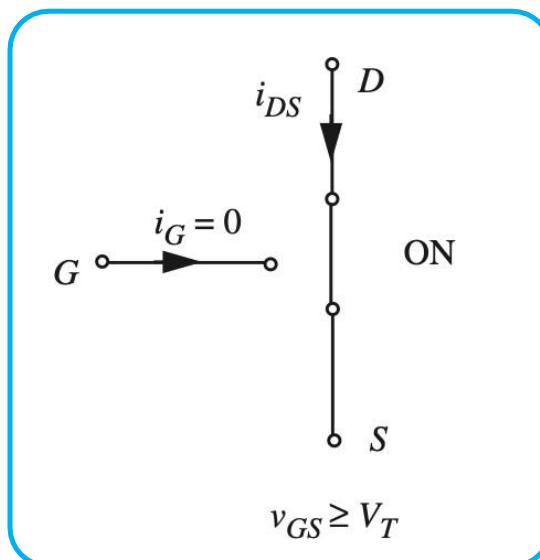
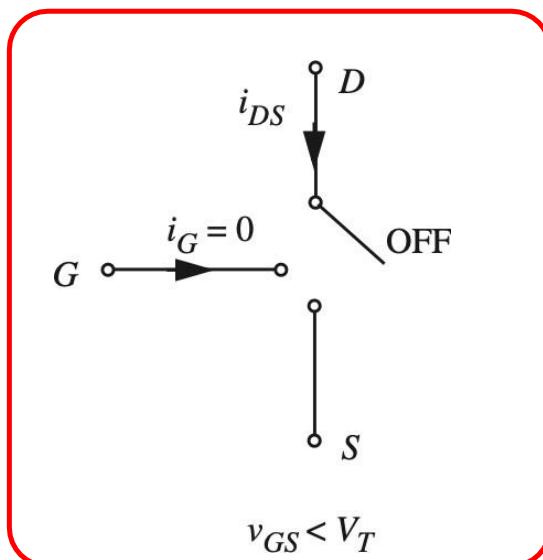
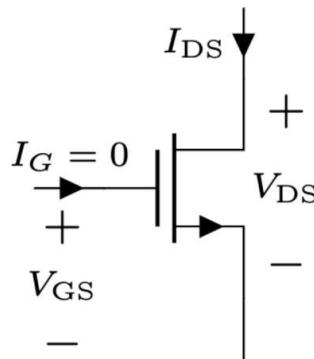
- Transistors are 3 terminal non-linear devices, can be used as switch
- 2 types – **Voltage Controlled**, **Current Controlled**
- Metal Oxide Semiconductor Field Effect Transistor (**MOSFET**) are **voltage controlled**
- Control, $C = V_{GS}$. The IV characteristics (I_{DS} vs V_{DS}) depends on V_{GS}
- Actual dependency is complex.
- Will start with a simple (but approximate) one – **S-Model** (Switch Model)



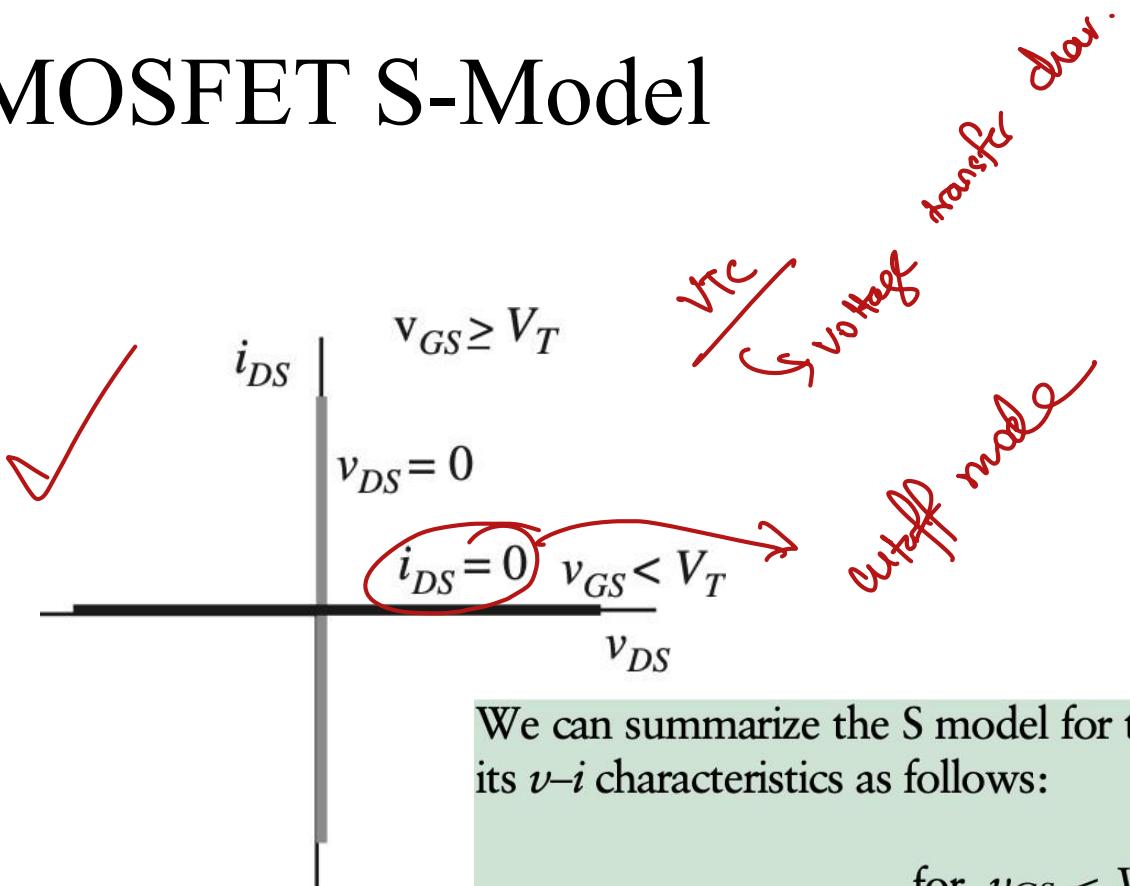
MOSFET S-Model

- The MOSFET (approximately) behaves like a switch

- $C = V_{GS}$. Here, $C = "0" \Rightarrow V_{GS} < V_T$, and $C = "1" \Rightarrow V_{GS} \geq V_T$



MOSFET S-Model



Switch

on \rightarrow satⁿ

off \rightarrow cut off

We can summarize the S model for the MOSFET in algebraic form by stating its $v-i$ characteristics as follows:

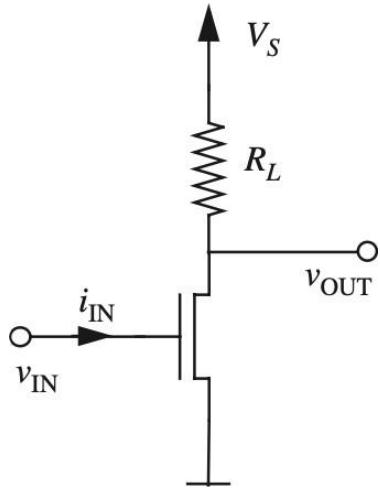
$$\text{for } v_{GS} < V_T, \quad i_{DS} = 0$$

and

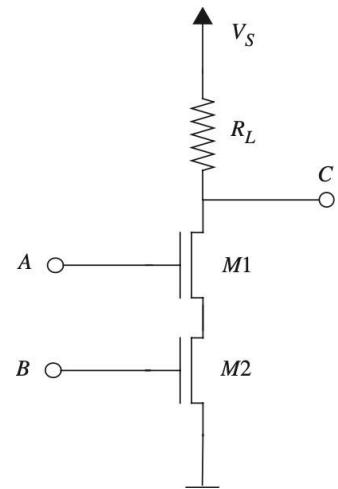
$$\text{for } v_{GS} \geq V_T, \quad v_{DS} = 0 \quad (6.2)$$

Logic Gates using MOSFET

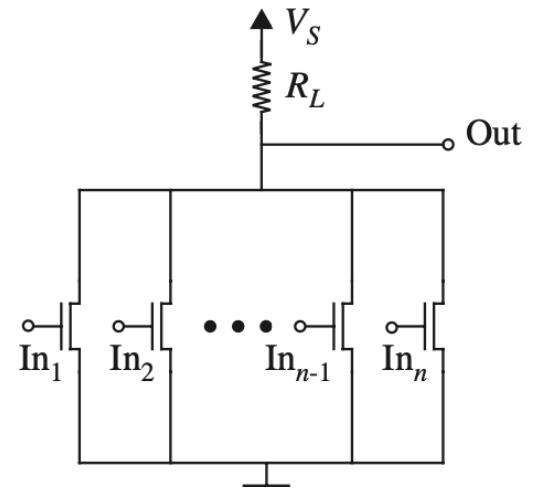
Just replace the switches with MOSFETs!



NOT Gate (Inverter)

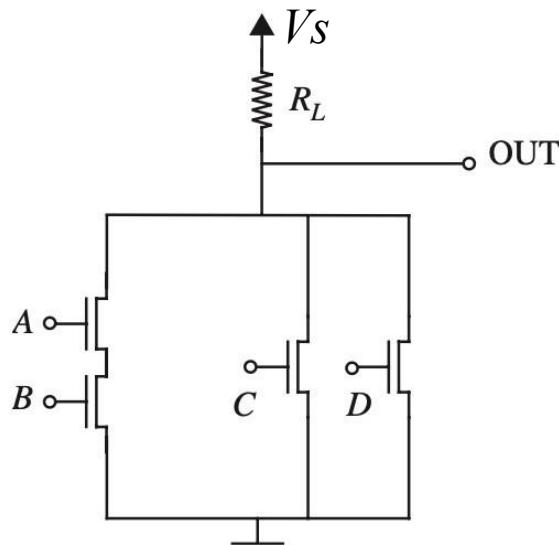


NAND Gate (Inverter)

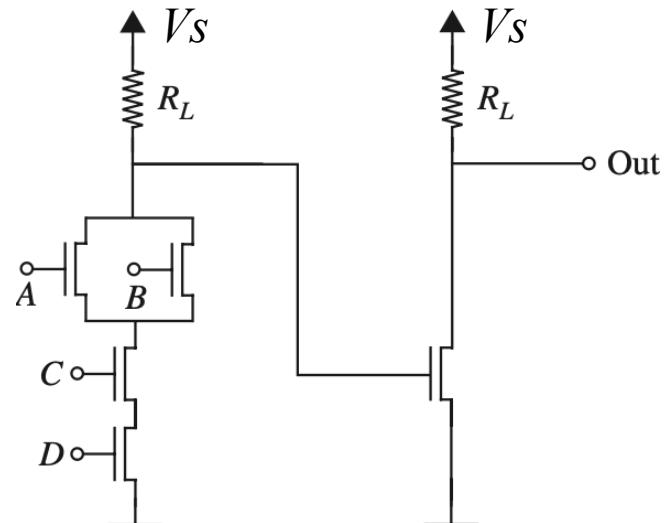


NOR Gate (Inverter)

MOSFET Logic Gates – More Examples



$$OUT = \overline{AB + C + D}$$



$$Out = \overline{\overline{(A + B)CD}} = (A + B)CD$$

Practice Problem 2

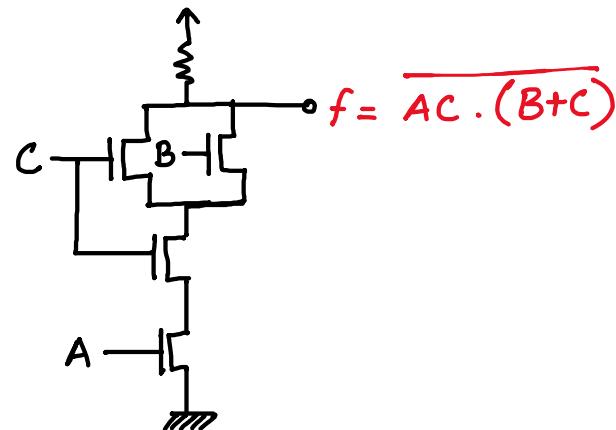
- **Design** a circuit using ideal MOSFETs (S-model) to implement the logic function

$$f = \overline{AC} + \overline{(B + C)}$$

$$= \overline{\overline{AC}} + \overline{\overline{(B + C)}}$$

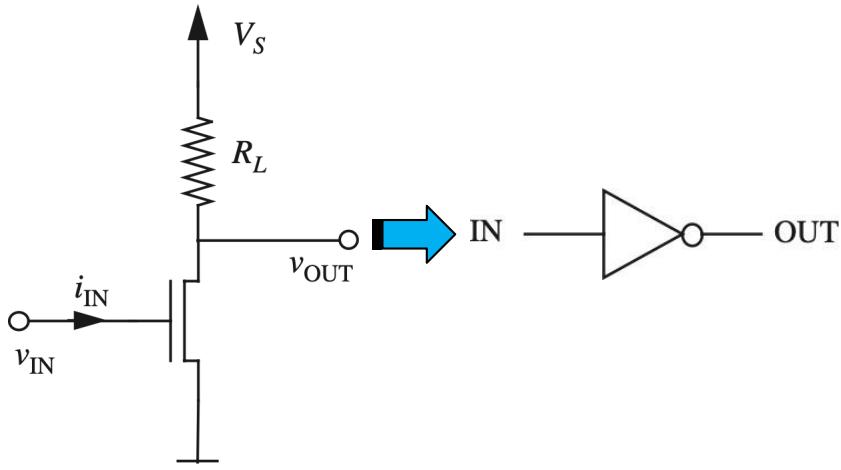
$$= \overline{\overline{AC}} \cdot \overline{\overline{(B + C)}} \quad [\text{De Morgan's Theorem}]$$

$$= \overline{AC} \cdot (B + C)$$

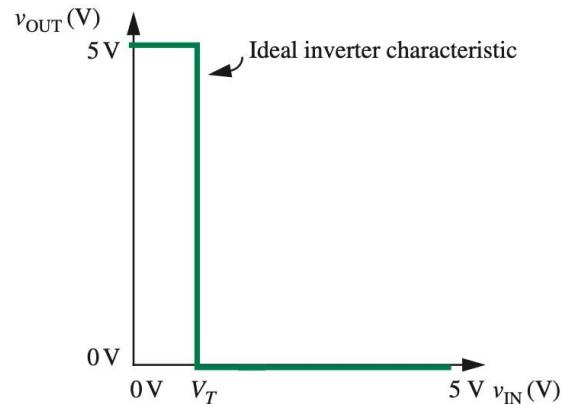


Voltage Transfer Characteristics (VTC)

- **Reminder:** VTC is a graph where x -axis = input voltage, y -axis = output voltage
- **Why?** Design logic gates to follow a given static discipline

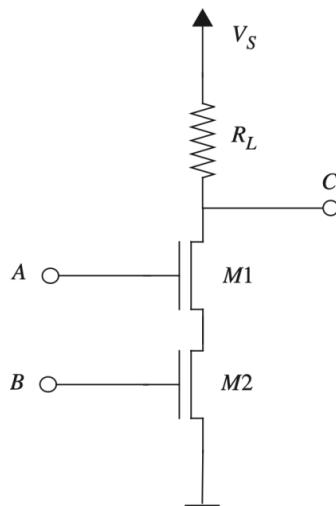


When $v_{IN} < V_T$ (Logical 0) $v_{OUT} = V_S = 5 \text{ V}$ (Logical 1)
When $v_{IN} \geq V_T$ (Logical 1) $v_{OUT} = 0 \text{ V}$ (Logical 0)

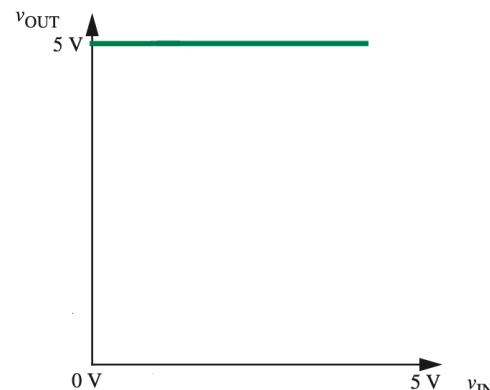


VTC of NAND gate

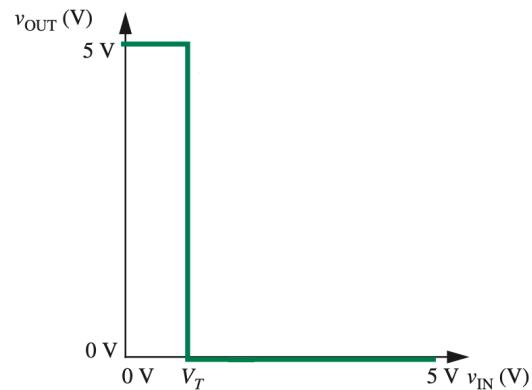
- We only have one x –axis, but two inputs
- **Solution:** Draw two VTC, one considering $V_A = 0$ one considering $V_A = 1$



When $V_A = 0$



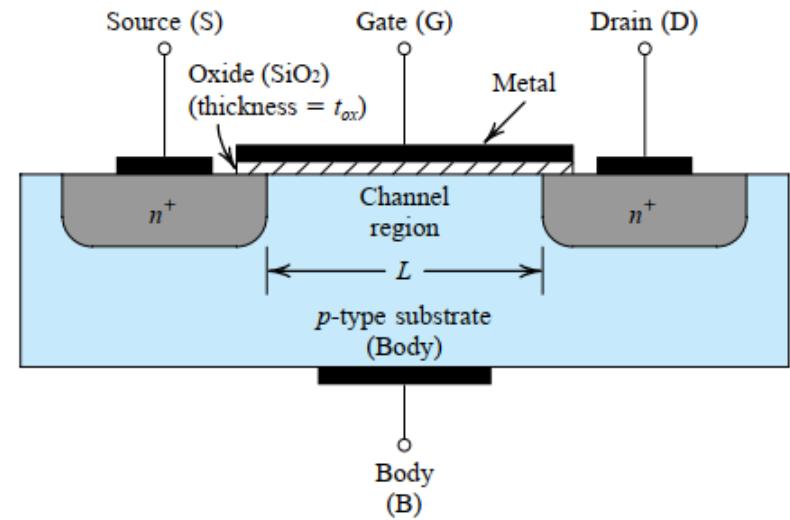
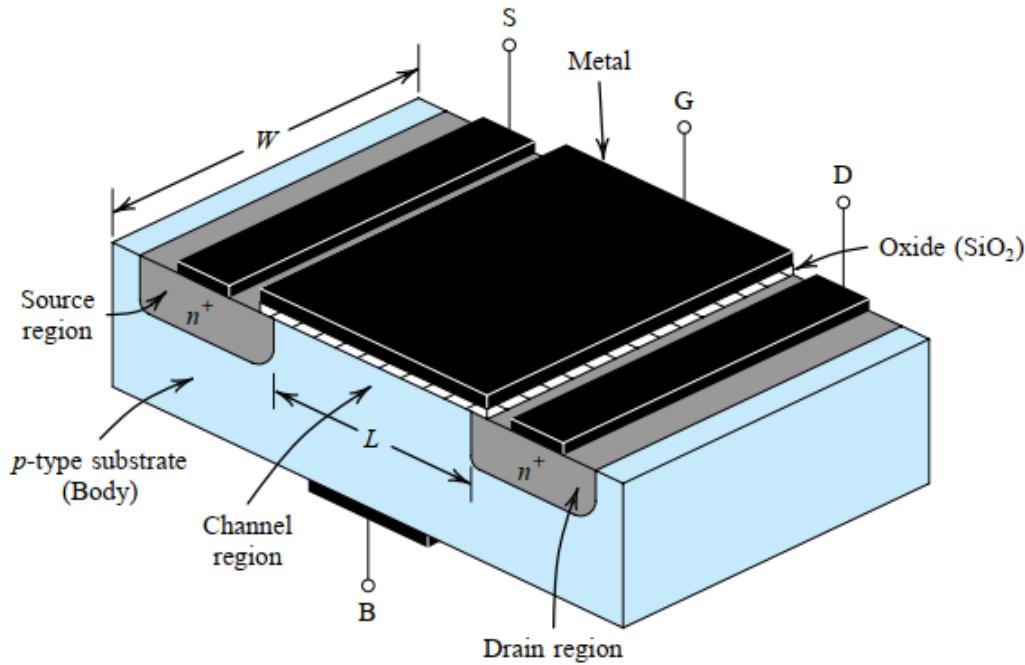
When $V_A = 1$



Homework: Find VTC for NOR gate

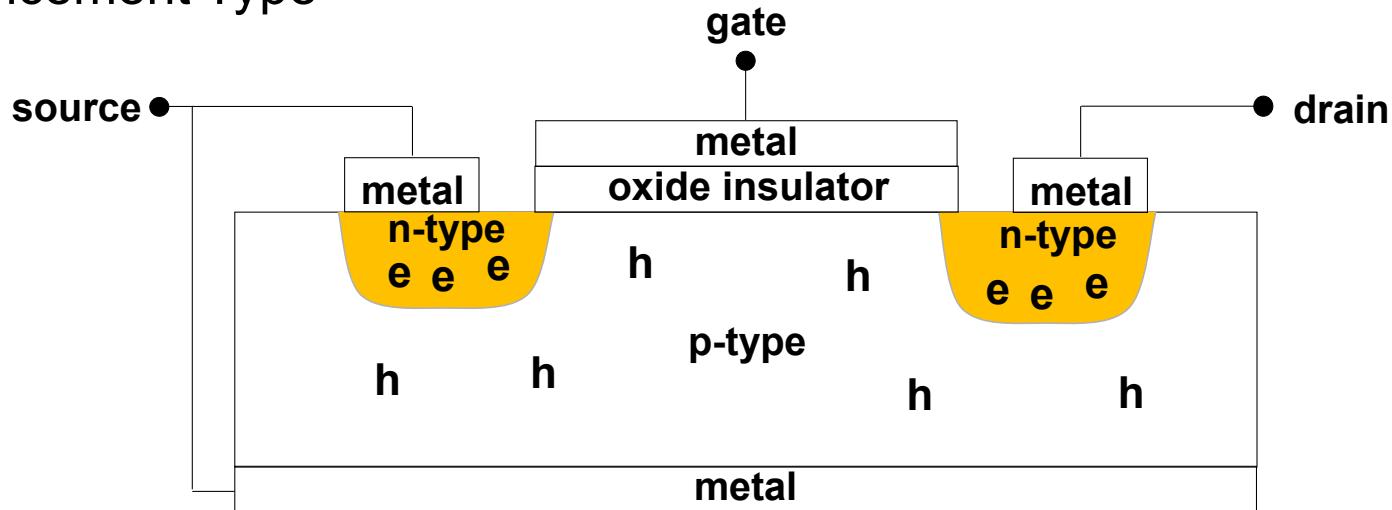
Real MOSFET – Enhancement Type

Device Structure (*n*-channel MOSFET)

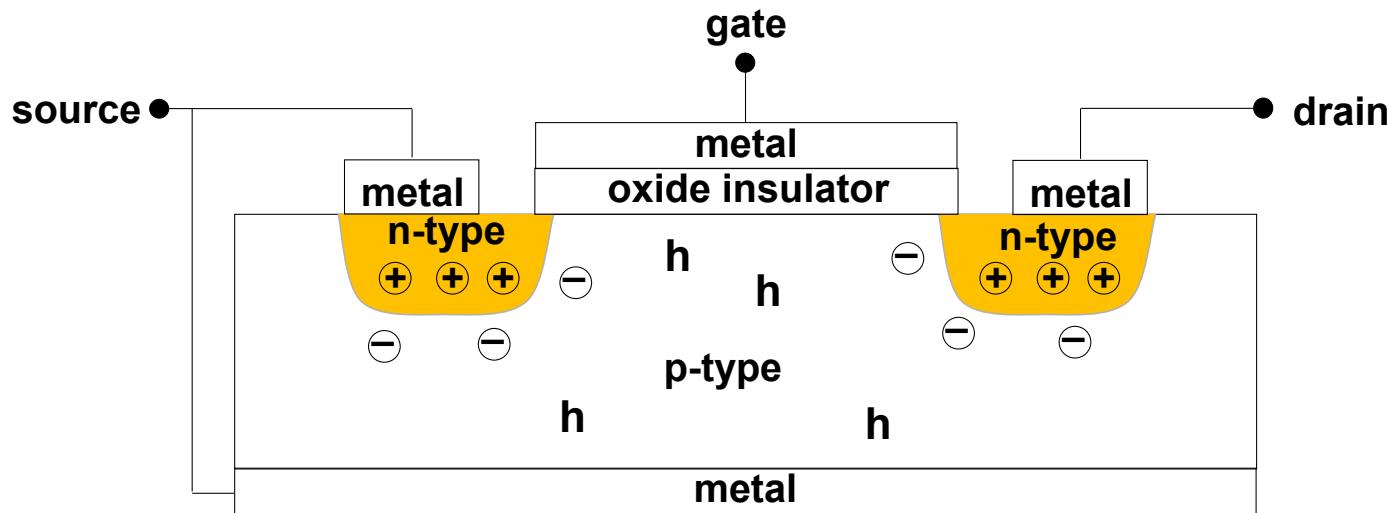


***n*-channel MOSFET (NMOS) Physical Structure**

Enhancement Type



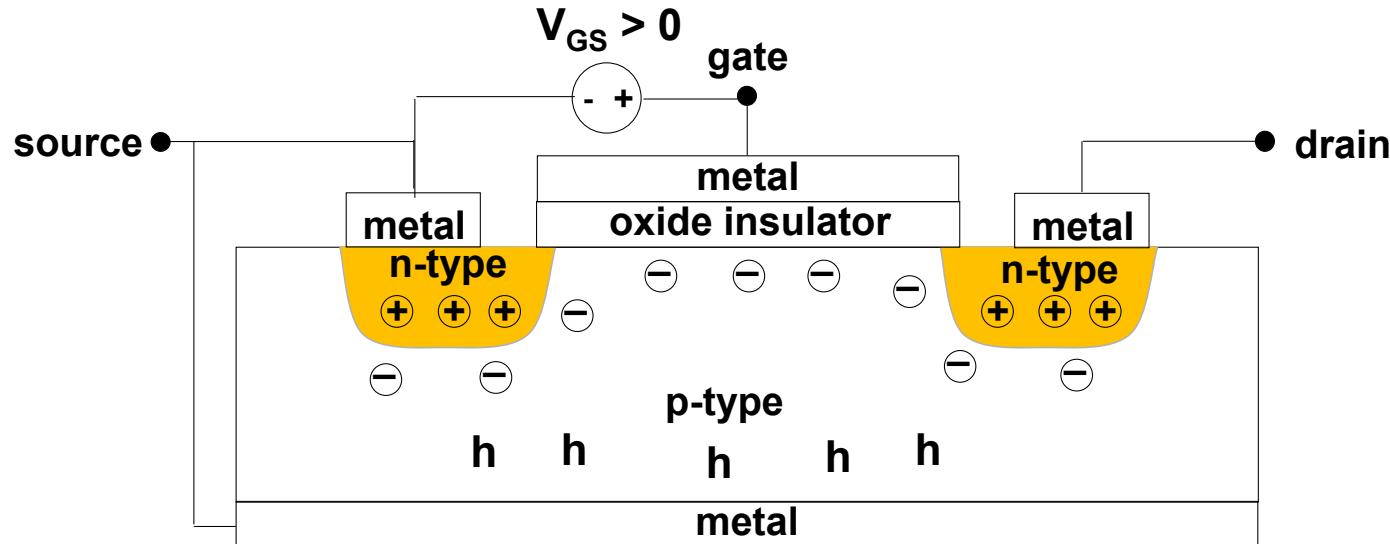
NMOS in Equilibrium



When the transistor is left alone, some electrons from the n-type wells diffuse into the p-type material to fill holes.

This creates negative ions in the p-type material and positive ions are left behind in the n-type material.

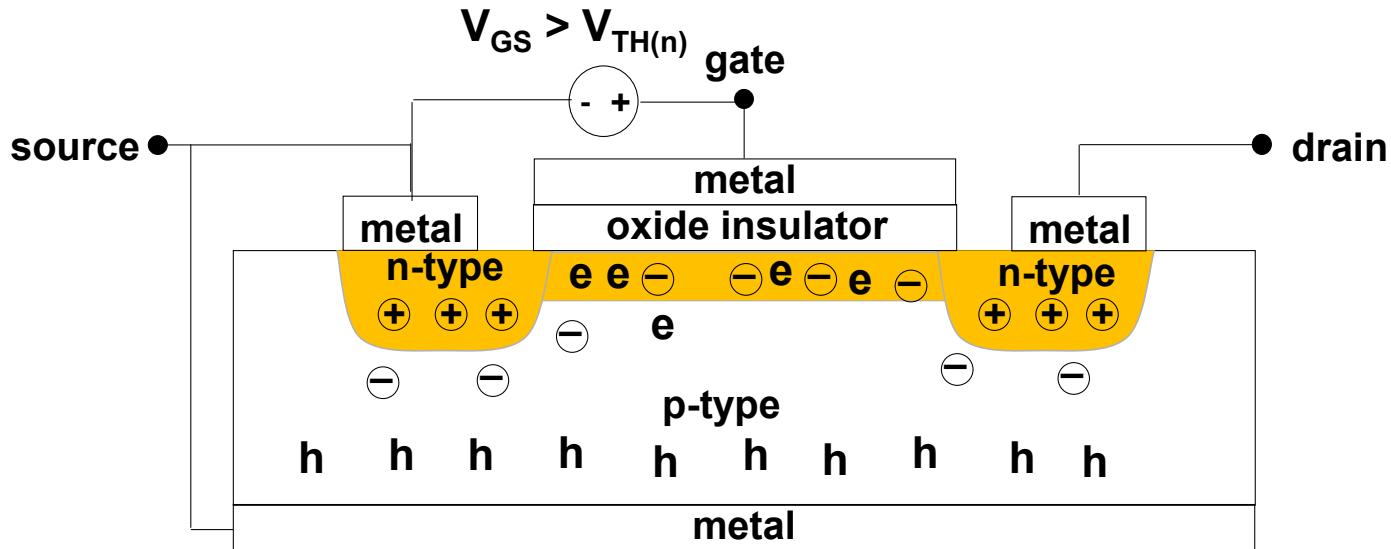
NMOS in Cutoff



When a small, positive V_{GS} is applied, holes “move away” from the gate.

Electrons from complete atoms elsewhere in the p-type material move to fill holes near the gate instead.

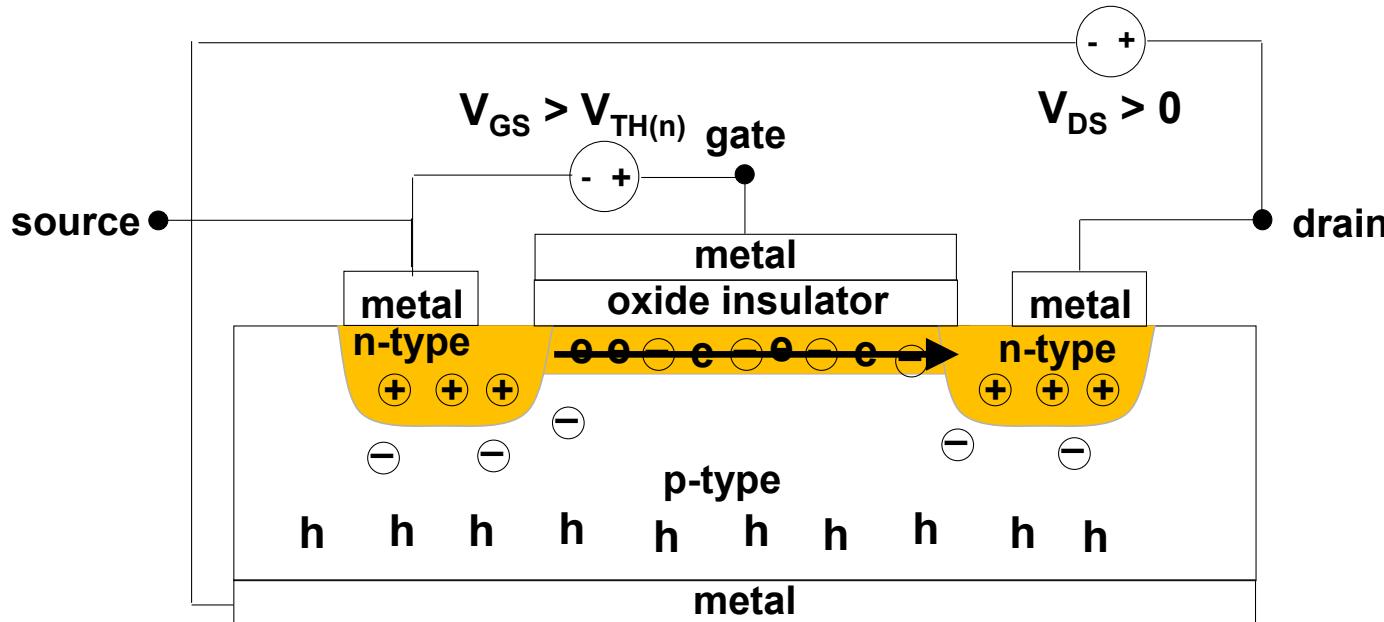
NMOS Transistor channel



When V_{GS} is larger than a **threshold** voltage $V_{TH(n)}$, the attraction to the gate is so great that free electrons collect there.

The applied V_{GS} creates an **induced n-type channel** under the gate (an area with free electrons).

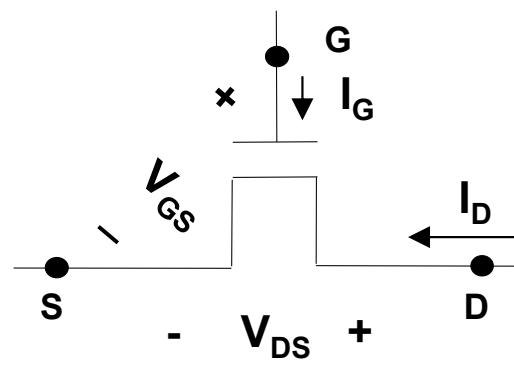
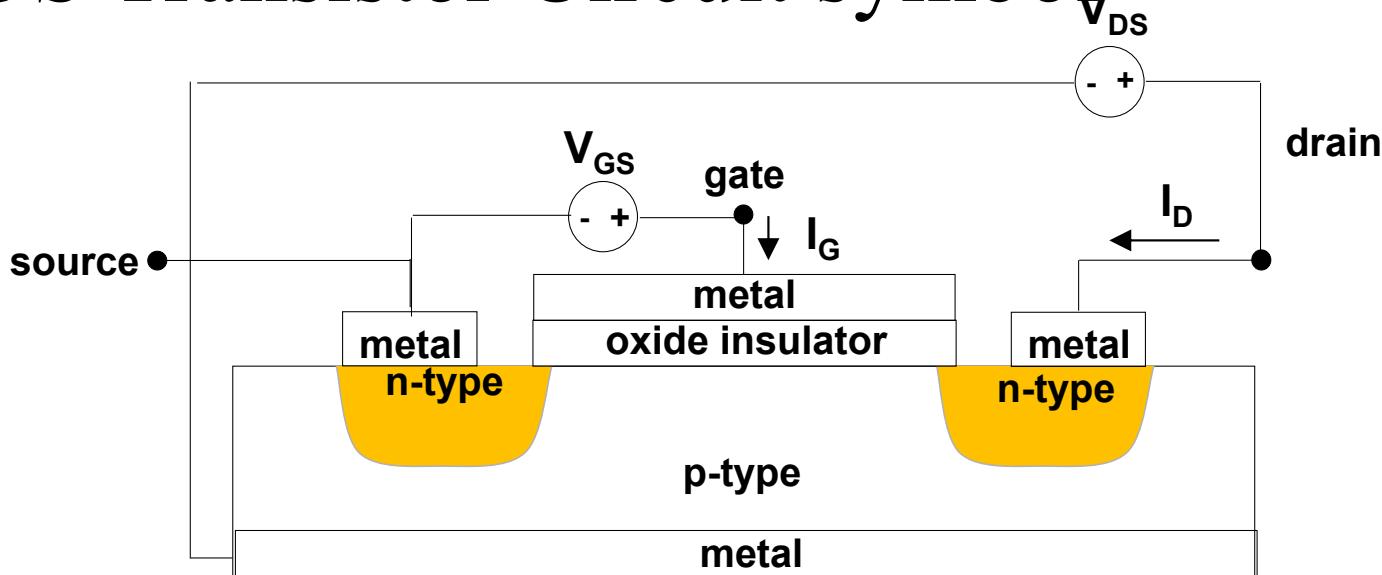
NMOS Transistor Drain Current



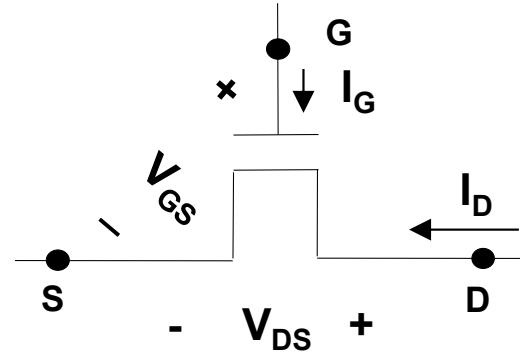
When a positive V_{DS} is applied, the free electrons flow from the source to the drain. (Positive current flows from drain to source).

The amount of current depends on V_{DS} , as well as the number of electrons in the channel, channel dimensions, and material.

NMOS Transistor Circuit symbol

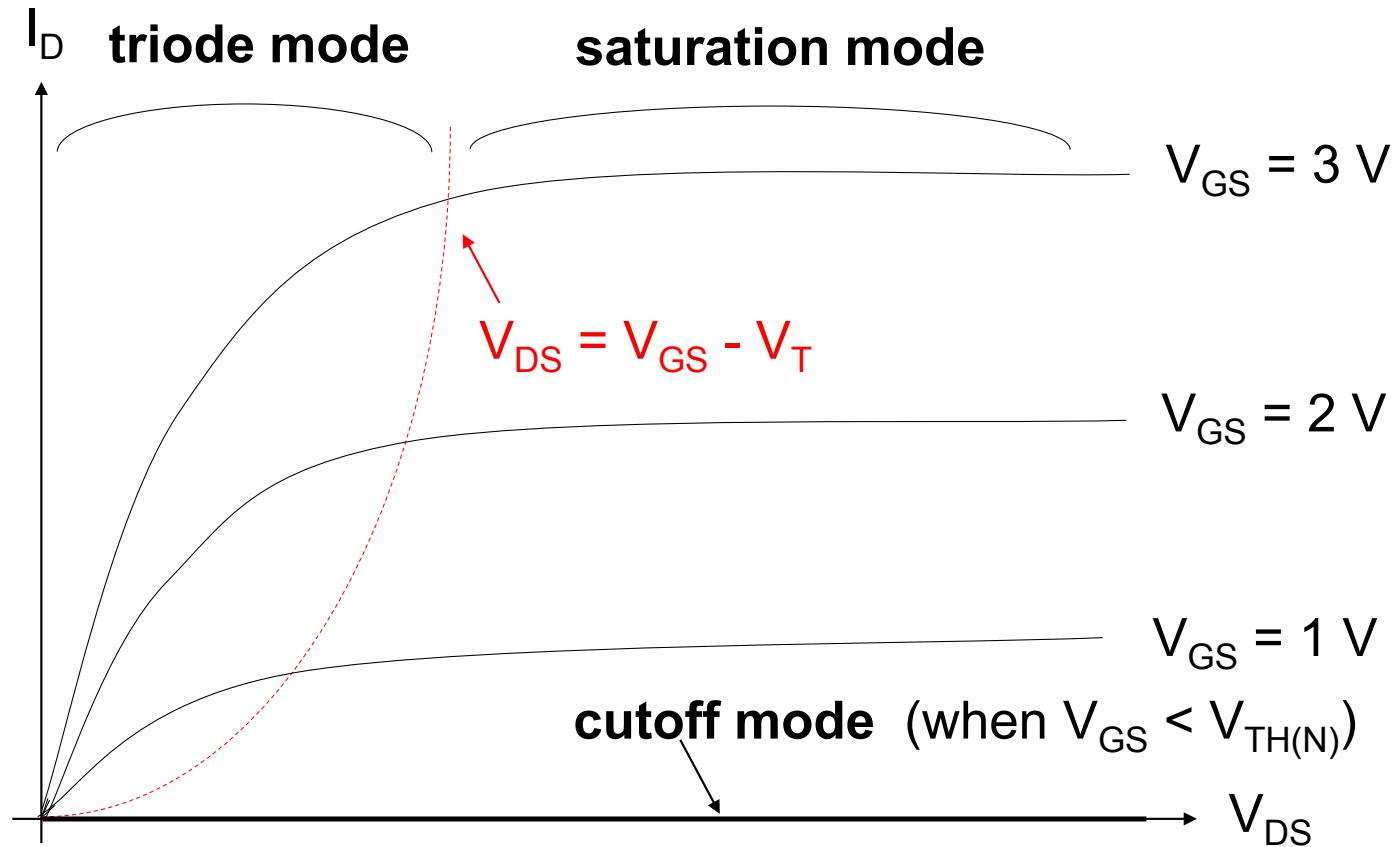


NMOS I-V Characteristic



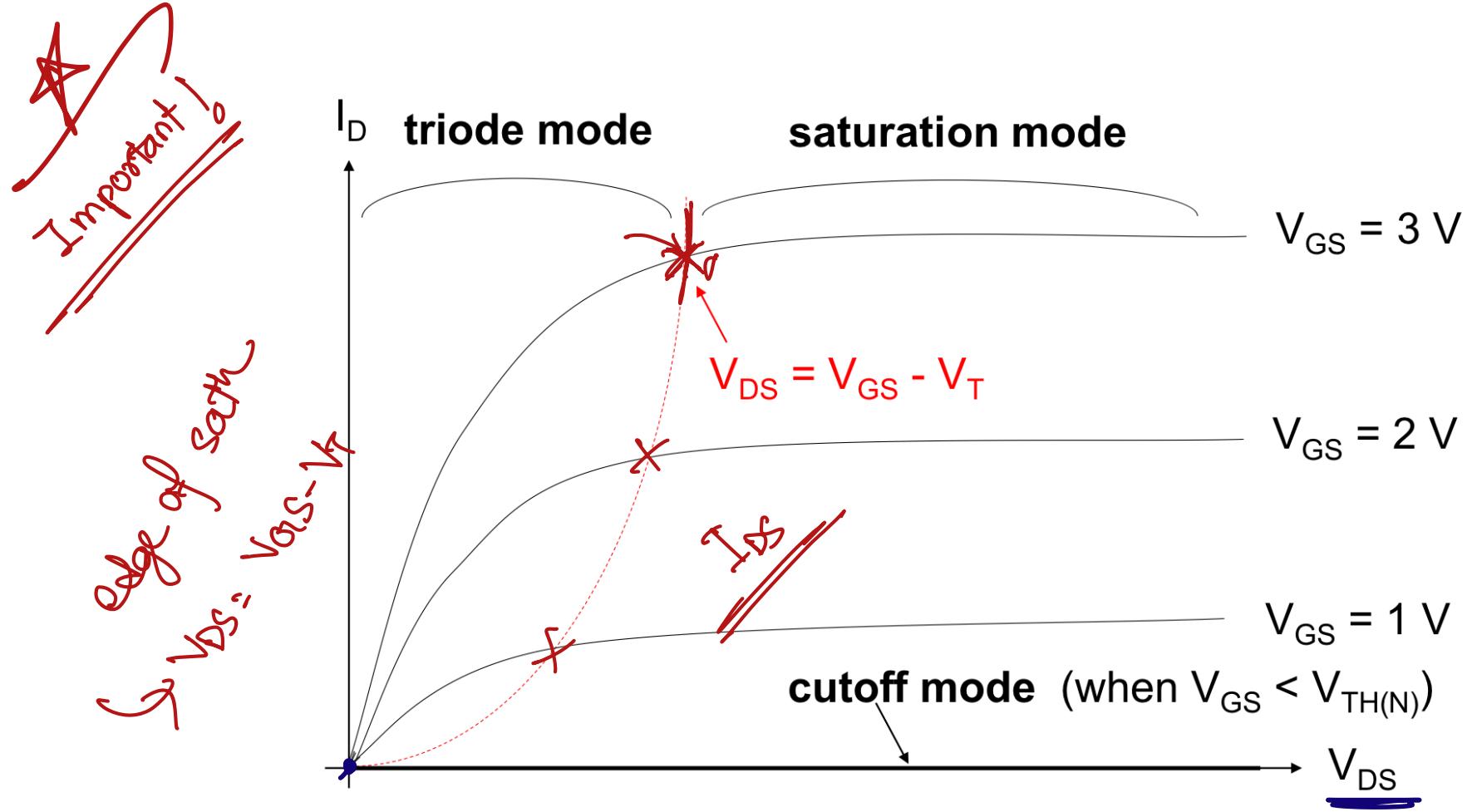
- Since the transistor is a 3-terminal device, there is no single I-V characteristic.
- Note that because of the insulator, $I_G = 0 \text{ A}$.
- We typically define the MOS I-V characteristic as I_D vs. V_{DS} for a fixed V_{GS} .
- The I-V characteristic changes as V_{GS} changes.

NMOS I-V Characteristic



Modes of Operation

- For small values of V_{GS} , $V_{GS} \leq V_{TH(n)}$, the n-type channel is not formed. No current flows. This is **cutoff mode**.
- When $V_{GS} > V_{TH(n)}$, current I_D may flow from drain to source, and the following modes of current flow are possible.
 - The mode of current flow depends on the propelling voltage, V_{DS} , and the channel-inducing voltage,
 $V_{GS} - V_{TH(n)}$.
 - When $V_{DS} < V_{GS} - V_{TH(n)}$, current is starting to flow. I_D increases rapidly with increased V_{DS} . This is **triode mode**.
 - When $V_{DS} \geq V_{GS} - V_{TH(n)}$, current is reaching its maximum value. I_D does not increase much with increased V_{DS} . This is called **saturation mode**.



Cutoff Mode

Occurs when $v_{GS} < V_T$

$$I_D = 0$$

Triode Mode

Occurs when $v_{GS} \geq V_T$ and $v_{DS} < v_{GS} - V_T$

$$\checkmark I_{DS} = k'_n \frac{W}{L} \left(v_{GS} - V_T - \frac{1}{2} v_{DS} \right) v_{DS}$$

$v_{GS} - V_T = V_{OV}$: Overdrive Voltage

V_{OV}
Indicates the available excess voltage at **gate** after forming the n-channel.

Mode	Condition	Equation
Cutoff	$V_{GS} < V_T$	$I_D = 0$
Triode	$V_{GS} \geq V_T$ $V_{DS} < V_{OV}$	$I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$
Saturation	$V_{GS} \geq V_T$ $V_{DS} \geq V_{OV}$	$I_D = \frac{k}{2}V_{OV}^2$

Saturation Mode

Occurs when $v_{GS} > V_T$ and $v_{DS} \geq v_{GS} - V_T$

$$\checkmark I_{DS} = \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_T)^2$$

V_T
The minimum voltage necessary at the **gate** terminal to form a channel.

$$V_{GS} - V_T = V_{OV}$$

$$k_n = \frac{k'_n W}{L} \approx \mu_n C_o x \frac{W}{L}$$

Real MOSFET

$$k_n = k'_n \frac{W}{L}$$

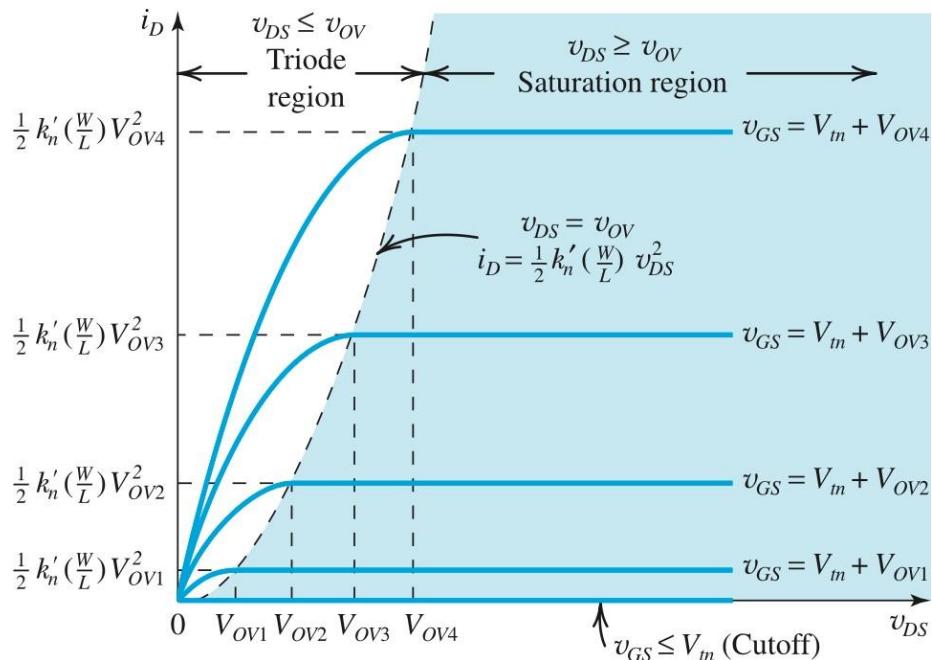
MOSFET transconductance

v_{GS} :  Gate Voltage
 v_{DS} :  Drain to Source Voltage

V_T : Threshold Voltage

$V_{ov} = v_{GS} - V_T$: Overdrive voltage

IV Characteristics of Real MOSFET



Mode	Condition	Equation
Cutoff	$V_{GS} < V_T$	$I_D = 0$
Triode	$V_{GS} \geq V_T$ $V_{DS} < V_{OV}$	$I_D = k [V_{OV} V_{DS} - \frac{1}{2} V_{DS}^2]$
Saturation	$V_{GS} \geq V_T$ $V_{DS} \geq V_{OV}$	$I_D = \frac{k}{2} V_{OV}^2$

$$V_{GS} - V_T = V_{OV}$$

$$k_n = \frac{k'_n W}{L}$$

~~Solving~~ circuits : Method of Assumed State

① Assumed:

Cutoff

1. V_A, V_D, V_S

2. $V_{DS}, V_{OV}, I_D,$

V_{DS}

② find

Triode

1. V_A, V_D, V_S

2. $V_{DS}, V_{OV}, I_D,$

V_{DS}

Saturation

1. V_A, V_D, V_S

2. $V_{DS}, V_{OV}, I_D,$
 V_{DS}

③ Validate

$V_{DS} < V_T$

$V_{DS} > V_T$

$V_{DS} > V_T$

$V_{DS} < V_{OV}$

$V_{DS} > V_{OV}$

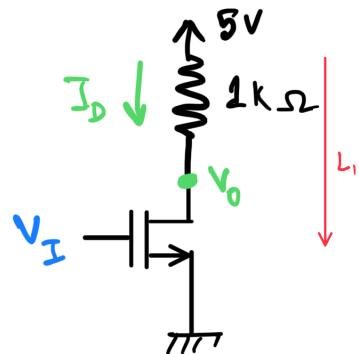
④ If validation wrong \rightarrow repeat 1, 2, 3 with new assumed state.

- Might need to solve quadratic equation ($ax^2 + bx + c = 0$).
- If we get two roots, choose the one that's favorable to your assumption

→ triode: $V_{DS} = \text{small}$

satn: $V_{DS} = \text{large}$

Example 1



The MOSFET is specified as $V_T = 1V$ and $k = 0.5 \text{ mA/V}^2$. Find I_D and V_o for $V_I = 2V$.

Solution:

Step 1: Assume the MOSFET in **saturation**

Step 2: $I_D = \frac{k}{2} V_{OV}^2$ Here, $V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 2V$
Therefore, $V_{OV} = V_{GS} - V_T = 2 - 1 = 1V$

$$\therefore I_D = \frac{0.5}{2} (1)^2 = 0.25 \text{ mA}$$

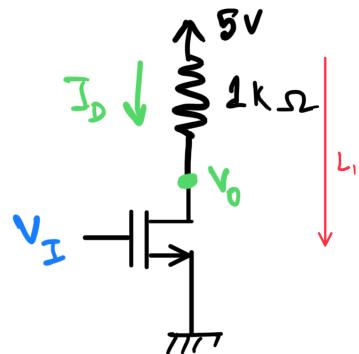
$$\text{Again, } V_{DS} = V_D - V_S = V_D - 0 = V_D = V_o$$

$$\begin{aligned} \text{KVL along } L_1: I_D \times 1k\Omega + V_o &= 5 - 0 \Rightarrow V_o = 5 - I_D \times 1k\Omega \\ \Rightarrow V_o &= 5 - 0.25 \times 1 = 4.75 \text{ V} = V_{DS} \end{aligned}$$

Step 3: $V_{GS} = 2V > V_T$ ✓ Therefore, **assumption correct!**

$V_{DS} = 1V > V_{OV}$ ✓ Correct ans: $I_D = 0.25 \text{ mA}, V_o = 4.75 \text{ V}$

Example 2



The MOSFET is specified as $V_T = 1V$ and $k = 0.5 \text{ mA/V}^2$. Find I_D and V_O for $V_I = 5V$.

Solution:

Step 1: Assume the MOSFET in **saturation**

Step 2: $I_D = \frac{k}{2} V_{OV}^2$ Here, $V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 5V$
Therefore, $V_{OV} = V_{GS} - V_T = 5 - 1 = 4V$

$$\therefore I_D = \frac{0.5}{2} (4)^2 = 4 \text{ mA}$$

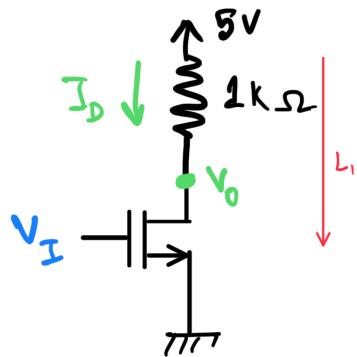
$$\text{Again, } V_{DS} = V_D - V_S = V_D - 0 = V_D = V_o$$

$$\begin{aligned} \text{KVL along } L_1: I_D \times 1k\Omega + V_o &= 5 - 0 \Rightarrow V_o = 5 - I_D \times 1k\Omega \\ \Rightarrow V_o &= 5 - 4 \times 1 = 1 \text{ V} = V_{DS} \end{aligned}$$

Step 3: $V_{GS} = 5V > V_T$ ✓ Therefore, **assumption wrong!**

$$V_{DS} = 1V \not> V_{OV} \times$$

Example 2



The MOSFET is specified as $V_T = 1V$ and $k = 0.5 \text{ mA/V}^2$. Find I_D and V_o for $V_I = 5V$.

Repeat:

Step 1: Assume the MOSFET in **triode**

$$\text{Step 2: } I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$\text{Here, } V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 5V$$

$$\text{Therefore, } V_{OV} = V_{GS} - V_T = 5 - 1 = 4V$$

$$\text{Again, } V_{DS} = V_D - V_S = V_D - 0 = V_D = V_o. \text{ Assuming } V_{DS} = x$$

$$\text{KVL along } L_1: I_D \times 1k\Omega + V_o = 5 - 0 \Rightarrow I_D = \frac{5-V_{DS}}{1} = 5 - x$$

$$\therefore I_D = 0.5 \left[4 \times V_{DS} - \frac{1}{2} V_{DS}^2 \right] \Rightarrow (5 - x) = 0.5 \left[4x - \frac{1}{2} x^2 \right]$$

$$\Rightarrow 5 - x = 2x - 0.25x^2 \Rightarrow 0.25x^2 - 3x + 5 = 0$$

$$\text{Solving, } x = 2V, \cancel{x = 10V}$$

Since $V_{DS} = x$ is small in triode, smaller value of x is favorable

$$\text{Therefore, } V_o = V_{DS} = x = 2V, \text{ and } I_D = 5 - x = 3 \text{ mA}$$

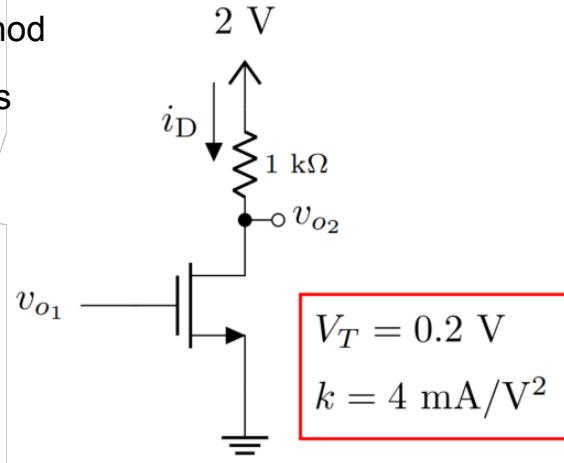
Step 3: $V_{GS} = 5V > V_T \checkmark$ Therefore, **assumption correct!**

$$V_{DS} = 2V < V_{OV} \checkmark$$

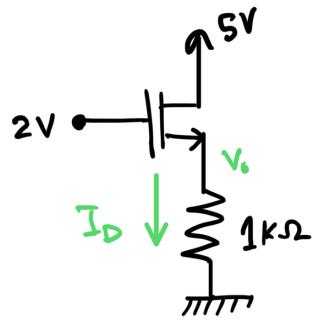
Correct ans: $I_D = 3 \text{ mA}, V_o = 2V$

Practice :

Analyze the circuit to find i_D and v_{o2} using the Method of Assumed State. Here, the input of the MOSFET is $v_{o1} = 1 \text{ V}$. You must validate your assumptions.



Example 3



The MOSFET is specified as $V_T = 1V$ and $k = 4 \text{ mA/V}^2$. Find I_D and V_o

Solution:

Step 1: Assume the MOSFET in **saturation**

$$\text{Step 2: } I_D = \frac{k}{2} V_{ov}^2$$

Let's assume $V_0 = V_S = x$

$$\text{Here, } V_{GS} = V_G - V_S = V_G - V_o = 2 - x$$

$$\text{Therefore, } V_{OV} = V_{GS} - V_T = (2 - x) - 1 = 1 - x$$

$$\text{Again, } V_{DS} = V_D - V_S = V_D - V_0 = 5 - x$$

$$\text{Ohm's law for the resistor: } I_D = \frac{V_0 - 0}{1k\Omega} = x$$

$$\therefore x = \frac{4}{2} (1 - x)^2 \Rightarrow x = 2(1 - 2x + x^2) \Rightarrow x = 2 - 4x + 2x^2 \\ \Rightarrow 2x^2 - 5x + 2 = 0$$

$$\text{Solving, } x = 0.5, \cancel{x = 2V}$$

Since $V_{DS} = 5 - x$ is large in saturation
smaller value of x is favorable

$$\therefore V_o = V_S = x = 0.5V, I_D = x = 0.5 \text{ mA}, \\ V_{DS} = 5 - x = 4.5V, V_{GS} = 2 - x = 1.5V, \text{ and } V_{OV} = 1 - x = 0.5V$$

Step 3: $V_{GS} = 1.5V > V_T \checkmark$ Therefore, **assumption correct!**

$$V_{DS} = 4.5V > V_{OV} \checkmark \quad \text{Correct ans: } I_D = 0.5 \text{ mA}, V_o = 0.5V$$

Practice

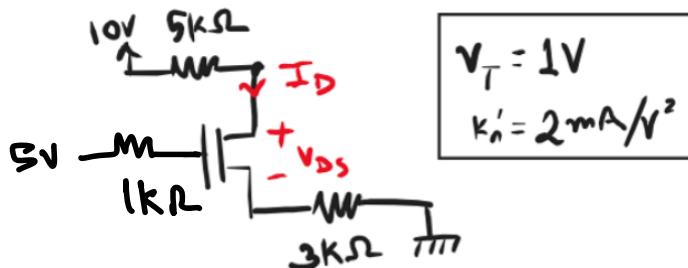
Question 4 [CO1, CO4]

10

Analyze the following circuit to find the values of I_D and V_{DS} using the Method of Assumed State. You must validate your assumptions.

[7 + 3]

Hint: Use I_D as unknown x . Use Ohm's law to represent V_D and V_S in terms of x .



Hint Explanation

Assume $I_D = x$. For $5k\Omega$: $I_D = \frac{10 - V_D}{5} \Rightarrow V_D = 10 - 5x$

For $3k\Omega$: $I_D = \frac{V_S - 0}{3} \Rightarrow V_S = 3x$.

Therefore, $V_{GS} = V_G - V_S = 5 - 3x$, and $V_{OV} = V_{GS} - V_T = (5 - 3x) - 1$

Also, $V_{DS} = V_D - V_S = (10 - 5x) - 3x = 10 - 8x$

Now if you assume saturation:

$$I_D = \frac{k}{2} V_{OV}^2 \Rightarrow x = \frac{2}{2} (4 - 3x)^2$$

And if you assume triode:

$$I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$$

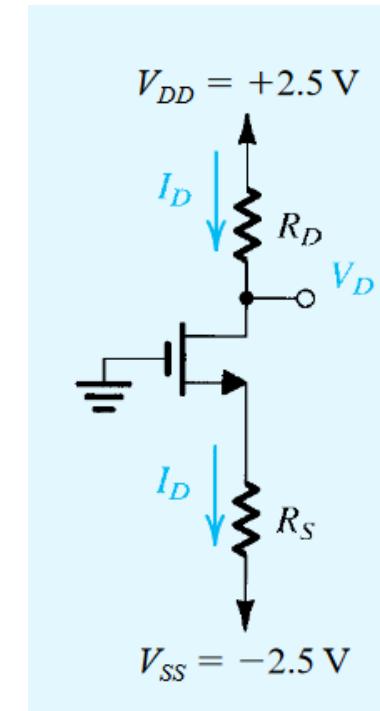
$$\Rightarrow x = 2[(4 - 3x)(10 - 8x) - 0.5 \times (10 - 8x)^2]$$

Solve for x , take the _____ root

Practice:

- Design the circuit, that is, determine the values of R_D and R_S , so that the transistor operates at $I_D = 0.4 \text{ mA}$ and $V_D = +0.5 \text{ V}$. The NMOS transistor has $V_T = 0.7 \text{ V}$, $k = 3.2 \text{ mA/V}^2$.

What is the mode of this transistor?



- Design the circuit, that is, determine the values of R_D and R_s , so that the transistor operates at $I_D = 0.4 \text{ mA}$ and $V_D = +0.5 \text{ V}$. The NMOS transistor has $V_T = 0.7 \text{ V}$, $k = 3.2 \text{ mA/V}^2$.

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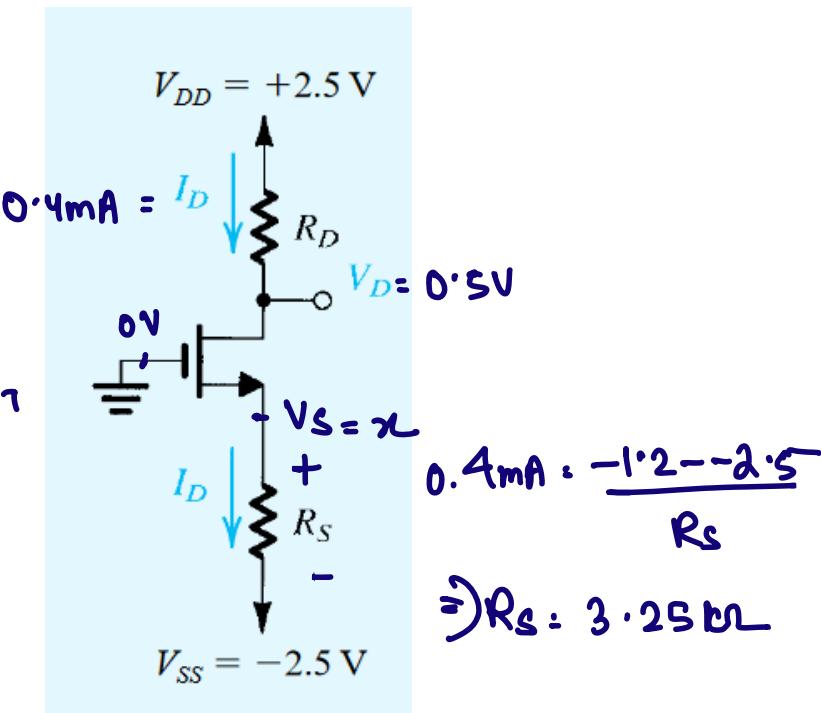
$$\frac{2.5 - 0.5}{R_D} = 0.4 \text{ mA} \Rightarrow R_D = 5 \text{ k}\Omega$$

Satn: $0.4 = \frac{3.2}{2} V_{DS}^2 \Rightarrow V_{DS} = 0.5 \text{ V} = V_{DS} - V_T$

$$V_{DS} = 1.2 \text{ V}$$

$$V_{DS} - V_S = 1.2 \Rightarrow V_S = -1.2 \text{ V}$$

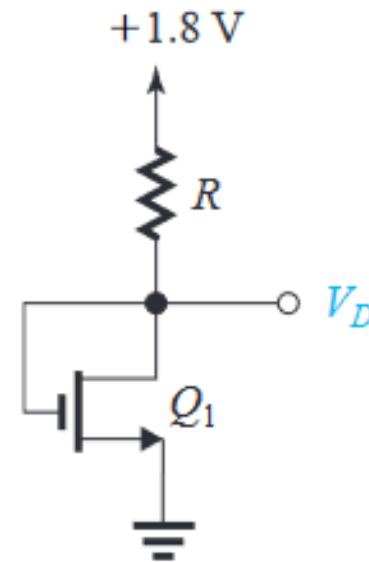
Validate: $V_{DS} > 0 ; V_{DS} = 0.5 - 1.2 = 1.7 > V_{DS}$



Practice:

- For the circuit, find the value of R that results in $V_D = 0.8$ V. The MOSFET has $V_T = 0.5$ V, $k'_n = \mu_n C_{OX} = 0.4$ mA/V², $\frac{W}{L} = \frac{0.72\ \mu\text{m}}{0.18\ \mu\text{m}}$

$$k_n = k'_n \frac{W}{L} = 1.6 \text{ mA/V}^2$$



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$$k_n = k'_n \frac{W}{L} = 1.6 \text{ mA/V}^2$$

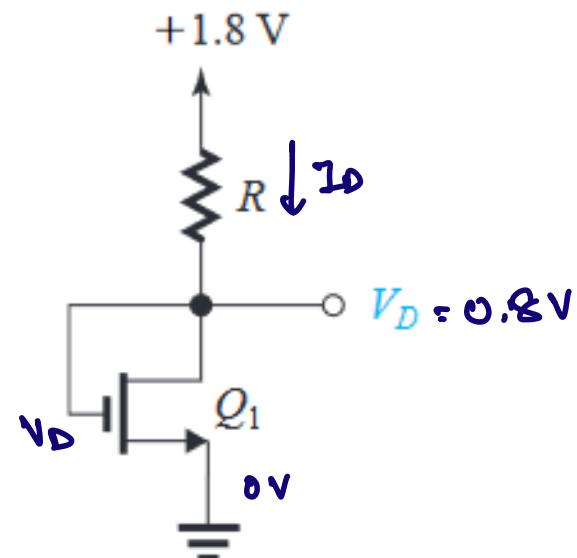
$$V_{DS} = 0.8 - 0 = 0.8 \text{ V}$$

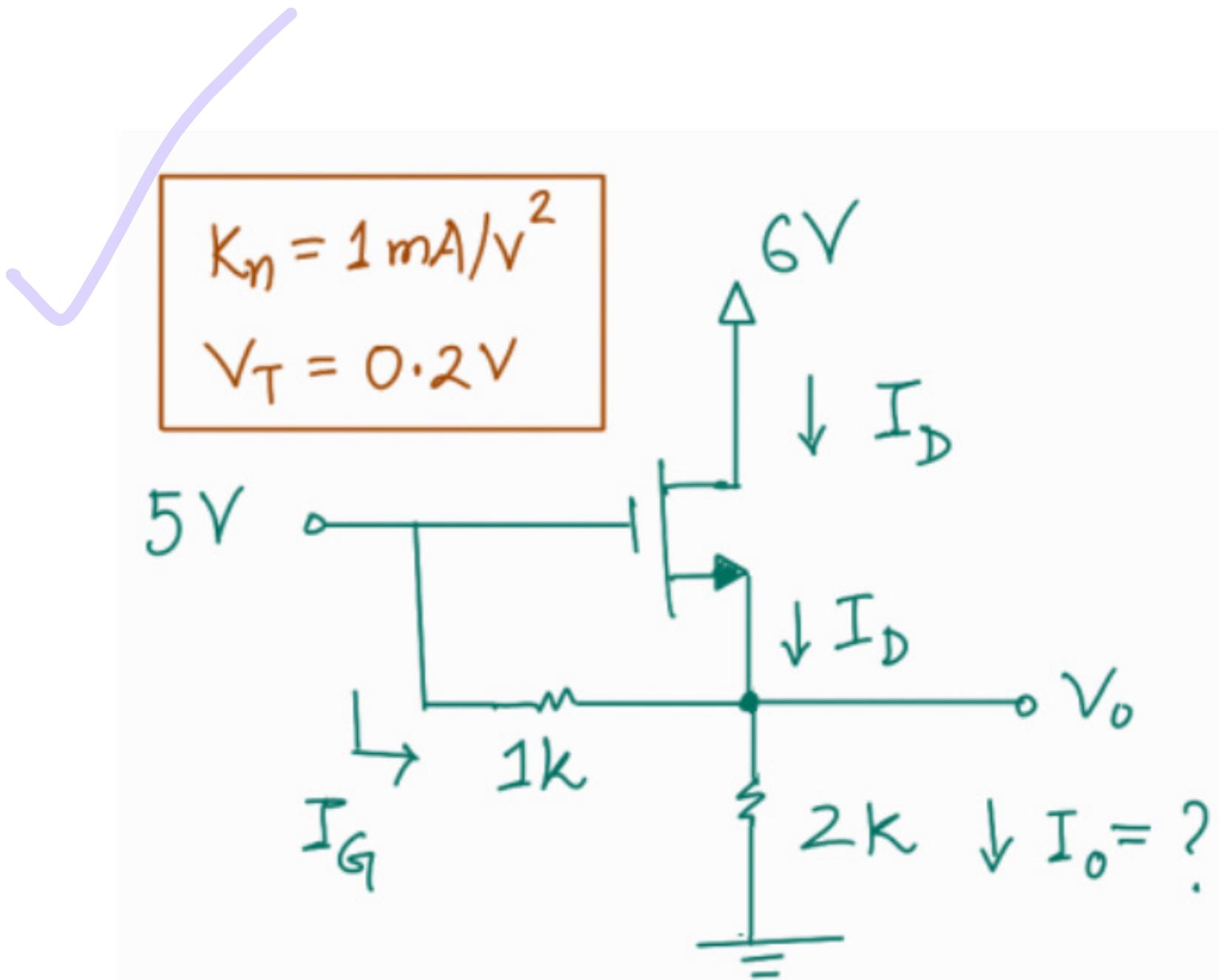
$$V_{OV} = 0.8 - 0.5 = 0.3 \text{ V}$$

$$V_{DS} = 0.8 \text{ V} > V_{OV} \therefore \text{sath}$$

$$I_D = \frac{1.6}{2} \times 0.3^2 = 0.072 \text{ mA}$$

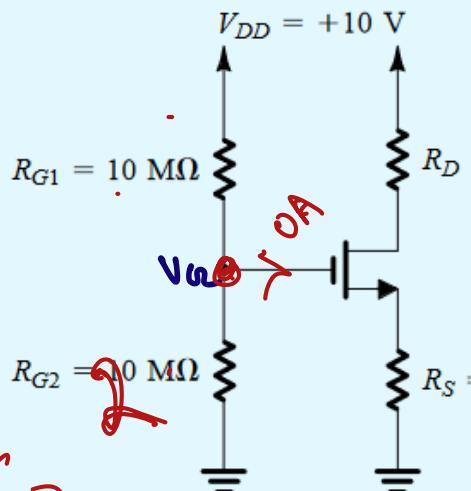
$$I_D = \frac{1.8 - 0.8}{R} = 0.072 \Rightarrow R = 13.89 \text{ k}\Omega$$



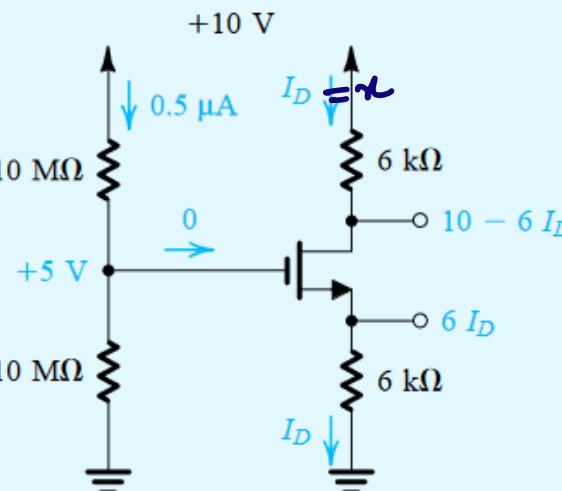


Practice :

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_t = 1$ V and $k'_n(W/L) = 1 \text{ mA/V}^2$. Neglect the channel length modulation effect (i.e., assume $\lambda = 0$).



(a)



(b)

$V_{in} = 20$
 $20 + 10$

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_t = 1$ V and $k'_n(W/L) = 1 \text{ mA/V}^2$. ~~Neglect the channel length modulation effect (i.e., assume $\lambda = 0$)~~

$$V_{DS} = 5 - 6x$$

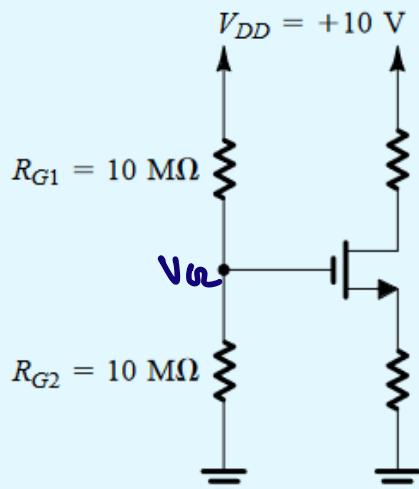
$$I_D : x \quad V_{DS} = 10 - 6x - 6x = 10 - 12x$$

$$V_{OV} = 4 - 6x$$

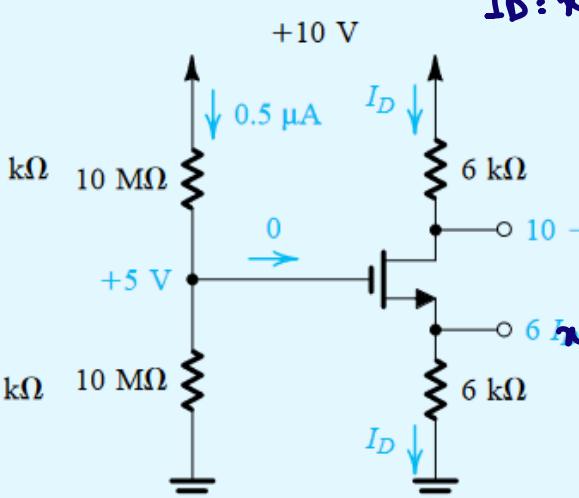
$$\underline{\text{Sat}}: x = \frac{1}{2} (5 - 6x)^2$$

triode:

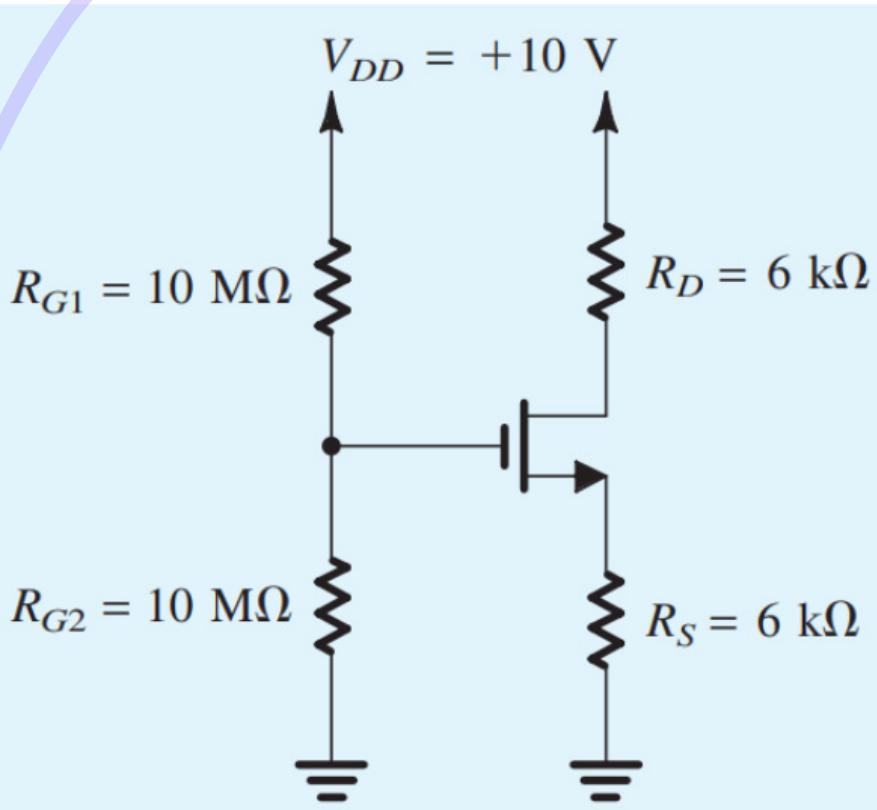
$$x = \frac{1}{2} ((4 - 6x)(10 - 12x) - \frac{1}{2}(4 - 6x)^2)$$



(a)



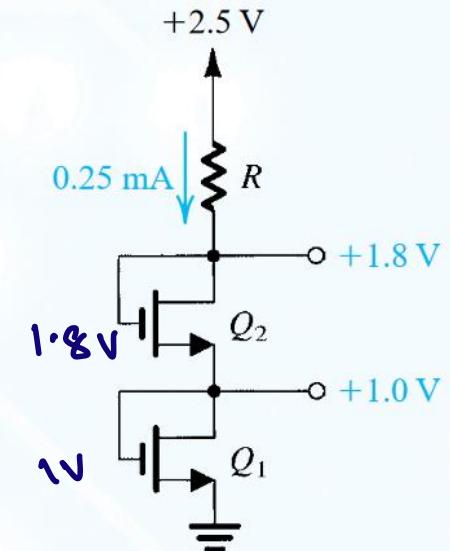
(b)



Analyze the circuit to find i_D and v_D using Method of Assumed State. You must validate your assumptions.
Here, $V_T = 1\text{V}$, $k = 5\text{ mA/v}^2$

Pratice:

D 5.50 The NMOS transistors in the circuit of Fig. P5.50 have $V_t = 0.5$ V, $\mu_n C_{ox} = 250 \mu\text{A/V}^2$, $\lambda = 0$, and $L_1 = L_2 = 0.25 \mu\text{m}$. Find the required values of gate width for each of Q_1 and Q_2 , and the value of R , to obtain the voltage and current values indicated.



D 5.50 The NMOS transistors in the circuit of Fig. P5.50 have $V_t = 0.5$ V, $\mu_n C_{ox} = 250 \mu\text{A/V}^2$, ~~$\lambda = 0$~~ , and $L_1 = L_2 = 0.25 \mu\text{m}$. Find the required values of gate width for each of Q_1 and Q_2 , and the value of R , to obtain the voltage and current values indicated.

$$\underline{Q_1}: V_{DS1} = 1 \quad V_{OV1} = 0.5$$

$$V_{DS1} = 1 - 0 = 1 \text{ V} > V_{OV1} \quad \therefore \text{Satn}$$

$$\frac{2.5 - 1.8}{0.25} = R = 2.8 \text{ k}\Omega$$

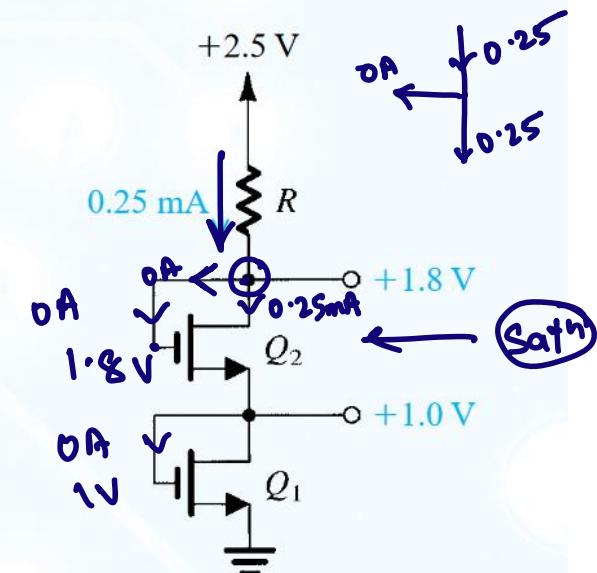
$$I_{DS1} = 0.25 = K \times \frac{1}{2} \times 0.5^2$$

$$\therefore \underline{K} = 2$$

$$2 = \mu_n C_{ox} \times \frac{W}{L}$$

$$\therefore Z_m = 250 \times \frac{W}{0.25} \Rightarrow W = 4 \mu\text{m}$$

$$\left. \begin{aligned} V_{D2} &= 1.8 \text{ V} \\ V_{G2} &= 1.8 \text{ V} \\ V_{S2} &= 1 \text{ V} \\ I_{DS2} &= 0.25 \text{ mA} \end{aligned} \right\}$$



for Q2: Try yourself!

$$V_{G1} = 1 \text{ V} \quad V_{D1} = 1 \text{ V} \quad V_{S1} = 0 \text{ V}$$

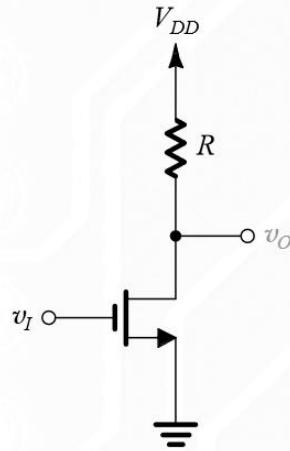
$$V_{DS} = 1 - 0 = 1 \text{ V} \quad V_{OV} = 1 - 0.5 = 0.5 \text{ V}$$

$\therefore V_{DS} > V_{OV} \rightarrow \text{satn}$

$$0.25 = K \times \frac{1}{2} \times 0.5^2$$

Practice:

5.54 The MOSFET in Fig. P5.54 has $V_t = 0.5$ V, $k'_n = 400 \mu\text{A/V}^2$, and $\lambda = 0$. Find the required values of W/L and of R so that when $v_I = V_{DD} = +1.8$ V, $r_{DS} = 50 \Omega$, and $v_O = 50$ mV.



$$r_{DS} = \frac{V_{DS}}{i_{DS}} = 50$$

r_{DS} is finite only in triode mode

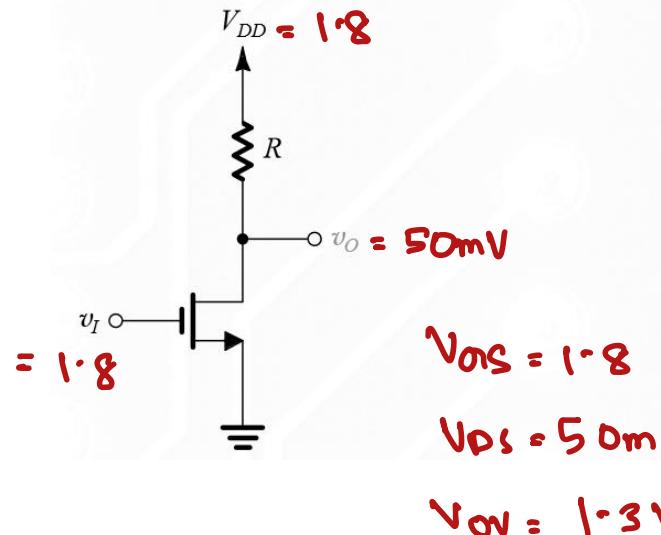
$$\therefore i_{DS} = k \left[(V_{DS} - V_T) - \frac{1}{2} V_{DS} \right] V_{DS}$$

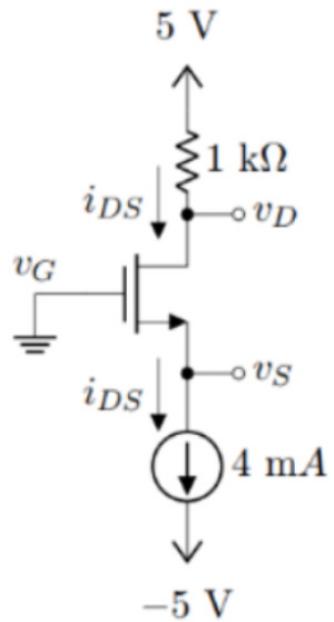
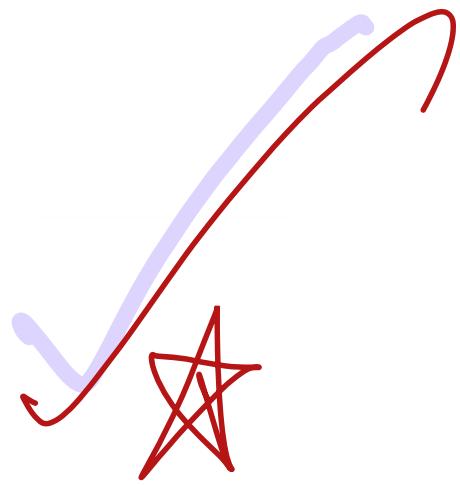
$$50 = \frac{1}{k(1.3 - \frac{1}{2} \times 50m)}$$

$$k = 15.68 m = 400 \mu A/V^2 \times \frac{W}{L}$$

$$\Rightarrow \frac{W}{L} = 39.2$$

- 5.54 The MOSFET in Fig. P5.54 has $V_t = 0.5$ V, $k'_n = 400 \mu A/V^2$, and $\lambda = 0$. Find the required values of W/L and of R so that when $v_I = V_{DD} = +1.8$ V, $r_{DS} = 50 \Omega$, and $v_o = 50$ mV.



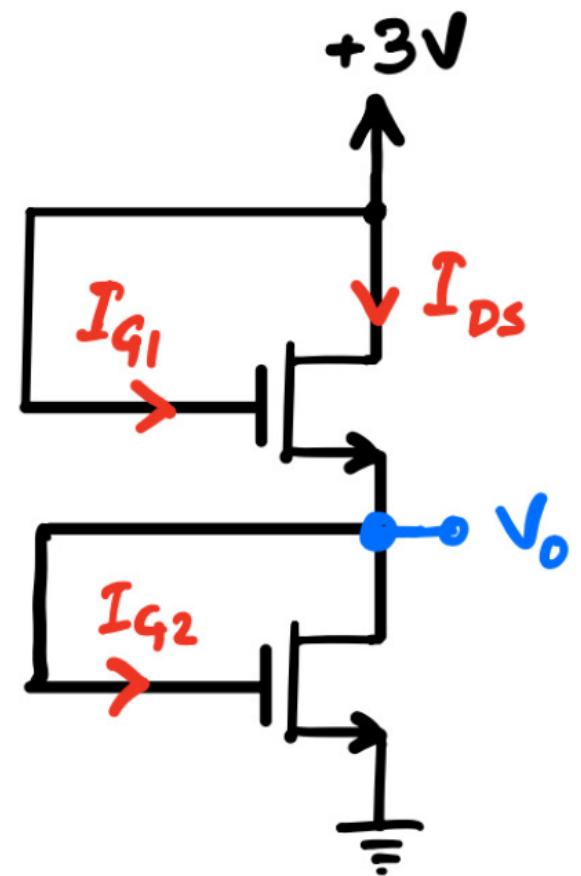


Refer to the **Circuit** above. For the MOSFET, $V_T = 1\text{ V}$ and $k = k'_n \frac{W}{L} = 4\text{ mA/V}^2$.

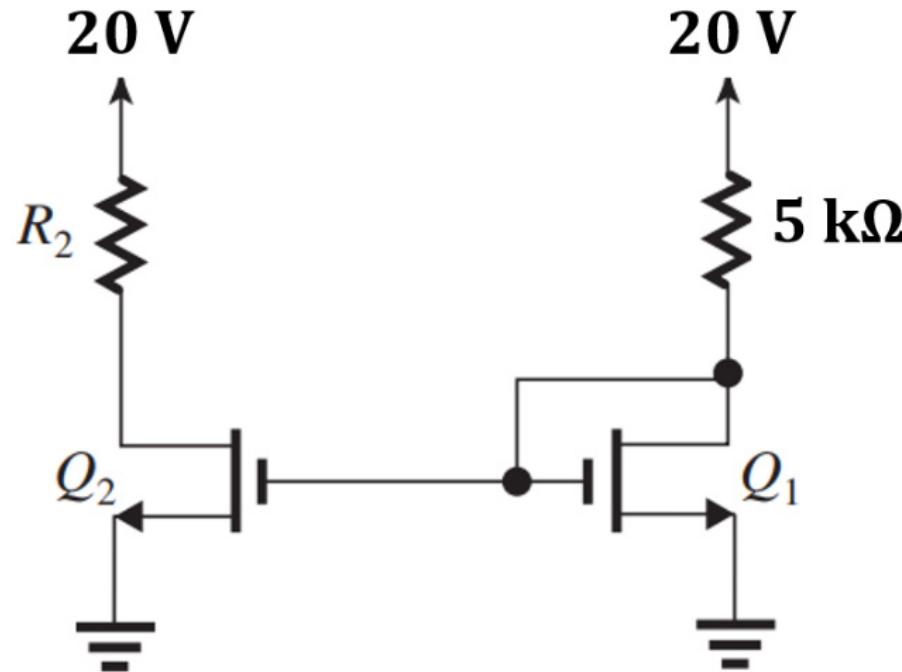
- Identify** the value of the gate voltage v_G and the drain-source current i_{DS} .
- Calculate** the value of the drain voltage v_D using the $1\text{ k}\Omega$ resistor.
- Analyze** the circuit to find v_S . Here, **use** the Method of Assumed State. You must **validate** your assumptions. [Hint: assume $v_S = x$]

In the circuit shown in the figure below, the transistor is characterized by $V_T = 1 \text{ V}$, $k = 1 \text{ mA/V}^2$. (Hint: Identify the modes of the two MOSFET, and equate the two currents.)

- (a) [3 marks] Find the value of V_O indicated in the figure.
- (b) [3 marks] Find the values of I_{DS} , I_{G1} and I_{G2} .

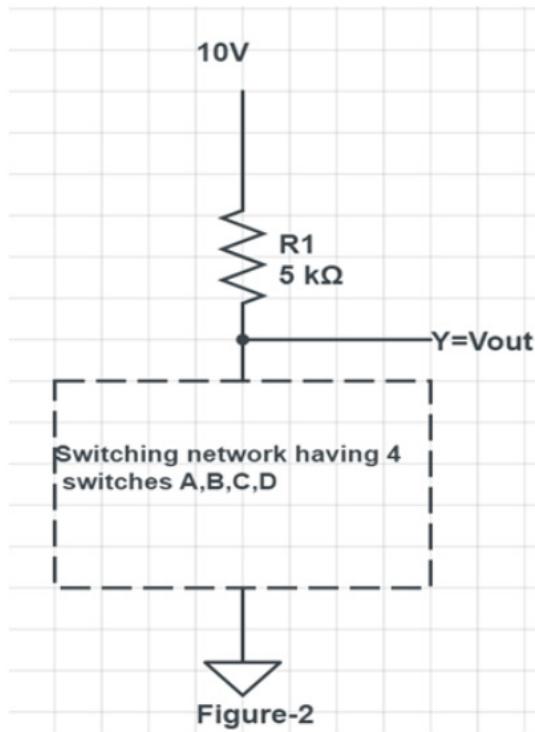


Q1.



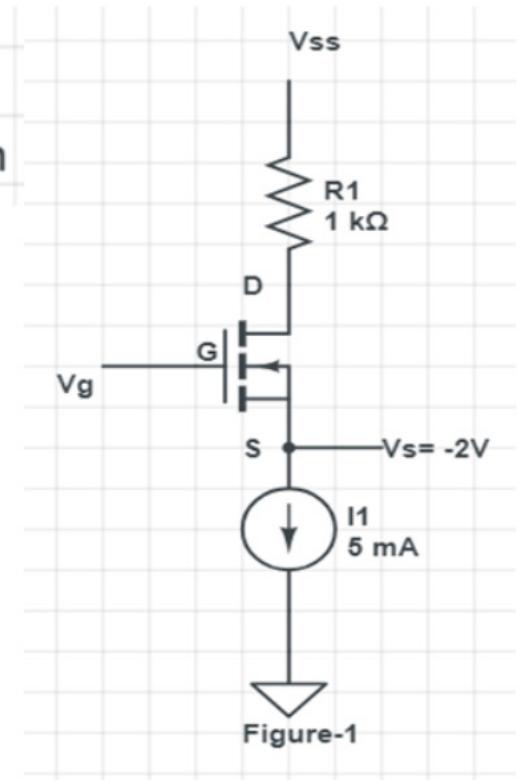
In the circuit above, the MOSFETs have the following parameters, $k'n=2 \text{ mA/V}^2$, $W/L = 2.5$, $VT=0.5 \text{ V}$.

- Find out** the operating mode of Q₁ [Hint: For Triode mode $V_{ds} < V_{ov}$ and for Saturation $V_{ds} \geq V_{ov}$]
- Determine** the value of R₂ that results in Q₂ operating at the edge of the saturation region.
- Calculate the on-state resistance**, R_{on} for Q₂. Assume, gate voltage of Q₂ is 20 V.
- An inverter is designed using Q₂ and a 10K resistor. **Draw** the VTC graph for the inverter.

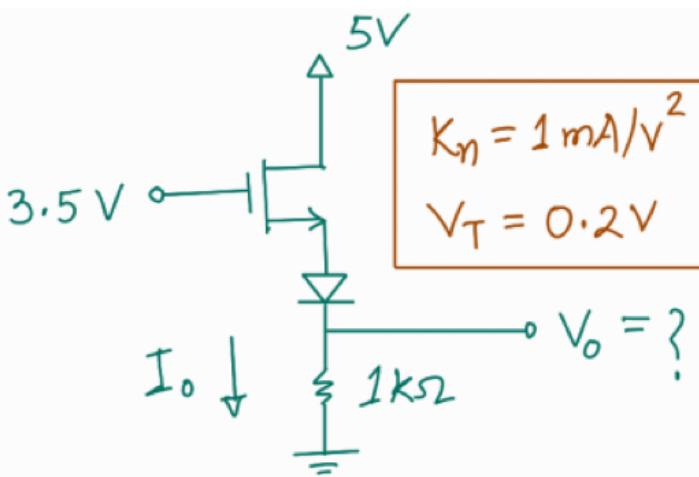


Conditions for Network on

- i) switch A must be on
- ii) Switches B,C simultaneously on or D on



- a) For figure-2, place the switches as nmos devices and write the output logic function Y in terms of A,B,C,D assuming nmos switch model. [2]
- b) From figure-2, assuming SR model for nmos find the output voltage when only A and D switches are ON(Assume $R_{on} = 0.1 \text{ k}\Omega$) [3]
- c) For figure-1, $k=2 \text{ mA/V}^2$, $V_T = 1 \text{ V}$ [3+2]
- i) Find the gate voltage so that the mosfet is in saturation mode.
 - ii) Then find the minimum supply voltage V_{ss} to operate the device in this condition. [Hints , $V_{ov} = V_{DS}$]
- d) **Bonus** - from figure-2 is it possible to drive a not gate cascaded to V_{out} ?



Sol'n

$$V_{GS} = 3.5 - V_s, \quad V_{DS} = 5 - V_s$$

$$\begin{aligned} \text{Diode } \rightarrow \text{CVD} \rightarrow V_s - V_o &= 0.7 \\ \Rightarrow V_s &= 0.7 + V_o \end{aligned}$$

$$\therefore V_{GS} = 3.5 - 0.7 - V_o = 2.8 - V_o$$

$$\&, V_{DS} = 5 - 0.7 - V_o = 4.3 - V_o$$

$$\text{Finally, } V_{ov} = V_{GS} - V_T = 2.6 - V_o$$

* Assume Saturation: $I_o = \frac{K_n}{2} V_{ov}^2$

$$\Rightarrow \frac{V_o - 0}{1} = \frac{1}{2} (2.6 - V_o)^2$$

$$\Rightarrow V_o = 1.11, \quad \cancel{6.09}$$

* Verify: $\left. \begin{array}{l} V_{GS} = 2.8 - 1.11 = 1.69 > V_T \\ V_{DS} = 4.3 - 1.11 = 3.19 \\ V_{ov} = 2.6 - 1.11 = 1.49 \end{array} \right\} \begin{array}{l} \text{Assumption} \\ \text{Correct} \end{array}$

Therefore, $V_{DS} > V_{ov}$

Ans:
 $V_o = 1.11 \text{ V}$