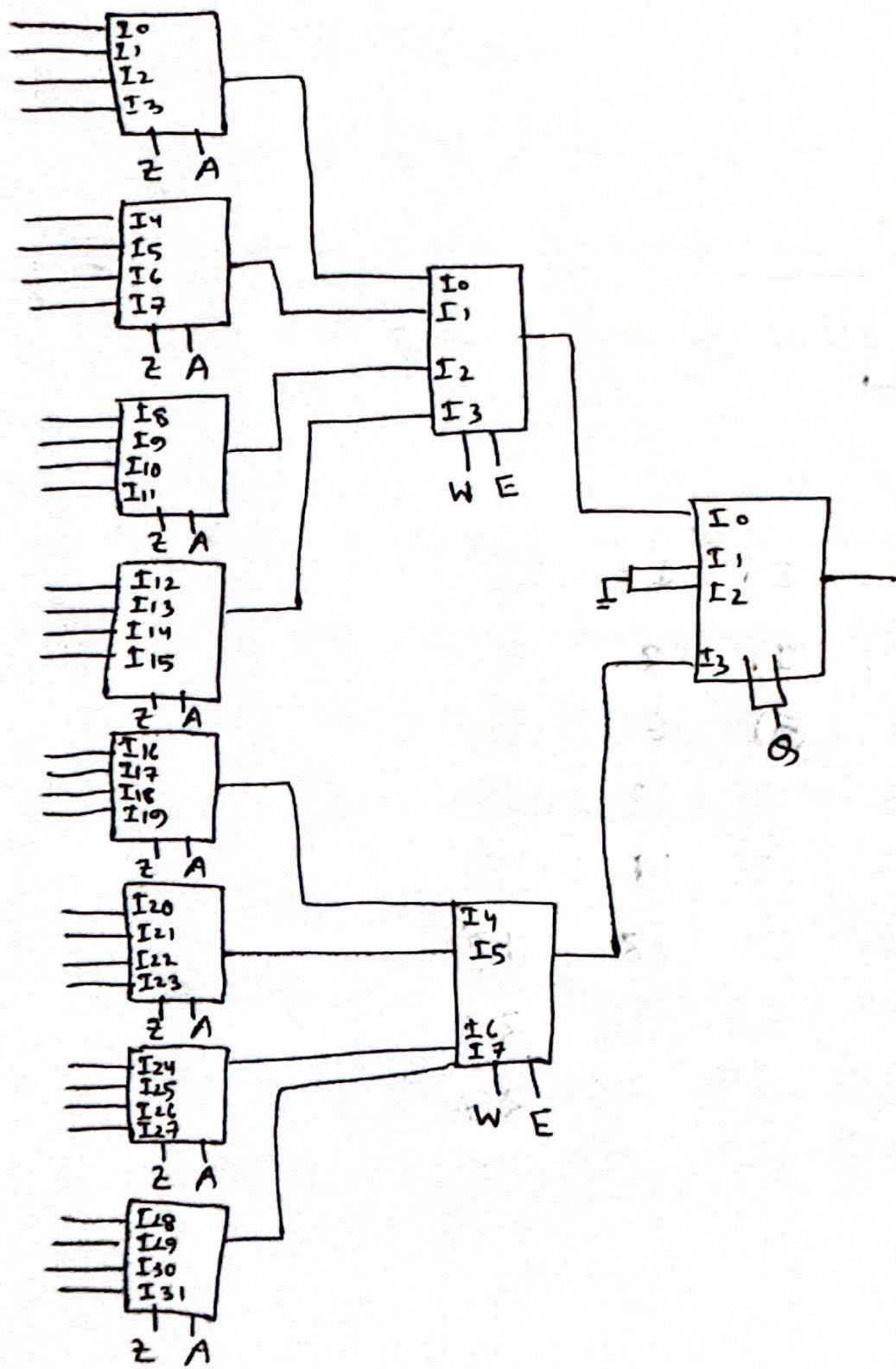


1. Design a 32:1 MUX using 4:1 Mux(s); Selector bits QWEZA
2. Implement the following function using only 4:1 Mux;
 $F(QWEZA) = \sum(0,1,5,7,11,15,19,21,24,25,26,28,30,31)$
3. Design a system using encoder and decoder that can convert a three bit number to its 1s complement form.
4. Design a system using encoder and decoder that can convert a 3 bit 2s complement number to its actual form.
5. Design a system using encoder and decoder that takes a 2 bit number and generates output by adding 2 with the input.
6. Design a half adder using encoder and decoder.
7. Design a full adder using encoder and decoder.
8. $F(O, A, S, L, B) = \sum(0,1,5,7,11,15,19,21,24,25,26,28,30,31)$
 1. Implement the above boolean function using three 2:1 Mux(s)
 2. Implement the above boolean function using a 2:1 Mux

HN(2)

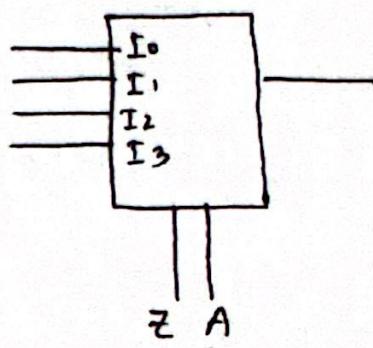
1. Design a 32:1 MUX using 4:1 MUX(S) & Selector

bits QWEZA.



2. Implement the following function using only 1:1 Mux;

$$F(QWEZA) = \Sigma (0, 1, 5, 7, 11, 15, 19, 21, 24, 25, 26, 28, 30, 31)$$



	I ₀	I ₁	I ₂	I ₃
Q'WE'	0	1	2	3
Q'WE	4	5	6	7
Q'WE'	8	9	10	11
Q'WE	12	13	14	15
Q'WE'	16	17	18	19
Q'WE	20	21	22	23
Q'WE'	24	25	26	27
Q'WE	28	29	30	31

I₀ \Rightarrow

$$\begin{aligned} & Q' W' E' + Q W E' + Q W E \\ &= Q' W' E' + Q W (E + E') \\ &= Q' W' E' + Q W \\ &= (Q' + Q' W' E') (W + Q' W' E') \\ &= (Q + Q') (Q + W') (Q + E') + (Q' + W) (W + W') (W + E') \\ &= (Q + W') (Q + E') + (Q' + W) (W + E') \end{aligned}$$

I₁ \Rightarrow

$$\begin{aligned} & (Q' W' E' + Q' W' E + Q W' E + Q W E) \\ &= Q' W' (E + E') + Q W' E + Q W E \\ &= Q' W' + Q W' E + Q W E \\ &= W' (Q' + Q E') + Q W E \\ &= W' (Q' + E) + Q W E \\ &= Q' W' + Q (W' E + W E') \\ &= Q' W' + Q (E \oplus W) \end{aligned}$$

I₂ ⇒

$$\mathcal{Q}WE' + \mathcal{Q}WE$$

$$\Rightarrow \mathcal{Q}W(E+E')$$

$$= \mathcal{Q}W$$

I₃ ⇒

$$\mathcal{Q}'W'E + \mathcal{Q}'WE' + \mathcal{Q}'WE + \mathcal{Q}'E' + \mathcal{Q}WE$$

$$= \mathcal{Q}'W'E + \mathcal{Q}'(WE'+WE) + \mathcal{Q}(W'E'+WE)$$

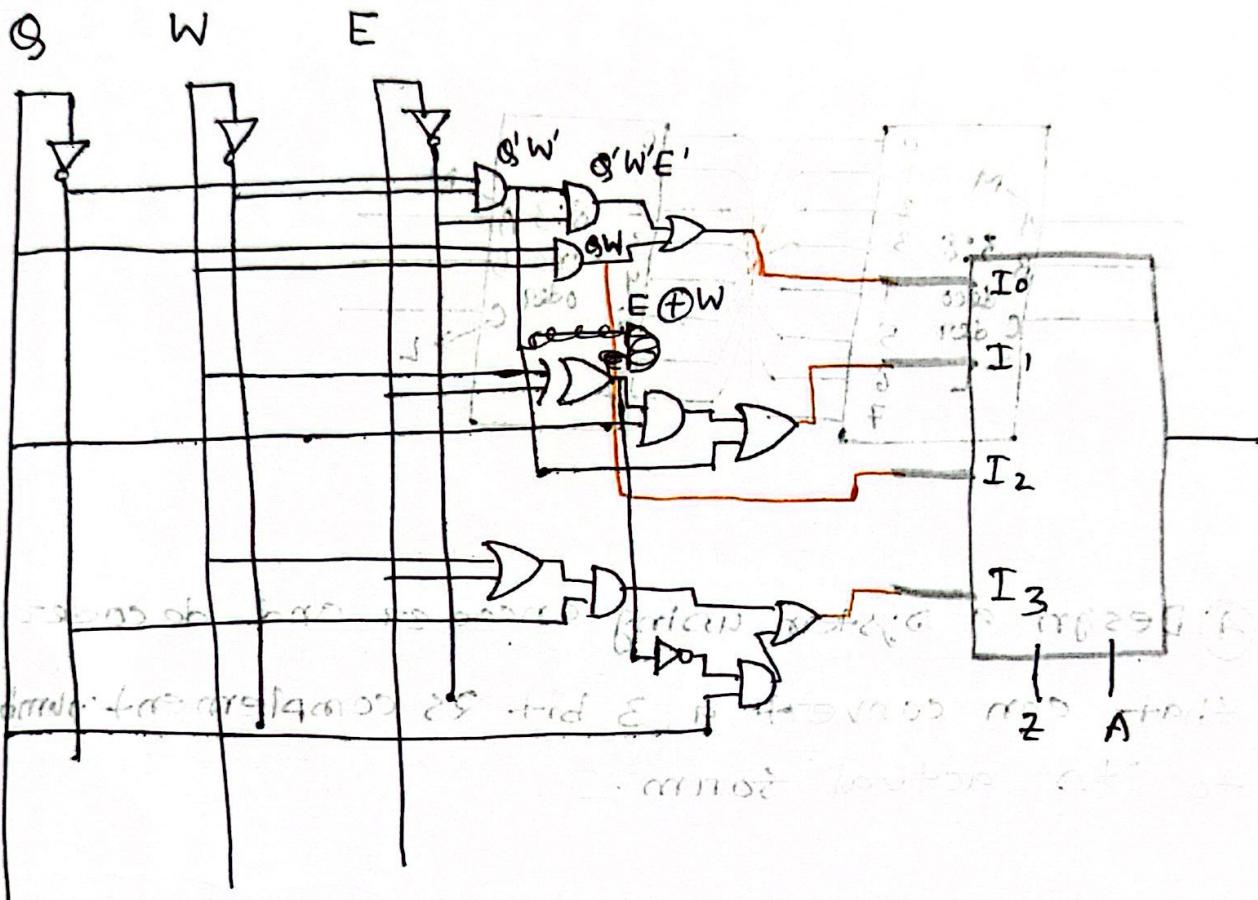
$$= \mathcal{Q}'W'E + \mathcal{Q}'(W(E+E')) + \mathcal{Q}(W \oplus E)',$$

$$= \mathcal{Q}'W'E + \mathcal{Q}'W + \mathcal{Q}(W \oplus E)'$$

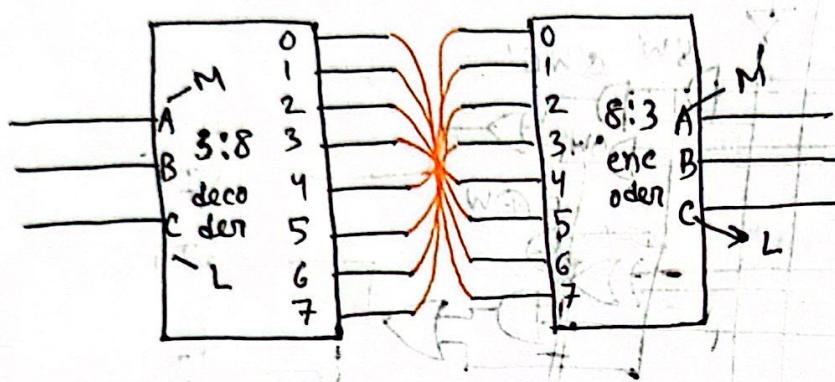
$$= \mathcal{Q}'(W'E+W) + \mathcal{Q}(W \oplus E)',$$

$$= \mathcal{Q}'(W+W')(W+E) + \mathcal{Q}(W \oplus E)',$$

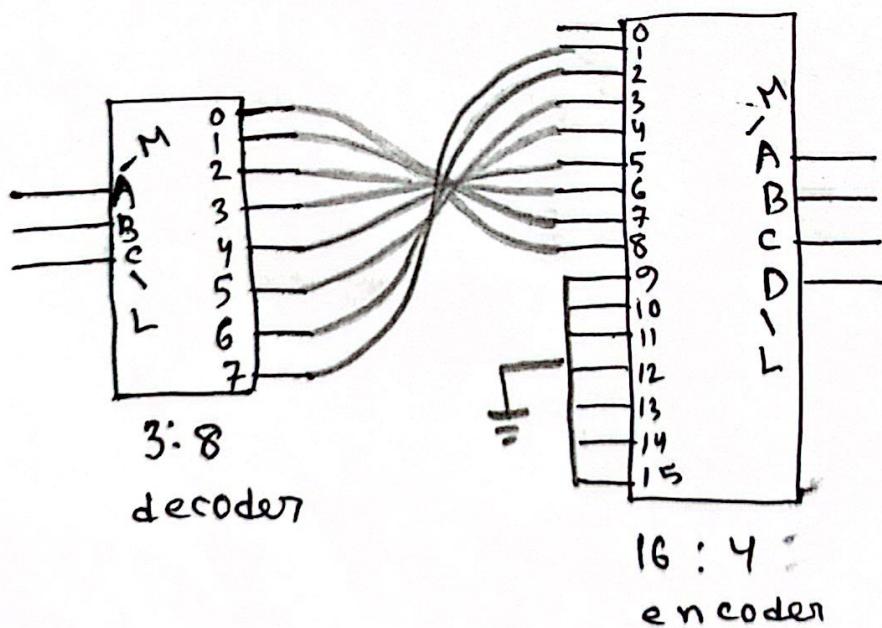
$$= \mathcal{Q}'(W+E) + \mathcal{Q}(W \oplus E)',$$



③ Design a system using encoder and decoder that can convert a three bit number to its 1's complement form.

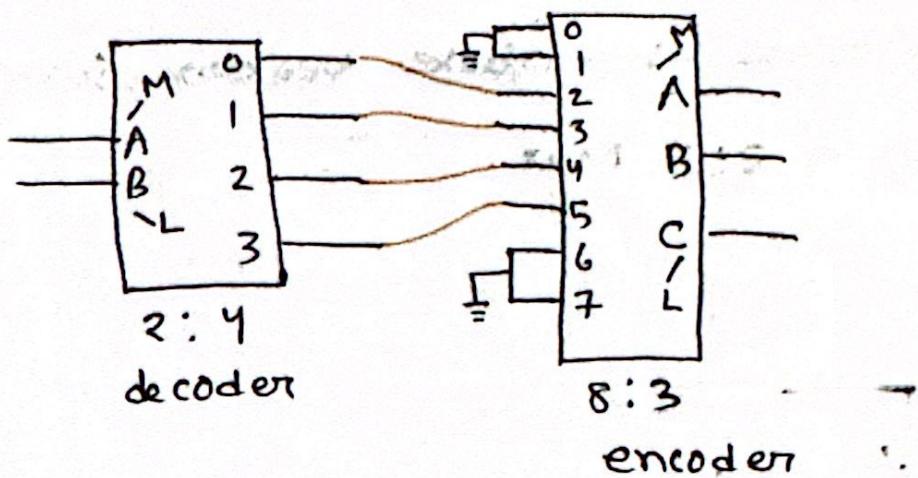


④ Design a system using encoder and decoder that can convert a 3 bit 2's complement number to its actual form.

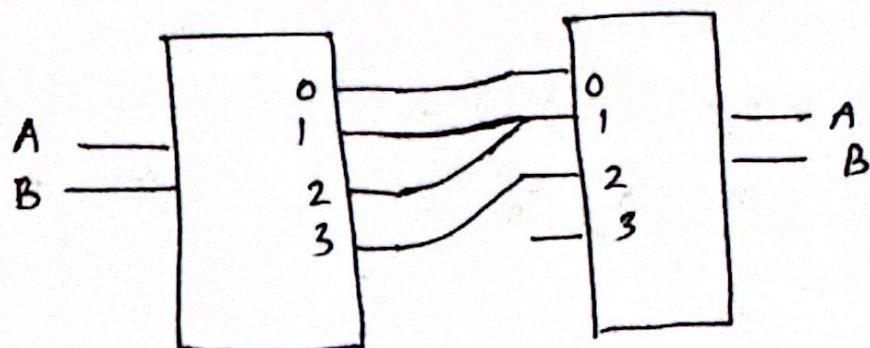


$$\begin{array}{r}
 u \rightarrow 100 \\
 +2 \\
 \hline
 110
 \end{array}
 \quad
 \begin{array}{r}
 000 \xrightarrow{+2} 0 \\
 +2 \\
 \hline
 010 \xrightarrow{G} 2
 \end{array}$$

- ⑤ Design a system using encoder and decoder that takes a 2 bit number and generates output by adding 2 with the input.

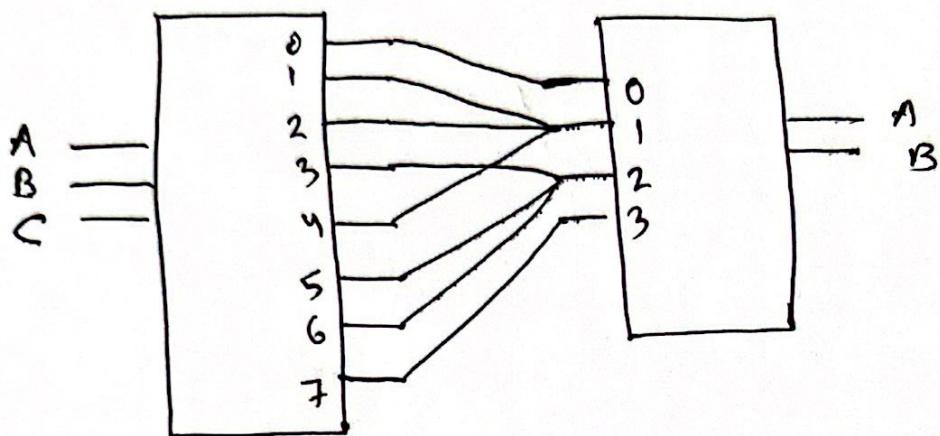


- ⑥ design a half adder using encoder and decoder



	A	B	Ca	S
1	0	0	0	0
2	0	1	0	1
3	1	0	0	1
4	1	1	1	0

7) Design a full adder using encoder and decoder.



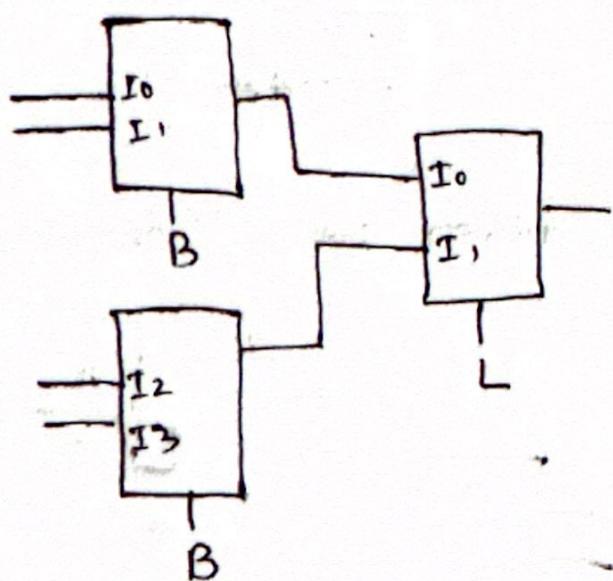
A	B	C	ca	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

⑧ $F(0, A, S, L, B) = \{0, 1, 5, 7, 11, 15, 19, 21, 24, 25, 26, 28, 30, 31\}$

i) Implement the above boolean function
using three 2:1 Mux(s)

ii) Implement the above boolean function
using a 2:1 Mux.

i)



	I_0	I_1	I_2	I_3
$O'A'S'$	0	1	2	3
$O'A'S$	4	5	6	7
$O'AS'$	8	9	10	11
$O'AS$	12	13	14	15
$OA'S'$	16	17	18	19
$OA'S$	20	21	22	23
OAS'	24	25	26	27
OAS	28	29	30	31

$$\begin{aligned}
 I_3 \Rightarrow & O'A'S + O'AS \\
 & + O'AS + OA'S \\
 = & O'A'S + O'(AS' + AS) \\
 & + OA'S \\
 = & O'A'S + O'(A(S + S')) \\
 & + OA'S \\
 = & O'A'S + O'A \\
 & + OA'S \\
 = & O'(A'S + A) + OA'S \\
 = & O'(A + A')(A + S) \\
 & + OA'S \\
 = & O'(A + S) + OA'S
 \end{aligned}$$

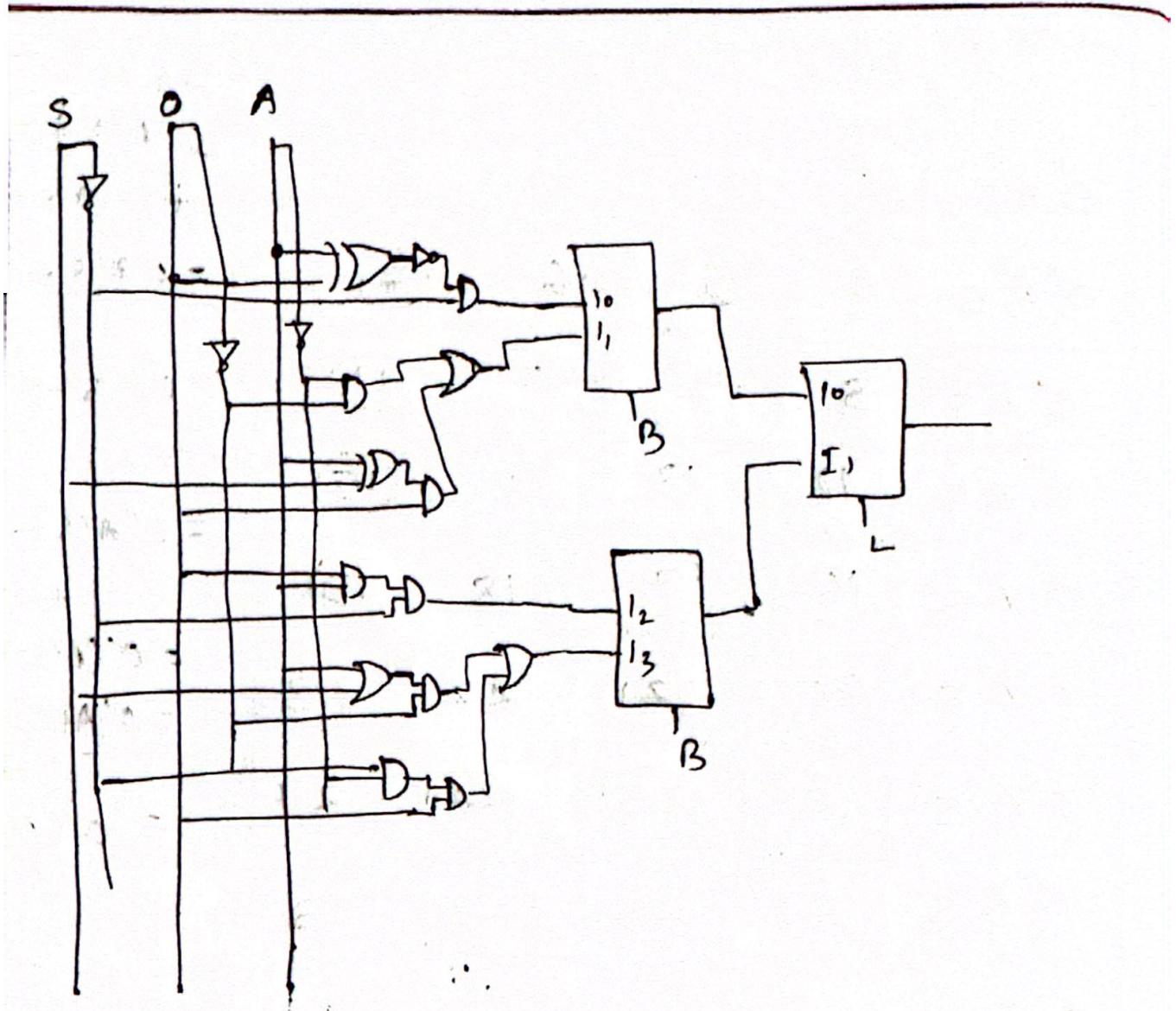
$I_0 \Rightarrow$

$$\begin{aligned}
 O'A'S' + OAS' &= S'(O'A' + OA) \\
 &= S'(O \oplus A)'
 \end{aligned}$$

$I_1 \Rightarrow$

$$\begin{aligned}
 O'A'S' + O'A'S + OA'S + OAS' \\
 &= O'A'(S + S') + O(A'S + AS') \\
 &= O'A' + O(A \oplus S)
 \end{aligned}$$

$I_2 \Rightarrow OAS'$



1. Design a circuit that will do the following:
 - i . add if both numbers are same
 - ii. sub if both numbers are different

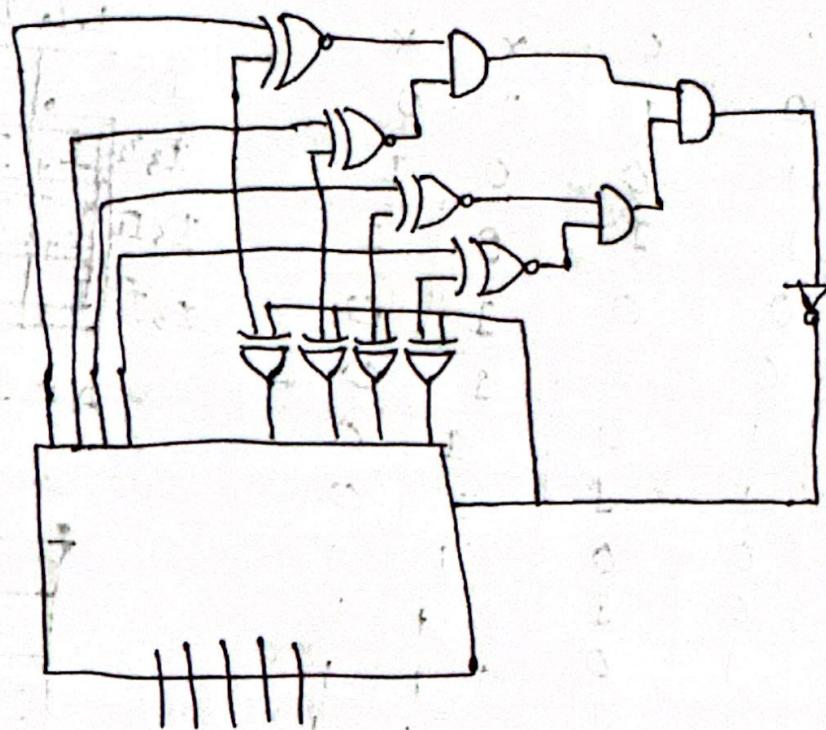
2. Design a circuit that will do the following:
 - i . sub if both numbers are same
 - ii. add if both numbers are different

3. Design a Half adder using a decoder.
4. Draw the circuit diagram of a 4 X 16 decoder.
5. Design a 5x32 decoder using only 3X8 decoder(s)
6. Design a 13-person voting system using only 3-bit parallel adder(s).

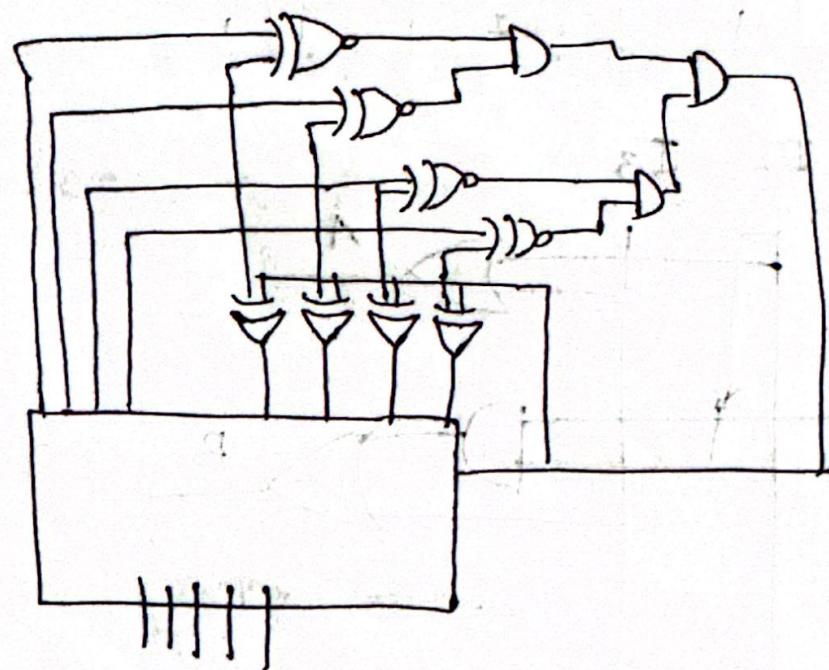
Note: You must mention MSB and LSB wherever necessary.

HW

①



②



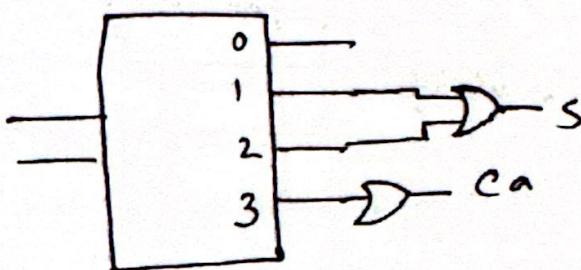
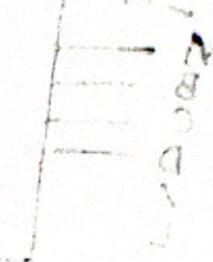
HW

③ Design a Half adder using a decoder

A	B	ca	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$ca = \Sigma(3)$$

$$S = \Sigma(1, 2)$$



$$0+0=000 = 0$$

$$0+1=001 = 1$$

$$1+0=010 = 2$$

$$1+1=100 = 8$$

$$0+0=000 = 0$$

$$0+1=001 = 1$$

$$1+0=010 = 2$$

$$1+1=100 = 8$$

$$0+0=000 = 0$$

$$0+1=001 = 1$$

$$1+0=010 = 2$$

$$1+1=100 = 8$$

$$0+0=000 = 0$$

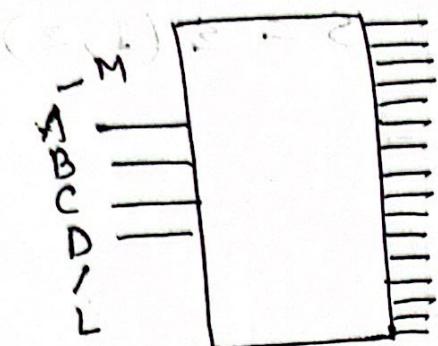
$$0+1=001 = 1$$

$$1+0=010 = 2$$

$$1+1=100 = 8$$

$$0+0=000 = 0$$

④ Draw the circuit diagram of a 4×16 decoder.



$$O_0 = 0000 = A'B'C'D'$$

$$O_1 = 0001 = A'B'C'D$$

$$O_2 = 0010 = A'B'C'D'$$

$$O_3 = 0011 = A'B'CD$$

$$O_4 = 0100 = A'B'C'D'$$

$$O_5 = 0101 = A'B'C'D$$

$$O_6 = 0110 = A'B'CD$$

$$O_7 = 0111 = A'BCD$$

$$O_8 = 1000 = AB'C'D'$$

$$O_9 = 1001 = AB'C'D$$

$$O_{10} = 1010 = AB'CD$$

$$O_{11} = 1011 = AB'CD$$

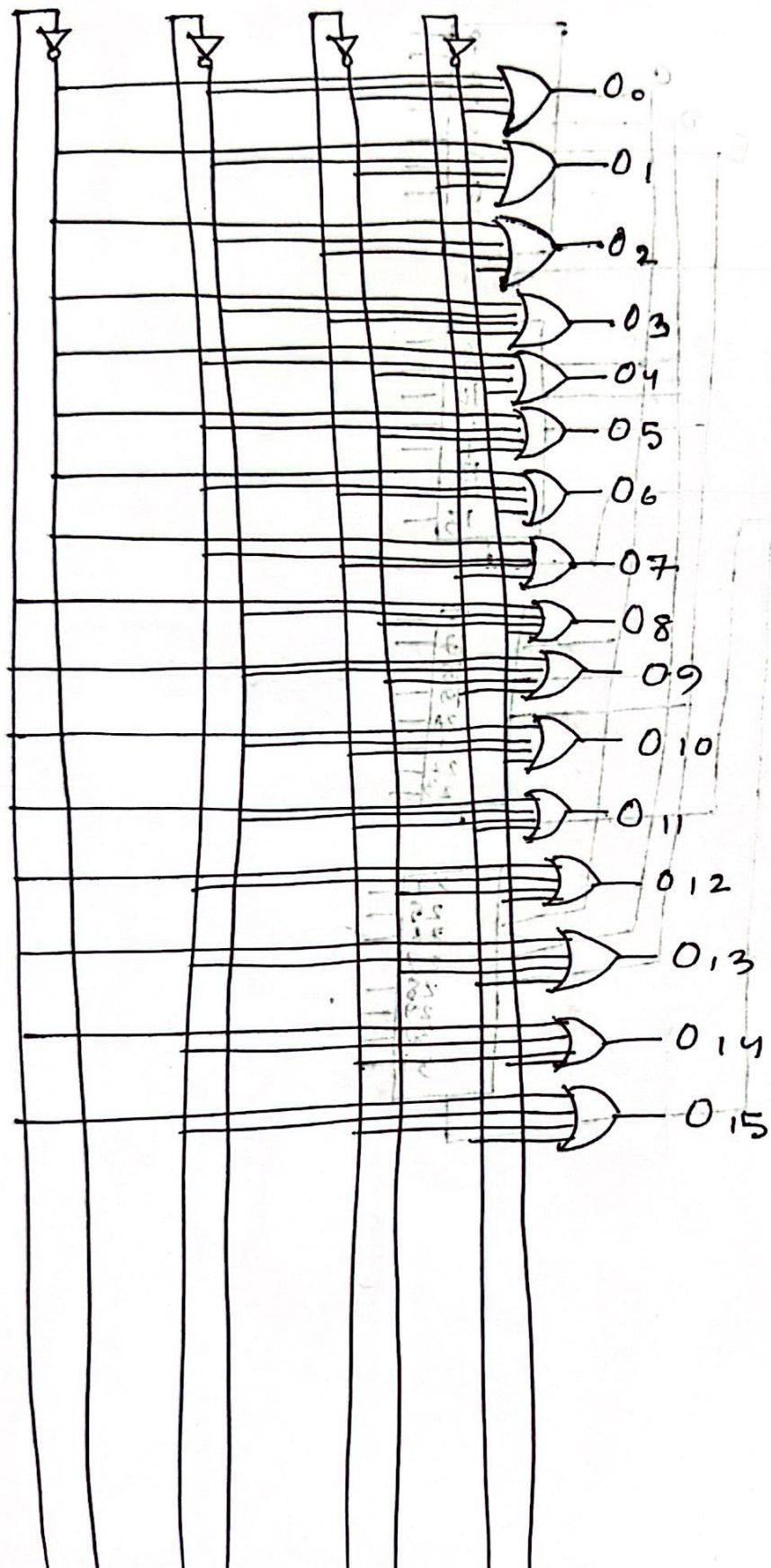
$$O_{12} = 1100 = ABC'D'$$

$$O_{13} = 1101 = ABC'D$$

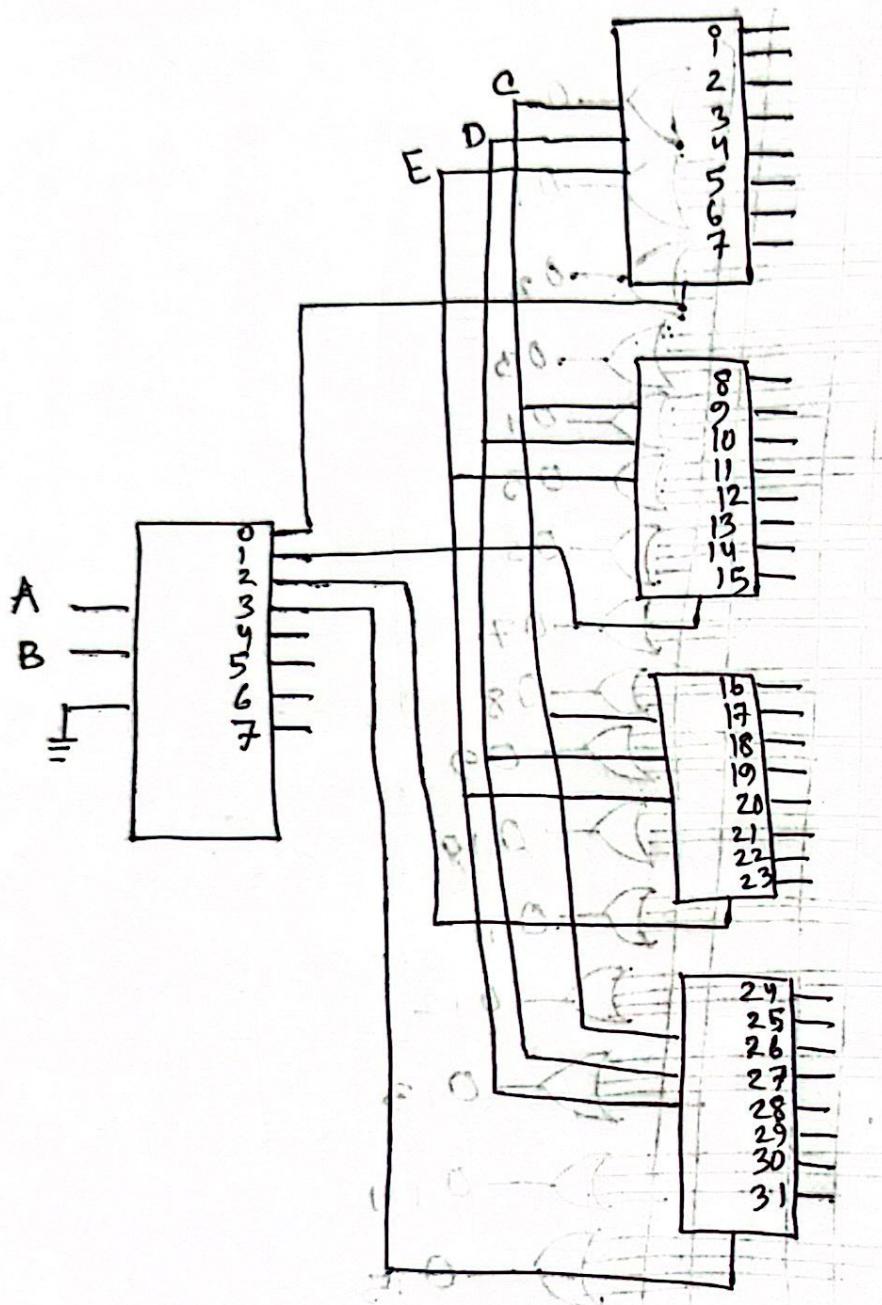
$$O_{14} = 1110 = ABCD'$$

$$O_{15} = 1111 = ABCD$$

A B C D



⑤ Design a 5×32 decoder using only 3×8 decoder(s)



⑥ Design a 13-person voting system using only 3-bit parallel adder(s).

