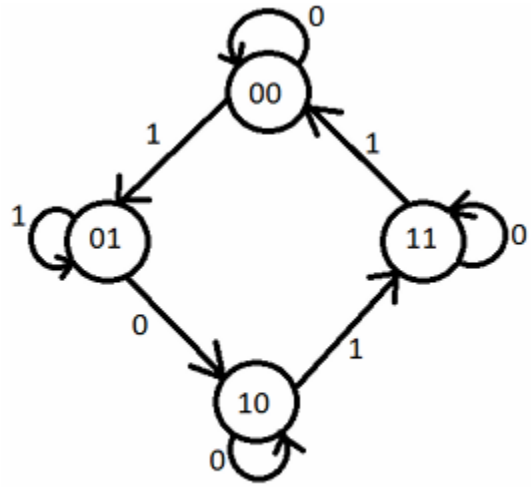
CSE260: Digital Logic Design

Assignment 4

Submission Link Section 01: Here
Submission Link Section 02: Here

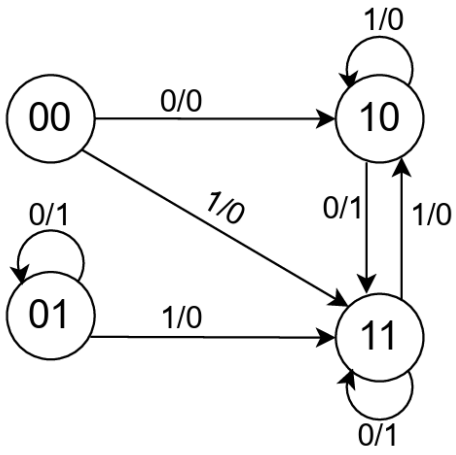
Complete only Question 8 for the assignment. The rest are for practice.

1. Design a D FFusing SR FF.
2. Design a T FFusing JK FF.
3. Design a D FFusing JK FF
4. Given the state diagram as follows, get the sequential circuit using SR flipflop.

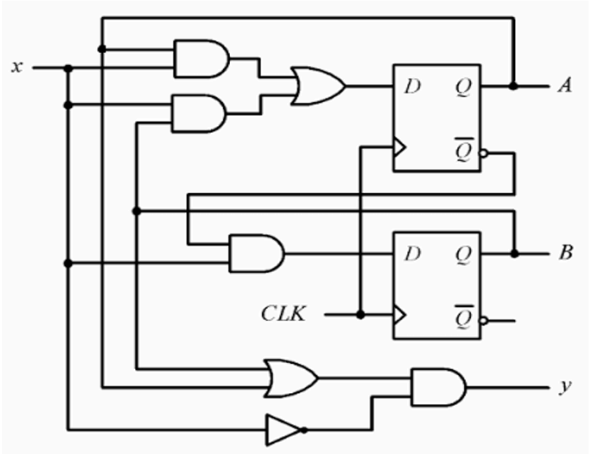


5. Given the state diagram as follows, get the sequential circuit using
   i. SR flipflop.
   ii. JK flipflop.

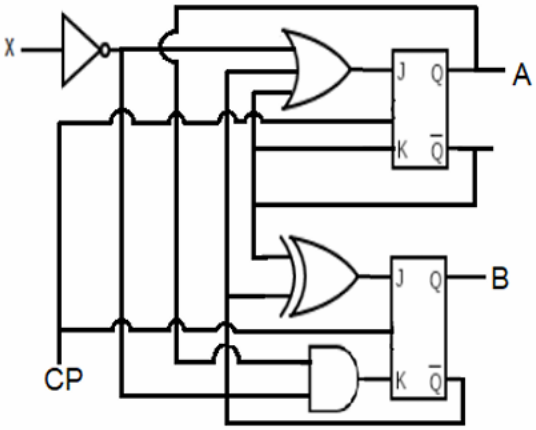
CSE260: Digital Logic Design



6. Draw the state diagram for the given circuit.



7. Draw the state diagram for the given circuit.



CSE260: Digital Logic Design

8. Implement the following counter using T flip flop
   CSE110-> CSE111-> CSE220-> CSE221-> CSE331-> CSE221-> CSE321-> CSE110
9. 3->4->6->10->12->13->15->3
   1. Implement the given counter using JK flip-flop.
   2. Implement the given counter using T flip-flop.

   NB: For states not given in the question, please move to the initial state as per the question.
10. Implement 4 bit up counter using JK flip-flop.
11. Implement 4 bit down counter using JK flip-flop
12. Implement the following counter using T FF:
    Green->Orange->Yellow->Red->Yellow->Orange->Yellow->Green
13. Implement the following counter using JK FF:
    Green->Yellow->Red->Yellow->Green
14. Implement the following counter using JK FF: 1->2->3->5->7->11->13->1