Lecture - 11

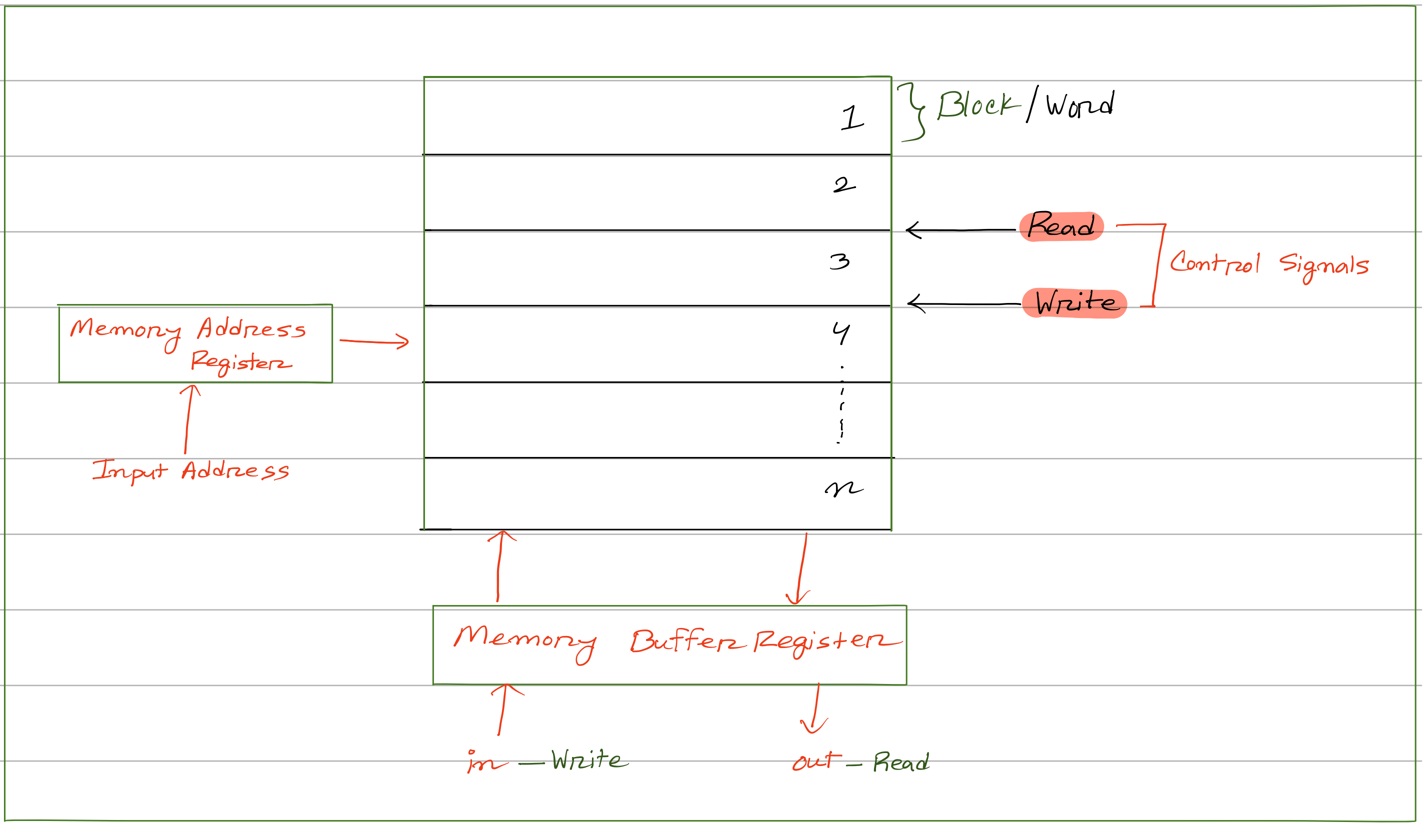


Figure : Memory Unit

\# Each block is called a Word. In the above diagram we have n words.

\# Each word we have m bits.

Read Operation:

Suppose CPU issues a Read request to the memory unit to fetch data from a specific location.

Steps:

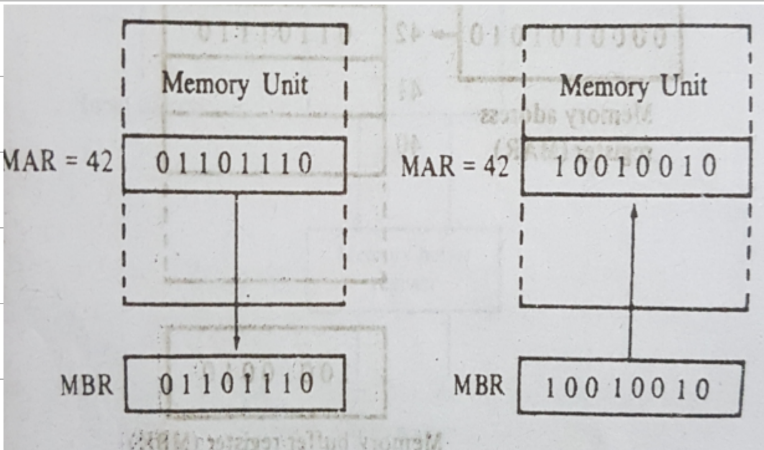
1. CPU sends the memory address from where the data will be read into the MAR.
2. The memory unit activates the corresponding memory location.
3. The read control signal will be activated. (Read = 1)
4. Data at the address is fetched and placed in the MBR.

Write Operation:

Suppose CPU issues a Write request to the memory unit to write data to a specific location.

Steps:

1. CPU sends the memory address where data will be written into the MAR.
2. Places the data to be written in the MBR.
3. The write control signal will be activated. (Write = 1)
4. Memory locates the given address and stores the Data in it.



(a) Read operation (b) Write operation

What do you understand by a 1024 X 16 bit memory.

$\underbrace{1024}_{\text{No. of words}} \times \underbrace{16}_{\text{How many bits can be stored in a word?}}$ bit memory

Memory Address (Binary)	Memory Address (Decimal)	Memory Content
00 0000 0000	0	
00 0000 0001	1	
00 0000 0010	2	
⋮	⋮	
11 1111 1111	1023	

} 16 bits can be stored

$1024 = 2^{10} \leftarrow K$

$\Rightarrow 10$

For 2^K words; the address register size will be K.

The control lines – Read & Write determine the direction of data transfer.

You can not perform read and write on a single location at the same time.

Using a Flip-Flop 1 bit data can be stored.

For 1024 X 16 bit Memory.

(a) How many F.Fs are needed to build the address reg.?

(b) " " " " " " " " buffer " ?

$2^{10} = 1024$

Soln:

address register size $\Rightarrow$ 10 ; so 10 F.Fs

buffer register size $\Rightarrow$ 16 ; so 16 FFs.

$$\text{Capacity} = \text{no. of word} \times \text{bit/word}$$

$$\text{No. of word} = 2^{\text{address line}}$$

⇒ How many address lines are needed for a 64 MB RAM with 32 bit word?

⇒ Capacity = $\underline{\text{No. of word}}$ × bit per word

⇒ $64\ MB = Y \times 32\ bits$ — B = Byte

⇒ $(64 \times 8)\ Mb = Y \times 32\ bits$ — b = Bit

⇒ $(64 \times 8 \times 1024)\ Kb = 32\,Y\ bits$ — 1 Mb = 1024 Kb

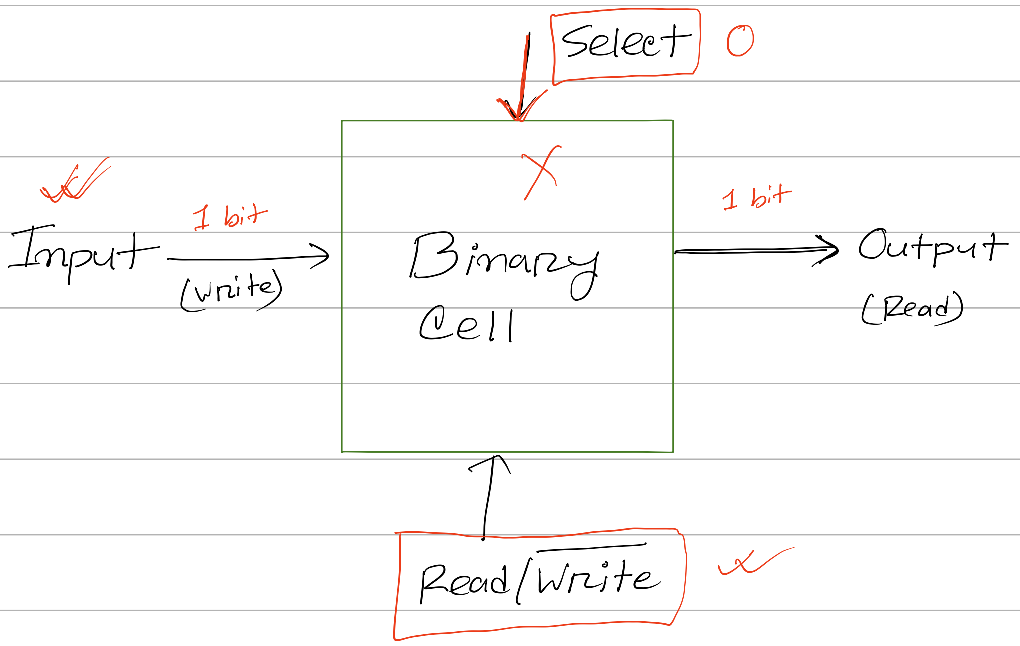
⇒ $(64 \times 8 \times 1024 \times 1024)\ b = 32Y\ b$ — 1Kb = 1024b

⇒ $Y = \dfrac{64 \times 8 \times 1024 \times 1024}{32} = 16{,}777{,}216 = 2^{24}$ → Address line = 24

Binary Cell

B.C → 1100 1010 — 8 bit

⇒ 1 binary cell can store 1 bit of data.



Design a 4X3 Ram