**BRAC UNIVERSITY**

**Department of Computer Science and Engineering**

**CSE 260: Digital Logic Design**

Examination: **Quiz 3** Semester: Spring 2025

Duration: 25 Minutes Full Marks: 15

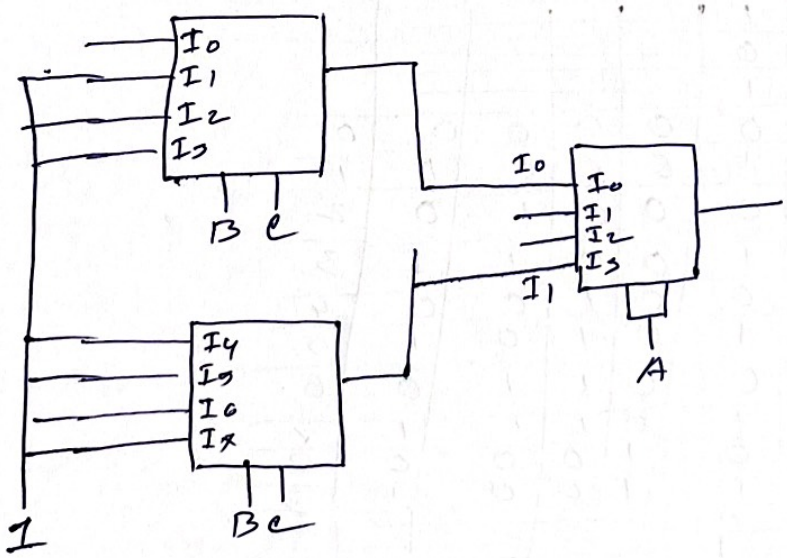
| Name: Solution | ID: |
|---|---|

Note: You must mention MSB, LSB in case of all the input and outputs.

| | | |
|---|---|---|
| **1. CO3** | Build a 3 input OR gate using three 4:1 MUX(s). (Consider A,B,C as inputs where A is MSB and C is LSB) | [8] |
| **2. CO3** | **Build** Excess-4 to BCD converter using Encoder-Decoder. | [7] |

| | A | B | C | A+B+C |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 1 |
| 3 | 0 | 1 | 1 | 1 |
| 4 | 1 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | 1 |
| 7 | 1 | 1 | 1 | 1 |

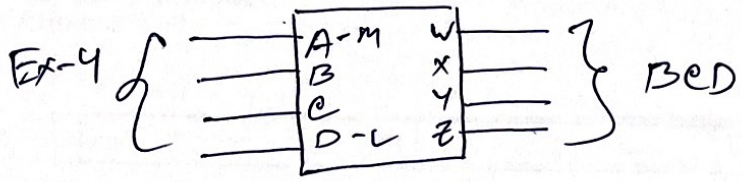
$F(A,B,C) = \Sigma(1,2,3,4,5,6,7)$

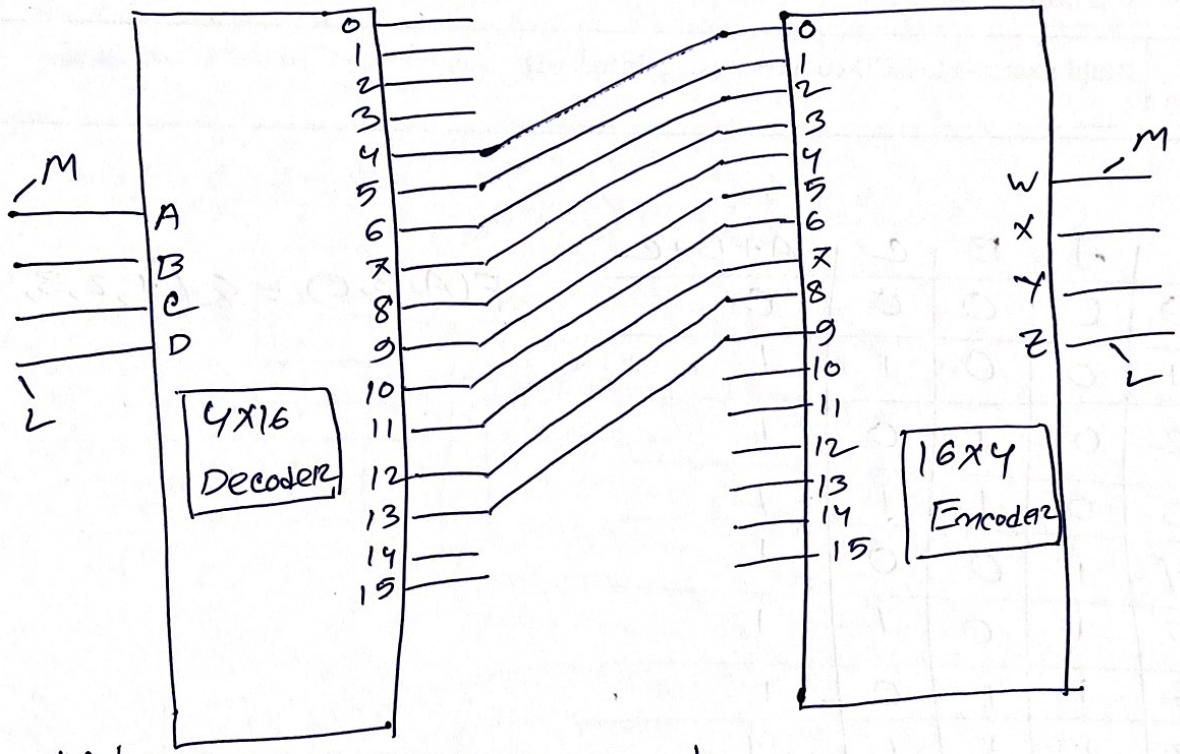


2

BCD → 0-9 → 9+4=13

1001 (4 bit)  1101 (4 bit)




| | A | B | C | D | W | X | Y | Z | |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | | | | | |
| 1 | 0 | 0 | 0 | 1 | | | | | |
| 2 | 0 | 0 | 1 | 0 | | | | | |
| 3 | 0 | 0 | 1 | 1 | | | | | |
| 4 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 2 |
| 7 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 3 |
| 8 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| 9 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 5 |
| 10 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 6 |
| 11 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 7 |
| 12 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 8 |
| 13 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 9 |
| 14 | 1 | 1 | 1 | 0 | | | | | |
| 15 | 1 | 1 | 1 | 1 | | | | | |