

## Brac University

CSE260: Digital Logic Design | Quiz – 3 | Full Marks – 9 + 6 = 15 | Time – 30 minutes | Spring 2025

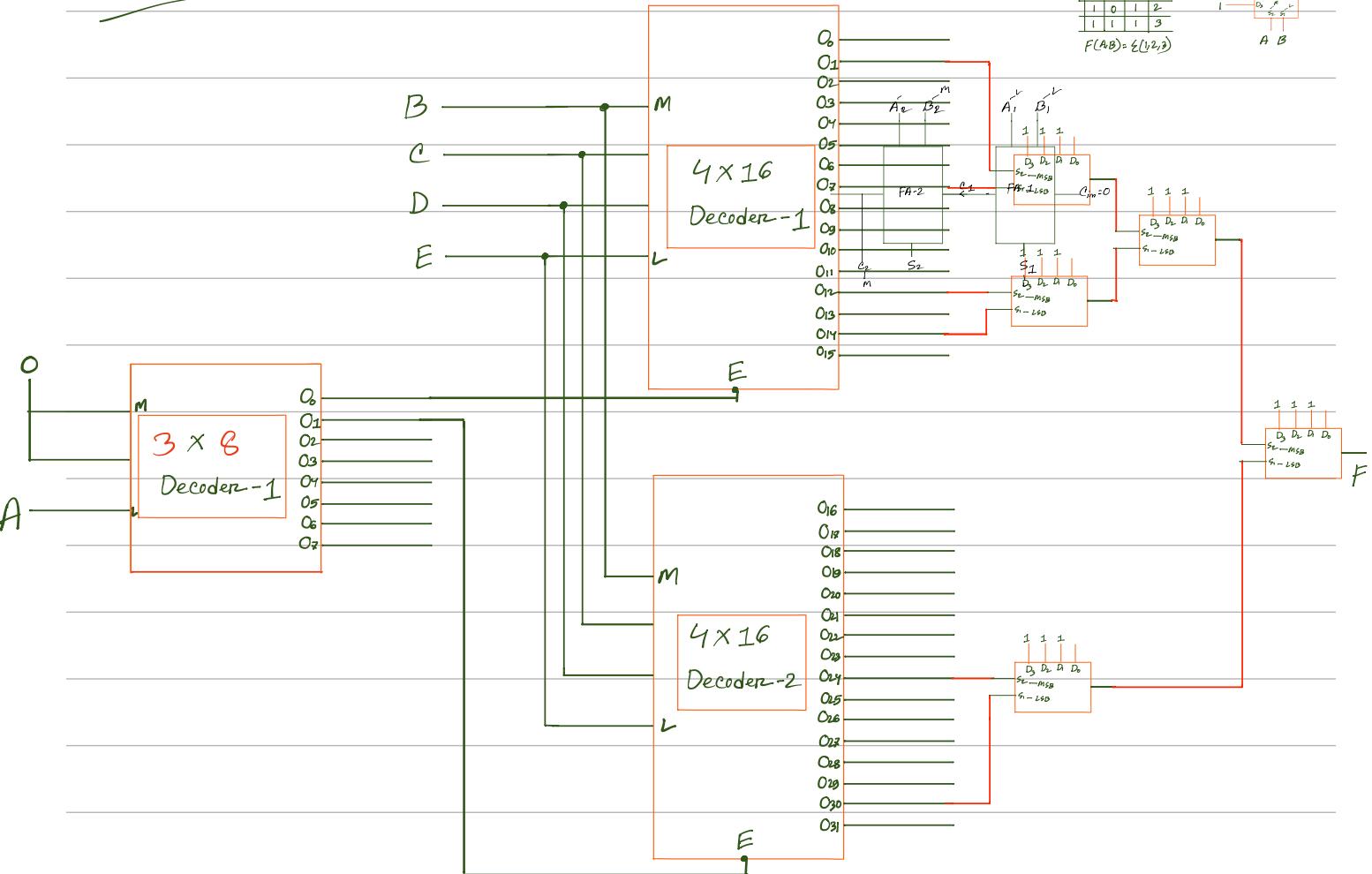
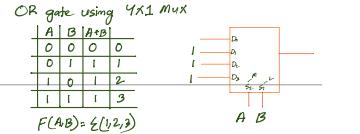
Name:

Student ID:

Section: *Solution*

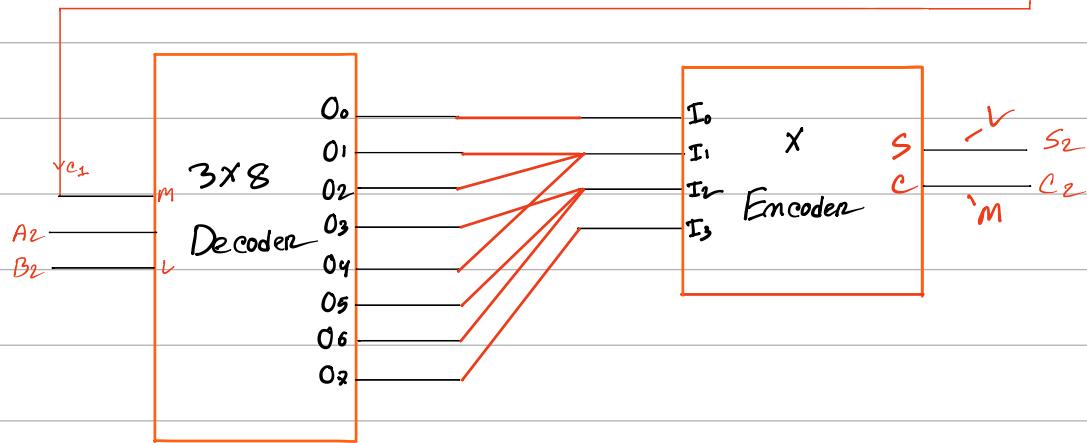
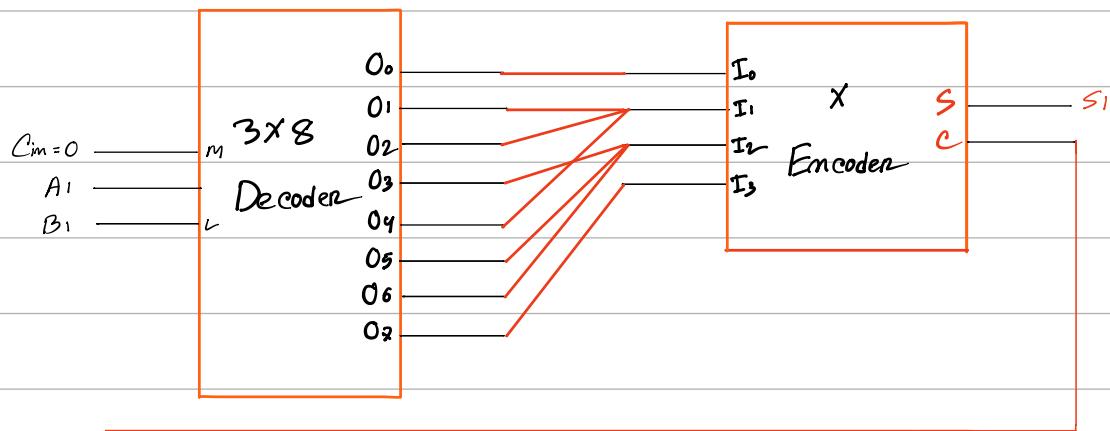
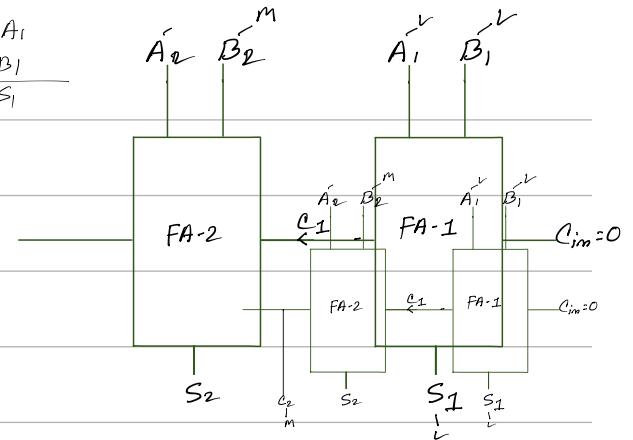
|       |   |
|-------|---|
| 1.CO3 | <b>Build</b> the following function using both 4x16 decoder(s) and 3x8 decoder(s) in a single circuit:<br>$F(A,B,C,D,E)=\sum (1, 7, 12, 14, 24, 30)$<br>If you need to use logic gates, you MUST build them using 4x1 mux(s). |
| 2.CO3 | <b>Design</b> a 2-bit parallel adder where you have to use appropriate encoders and decoders to build the internal circuit.   |

*Q-1:*



$$\begin{array}{r}
 A_2 \ A_1 \\
 + \ B_2 \ B_1 \\
 \hline
 C_2 \ S_2 \ S_1
 \end{array}$$

Q2



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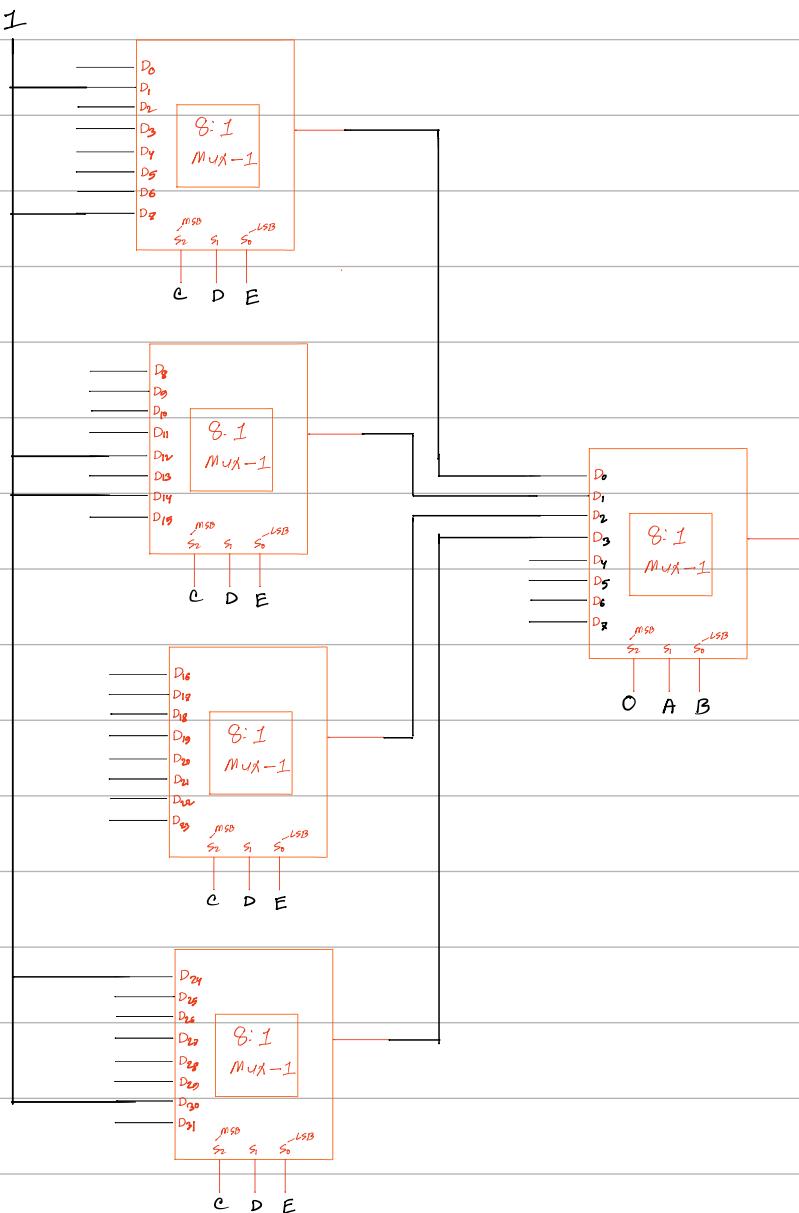
*Solution*

Student ID:

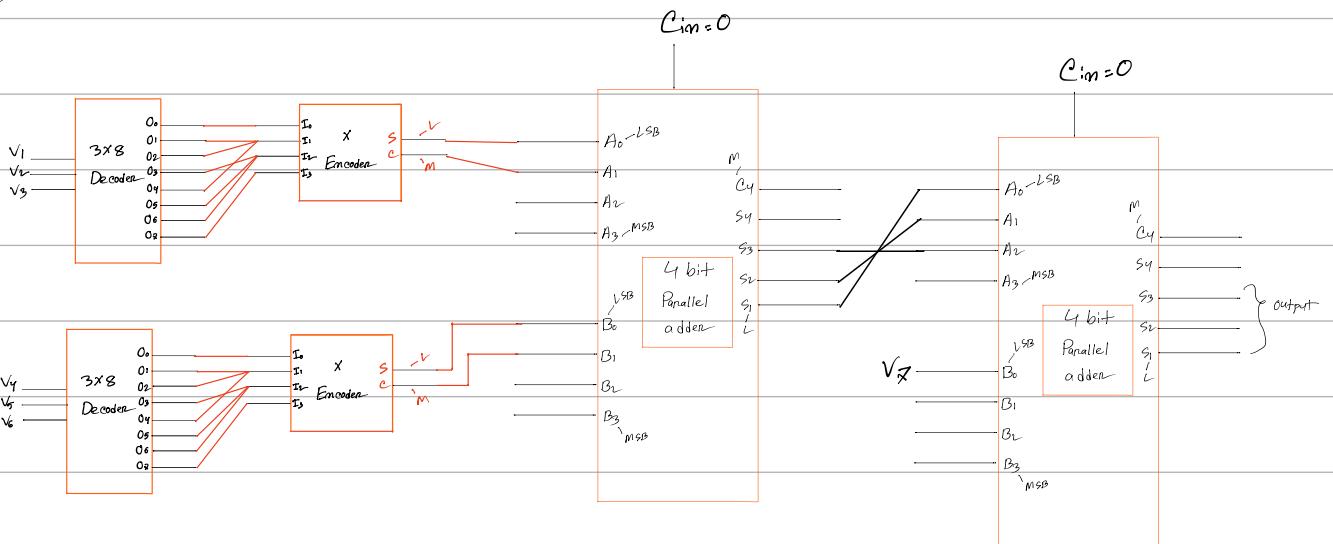
Section:

|       |  |
|-------|--|
| 1.CO3 | <b>Build</b> the following function using five 8x1 mux(s) exactly: $F(A,B,C,D,E)=\Sigma (1, 7, 12, 14, 24, 30)$ . If you need to use logic gates, you MUST build them using 4x1 mux(s).            |
| 2.CO3 | <b>Design</b> a 7 person voting system using encoder(s), decoder(s), and parallel adders. You cannot use full adders. Meaning, for the inputs, you MUST use encoder(s) and decoder(s) as required. |

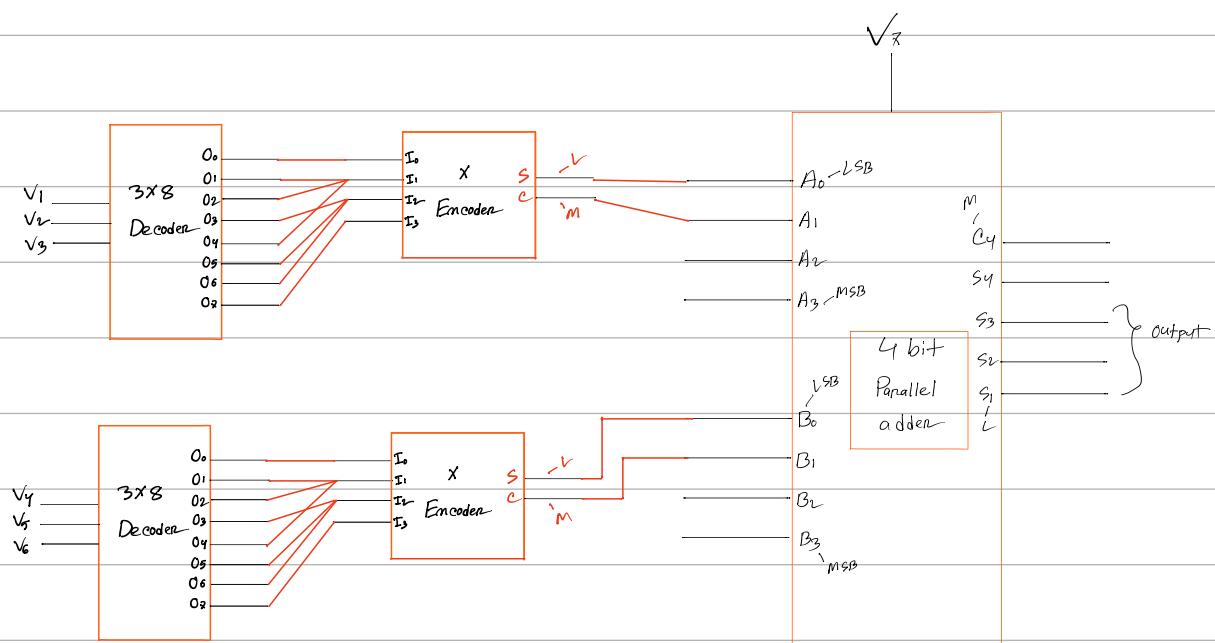
*Q1*



G2



## Alternate Solution



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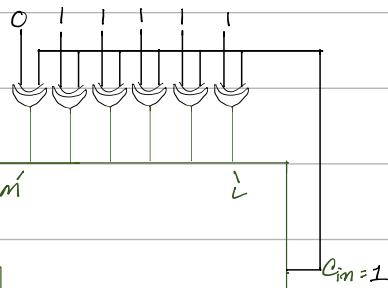
Name: *Solution*  
Section:

Student ID:

|       |  |
|-------|--|
| 1.CO3 | Build (A-31) using a 6 bit parallel adder where A and B are 6 bit numbers. Use external logic gates if required. |
| 2.CO3 | Implement the following function using only 2x4 decoder: $F(A,B,C,D) = \sum(0,2,3,5,7,11,13,15)$                 |

*Q-1*

$A_6 \quad A_5 \quad A_4 \quad A_3 \quad A_2 \quad A_1$



$$A - 31$$

$$= A + (-31)$$

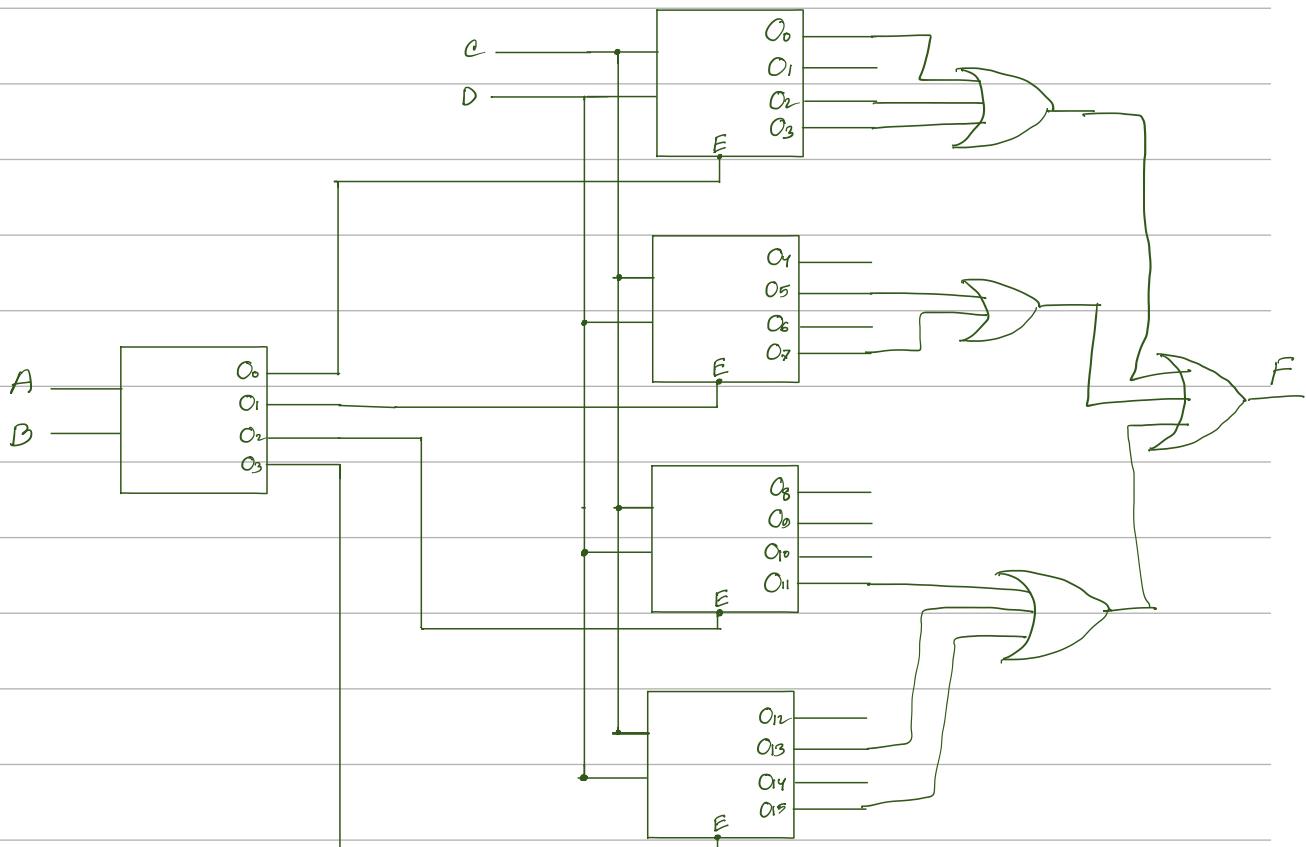
-31 in 2's comp.

$$+ 31 = 011111$$

$M \quad L \quad L'$

$c_6 \quad s_6 \quad s_5 \quad s_4 \quad s_3 \quad s_2 \quad s_1$

*Q-2*



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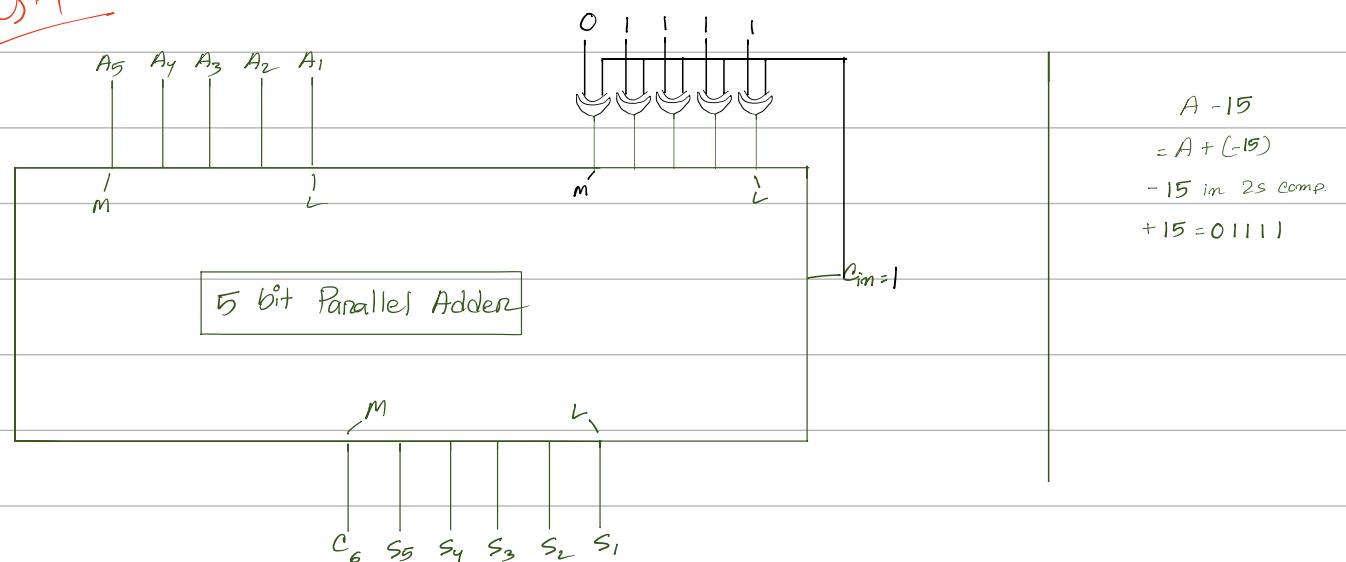
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Name: Solution  
Section:

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|       |  |
|-------|--|
| 1.CO3 | <b>Build (A-15)</b> using a 5 bit parallel adder where A and B are 5 bit numbers. Use external logic gates if required.  |
| 2.CO3 | <b>Implement</b> the following function using both $2 \times 4$ and $3 \times 8$ decoder(s) in a single circuit:<br>$F(A,B,C,D,E) = \Sigma(0,2,3,5,7,11,13,15,21,27,30)$ |

Q-1



Q-2

