BRAC UNIVERSITY

Department of Computer Science and Engineering

CSE 260: Digital Logic Design

Examination: Quiz 3
Duration: 25 Minutes

Semester: Spring 202

Full Marks: 15

Name: Solution	ID:
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Note: You must mention MSB, LSB in case of all the input and outputs.

1. CO3	Build a 3 input OR gate using a 2x1 MUX. (Consider A,B,C as inputs where A is MSB and C is LSB)	[8]
2. CO3	Build Excess-4 to BCD converter using parallel adder.	[7]

	IA	BI	c	A+B+C	1117211567
0	0	0	0	0	F(A,B,e) = &(1,3,3,4,5,6,7)
1	0	0	1	1	- [128] 12. 이 4002 22. 20. 1. 2022 (1.1.) 12. 12. 12.
2	0	+	0		AB
-4	1	0	0	1	A+B To
5	'	0	1	1	1 1 1 1
8	1		, 0		
	11		-+		
					C

	1 To	III	1
AIB'	0		
AIB	2	3	
AB'	4	6	
AB	6	②	
—	A+B	1	

A'B+AB'+AB => A'B+A(B+B) => A'B+A => (A+A) (A+B) = A+B

