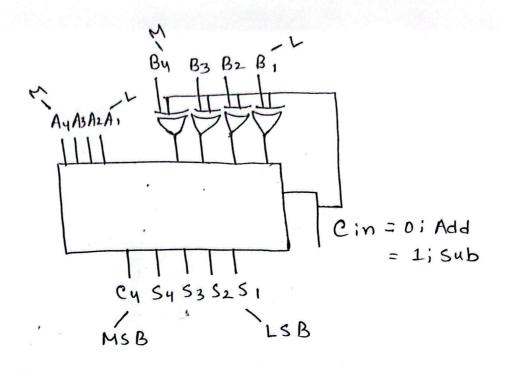
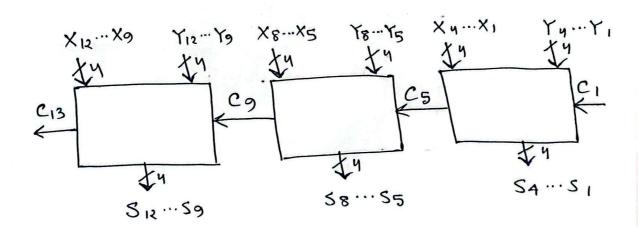
Azmani Sultana
Id: 22201949
CSE260
Section: 02
Assignment 03

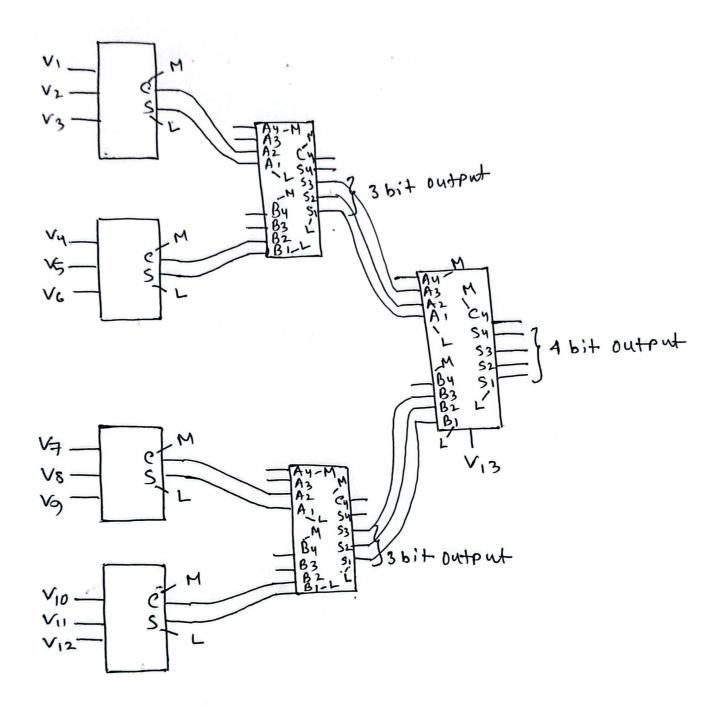
1

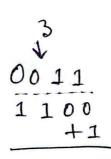


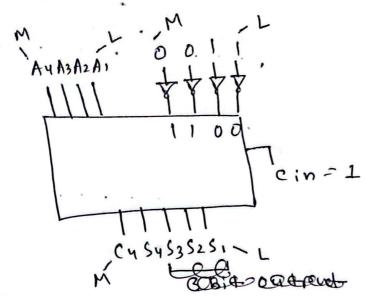
4 bit adden - subtractor

(2)

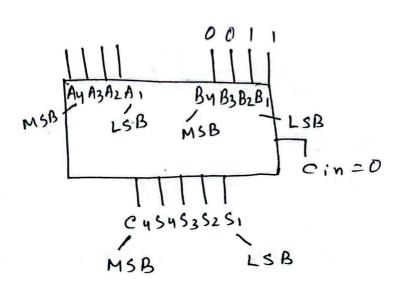


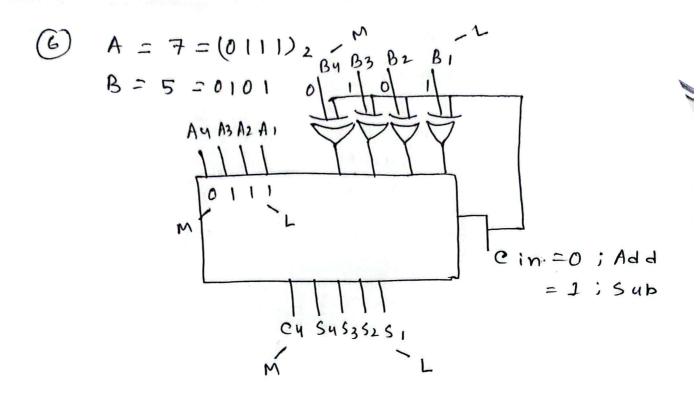




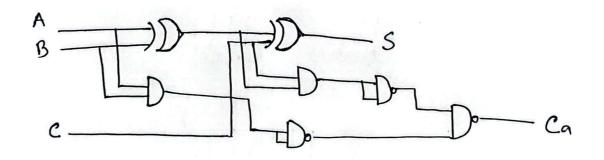


(5)

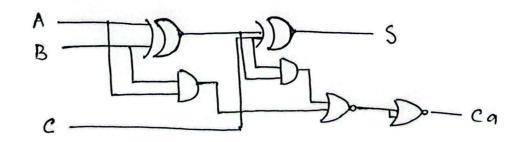




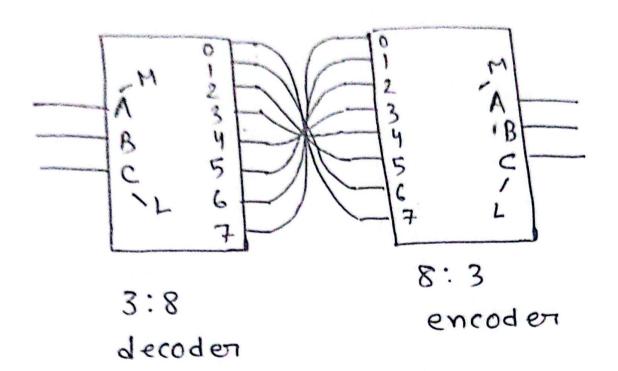
Using 3 NAND gate and no OR gates

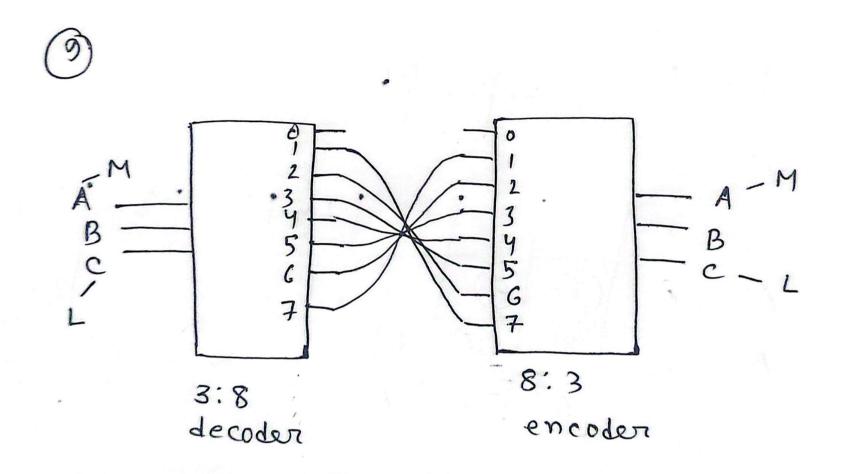


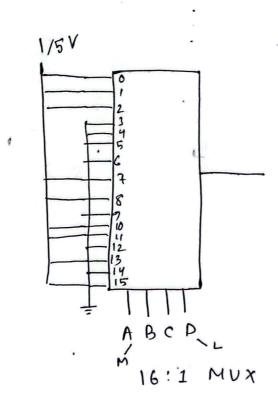
Using 2 NOR gates and no or gates

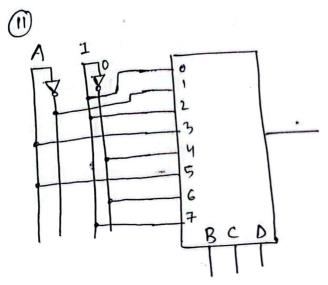




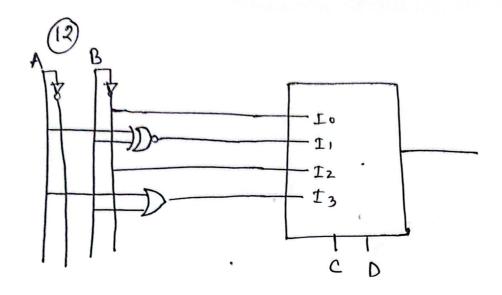








	Io	I,	IZ	I3	Iy	I 5	I6	Ia
A	0	1	(2)°	3	4	5	6	3
A	(B)	9	.0		12	(3)	14	(15)
	1	A'	1	Α	0	Α	0	1



	Ιο	II	Iz	I ₃
A'B'	0	1	(2)	3
A'B	4	5	6	7
AB'	8	9	10	
AB	12	(3)	14	(5)
	B'	AOB	B'_	A+B

$$B' \mid AOB \mid B' \mid A+B$$

$$I \circ \Rightarrow$$

$$A'B' + AB' = B' (A + Ai) = B'$$

$$I \Rightarrow A'B' + AB = AOB$$

$$I \Rightarrow A'B' + AB' = B' (A+Ai) = B'$$

$$I \Rightarrow A'B + AB' + AB = A'B + A(B+B')$$

$$= A'B + A$$

$$= (Ai + A)(B + A)$$

$$= A+B$$

