CSE341 FALL-2025 Assignment-3 & 4

1. The 8086 wants to read 2 bytes of data from an odd memory location. However, the memory operates at a slower speed than the 8086. Hence when reading the 1st byte of data, the 8086 has to wait for an additional 2 clock pulses. But the 2nd byte was read without any delay. Now assuming the 8086 is working at a frequency of 5MHz calculate the following: **[2 Marks]**

a. Calculate the duration of one clock state.
b. How many bus/machine cycles needed to execute this read instruction.
c. Calculate the duration of bus/machine cycles.
d. Calculate the value of the Instruction Cycle (in nanoseconds).
e. Calculate the values of A0 and BHE' pins while transferring the 2 bytes of data.

2. Draw the timing diagram of the **Memory-Read cycle** if there is 1 waiting state after T2. **[0.5 Marks]**
3. Draw the timing diagram of the **IO-Read cycle** if there is 1 waiting state after T2. **[0.5 Marks]**

4. Suppose a 8086 has a duty cycle of 40% and one clock state is 200 ns. **[2 Marks]**

a. Calculate value of TON and TOFF.
b. Calculate the frequency of the microprocessor.
c. Calculate the duration of one bus/machine cycle.
d. Suppose the 8086 is executing the following read instructions. Calculate the instruction cycle.
i). MOV AH, [01211H] ii). MOV BH, [01212H]
iii). MOV AX, [01211H] iv). MOV BX, [01212H]
e. Using the instruction [iii and iv] given in d and explain the pin A0 and BHE' values in each bus cycle.

---

5. Suppose, the Interrupt Vector (IV) of an Interrupt Service Routine (ISR) is 12E5Ch whose segment address is stored at memory locations 0008Eh and 0008Fh. If the segment address of this IV is 1234h, answer the following questions:

a. Calculate the value at memory location 0008Dh. **[2 Marks]**
b. Calculate the Interrupt type responsible for the above ISR.
c. What is the difference between the maskable and non-maskable interrupt?
d. Explain in detail all the steps on how an 8086 responds to a signal received on the INTR pin.

6. Assume you have a different version of the 8259A Programmable Interrupt Controller (PIC) known as PICx to control the numerous hardware interrupts. The PICx can take 14 interrupt requests using the pins IR0 - IR13. The Interrupt Service Register (ISR) size is X bits and the Interrupt Mask Register (IMR) is Y bits. The IR3 pin is masked by default. There are priority levels assigned to each request pin. Now suppose PICx is receiving multiple interrupt requests in the following order:

At T= 0ns, an interrupt request occurred at IR12 that will take 35ns to be served. **[2 Marks]**
At T= 10ns, IR10 and IR3 receive requests each of which takes 40ns to be served.
At T= 25ns, IR0 and IR2 receive requests each of which takes 50ns to be served.

a. Deduce the values of X and Y.
b. Explain the role of the Priority Resolver in PICx.
c. Explain in detail how the values of the ISR and IMR registers will change according to the above requests.
d. Calculate the value of T (time) when all the interrupt requests have been served.

7. Illustrate the way DMA operates. You may draw a diagram if you need. **[1 Marks]**

Deadline: 05/01/2026 11.59PM

The submitted file should be handwritten and scanned as a PDF file.
Naming Format: ID_Section_CSE341_Assignment3-4