QUIZ 3

Question 1:[4 marks] Write two differences between software interrupts and hardware interrupts of 8086.

Question 2:[8 marks]

Address	00117h	00116h	00115h	00114h	00276h	00277h
Data	45h	86h	22h	14h	12h	34h

Use the given table to calculate the starting address of the ISR for interrupt type 69.

Question 3: [4+4 marks] For the following instructions, mention the states of $\overline{RD}$, $\overline{WR}$, $M/\overline{IO}$, $\overline{BHE}$ pins during the T2 cycle.

a. MOV AL, [34h]

$\overline{RD}$	$\overline{WR}$	$M/\overline{IO}$	$\overline{BHE}$

b. OUT 82h, AL

$\overline{RD}$	$\overline{WR}$	$M/\overline{IO}$	$\overline{BHE}$

Question 1:[4 marks] Write two differences between maskable interrupts and non-maskable interrupts of 8086.

Question 2:[8 marks]

Address	0006A	0006B	0006C	0006D	0006Eh	0006F
Data	00h	08h	00h	03h	00h	05h

Use the given table to calculate the starting address of the ISR for interrupt type 27.

Question 3: [4+4 marks] For the following instructions, mention the states of $\overline{RD}$, $\overline{WR}$, $M/\overline{IO}$, $\overline{BHE}$ pins during the T2 cycle.

a. MOV [33h], BL

$\overline{RD}$	$\overline{WR}$	$M/\overline{IO}$	$\overline{BHE}$

b. IN AL, 82h

$\overline{RD}$	$\overline{WR}$	$M/\overline{IO}$	$\overline{BHE}$

QUIZ 4

Question 1:[8 marks] A keyboard connected to the 8086 asserts the INTR pin while the CPU is executing a program. **Explain the sequence of actions** the 8086 performs to service this **interrupt and corresponding working** of ISR, IMR, IRR, Priority Resolver, Cascade Buffer Comparator, Data Bus, INT and INTA' pin.

Question 2:[2+8+2 marks] Assume you have a modified version of the 8259A Programmable Interrupt Controller called **PICy** to manage hardware interrupts. The PICy can accept **8 interrupt requests** through the pins **IR0–IR7**. The size of the **Interrupt Service Register (ISR)** is **X bits** and the size of the **Interrupt Mask Register (IMR)** is **Y bits**. The interrupt pins **IR1 and IR6 are masked by default**, and priority levels are assigned such that a lower IR number has a higher priority. Now suppose PICy receives multiple interrupt requests in the following order:

- at **T = 0 ns**, an interrupt request occurs at **IR4** that takes **30 ns** to be serviced;
- at **T = 5 ns**, interrupt requests occur simultaneously at **IR2 and IR7** that requires **25 ns** of service time;
- at **T = 15 ns**, an interrupt occurs at **IR0 and IR1** that takes **40 ns** to be serviced; and
- at **T = 20 ns**, an interrupt occurs at **IR6** that takes **35 ns** to be serviced.

Now Answer the following questions:

a. Deduce the values of **X and Y**.
b. Describe in detail how the contents of the **ISR and IMR registers** change as the interrupts are serviced,
c. Calculate the time at which all valid interrupt requests have been completely serviced.

Question 1:[8 marks] In an 8086 system used for real-time image capture, an external ADC triggers the 8237 DMA controller to move continuous pixel data directly into RAM. **Explain the DMA operation sequence and the corresponding states** of HRQ, HLDA, DREQ, DACK, IOR', IOW', READY, MEMR', and MEMW'.

Question 2:[2+8+2 marks] Consider a PICx controller based on the 8259A architecture that supports **nested interrupt handling**. The controller can accept **8 interrupt requests through IR0–IR7**, where **IR0 has the highest priority** and **IR7 has the lowest priority**. The **Interrupt Service Register (ISR)** and **Interrupt Mask Register (IMR)** have sizes of **X bits** and **Y bits**, respectively, and tThe interrupt pins **IR1 and IR6 are masked by default**. Suppose the following interrupt requests are generated:

- at **T = 0 ns**, an interrupt occurs at **IR5** that takes **50 ns** to be serviced;
- at **T = 12 ns**, an interrupt occurs at **IR2 and IR7** that requires **30 ns** of service time;
- at **T = 18 ns**, an interrupt occurs at **IR1 and IR3** that requires **20 ns** to be serviced; and
- at **T = 40 ns**, an interrupt occurs at **IR6** that takes **25 ns** to be serviced.

Now Answer the following questions:

a. Deduce the values of **X and Y**.
b. Describe in detail how the contents of the **ISR and IMR registers** change as the interrupts are serviced,
c. Calculate the time at which all valid interrupt requests have been completely serviced.