BRAC University

CSE341: Microprocessor

Quiz#3

Duration : 20 Minutes

Total Marks : 20

ID: **Name:** **Sec:**

1.

Address	00083h	00084h	00085h	00086h	00087h	1B5C0h	1B5C1h	1B5C2h
Data	9Ch	A0h	15h	02h	1Ah	5Bh	6Eh	78h

a. Explain if the interrupt caused by the INT 33 instruction is maskable or not. Provide your reasoning. [1]

b. If the Intel 8086 encounters the INT 33 instruction, then calculate the starting address of the corresponding ISR. Also, what will be the first 2-byte hex instruction that will be fetched to the instruction queue from the ISR? [1 + 2 + 1]

c. Explain in detail all the steps on how an 8086 responds to a signal received on the INTR pin. [4]

2. A student designed a new PIC called 'PIC 2.0' which takes 20 interrupt requests via its IRR0 –IRR19 pins. The size of its Interrupt Mask register (IMR), Interrupts Service Register (ISR), and Interrupt Request Register (IRR) is 20 bits. It also has 4 Cascading (CAS) pins.

a. Assume the value of ISR0 - ISR4 is 10000, the value of IMR0 - IMR4 is 10101, and the value of IRR0 - IRR4 is 01110. Now, explain the order in which the interrupts IR0-IR4 will be serviced. Assume IR0 has the highest priority and IR19 has the least priority. [3]

b. Calculate the maximum number of interrupts that a master PIC 2.0 can handle in cascade mode. Show necessary calculations. [2]

c. Due to a design flaw in the PIC 2.0, the student noticed that the master PIC 2.0 could not communicate with all the connected 20 slave PIC 2.0s. Explain how you would correct the flaw in the design so that the master can communicate with all the 20 slave PIC 2.0s. [2]

d. Explain 2 possible methods of stopping the servicing of any interrupts between the master and the 8086 without disconnecting the wires or disabling the INTR / INT / INTA' pins. [2]

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CSE341 : Microprocessors

Quiz#4

Duration : 25 Minutes

Total Marks : 20

ID: **Name:** **Sec:**

If XXXX are the first 4 digits of your student ID, consider the following instructions:

i. MOV AX, [$XXXX_h$]
ii. IN AL, [$XXXX_h$]
iii. IN AL, DX where DX = $XXXX_h$

a. Find the instructions which are valid and invalid from the given ones, provide your reasoning. [3]
b. If instruction (i) and instruction (iii) both are being used for I/O, what are their addressing types? What are their differences? [2 + 3]
c. Briefly explain the data transfer process between memory and I/O when 8237 DMAC is being used. [7]
d. Suppose, we are using an intel 8237 DMAC which has a faulty DREQ pin. Now we cascade the DMAC with full first-level cascading. How many I/O channels can we use? If the last digit of your student ID is X, consider the X-th I/O channel is also not working. Again, we cascade the second level of DMACs fully. How many I/O channels do we have now? Show your working. [2 + 3]