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Section 5

Assignment 2

(1) a)

$$\text{Duty cycle} = 50\%$$

$$T_{on} = 60 \text{ ns}$$

$$T_{on} = T_{off} = 60 \text{ ns}$$

$$T = T_{on} + T_{off} = 60 + 60 = 120 \text{ ns}$$

$$f = \frac{1}{T} = \frac{1}{120 \times 10^{-9}} = 8.33 \text{ MHz}$$

b) MOV AX, [1235h]

$$1235h \rightarrow \text{odd}$$

AX \rightarrow 16 bit register

A word access from an odd address requires two memory read bus cycles.

$$1 \text{ bus cycle} = 4 \text{ T-states}$$

$$\text{Total T-states} = 4 \times 2 = 8$$

$$\text{Total instruction time} = 8 \times 120 = 960 \text{ ns}$$

c)

Cycle 1:Address: 1235h \rightarrow odd

$$A_0 = 1, \overline{BHE} = 0$$

Reason: Accessing an odd address, $A_0 = 1$ disables the

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even bank, while $\overline{BHE} = 0$ enables the odd bank (lines D15 - D8)

Cycle 2:

Address: 1236h \rightarrow even address \rightarrow $A_0 = 0$

$A_0 = 0$, $\overline{BHE} = 1$

Reason: Accessing the even address.

$A_0 = 0$ enables the even bank (lines D7 - D0), while $\overline{BHE} = 1$ disables the odd bank.

(2) a)

$$T = \frac{1}{f} = \frac{1}{5 \text{ MHz}} = 200 \text{ ns}$$

Word from odd address \rightarrow 2 memory read bus cycles

$$\text{1st bus cycle} = 4T + 2T = 6T$$

$$\text{2nd bus cycle} = 4T$$

$$\text{Total} = 6T + 4T = 10T$$

$$\text{Instruction cycle time} = 10 \times 200 = 2000 \text{ ns}$$

b)

Bun cycle	A_0	\overline{BHE}	Description
1st	1	0	Accesses Upper Bank (D8 - D15)
2nd	0	1	Accesses Lower Bank (D0 - D7)

c) Total clock period $\Rightarrow T = 200\text{ ns}$

Duty cycle = 60%.

$$T_{ON} = 200 \times 0.60 = 120 \text{ ns}$$

$$T_{\text{loss}} = 0.40 \times 200 = 80 \text{ ns}$$

(3) a)

$$T_{CPU} = \frac{1}{f_{CPU}} = \frac{1}{5MHz} = 0.2ms = 200ns$$

Total cycle = 1 + 2 = 6

Total time = $6 \times 0.2 = 1.2ms$

b) $T_{high} = 0.33 \times 200 = 66ns$

Total time High = Total cycles $\times T_{high}$

$$= 6 \times 66 = 396ns$$

$d_{01} = 8 \times d_{00} = 20ns$

$d_{00} = 8 \times d_{00} = 20ns$

$d_{02} = 8 \times d_{00} = 20ns$

$d_{03} = 8 \times d_{00} = 20ns$

$d_{04} = 8 \times d_{00} = 20ns$

$d_{05} = 8 \times d_{00} = 20ns$

$d_{06} = 20ns$

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④ The difference between non-maskable and maskable interrupt?

Maskable interrupt	Non-Maskable, Interrupt
Can be disabled by software	Cannot be disabled by software
Controlled by IF	Independent of IF
Lower priority	Highest priority
Interrupt type is variable	Interrupt type is fixed
Used for normal I/O operation	Used for critical system events
can be delayed or ignored	Must be serviced immediately
generated through INTR pin	generated through NMI pin
Used for keyboard, timer, I/O devices	Used for power failure, parity error

⑤ a) Yes, the flag register bits change.

When an Intel 8086 microprocessor decides to service an interrupt (INTR), it performs a sequence of operations to preserve the current state and prepare for the interrupt service routine (ISR). It performs the following automatically:

- i) Pushes FLAGS onto the stack
 - ii) Clears IF
 - iii) Clears TF
- b) Interrupt type = $68 \text{d} = 100100\text{b}$

$$\text{Address} = 68 \times 4 = 272 = 110\text{h} = 00110\text{h}$$

Address $00110\text{h} \rightarrow$ value 45h

Address $00111\text{h} \rightarrow$ value 86h

$$\text{New IP} = 8645\text{h}$$

Address $00112\text{h} \rightarrow$ value 23h

Address $00113\text{h} \rightarrow$ value 14h

$$\text{New CS} = 1422\text{h}$$

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Q) In an 8086 microprocessor system, when multiple interrupts occur at the same time, the processor resolves them based on a fixed internal interrupt priority schedule. When both Single Step and Divide Error interrupts occur simultaneously, the Divide Error interrupt (Type 0) is serviced first. This is because the divide error is detected during instruction execution, whereas the single step interrupt is generated after successful completion of an instruction.