Timing Diagrams:

1. Suppose you have an Intel 8086 which is operating at a Duty Cycle of 60% and for each clock pulse assume T_{off} = 40ns. The 8086 is now going to execute the instruction MOV [1235h], AX. Based on this, answer the following questions:

a. Estimate the frequency at which the 8086 is operating.
b. Calculate the total time for one Instruction Cycle of the given instruction.
c. Calculate the values of the A_0 and BHE' pins during the execution of the given instruction.

2. Suppose an 8086 is operating in a way such that T_{ON} is 1/4th of the total time required for one clock pulse. Consider T_{ON} is 30ns. Now the 8086 is going to execute the instruction MOV AX, [2315h] i.e. 16 bits of data will be read from memory.

a. Calculate the frequency in MHz at which the 8086 is operating.
b. Calculate the time required for 1 Machine / Bus Cycle.
c. Deduce the total time required to execute the given instruction MOV AX, [2315h].
d. Explain with proper reasoning the values of pins A_0 and BHE' during the execution of the given instruction MOV AX, [2315h].

3. For the following instructions, mention the states of $\overline{RD}$, $\overline{WR}$, $M/\overline{IO}$, $\overline{BHE}$ pins during the T2 cycle.

a. MOV AL, [34h]
b. MOV [33h], BL
c. OUT 82h, AL
d. IN AL, 82h

4. 8086 executes MOV AX, [1233H] on a system clocked at **20MHz** with **a 50% duty cycle**.

(a) Draw the **timing diagram** for both bus cycles showing A0–A19, D0–D15, ALE, RD, DEN', DT/R', and BHE'.

(b) Label the states (T1–T4) and indicate where the address and data appear.

(c) Highlight where a **wait state** would be inserted if memory response was delayed by 1 cycle during the first byte transfer.

Memory Banks:

1. The 8086 is executing the instruction MOV AX, [5679H] and the RAM is organized in two banks (even and odd).

(a) Identify whether this is an aligned or unaligned word access.
(b) Determine the values of A_0 and BHE' for each bus cycle.
(c) Which memory bank(s) will be accessed in each cycle?
(d) Draw a 2-step data bus usage summary for this instruction, specifying data lines and accessed addresses.

2. A 64-bit processor is attempting to read a 64-bit (8-byte) word from memory, where each memory bank is 8 bits wide and memory banking is used to improve performance. The read begins at byte address 03H.

Determine whether this address is aligned or unaligned. Then, calculate how many memory cycles are required to complete the full 8-byte read operation from this unaligned address. Justify your answer based on how data is distributed across the memory banks.

3. An 8086 cpu has a RAM of 1MB split into two equal memory banks. The A_0 and BHE' pins of the cpu are used to access the two memory banks. For each of the given instructions, determine the following information:

(i) Size of the data being transferred (byte/word)
(ii) Which portion of the data bus was used to transfer the data from source location to destination register
(iii) Value of A_0 and BHE' required to make the transfer
(iv) Memory bank from which the data is fetched
(v) Total number of data cycles used to move data

4. Assuming DS=0000h, consider the following instructions-

a. MOV AH, [8086h]
b. MOV AL, [8086h]
c. MOV AX, [8086h]
d. MOV BH, [8085h]
e. MOV BL, [8085h]
f. MOV BX, [8085h]

5. Complete the following table:

Instruction	Size	Address	A_0	BHE'	Memory Bank(s) Used	Bus Cycles
MOV AX, [1001H]	Word	Odd	?	?	?	?
MOV AH, [1002H]	Byte	Even	?	?	?	?
MOV BX, [1000H]	Word	Even	?	?	?	?
MOV DL, [1003H]	Byte	Odd	?	?	?	?

6. Suppose a faulty compiler always places 16-bit variables at **odd addresses**.

(a) What performance penalty would this impose on the 8086?
(b) How would this affect the values of A_0 and BHE'?
(c) If a memory system adds a 1-cycle delay for switching banks, estimate the impact of misalignment across 1000 instructions.

7. Imagine Intel redesigned the 8086 to support 4 memory banks, each 4 bits wide.

(a) How would this change the A_0/BHE' decoding logic?
(b) How many control lines would be needed to select among 4 banks?
(c) For a word access from an unaligned address, how many banks and cycles are now involved?

Interrupts:

1. Explain how the 8259A PIC manages to handle multiple interrupt requests using a single interrupt pin (INTR) of the 8086 microprocessor. Use a simple diagram or sequence to illustrate the handshake process.
2. A student developed a custom interrupt controller named "PIC-X", which can handle 16 interrupt requests via pins IR0 – IR15. It has three 16-bit registers: Interrupt Request Register (IRR),Interrupt Mask Register (IMR), In-Service Register (ISR)

   Each bit corresponds to one interrupt line, where bit 0 represents IR0 (highest priority) and bit 15 represents IR15 (lowest priority).

   Assume the following partial values for bits 0–5 of these registers:

   ISR[0–5] = 001000

   IMR[0–5] = 010101

   IRR[0–5] = 111001

   a. Identify which interrupt(s) are currently being serviced.
   b. Identify which interrupt(s) are currently masked and hence cannot be serviced.
   c. Determine the order in which the pending interrupts from IRR will be serviced, if any.

   [Assume IR0 has the highest priority, and only one interrupt can be serviced at a time.]

3. Assume the table below represents a portion of the 8086 memory address space. At the time of execution, the microprocessor has the following register values:

   SS = 1F00h, SP = 10FAh
   CS = 2A00h, IP = 1230h

   Suddenly, a signal arrives at the INTR pin.

Address	00A08h	00A09h	00A0Ah	00A0Bh	00100h	00101h	00102h	00103h
Data	34h	12h	78h	56h	78h	56h	34h	12h

a. Which bits of the FLAGS register will change when the interrupt is accepted? Explain briefly.
b. If the signal corresponds to interrupt type 40h, determine the new values of IP and CS as the 8086.
c. Show how the stack changes after the interrupt is acknowledged (show what values are pushed and where, in terms of addresses)

4. Suppose the CS value needed to reach a particular Interrupt Service Routine (ISR) is A12Bh, and it is stored at memory locations 000B2h (low byte) and 000B3h (high byte). Additionally, suppose the physical address of the ISR is A45D4h.

a. Determine the Interrupt Type that triggered this ISR.
b. Calculate the value that will be stored at memory location 000B1h.

5. A new PIC "Z" handles 16 interrupt request lines and mimics the 8259A architecture.

a. What is the size of the Interrupt Request Register (IRR), Interrupt Service Register (ISR), and Interrupt Mask Register (IMR)?
b. Justify if 8 data bus lines would be sufficient to communicate with an 8086 processor

6. Design a scenario where the PIC "X" is in cascading mode with 1 master and multiple slave PICs.

a. If PIC "X" can support 10 IR lines per controller, how many PICs are required to support 100 I/O devices?
b. How many cascade lines must be implemented?.

7. A new PIC handles 16,384 interrupts.
a. Calculate the number of bits needed to uniquely identify each interrupt type.
b. What implication does this have on the internal architecture of the PIC?

8. You are designing a PIC named “X” with 12 interrupt request lines (IR0–IR11). At some point during operation, the following register states are observed:

IRR = 000001000000

ISR = 000000010000

IMR = 000000100100
An interrupt request is now received on **IR5**.

a. Will the PIC generate a new interrupt signal to the CPU?
b. Will the currently executing ISR (IR4) be stopped? Justify your answers.

9. PIC “X” is designed to support **4096 types of interrupts**. It communicates interrupt type information to the 8086 via the data bus.

a. How many bits are required to encode 4096 types of interrupts.
b. Based on this, how many **data bus lines** should be connected between PIC “X” and the 8086 processor?

10. PIC “X” is connected to the 8086 and designed to support **4096 different interrupt types**. If each interrupt type takes 4 bytes in the interrupt vector table, how much memory is required for the complete table?

Addr	C1h	C2h	C3h	C4h	4710h	4711h	190h	191h	192h	193h
Data	7Ah	1Dh	2Bh	9Eh	22h	44h	5Ch	6Fh	88h	1Ah

a. Deduce the size of the Interrupt Vector Table (IVT) of the Intel 8086.
b. Calculate the interrupt vector of the ISR corresponding to the interrupt caused by INT 45. Also, deduce the first 2-byte hex instruction that will be fetched to the instruction queue from the ISR.
c. Explain in detail the actions taken by 8086 when responding to an interrupt request in the INTR pin.

11. When servicing an interrupt explain why does the 8086 clear IF and TF?

Basic I/O System, DMA and DMAC:

1. Explain what is variable addressing? Which register is used for variable addressing?

2.

A. To adopt the utility of 15 channels, estimate the minimum number of secondary 8237 DMA controllers needed.
B. Construct the DMA cascading diagram based on your answer in (A). Your diagram should show how the secondary controllers are connected with the primary controller using the appropriate pins.

3. Describe the values of the given pins of an 8237 DMA Controller during a DMA write cycle: i. $\overline{IOR}$ ii. $\overline{IOW}$ iii. $\overline{MEMW}$ iv. $\overline{MEMR}$

4. Describe the values of the given pins of an 8237 DMA Controller during a DMA read cycle: i. $\overline{IOR}$ii. $\overline{IOW}$ iii. $\overline{MEMW}$ iv. $\overline{MEMR}$

5. For data transfer the following scenarios, among programmed I/O, Interrupt based I/O and DMA based I/O, which one would you prefer and why?

a. Matrix keypad connected to a door locking mechanism
b. Power outage detection in computers
c. Transferring data from Hard disk to RAM.

6. How many I/O ports does the 8086 processor support in the isolated I/O method?

7. A particular I/O device utilizes the MOV operation to take input from a temperature sensor. Is the device memory-mapped or isolated?

8. i. IN AX, DX ii. MOV AX, [1234h] Explain in detail how the I/O addressing technique in i. and ii. is different from each other.

9. Suppose a developed data acquisition system which is using an Intel 8086 microprocessor interfaced with an 8237 DMA controller. Where a high-speed

memory-mapped sensor periodically sends large blocks of data that need to be stored directly into memory without involving the CPU.

During one such transfer, the sensor sends a signal to the DMA controller indicating that data is ready to be moved. The DMA controller initiates a DMA operation to transfer the data from the sensor to system memory.

Explain the sequence of operations that takes place between the DMA controller, the 8086 CPU, memory, and the sensor during the mentioned DMA process. Also, describe the expected states of the following control signals at each stage: HRQ, HLDA, DREQ, DACK, IOR', IOW', READY, MEqqqqqqMR', and MEMW'.