CSE341: Microprocessors
Assignment 2

Deadline: 05.01. 2026; 11:59 PM

MOV AX, [1235h]

1. Suppose you have an Intel 8086 which is operating at a Duty Cycle of 50% and for each clock pulse assume T_{on} = 60ns. The 8086 is now going to execute the instruction above.
   Based on this, answer the following questions:
   a. Estimate the frequency at which the 8086 is operating.
   b. Calculate the total time for one Instruction Cycle of the given instruction.
   c. Calculate the values of the A_0 and BHE' pins during the execution of the given instruction. Explain the reasons for each value.

2. Suppose an 8086 wants to read 2 bytes of data from an odd memory location. Now, the memory is working at a slower rate than the 8086. Hence, when reading the 1st byte of data, the 8086 has to wait for an additional two clock pulses. But the 2nd byte was read without any delay. Now, assuming the 8086 is working at a frequency of 5MHz, calculate the following:

a. The value of the Instruction Cycle (in nanoseconds).
b. The values of A0 and BHE' pins while transferring the 2 bytes of data.
c. The value of T_ON and T_OFF, assuming the 8086 is running at a duty cycle of 60%.

3. Suppose you have an Intel 8086 which is operating at 5 Mhz frequency. The memory is working at 3 Mhz. The duty cycle for both is 33%. While executing the instruction MOV [1234h], AX, 8086 sits idle for 2 clock cycles.

a. Find out the total time taken for executing the instruction.
b. Estimate the total time the clock signal was high for the whole instruction.

4. What is the difference between non-maskable and maskable interrupt?

5. Assume the above table is a portion of the current memory address space of an Intel 8086. The microprocessor currently has the following values in its registers: SS = 2000h, SP = 1124h, CS = 3000h, IP = 1450h. Now, a signal arrives at the INTR pin of this 8086.

Address	00110h	00111h	00112h	00113h	00272h	00273h	00274h	00275h
Data	45h	86h	22h	14h	12h	34h	56h	78h

a) Do the flag register bits change if the 8086 decides to service the interrupt? Explain with reasoning

b) If the signal is of Interrupt type 68, then deduce the values of CS and IP as the 8086 starts the service routine.

6. In an 8086 system, both **Single Step Interrupt** and **Divide Error Interrupt** are active. The Single Step Interrupt is used for debugging, and the Divide Error Interrupt occurs when a division by zero is encountered during program execution. Assume the program is being single-stepped, and a division by zero occurs during one of the instructions.

If both of the interrupts occur simultaneously, which interrupt will be serviced first? Justify your answer with proper reasoning along with a diagram.