

CSE 341: Microprocessors
Department of Computer Science and Engineering
Brac University

Examination: Quiz 4

Semester: Fall 2025

Duration: 25 Minutes

Full Marks: 15

Name:

ID:

Section:

Answer all the questions.

- a. To adopt the utility of 13 I/Os, estimate the minimum number of secondary/2nd-level 8237 DMA controllers needed. [2]

Ans. 3

- b. Illustrate the DMA cascading **diagram** based on your answer in (a). Your diagram should show how the secondary controllers/ 2nd level are connected with the primary controller/1st level using the appropriate pins. [4]

- c. Write down the values of the given pins of an 8237 DMA Controller during a DMA read cycle: i. **IOR**' ii. **IOW**' iii. **MEMW**' iv. **MEMR**' [2]

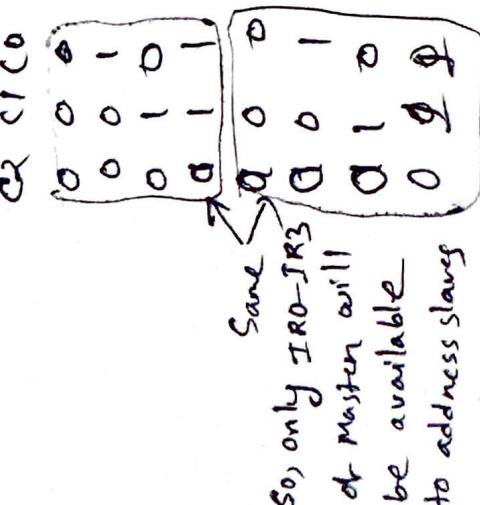
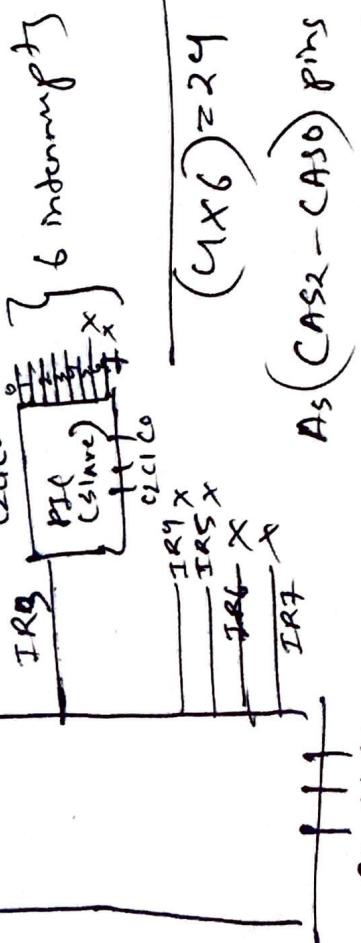
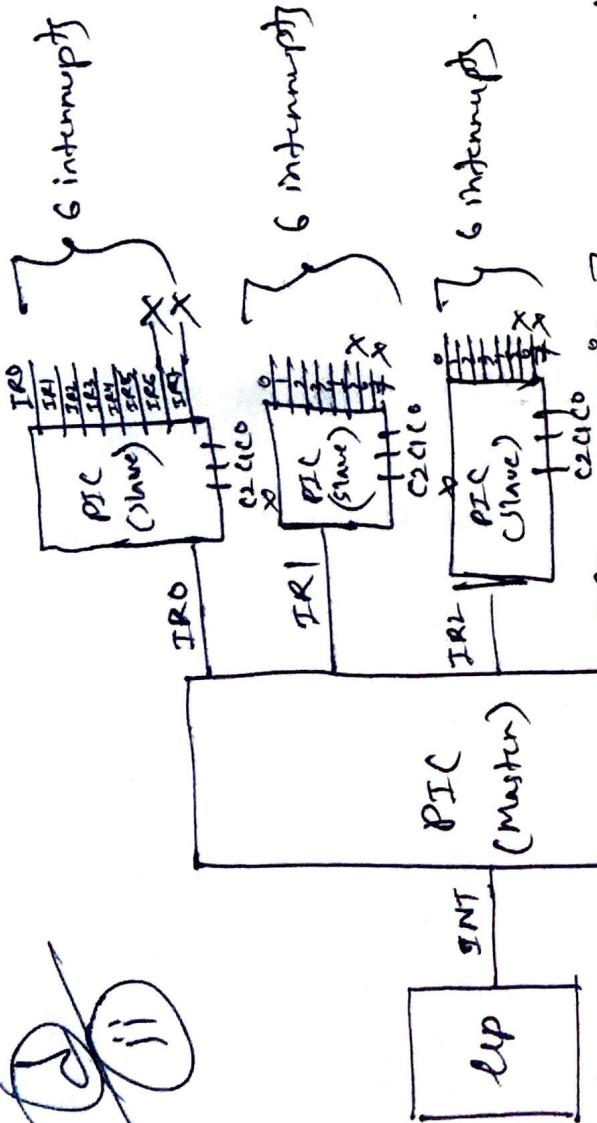
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- d. Assume you have several faulty 8259 PICs where the **IR6** and **IR7** pins do not work, and **CAS2** is always giving a **low (0)** signal.

- i. In this scenario what will be the maximum number of interrupts that can be serviced through these faulty PICs at 1st-level cascading? [2]

Ans. 24

- ii. For a particular project, your microprocessor needs to provide service to 18 interrupts coming from I/O devices. If you use the same faulty PICs mentioned above then explain **how many** slave PICs will be required? Also using the proper diagram **illustrate** how the master and slave PICs will be connected with each other. [1+4]



As $(CA_{S2} - CA_{S0})$ pins are used to address slaves/slave PICs and second level cascading 2nd level cascading is not possible so, IRQ_1, IRQ_5 pins will simply pass interrupt signals to master PIC.

And using tree faulty PICs, to service 18 interrupt we will need at least 3 slave PICs. [just draw 3 slave PICs in tree diagram]