Question 1

An 8086 microprocessor is executing the instruction MOV AX, [1A3Ch] on a system clocked at 25 MHz with a 40% duty cycle.

A. The time duration of one clock cycle (T-state) and The total time required to execute this instruction (assume standard 4 T-states) [3]
B. Draw the complete timing diagram for the instruction. [3]
C. If there are 500 aligned word reads and 500 unaligned word reads, how much time would they take? [2]

Question 2

Interrupt Vector Table (IVT):

Address	**000B0h**	**000B1h**	**000B2h**	**000B3h**	**000E8h**	**000E9h**	**000EAh**	**000EBh**
Data	40h	05h	00h	18h	C0h	03h	00h	22h

Stack Memory:

Address	**0FF8h**	**0FF9h**	**0FFAh**	**0FFBh**	**0FFCh**	**0FFDh**	**0FFEh**	**0FFFh**
Data	25h	67h	A3h	B4h	(empty)	(empty)	(empty)	(empty)

Stack Pointer (SP): 0FFCh Code Segment (CS): 1800h Instruction Pointer (IP): 0156h FLAGS Register: 0A42h

a. If the signal corresponds to interrupt type 2Ch, determine the new values of IP and CS as the 8086 services the interrupt. [3]
b. Show how the stack changes after the interrupt is acknowledged (show what values are pushed and where, in terms of addresses). [4]
c. Some instructions require one bus cycle, while others require two bus cycles, WHY? [1]

Question 1

An 8086 microprocessor operates at 12 MHz with a 35% duty cycle.

1. Calculate TON (high time) and TOFF (low time) for one clock cycle and If an instruction requires 3 bus cycles with each bus cycle having 4 T-states, calculate total execution time [3]
2. The 8086 reads a word from memory address 2A45h. Which bank(s) will be activated (even/odd/both)? [2]
3. A. Calculate time for 600 byte reads from even addresses only (each takes 4 T-states) [1.5]

   B. Calculate time for 300 word reads where all are unaligned (each takes 8 T-states due to two bus cycles) [1.5]

Question 1

During execution, the following events occur in this exact sequence within a 2 µs window:

1. INTR pin is activated (interrupt type 40H requested via 8259 PIC)
2. A divide-by-zero occurs (Type 0 interrupt)
3. NMI pin is activated
4. Single-step flag (TF) is set to 1

The processor is currently executing a MOV instruction when event 1 occurs.

a) List the order in which these four interrupts will be serviced, and explain your reasoning based on 8086 priority rules. **[2]**

b) For the interrupt that gets serviced first, if its IVT entry is at physical addresses 00008H-0000BH containing [20H, 30H, 40H, 50H], calculate where the processor will jump. **[2]**

Question 2

A diagnostic tool reports that the IP address of an interrupt is stored at physical location 000B8H. After running diagnostics, it's found that both the CS and IP locations for this interrupt contain values (CS = FFFFH, IP = FFFFH).

1. What is the interrupt type number? [2]
2. What physical memory address stores the CS for this interrupt? [2]

Question 3

An 8086 system is executing a main program when the following interrupts occur at different time stamps:

- **t = 0 ms**: Interrupt Type 08H (IRQ0 - Timer) occurs
- **t = 2.5 ms**: Interrupt Type 09H (IRQ5 - Keyboard) occurs
- **t = 4 ms**: NMI (Type 02H) occurs
- **t = 5 ms**: Interrupt Type 0BH (IRQ3 - Serial Port) occurs

Each ISR execution time: Type 08H = 8 ms, Type 09H = 5 ms, NMI = 3 ms, Type 0BH = 6 ms . IMR value is 10h

- NMI cannot be masked and has highest priority

1. The exact time stamp when each ISR starts execution [2]
2. The exact time stamp when each ISR completes execution [2]
3. Total execution time. [3]

IMR Values: Master=91H, Slave-1=00H, Slave-2=44H, Slave-3=20H

Event Timeline

Initial: CS=1000H, IP=2000H, SP=0200H, IF=1

Time	Type	Source	Pin Info	Duration
5ms	08H	Master	IR0	18ms
10ms	20H	Slave-1	IR0 → Master IR1	12ms
15ms	32H	Slave-2	IR2 → Master IR2	10ms
20ms	0CH	Master	IR4	8ms
25ms	40H	Slave-3	IR0 → Master IR3	15ms
30ms	02H	NMI	NMI Pin	5ms
35ms	30H	Slave-2	IR0 → Master IR2	20ms
40ms	0FH	Master	IR7	6ms
45ms	00H	Exception	Divide Error	4ms
50ms	21H	Slave-1	IR1 → Master IR1	10ms
55ms	60H	Software	INT 60H	7ms

Delays: Slave preempt = 1ms, Non-slave preempt = 0.5ms

Q1 [2]: Which interrupts are masked? How many will be serviced?

Q2 [2]: For Type 30H: Physical address of CS higher byte?

Q3 [2]: How many overflow detection methods? Name and explain them.

Q4 [3+3]: Create complete timeline showing start/end times with delays and preemptions.

Q5 [3]: Calculate total time.