Question 1

Suppose you have an Intel 8086 which is operating at a duty cycle of 55% and for each clock pulse assume T_OFF = 45 ns. The 8086 is now going to execute the instruction MOV [3456h], BX.

(a) Estimate the frequency at which the 8086 is operating.

(b) Calculate the total time for one instruction cycle of the given instruction.

(c) Calculate the values of the A0 and BHE' pins during the execution of the given instruction.

Question 2

Suppose an 8086 wants to read 2 bytes of data from an odd memory location. The memory is working at a slower rate than the 8086. When reading the first byte of data, the 8086 has to wait for an additional 3 clock pulses. But the second byte was read without any delay. Assuming the 8086 is working at a frequency of 12 MHz, calculate the following:

(a) The value of the instruction cycle (in nanoseconds).

(b) The values of A0 and BHE' pins while transferring the 2 bytes of data.

(c) The value of T_ON and T_OFF assuming the 8086 is running at a duty cycle of 45%.

Question 3

Suppose the time required to complete one instruction cycle for the instruction MOV AX, [4567h] is 500 ns. For each bus cycle, T_ON = 0.3T, where T represents the time required for one clock pulse.

(a) Deduce the values of T_ON, T_OFF, and the frequency at which this 8086 is operating.

(b) Deduce the values of the A0 and BHE' pins during one instruction cycle of the given MOV operation.

(c) Illustrate the timing diagram for the given MOV operation showcasing the CLK, M/IO', ALE, AD0–AD15, and RD'/WR' pins (use either RD' or WR' depending on the operation).

Question 4

A program performs the following memory operations:

Read WORD from address 3A2F7h

Write BYTE to address 3A2F9h

Read WORD from address 3A2FAh

Write WORD to address 3A2FDh

(a) For each operation, determine:

• Which bank(s) will be accessed (Even/Odd/Both)

• BHE' and A0 signal values

• Number of bus cycles needed

(b) Draw a table showing all operations with their bank usage.

(c) Calculate total bus cycles and time taken (assume 8 MHz clock, 4 T-states per cycle).

(d) If all operations were aligned to even addresses, how much time would be saved?

Question 5

Given the following memory table:

Address:	000B8h	000B9h	000BAh	000BBh	2A4C0h	2A4C1h	2A4C2h	2A4C3h
Data:	30h	40h	50h	2Ah	78h	9Ah	BCh	DEh

(a) If the Intel 8086 encounters the INT 46 instruction, calculate the starting address of the corresponding ISR. Also determine the first 2-byte hexadecimal instruction that will be fetched to the instruction queue from the ISR.

(b) Assume a hypothetical scenario where CS and IP values for the starting address of an ISR are 1230h and 2000h respectively. Each memory location can store a maximum of 1 byte of data. The ISR consists of 20 lines of code and assume 4 bits are required to store each line of code. Deduce mathematically the address where the IRET instruction will be found.

Question 6

Assume at T = 0 ns an interrupt request is made at IR = 5 of a PIC working in fixed priority mode. The duration required to serve the interrupt is 40 ns. At T = 15 ns another interrupt request is made at IR = 2 which requires 30 ns to be served. Finally, at T = 25 ns two interrupt requests arrive at IR = 7 and IR = 1, each requiring 35 ns.

(a) Explain how the PIC performs its task in this case with reference to changes in the ISR and IRR at each stage. Assume the interrupt flag can never be reset to 0.

(b) Deduce the time at which the PIC starts serving the IR = 7 interrupt request.

(c) Illustrate the internal block diagram of an 8259A PIC.

Question 7

(a) To utilize 15 DMA channels, estimate the minimum number of secondary 8237 DMA controllers required.

(b) Construct the DMA cascading diagram based on your answer in part (a). Show how the secondary controllers are connected with the primary controller using appropriate pins (DREQ, DACK, HRQ).

(c) Assume an 8237 DMAC where the DREQ2 and DACK3 pins are disabled. Deduce the maximum number of peripheral devices accommodated in a first-level cascading scheme. Would this number change if only the DREQ0 and DACK0 pins were disabled? Justify your answer.

Question 8

(a) Based on the operation of the DMA controller, explain which pins of the 8237 IC should be connected to the corresponding pins of the 8086 IC. Specify:

• HRQ pin connection

• HLDA pin connection

• Purpose of the AEN pin

• Address bus and data bus connections

(b) Consider an Intel 8086 with an 8237 DMA controller. An I/O device requests the DMA to initiate a data transfer with memory (I/O to Memory). Explain the sequence of operations among the DMA, I/O device, memory, and the 8086. Also describe the values of HRQ, HLDA, DREQ, DACK, IOR', IOW', MEMR', and MEMW' pins at each stage.

(c) Describe the pin values of an 8237 DMA controller during a DMA read cycle (Memory to I/O):

IOR'

IOW'

MEMW'

MEMR'