[UJT]

CSE 341: Microprocessors

Department of Computer Science and Engineering

Brac University

Examination: Quiz 2 **Semester: Fall 2025**

Duration: 25 Minutes **Full Marks: 15**

Name: ID:

Section:

Answer all the questions.

Q1. Given, DS = 1000h, CS = 2000h, SS = 3000h, ES = 4000h, BX=0012h, SI = 1200h, DI = 00ABh, SP = 1020h, BP = 0230h, IP = 0899h. **[5]**

i) MOV CL, [BX+SI];

ii) MOV [1000H], AX;

iii) RET;

iv) MOV 7879H[BX+DI], 8543H[SI];

V) MOV AL, 1Fh;

Addressing Mode	**Source**	**Destination**
Base-plus-index Add.	**11212h**	**CL**
Register relative Add.	**AX**	**11000h**
Implied Add.	**N/A**	**N/A**
Invalid Add.	**N/A**	**N/A**
Immediate Add.	**1Fh**	**AL**

[3]

Q2.
MOV AX, 5C87h;
MOV BX, 78A5h;
ADD AX,BX;
	Write down the values of the status register:
	AF = 0; **CF=0**
	PF = 0; **OF =1;**
	SF =1; **ZF = 0;**

Q3. SS = 2000H, CS = 3000H, DS = 1000H, BP = 0020H, DI = 00F0H, IP = 0020H, BX = 0010H. The **JMP [BX + DI]** instruction is executed. Calculate the **physical address** of the **next instruction's first byte**. **[3]**

30100H	30101H	30102H	30103H	30104H	30105H	30106H	10100H	10101H	10102H	10103H
23	01	8B	86	20	10	8B	02	01	00	EB

Q4. 898F2A50h convert this into an assembly instruction. **[4]**

1	0	0	0	1	0	0	1	1	0	0	0	1	1	1	1
OPCODE						D	W	MOD		REG			R/M		

0	0	1	0	1	0	1	0	0	1	0	1	0	0	0	0
Low byte displacement								Higher byte displacement							

Write the instruction here:	MOV [BX+502A], CX;

MOD / RM	00	01	10	11	
				W = 0	W = 1
000	[BX] + [SI]	[BX] + [SI] + d8	[BX] + [SI] + d16	AL	AX
001	[BX] + [DI]	[BX] + [DI] + d8	[BX] + [DI] + d16	CL	CX
010	[BP] + [SI]	[BP] + [SI] + d8	[BP] + [SI] + d16	DL	DX
011	[BP] + [DI]	[BP] + [DI] + d8	[BP] + [DI] + d16	BL	BX
100	[SI]	[SI] + d8	[SI] + d16	AH	SP
101	[DI]	[DI] + d8	[DI] + d16	CH	BP
110	d16 (direct address)	[BP] + d8	[BP] + d16	DH	SI
111	[BX]	[BX] + d8	[BX] + d16	BH	DI

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Q1. Given, DS = 1000h, CS = 2000h, SS = 3000h, ES = 4000h, BX=0012h, SI = 1200h, DI = 00ABh, SP = 1020h, BP = 0230h, IP = 0899h **[5]**

i) RET [1B5Ch];

ii) MOV [BX+SI+10], CL;

iii) MOV [DI], BL;

iv) MOV [BP+DI], 8543H[SI];

V) MOV AX, [BP+4]

Addressing Mode	Source	Destination
Invalid Add.	N/A	N/A
Base-relative-plus-index Add.	CL	11222h
Register indirect Add.	BL	100ABh
Invalid	N/A	N/A
Registe relative	30234h	AX

[3]

Q2.
MOV AX, 79CBh;
MOV BX, 68FFh;
ADD AX,BX;
	Write down the values of the status register:
	
	AF = 1; **CF=0**
	PF = 1; **OF =1;**
	SF =1; **ZF = 0;**

Q3. SS = 2000H, CS = 3000H, DS = 1000H, BP = 0020H, DI = 00F0H, IP = 0020H, BX = 0010H. The **JMP [BX + DI]** instruction is executed. Calculate the **physical address** of the **next instruction's first byte**. **[3]**

30100H	30101H	30102H	30103H	30104H	30105H	30106H	10100H	10101H	10102H	10103H
23	01	8B	86	20	10	8B	02	01	00	EB

Q4. 898F2A50h convert this into an assembly instruction. **[4]**

1	0	0	0	1	0	0	1	1	0	0	0	1	1	1	1
OPCODE						D	W	MOD		REG			R/M		

0	0	1	0	1	0	1	0	0	1	0	1	0	0	0	0
Low byte displacement								Higher byte displacement							

Write the instruction here:	MOV [BX+502A], CX;

MOD / RM	00	01	10	11	
				W = 0	W = 1
000	[BX] + [SI]	[BX] + [SI] + d8	[BX] + [SI] + d16	AL	AX
001	[BX] + [DI]	[BX] + [DI] + d8	[BX] + [DI] + d16	CL	CX
010	[BP] + [SI]	[BP] + [SI] + d8	[BP] + [SI] + d16	DL	DX
011	[BP] + [DI]	[BP] + [DI] + d8	[BP] + [DI] + d16	BL	BX
100	[SI]	[SI] + d8	[SI] +d16	AH	SP
101	[DI]	[DI] + d8	[DI] +d16	CH	BP
110	d16 (direct address)	[BP] + d8	[BP] +d16	DH	SI
111	[BX]	[BX] + d8	[BX] + d16	BH	DI