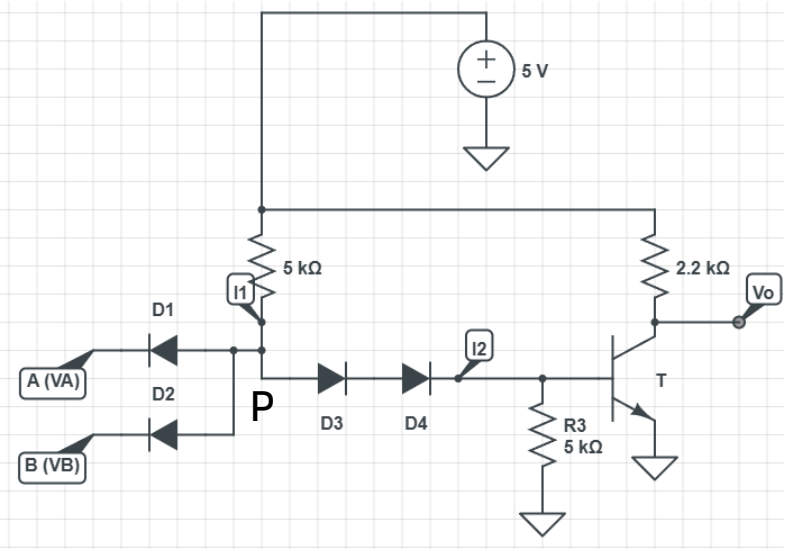
Basic Operation

Exercise 1



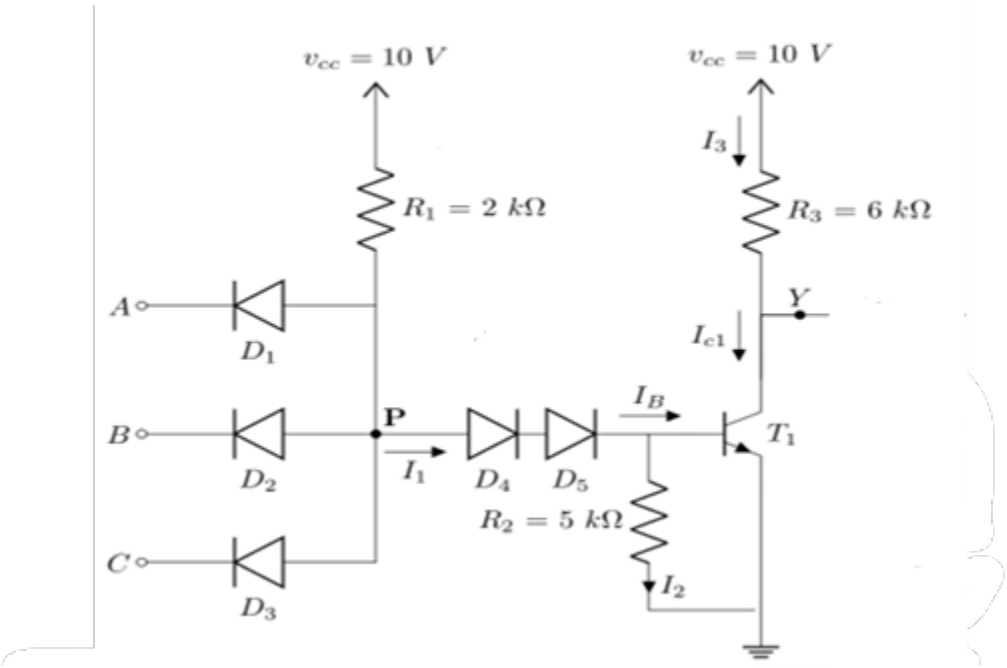
For the DTL NAND gate-
Find all the voltages & currents for all logic cases with verification of assumption.
Assume high input = 5 V, low input = 0.2 V

$$V_o = 5\ V, 0.2\ V$$

$$I_{5\ k\Omega} = 0.82\ mA$$

$$I_{b_1} = I_{b_2} = 0.41\ mA$$

Exercise 2



For the above circuit, $V_{OH} = 9.5\ V, V_{OL} = 0.1\ V, \beta_F = 30$

a) Find the value of β_{min} when all inputs are high.
b) If all the inputs are high, what is the magnitude of noise voltage at input A, that would cause the gate to malfunction?
c) If at least one input is low, what is the magnitude of noise voltage at input A, that would cause the gate to malfunction?

Ans: a) 0.441
b) 8.4 V
c) 0.9 V

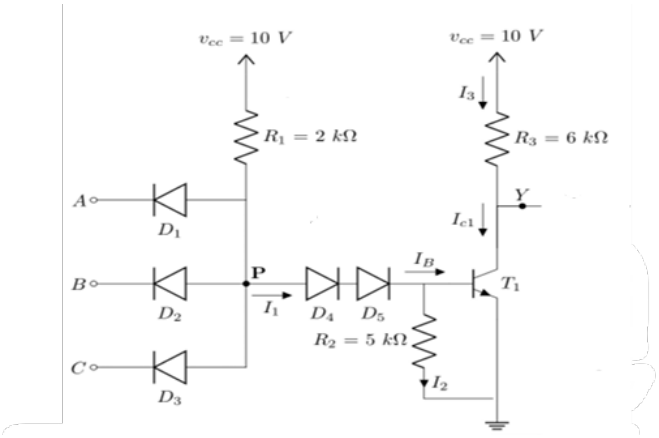
Practice Problem 1:

What is the current through D_B in the circuit of **Exercise 2**, for the logic case (1,0,0)?

Ans: 2.3 mA

Power Dissipation

Exercise 3



a) Find power dissipation for all cases.
b) Maximum & average power dissipation.

Ans: a) $45.54\ mW, 55.5\ mW$
b) $55.5\ mW, 46.785\ mW$

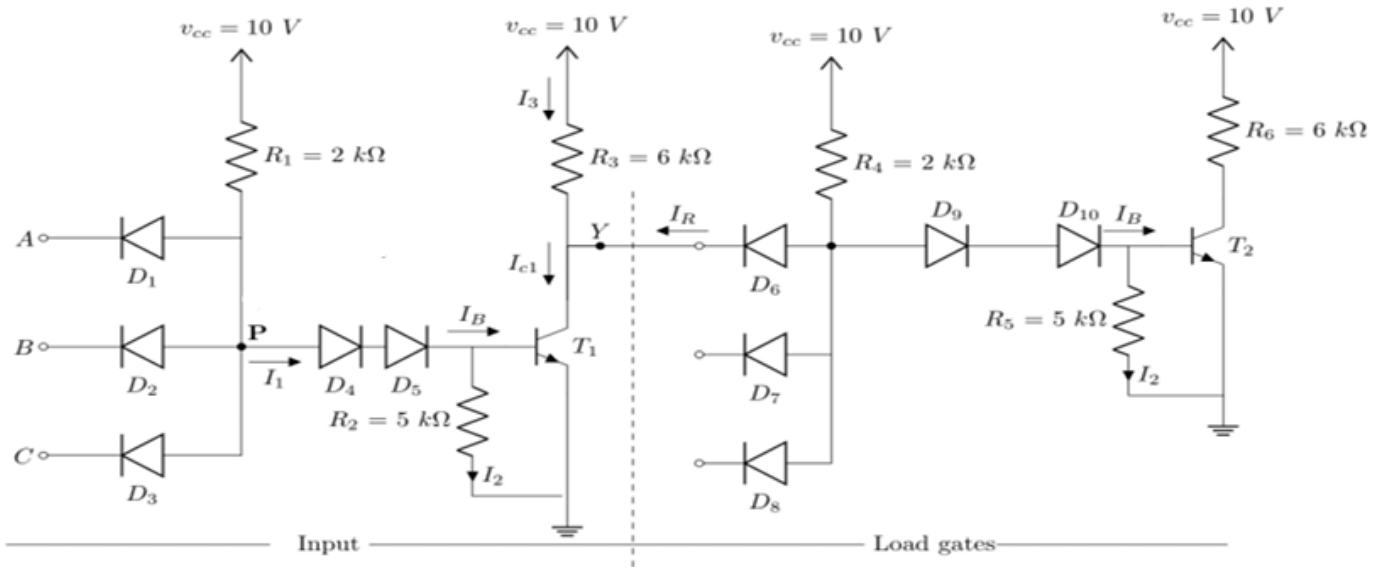
Practice Problem 2:

If the number of inputs to the DTL NAND gate in **Exercise 3**, is increased to 5, what will be the maximum & average power dissipation?

Ans: $55.5\ mW, 45.85\ mW$

Fanout

Exercise 4



For the above circuit- $V_{OH} = 9.5\ V, V_{OL} = 0.1\ V, \beta_F = 30$

a) Find the maximum fanout.
b) Find the maximum power dissipation of the driver circuit, when N (maximum fanout) loads are connected.

Ans: a) 24
b) 66.54 mW

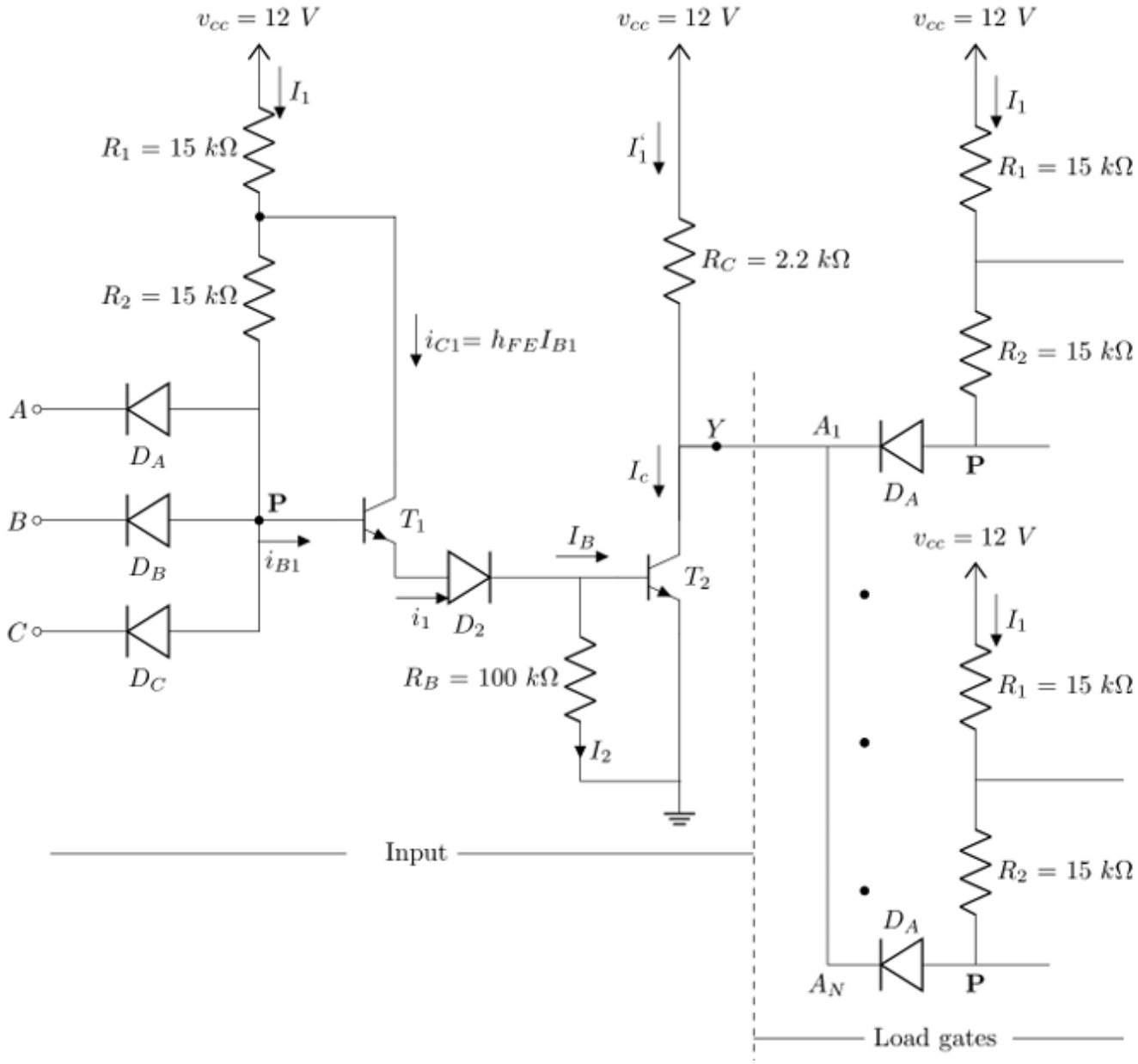
Practice Problem 3:

Find the value of R_3 that would reduce the maximum fanout found in **Exercise 4** to 20.

Ans: 490 Ω

Modified DTL

Exercise 5



For the circuit above- $V_{OH} = 11.5\ V, V_{OL} = 0.2\ V, \beta_F = 30$

a) Find the value of β_{min} when all inputs are high.
b) Find the maximum fanout.
c) Find the power dissipation of the driver for all cases.
d) If all the inputs are high, what is the magnitude of noise voltage at the input A, that would cause the gate to malfunction?

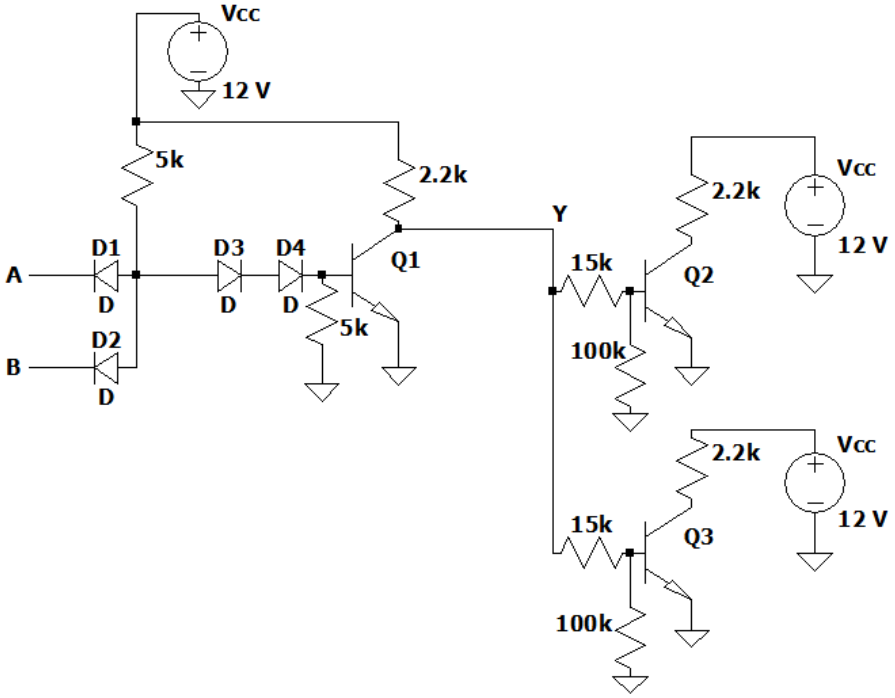
Ans: a) 8.654
b) 35
c) 4.4387 mW, 73.82 mW
d) 10.4 V

Practice Problem 4:

If at least one input is low, what is the magnitude of the noise voltage at input A, that would cause the gate to malfunction in **Exercise 5**?

Ans: 0.8 V

Exercise 6



For the given circuit: $V_{OH} = 10\ V, V_{OL} = 0.2\ V, \beta_F = 30$

a) When N=1, what logic function do we get from the output of the load?
b) Find the maximum fanout.
c) For N=maximum fanout, find the maximum power dissipation in the loads.

Ans: a) $Y = AB$

b) 1

c) 70.5 mW

Exercise 7

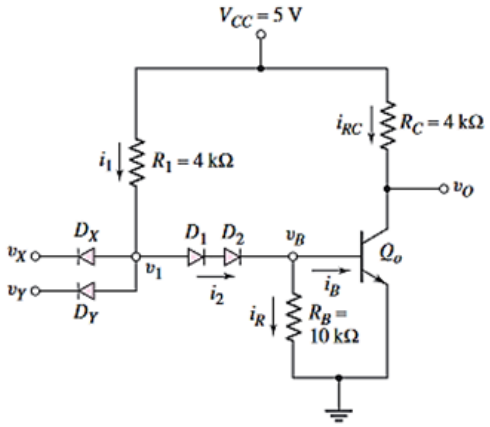


Table Piecewise linear parameters for a pn junction diode and npn bipolar transistor

Parameter	Value
V_γ	0.7 V
V_{BE}(on)	0.7 V
V_{BE}(sat)	0.8 V
V_{CE}(sat)	0.1 V

For the DTL circuit in the above figure. Assume the transistor parameters areas given in Table and let $\beta_F = 25$. In the picture, V_γ represents the cut in voltage of diodes. Assume any of the input is low, where low input is $0.1\ V$.

a) Find i_1.
b) Find i_2.
c) Find i_R.
d) Find i_B.
e) Find i_{RC}.

Ans: a) 1.05 mA
b) 0 mA
c) 0 mA
d) 0 mA
e) 0 mA

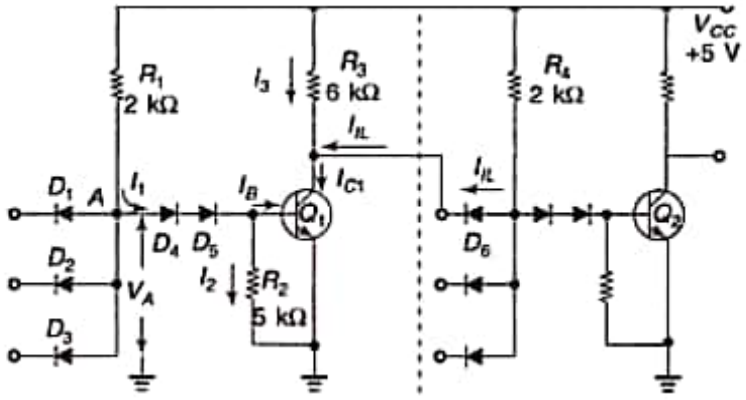
Exercise 8

For the DTL circuit in Exercise 7, assume both inputs are high.

a) Find i_1.
b) Find i_2.
c) Find i_{RC}.
d) Find i_R.
e) Find i_B.

$Ans: a)\ 0.7\ mA$
$b)\ 0.7\ mA$
$c)\ 1.225\ mA$
$d)\ 0.08\ mA$
$e)\ 0.62\ mA$

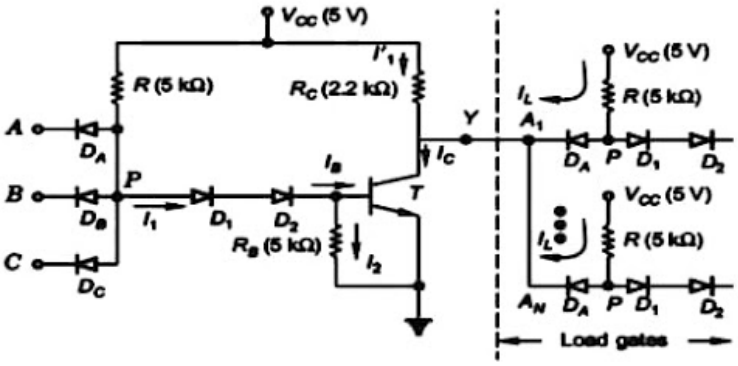
Exercise 9



For the DTL circuit given, find the FANOUT of the driver DTL NAND Gate.

$Ans: 17$

Exercise 10



For the circuit given, assume any of the input is low which means any of the input (Suppose, input A) is $0.1\ V$.

For this part assume inputs of the load devices are not connected to the driver device.

a) Find I_L.
b) Find I_1.
c) Find I_2.
d) Find I_B.
e) Find I_C.

Ans: a) $0.84\ mA$
b) $0\ mA$
c) $0\ mA$
d) $0\ mA$
e) $0\ mA$

Practice Problem 5

For the circuit in Exercise 10, assume all the inputs are high ($V_A = V_B = V_C = 5\ V$).

For this part assume inputs of the load devices are not connected to driver device.

a) Find I_L.
b) Find I_1.
c) Find I_2.
d) Find I_B.
e) Find I_C.

Ans: a) 0 mA
b) 0.56 mA
c) 0.16 mA
d) 0.39 mA
e) 2.227 mA

Practice Problem 6

Find the FANOUT of the DTL circuit in Exercise 10.

Ans: 11