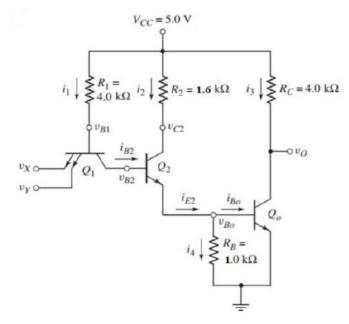
## **Exercise 1**



For the TTL NAND circuit, assume  $\beta_F=25$ ,  $\beta_R=0.1$   $V_{OH}=3.4~V$ ,  $V_{OL}=0.1~V$  For saturation mode, assume,  $V_{CE}=0.1~V$ 

- a) Assume no loads are connected to the driver device. If at least one input is low (0.1 V), find  $i_1, i_{B_2}, i_{B_0}, i_3$ .
- b) Repeat the calculation of (a) if both inputs are high ( $v_x = v_y = 5 V$ ).
- c) Find the maximum possible fanout if the loads are also this TTL NAND gate.
- d) Assume all inputs of the **driver** are **high**.
  - 1. Find the maximum fanout if the other input of the load  $v_y = 5 V (High)$ .
  - 2. If both inputs of the load circuits are low, then what would be the maximum fanout? Comment and compare on the above two cases to identify which case has better fanout and why?
- e) Find the power dissipation for all cases [Assume 4 loads are connected to the driver's output]

Wm 79E.ES (9

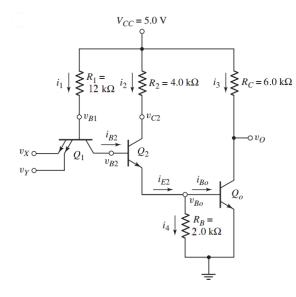
£21.2,12.1 (b

၄ (၁

Am 252.1, Am 2572.2, Am 18.0, Am 270.0 (d

Ans: a) 1.025 mA, all other currents 0 mA

## **Practice Problem 1**



For the given TTL circuit,  $\beta_F = 25$ ,  $\beta_R = 0.1$  Assume any of the input to the driver is low and loads are not connected.

- a) Find  $i_1$ .
- b) Find  $i_{B_2}$ .
- c) Find  $i_2$ .
- d) Find  $i_{B_o}$ .
- e) Find  $i_3$ .

Ans: a) 0.342 mA

- b) 0 mA
- c) 0 mA
- d) 0 mA
- e) 0 mA

Now consider all input voltages high, find the same current values again.

7918.0 (9

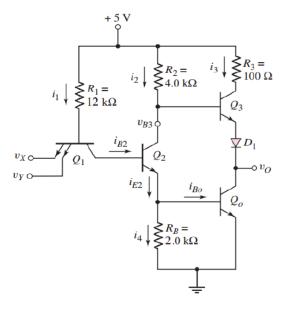
268.0 (b

220.1 (2

72.0(d

222.0 (n:snA

## **Exercise 2**



For the given TTL circuit with totem-pole output, assume common emitter current gain,  $\beta_F=25$  and reverse common emitter current gain of the transistors  $\beta_R=0.1$ .

- a) Find the value of  $\beta_{min}$  for transistor Q, so that Q, can remain in saturation when both inputs are high.
- b) Assume inputs of the load devices are not connected to driver device. If at least one input (0.1 V), find  $i_1$ ,  $i_{B_2}$ ,  $i_2$ ,  $i_{B_0}$ , and  $i_3$ .
- c) Repeat the calculation of (b) if both the inputs are high ( $v_x = v_y = 3.6 V$ )
- d) Find the maximum fanout of this TTL circuit for the case mentioned in (c).
- e) Find out the maximum power dissipation of the TTL circuit for the case mentioned in (c).
- f) Calculate maximum fanout for  $v_x = v_y = 0.1 V$ . Given that  $v_o(No\ load) = 3.5 V$ . And, from this calculation prove that  $T_4$  is in **forward active mode**.

87 (*f* 

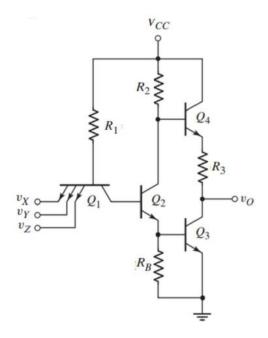
Wm 214.0 (9

Am 0, Am 268.0, Am 72.0, Am 222.0 (2

Am 0,0,0,0,Am 5148.0 (d

967.E (n:snA

## **Exercise 3**



For the given TTL circuit, given

$$R_1 = 3 k\Omega, R_2 = 1.3 k\Omega,$$

$$R_3 = 0.55 k\Omega$$
, and  $R_B = 8 k\Omega$ .

Assume  $V_{cc}=3.5~V$ , common emitter current gain,  $\beta_F=15$  and reverse common emitter current gain of the transistors,

$$\beta_x = 0.8.$$

- a) If all inputs are high  $(v_x = v_y = v_z = 3.5 \ V)$ , find  $i_{B_1}$ ,  $i_{B_2}$ ,  $i_{B_3}$ ,  $i_{B_4}$ , and  $i_{E_3}$ .
- b) Assume inputs of the load devices are not connected to the driver device. If at least one input is low (0.1 V), find  $i_{B_1}, i_{EX}, i_{B_2}, v_o$ .
- c) Find out the power dissipation of the TTL circuit for both (a) and (b).
- d) Find the maximum fanout of this TTL circuit for the case described in (a).
- e) If at least one input is low (0.1 V) and 2 loads are connected to the output find the new value for  $v_o$ .

V 99E.2(9

95 (b

Wm 8749.5, Wm 85.51 (3

V 8.2, Am 0, Am EE4.0, Am 78.0 (d

Am 184.8, Am 4110.0, Am 842.8, Am 88.1, Am 4.0 (v:snA