Exercise 1

a) For input logic low, $V_I = 0\ V < V_{TN}$. Thus the inverter is in cutoff. $\therefore P_{low} = 0\ W$
Thus, average power, $P_{avg} = \frac{P_{high}+P_{low}}{2} = \frac{P_{high}}{2} \rightarrow P_{high} = 2P_{avg}$
For input logic high, $V_I = 6\ V > V_{TN}$. Assuming triode mode operation,
$K_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2] = \frac{V_{DD}-V_{DS}}{R_D} \rightarrow 0.2[2(6 - 0.3)V_{DS} - V_{DS}^2] = \frac{6-V_{DS}}{R_D}$
Also, $P_{high} = (V_{DD} - 0) \times I_{DS} = (6 - 0) \times \frac{6-V_{DS}}{R_D} = 2 \times 1.1654 = 2.3308$
$\rightarrow \frac{6-V_{DS}}{R_D} = \frac{2.3308}{6} = 0.388$
$\therefore 0.2[11.4 \times V_{DS} - V_{DS}^2] = 0.777 \rightarrow V_{DS} = 11.56\ V, 0.173\ V$
Now, $11.56 > V_{DD}$, hence not acceptable. $\therefore V_{DS} = 0.173\ V$
$\therefore R_D = \frac{6-V_{DS}}{0.388} = 15\ \Omega$

b) For maximum power dissipation, the drain current must be maximum. The drain current has the highest value when $V_{GS} = V_{DD} = 6\ V$
From (a), we found, for $V_I = V_{GS} = 6\ V, V_{DS} = 0.173\ V$
$\therefore I_{DS_{max}} = \frac{6-0.173}{15} = 0.388\ A$

c) At the transition point, $V_{DS} = V_{GS} - V_{TN} = V_{GS} - 0.3$ & $I_{DS} = I_{DS_{sat}} = K_n[V_{GS} - V_{TN}]^2$
However, $I_{DS} = \frac{V_{DD}-V_{DS}}{R_D}$
Thus, $\frac{6-V_{DS}}{15} = 0.2V_{DS}^2 \rightarrow V_{DS} = 1.26\ V, -1.59\ V$
V_{DS} cannot be lower than V_S. Thus, $V_{DS} = 1.26\ V$
$\therefore Transition\ point, V_I = V_{GS} = V_{DS} + V_{TN} = 1.26 + 0.3 = 1.56\ V$

d) $P_{transition} = (V_{DD} - 0) \times I_{DS_{transition}} = (6 - 0) \times \frac{6-V_{DS_{transition}}}{R_D} = (6 - 0) \times \frac{6-1.26}{15}$
$= 1.896\ W$

e) Assuming triode mode operation,
$\frac{V_{DD} - V_{DS}}{R_D} = K_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2] \rightarrow \frac{6 - 4.2}{15} = 0.2[2(V_{GS} - 0.3)4.2 - 4.2^2]$
$\rightarrow V_{GS} = 2.47\ \text{V}$
Now, $V_{ov} = V_{GS} - V_{TN} = 2.47 - 0.3 = 2.17 < 4.2$
Thus, our assumption of triode mode is not satisfied, and the assumption was wrong.
Again, assuming saturation mode,
$\frac{6-4.2}{15} = 0.2(V_{GS} - 0.3)^2 \rightarrow V_{GS} = 1.07\ V$
Now, $V_{ov} = 1.07 - 0.3 = 0.77 < 4.2$
Thus, our assumption of saturation mode is correct. Also, the determined input voltage is higher than the threshold voltage, and thus is valid. $\therefore V_I = V_{GS} = 1.07\ V$

Exercise 2

a) **Case (0,1):**

Assuming triode mode operation for NMOS B, since NMOS A will be cutoff, KCL at common drain, $I_R = I_{D_A} + I_{D_B} \rightarrow \frac{V_{DD}-V_{DS}}{R} = 0 + K_{n_B}[2(V_{GS} - V_{TN_B})V_{DS} - V_{DS}^2]$

$\rightarrow \frac{5-V_{DS}}{20} = 0.5[2(5-0.3)V_{DS} - V_{DS}^2] \rightarrow V_{DS} = 0.052\ V, 9.45\ V$

Since, $9.45\ V > V_{DD}, V_{DS} = 0.052\ V$

Verification of assumption: $V_{DS} = 0.052 < (V_{GS} - V_{TN_B}) = (5-0.3) = 4.7$

Case (1,0):

Assuming triode mode operation for NMOS A, since NMOS B will be cutoff, KCL at common drain, $I_R = I_{D_A} + I_{D_B} \rightarrow \frac{V_{DD}-V_{DS}}{R} = K_{n_A}[2(V_{GS} - V_{TN_A})V_{DS} - V_{DS}^2] + 0$

$\rightarrow \frac{5-V_{DS}}{20} = 0.4[2(5-0.25)V_{DS} - V_{DS}^2] \rightarrow V_{DS} = 0.063\ V, 9.56\ V$

Since, $9.56\ V > V_{DD}, V_{DS} = 0.063\ V$

Verification of assumption: $V_{DS} = 0.063 < (V_{GS} - V_{TNA}) = (5-0.25) = 4.75$

Case (1,1):

Assuming triode mode operation for both the NMOS,

$I_R = I_{D_A} + I_{D_B}$

$\rightarrow \frac{5-V_{DS}}{20} = K_{n_A}[2(5 - V_{TN_A})V_{DS} - V_{DS}^2] + K_{n_B}[2(5 - V_{TN_B})V_{DS} - V_{DS}^2]$

$\rightarrow \frac{5-V_{DS}}{20} = 0.4[2(5-0.25)V_{DS} - V_{DS}^2] + 0.5[2(5-0.3)V_{DS} - V_{DS}^2]$

$\rightarrow V_{DS} = 9.47\ V, 0.029\ V$

Since, $9.47 > V_{DD}, V_{DS} = 0.029\ V$

Verification of assumption: $V_{DS} = 0.029 < (5 - V_{TN_A}) = (5-0.25) = 4.75$

$V_{DS} < (5 - V_{TN_B}) = (5-0.3) = 4.7$

$\therefore Low\ output\ threshold, V_{OL} = \max(0.052, 0.063, 0.029) = 0.063\ V$

b) **Case(0,0):** Both NMOS are off. Thus, $I_R = I_{D_A} + I_{D_B} = 0 + 0 = 0$

Case	$\boldsymbol{I_R = \frac{5-V_{DS}}{20}\ (A)}$	$\boldsymbol{P = (V_{DD} - 0) \times I_R\ (W)}$
0,0	0	0
0,1	0.2474	1.237
1,0	0.2469	1.234
1,1	0.2486	1.243

Total		3.714

$\therefore P_{avg} = \frac{3.714}{4} = 0.9285\ W$

c) $I_R = I_{D_A} + I_{D_B} \rightarrow \frac{5-V_{DS}}{20} = K_{n_A}\left[2\left(5 - V_{TN_A}\right)V_{DS} - V_{DS}^2\right] + K'_{n_B}\left[2\left(5 - V_{TN_B}\right)V_{DS} - V_{DS}^2\right]$
$\rightarrow \frac{5-V_{DS}}{20} = 2 \times 0.4[2(5 - 0.25)V_{DS} - V_{DS}^2] \rightarrow V_{DS} = 0.033\ V, 9.53\ V(not\ valid)$
[As both the drain currents are equal]
$\therefore I_{DA} = \frac{1}{2}I_R = \frac{1}{2} \times \frac{5-0.033}{20} = 0.124\ A = I_{D_B} = K_{n'_B}[2(5 - 0.3)0.033 - 0.033^2]$
$\rightarrow K_{n'_B} = 0.401\ A/V^2$

Exercise 3

a) Y=A+B
b) **Case (0,0):**
Both NMOS A & B are in cutoff. NMOS Y on.
Since, the gate current is always zero, current through the $25\ \Omega$ on the left will be zero.
Thus, input to NMOS Y for this case is equal to source voltage.
Assuming triode mode operation for NMOS Y,
$I_{25\,\Omega} = \frac{5-V_Y}{25} = K_{N_Y}\left[2\left(V_{GS} - V_{TN_Y}\right)V_Y - V_Y^2\right] \rightarrow \frac{5-V_Y}{25} = 0.5[2(5 - 0.3)V_Y - V_Y^2]$
$\rightarrow V_Y = 0.044\ V, 9.44\ V\ (not\ valid)$
Verification of assumption: $V_Y = 0.044 < V_{GS} - V_{TN} = 5 - 0.3 = 4.7$
Case (0,1)|(1,0):
Since, all the MOSFET parameters for the three NMOS are same, Case (0,1) & Case (1,0) will have similar results. Let's consider (0,1). NMOS A is in cutoff & NMOS B is on. Output of the NOR portion is low. Let's assume triode mode operation for NMOS B. Since again no gate current flows to NMOS Y,
$I_{25\Omega} = \frac{5-V_{DS_B}}{25} = K_{N_B}\left[2\left(V_{GS} - V_{TN_B}\right)V_{DS_B} - V_{DS_B}^2\right] = 0.5[2(5 - 0.3)V_{DS_B} - V_{DS_B^2}]$
$\rightarrow V_{DS_B} = 0.044\ V, 9.44\ V\ (not\ valid)$
Verification of assumption: $V_{DS_B} = 0.044 < V_{GS} - V_{TN} = 5 - 0.3 = 4.7$
Now, this is the input voltage to NMOS Y. Here, $V_{DS_B} = 0.044 < 0.3 = V_{TN_Y}$. Thus, NMOS Y will be in cutoff mode. $\therefore V_Y = 5\ V$

Case (1,1):

NMOS A & B both on. Assuming triode mode operation for both,

$I_{25\,\Omega} = \frac{5-V_{DS}}{25} = 2 \times 0.5[2(5-0.3)V_{DS} - V_{DS}^2] \rightarrow V_{DS} = 0.022\,V, 9.42\,V\ (not\ valid)$

Verification of assumption: $V_{DS} = 0.022 < 5 - 0.3 = 4.7$

Now, this is the input voltage to NMOS Y. Here, $V_{DS} = 0.022 < 0.3 = V_{TN_Y}$. Thus, NMOS Y will be in cutoff mode. $\therefore V_Y = 5\,V$

Case	$V_{DS}\ of\ NOR\ gate$	V_Y	$I_{25\,\Omega}\ of\ NOR\ gate$	$I_{25\,\Omega}\ of\ NOT\ gate$	P
0,0	5	0.044	0	0.198	$(5-0) \times 0.198 = 0.99\,W$
0,1	0.044	5	0.198	0	$(5-0) \times 0.198 = 0.99\,W$
1,0	0.044	5	0.198	0	$(5-0) \times 0.198 = 0.99\,W$
1,1	0.022	5	0.199	0	$(5-0) \times 0.199 = 0.995\,W$

$\therefore P_{max} = 0.995\,W$

c) $V_{OH} = \min(5, 5, 5) = 5V$