

**BRAC UNIVERSITY**  
**Department of Computer Science & Engineering**  
**Practice Problem sheet (Week5)**  
**CSE 350: Digital Electronics and Pulse Technique**

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## Question 1

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|-----|--|
| (a) | An analog signal in the range $-1V$ to $16V$ is to be converted to a digital signal with a quantization error of less than or equal to $0.781\%$ of the input voltage range for quantization. e.g <b>the overall quantization error for this input signal should be less than or equal to <math>0.781\%</math> of the ADC's maximum quantization error.</b> The quantization error is the maximum error occurring after quantizing the analog signal.<br><br><b>Find</b> the required number of bits for the above expression. |
| (b) | <b>Determine</b> the minimum sampling frequency of a signal.   |

$$a) \Delta Q = \text{Quantization error} = \frac{1}{2} \frac{V_{max} - V_{min}}{2^N}$$

$$\therefore \text{Quantization error} = \frac{0.781}{100} \times (V_{max} - V_{min})$$

$$\Rightarrow \frac{\Delta Q}{V_{max} - V_{min}} = \frac{0.781}{100}$$

$$\Rightarrow \frac{1}{2} \times \frac{V_{max} - V_{min}}{2^N} \times \frac{1}{V_{max} - V_{min}} = \frac{0.781}{100}$$

$$\Rightarrow \frac{1}{2^{N+1}} = \frac{0.781}{100}$$

$$\Rightarrow 2^{N+1} = 128 \Rightarrow \boxed{N = 6}$$

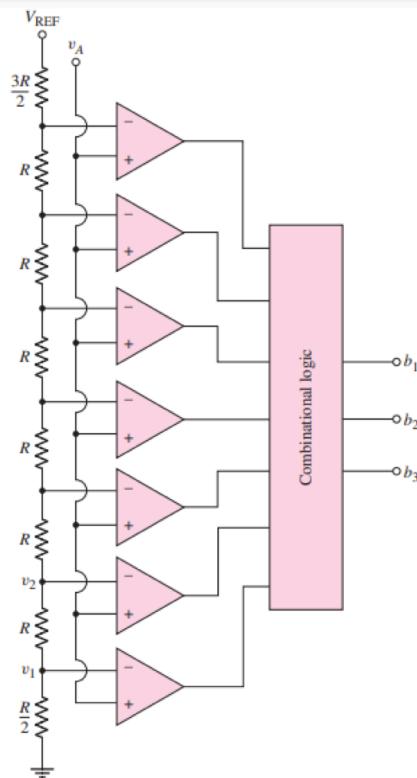
b) 
$$\boxed{f_{sampling} = 2 \times f_{input}}$$



## Question 2

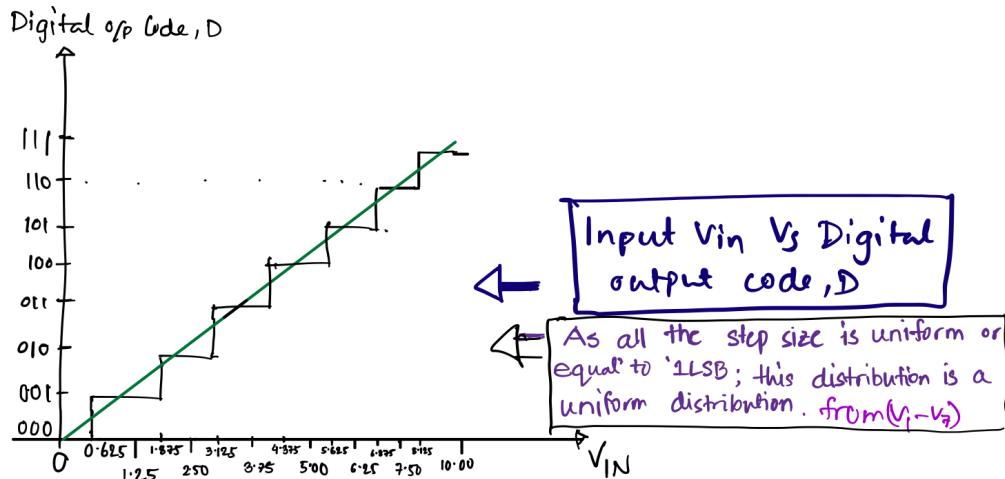
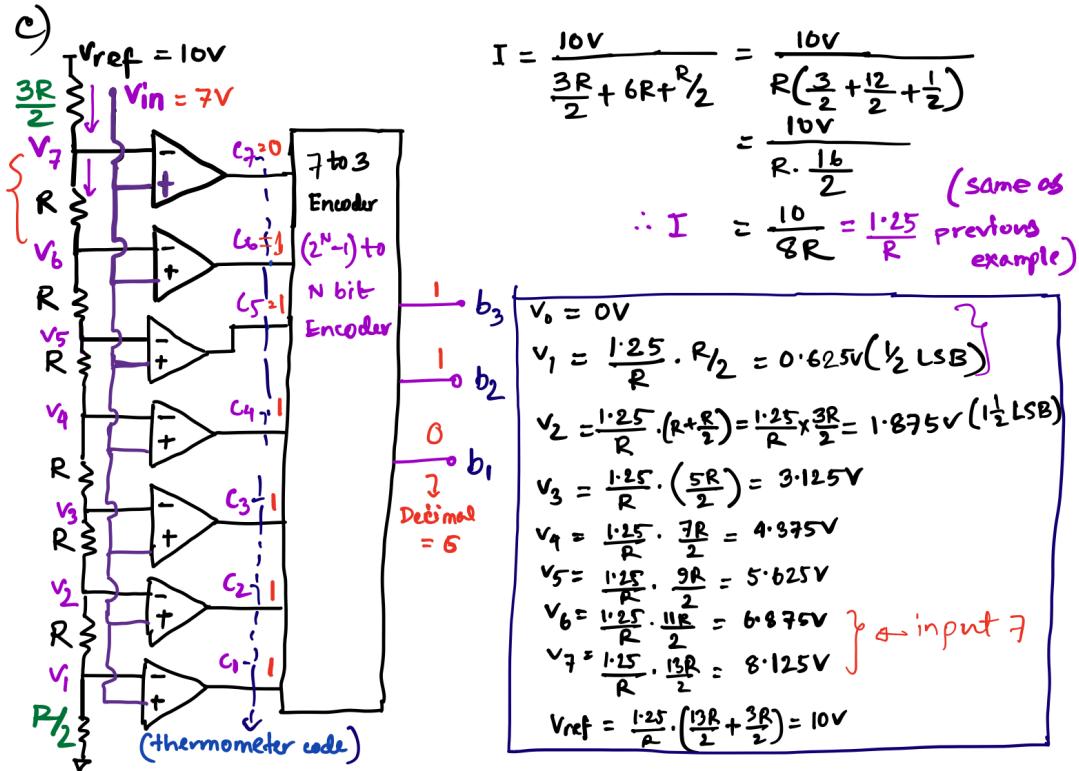
Design a 3 bit flash ADC with a reference voltage of  $V_{REF}=10V$ . The quantized levels for this ADC should be **uniform (Equal step size)**.

- |     |   |
|-----|---|
| (a) | <b>Calculate</b> total number of resistors and comparators required to fabricate a 3-bit flash A/ D converter.  |
| (b) | Calculate the 1LSB value or each step size (quantization range) for this 3 bit ADC. What would be the resolution for this ADC?  |
| (c) | Calculate each <b>quantization level</b> and plot the <b>Vin vs Dout</b> graph.   |
| (d) | If the input voltage <b>Vin= 7 V</b> ,<br>i) Comment on the <b>quantization range</b> in which the input lies.<br>ii) Find the <b>digital output</b> for the given input. |
| (e) | If the 3-bit output is <b>100</b> What is the maximum and minimum value of $v_A$ that produces this output?(Hint:find the quantization range).                            |
| (f) | If 1 bit was increased from this 3 bit Flash ADC, how many resistors and comparators are required? comment on the hardware changes for this 1 bit of increment.           |



a)  $N = 3$ ; Resistor required =  $2^N = 2^3 = 8$   
 Comparator required =  $2^3 - 1 = 7$

b) 1 LSB = resolution or step size =  $\frac{V_{max} - V_{min}}{2^N} = \frac{10 - 0}{2^3} = 1.25 \text{ V}$



d) if input = 7V ; it will be in between the quantization range of  $v_6 - v_7$  or  $6.875V - 8.125V$ .

Quantization Range	Quantized value	Digital o/p ( $b_2 b_1 b_0$ )
$6.875V - 8.125V$	6	110

e) If digital output = 110 = 6 ( quantized value)

$$\text{Maximum value of } v_A = 8.125V$$

$$\text{Minimum value of } v_A = 6.875V$$

f) If 1 bit was increased  $\rightarrow N = 3+1 = 4 \text{ bit}$

$$\text{No. of } Q = 2^N = 2^4 = 16$$

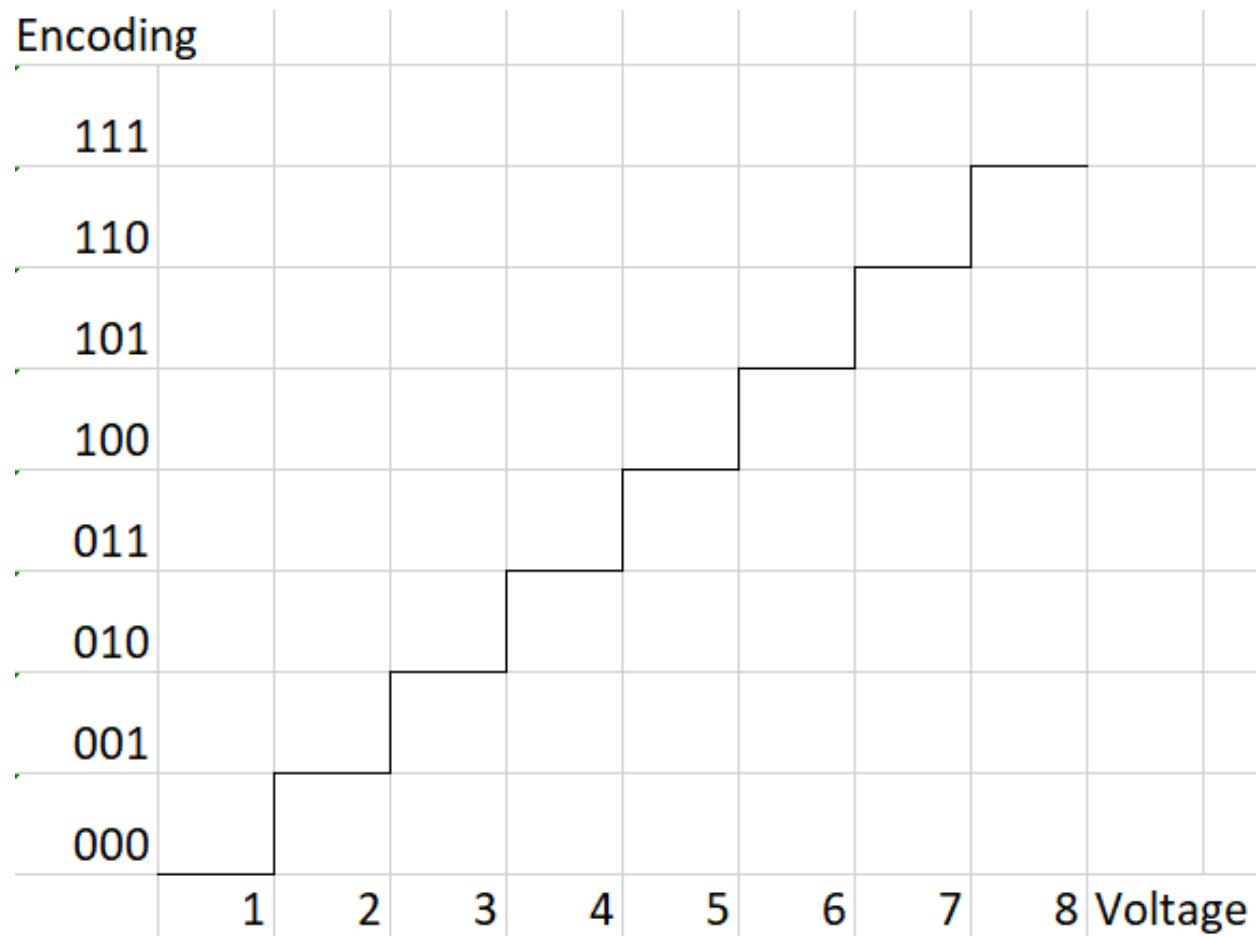
$$\text{No. of comparator} = 2^4 - 1 = 15$$

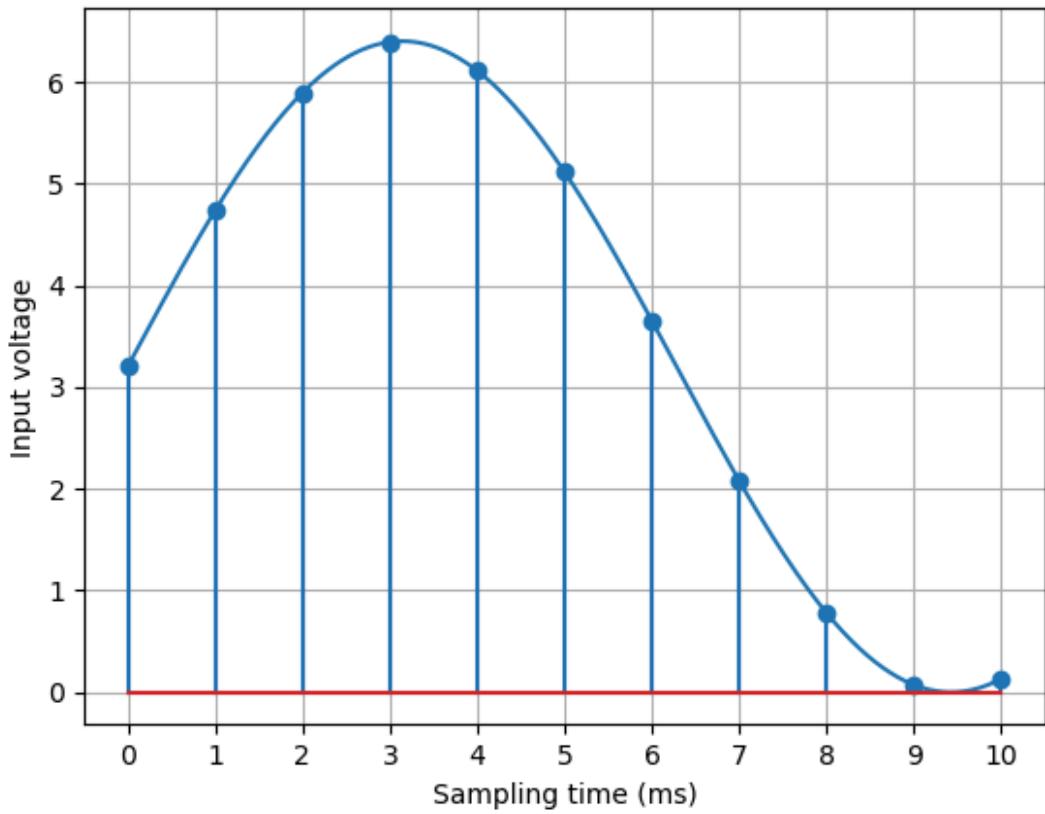
Encoder = 15 lines to 4 lines

1 bit of increment doubles the hardware needed.

## Question 3

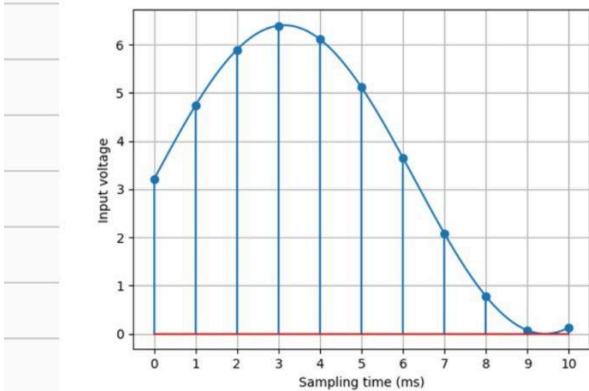
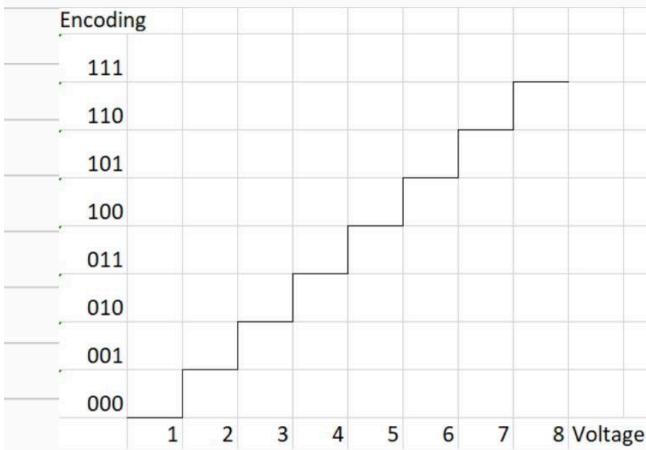
## Encoding



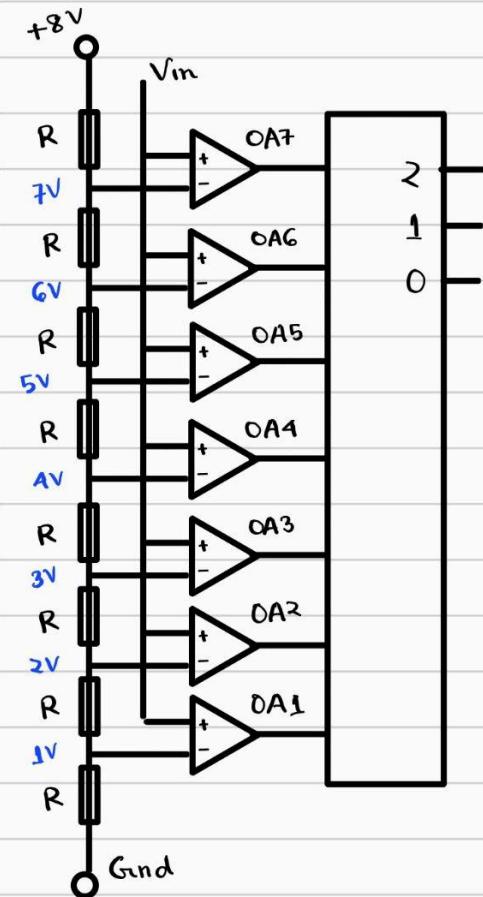


(a)	Design a 3-bit Flash ADC circuit for the given input-output characteristics.
(b)	An unknown signal is passed to the ADC as input. The ADC takes samples at a rate of 1kHz. In the graph, the input signal is shown where the x-axis represents time, and the y-axis represents the voltage at any specific time. The sampling instances are given in the figure. Find the encoded output that represents the analog signal inside the given time frame.

# Solution:



(a) 3 bit ADC -  $2^3 - 1 = 7$   
op amps and 8 resistors required.



(b)

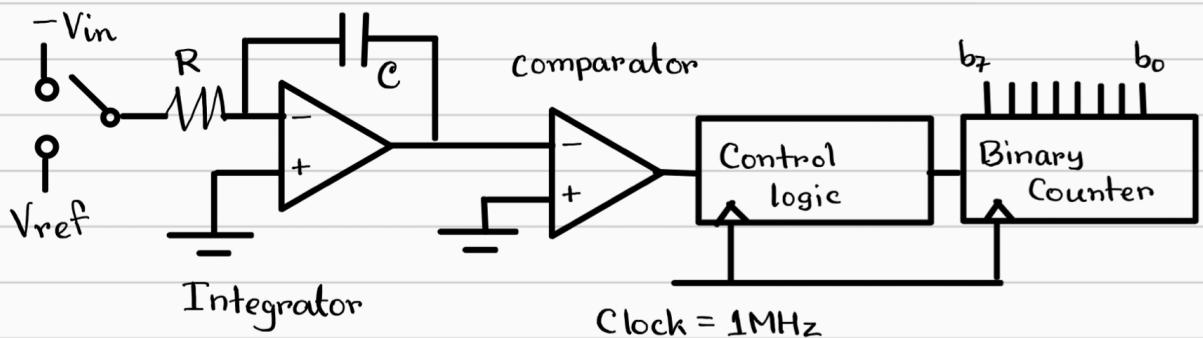
Sampling instance	Level	Encoding
0	3	011
1	4	100
2	5	101
3	6	110
4	6	110
5	5	101
6	3	011
7	2	010
8	0	000
9	0	000
10	0	000



# Question 4

## Dual-Slope A/D Converter

- A dual slope A/D converter has  $V_{ref} = 5V$ , and a 8 bit counter that outputs an 8-bit representation of the input signal. A  $1\text{ MHz}$  clock is used for the clock and counter circuits



- ① Determine the input voltage range, number of steps and step size (resolution) of the A/D converter.
- ② For a specific input voltage, the ADC outputs a count of  $m=100$ . Determine the input voltage.
- ③ Determine the total time required to get the reading in ②
- ④ Calculate the maximum sampling rate of the ADC.
- ⑤ A person wishes to get a sampling rate 4 times that of the current circuit. Determine how many bits should be used for the counter without changing any other system parameters.

(I) Input voltage range :  $5V (0-V_{ref})$

$$\text{number of steps} = 2^n = 2^8 = 256$$

$$\text{step size} = \frac{\text{voltage range}}{\text{number of steps}} = 0.0195 V$$

(II) We know,  $V_{in} = \frac{m}{2^n} V_{ref} = \frac{100}{256} \times 5V = 1.95V$

(III) For a single conversion, the integrator

(a) integrates  $-V_{in}$  for  $t_1$  duration as counter counts from  $0-2^n$

$$t_1 = \frac{2^n}{\text{clock rate}} = \frac{256}{1 \times 10^6} = 2.56 \times 10^{-4} s$$

(b) integrates  $V_{ref}$  for  $t_2$  duration as counter counts from  $0-m$

$$t_2 = \frac{m}{\text{clock rate}} = \frac{100}{1 \times 10^6} = 1 \times 10^{-4} s$$

$$\text{total conversion time} = t_1 + t_2 = 3.56 \times 10^{-4} s$$

(IV) Maximum sampling rate is limited by the time required for worst case conversion of input = 5V

$$\text{In that case, } t_1 = t_2 = 2.56 \times 10^{-4} s$$

$$\text{thus, worst case conversion duration} = t_1 + t_2 = 5.12 \times 10^{-4} s$$

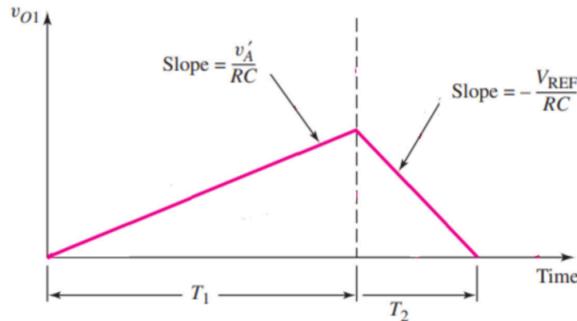
$$\text{Max sampling rate} = \frac{1}{5.12 \times 10^{-4} s} = 1953.125 \text{ Hz}$$

(V) Sampling duration  $\propto 2^n$  // Sampling rate  $\propto \frac{1}{2^n}$

For 4 times sampling rate, counter bit =  $(8-2) = 6$

$$f) \frac{D}{2^N} = \frac{V_A'}{V_{REF}} \Rightarrow D = \frac{V_A' \times 2^N}{V_{REF}} = \frac{3}{5} \times 2^8 = 153.6 \approx 153$$

Digital o/p (binary value of 153) = 10011001



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|-----|---|
| (a) | Find the value of $V_{O1}$ at $t=T_1$ , suppose $R=25k\Omega$ and $C=2\mu F$ .  |
| (b) | If $R=50k\Omega$ and we $C=2\mu F$ , calculate the new value of $V_{O1}$ at $t=T_1$ , compare it with (a) and comment on the changes between two output voltages. |

$$a) \text{slope} = \frac{\Delta Y}{\Delta X} = \tan\theta = \frac{OB}{AB}$$

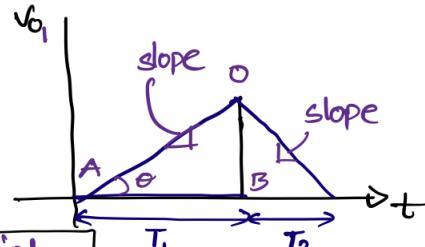
$$\text{As, } \tan\theta = \frac{V_A'}{RC}; \text{ so } \frac{OB}{AB} = \frac{V_A'}{RC}$$

$$\Rightarrow V_{O1} = OB = \frac{V_A'}{RC} \times AB$$

$$\Rightarrow V_{O1} = \frac{V_A'}{RC} \times T_1 \quad \boxed{T_1 = 2^N \cdot 1 \text{ clock period} \\ = 2^N \cdot T = 2^6 \cdot 6\mu s}$$

$$\Rightarrow V_{O1} = \frac{2}{25k\Omega \times 2\mu F} \times 2^6 \times 6\mu s$$

$$\boxed{V_{O1} = 0.01536V}$$



$$b) V_{O1} = \frac{2}{50k\Omega \times 2\mu F} \times 2^6 \times 6\mu s$$

$$\boxed{V_{O1} = 0.00768V}$$

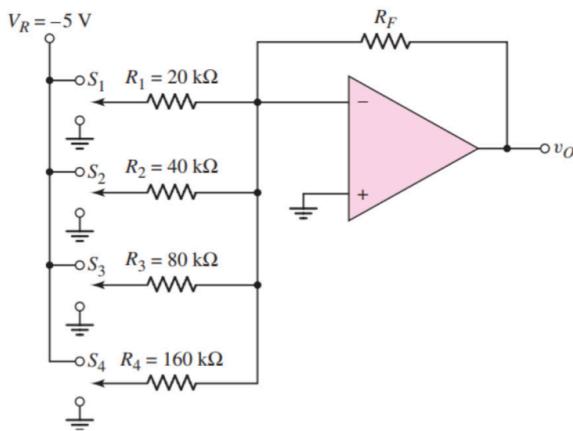
Comment:

As, resistance increases by 2, it decreases the output by half.

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## Question 5

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|-----|--|
| (a) | Determine the output voltage, $v_o$ in V of the 4-bit weighted-resistor D/A in the following figure for input =1010 and input=1100? Assume $R_F = 5\text{k}\Omega$ .   |
| (b) | Identify the maximum allowed tolerance ( $\pm$ percent) in the value of $R_1$ so that the maximum error in the output is limited to $\pm \frac{1}{2}$ LSB quantized voltage value?<br>(hint: Do two separate calculations for output error being $+\frac{1}{2}$ LSB and $-\frac{1}{2}$ LSB Then, calculate the percentage change in $R_1$ in these two cases.) |



a) Input = 1010 ;  $R_F = 5\text{k}\Omega$

$$v_o = 5 \times \frac{5}{20} + 5 \times \frac{5}{80} = 1.5625\text{V}$$

Input = 1100 ;  $R_F = 5\text{k}\Omega$

$$v_o = 5 \times \frac{5}{20} + 5 \times \frac{5}{40} = 1.875\text{V}$$

b)  $1 \text{ LSB} = 5 \times \frac{5}{160} = 0.15625\text{V}$

$$\Rightarrow \frac{1}{2} \text{ LSB} = 0.078125\text{V}$$

$$1 \text{ MSB} = 1.25\text{V} \rightarrow$$

$$v_o = 1.25 \pm 0.078125\text{V}$$

$$= 1.328125\text{V} \text{ or } 1.171875\text{V}$$

$$-5 \times \frac{5}{R_1} = 1.328125\text{V}$$

or

$$-5 \times \frac{5}{R_1} = 1.171875\text{V}$$

$\Rightarrow$

$$R_1 = 18.823\text{k}\Omega \rightarrow \% \text{ change in } R_1 = \frac{20-18.823}{20} \times 100 = 5.88\%$$

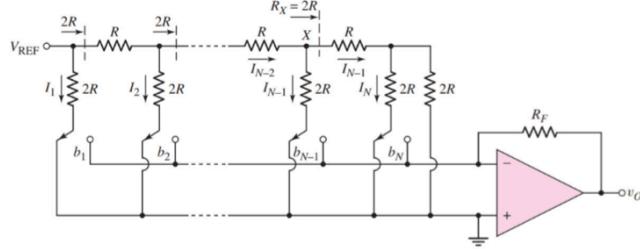
$$\text{Or } 21.33\text{k}\Omega \rightarrow \% \text{ change in } R_1 = \frac{21.33-20}{20} \times 100 = 6.67\%$$

$$\boxed{\text{Max tolerance} \rightarrow 5.88\%}$$

$$\left. \begin{array}{l} v_o = 1 \text{ MSB} + \frac{1}{2} \text{ LSB} \\ v_o = 1 \text{ MSB} - \frac{1}{2} \text{ LSB} \end{array} \right\} \text{Output error}$$

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## Question 6



The  $N$ -bit D/A converter with an  $R-2R$  ladder network in the above figure is to be designed as a 6-bit D/A device. Suppose  $V_{REF} = -5V$  and  $R_F = 5k\Omega$ .

(a)	Find currents $I_1, I_2, I_3, I_4, I_5, I_6$ .
(b)	What is the output voltage if the input is 010011?
(c)	What is the change in output voltage if the input changes from 101010 to 010101?

$$a) I_1 = \frac{V_{REF}}{2R} = \frac{-5}{10} \Rightarrow I_1 = -0.50mA$$

$$I_2 = \frac{I_1}{2} = -0.25mA$$

$$I_3 = \frac{I_2}{2} = -0.125mA$$

$$I_4 = \frac{I_3}{2} = -0.0625mA$$

$$I_5 = \frac{I_4}{2} = -0.03125mA$$

$$I_6 = \frac{I_5}{2} = -0.015625mA$$

$$b) \text{ Input } = 010011$$

$$v_o = -[I_2 + I_5 + I_6] R_F = [0.25 + 0.03125 + 0.015625]mA \times 5k\Omega = 1.484375V$$

$$c) \text{ Input } = 101010$$

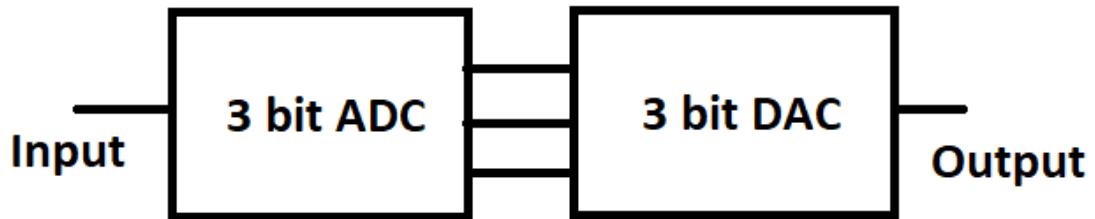
$$v_o = -[I_1 + I_3 + I_5] R_F = [0.50 + 0.125 + 0.03125]mA \times 5k\Omega = 3.28125V$$

$$\text{Input } = 010101$$

$$v_o = -[I_2 + I_4 + I_6] R_F = [0.25 + 0.0625 + 0.015625]mA \times 5k\Omega = 1.640625V$$

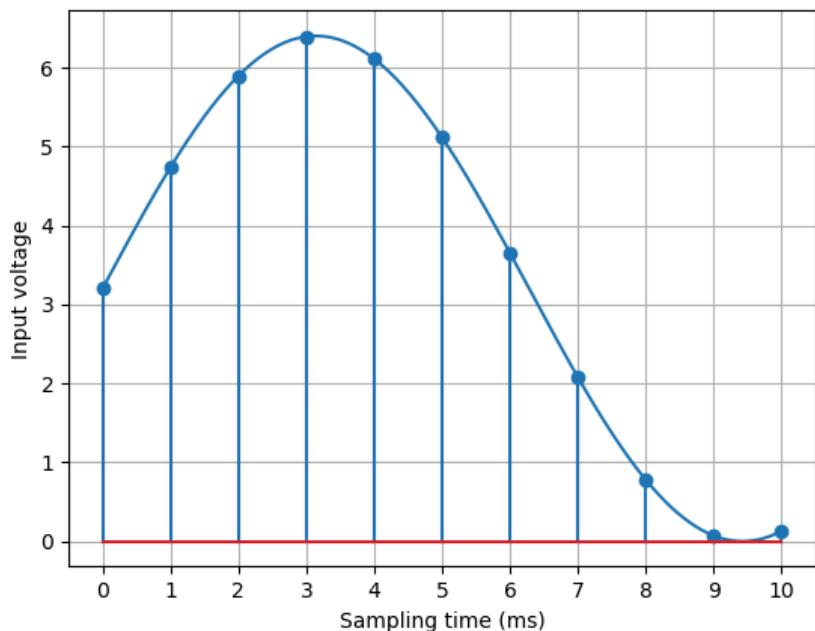
$$\Delta v_o = 1.640625V$$

## Question 7



ADC Input Voltage	Encoding	DAC Output Voltage
0-1	000	0.5
1-2	001	1.5
2-3	010	2.5
3-4	011	3.5
4-5	100	4.5
5-6	101	5.5
6-7	110	6.5
7-8	111	7.5

- |     |   |
|-----|---|
| (a) | For the following input waveshape, draw the reconstructed output by the DAC. The sampling instances are marked on the input waveshape.          |
| (b) | Comment on the quality of the reconstructed signal and how the quality would be affected if additional bits were used for both the ADC and DAC. |

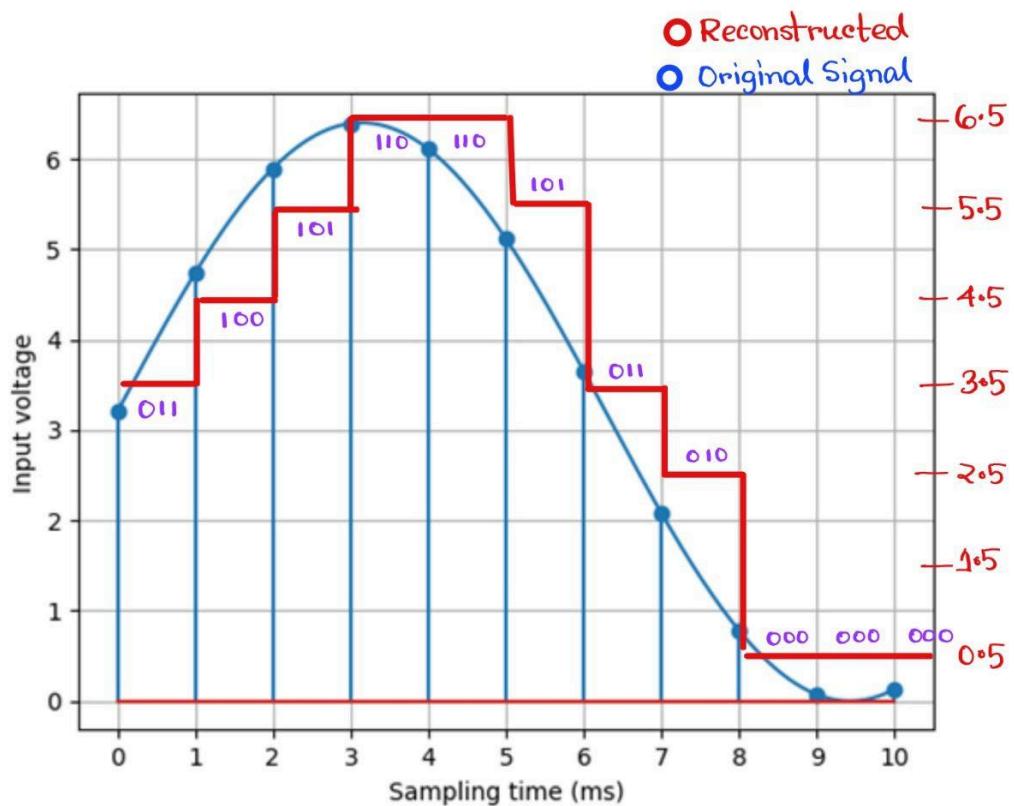


Solution:

(a)



ADC Input Voltage	Encoding	DAC Output Voltage
0-1	000	0.5
1-2	001	1.5
2-3	010	2.5
3-4	011	3.5
4-5	100	4.5
5-6	101	5.5
6-7	110	6.5
7-8	111	7.5



(b)

Reconstructed signal roughly estimates the original input, and the quality is not very good.

Using higher number of bits for both the ADC and DAC will give a better voltage resolution. The reconstructed voltage levels would be closer to that of the originally sampled value.