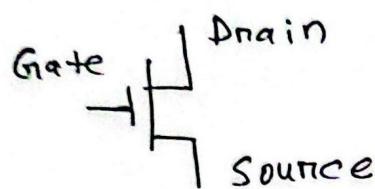


CMOS → complementary MOSFET logic gates.

NMOS       $\rightarrow \boxed{\text{H}} \text{ on } \rightarrow \boxed{\text{L}}$

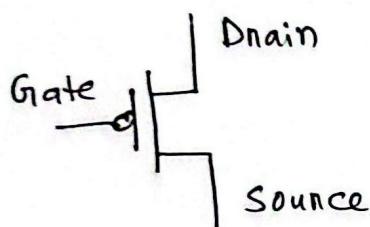
PMOS       $\rightarrow \boxed{\text{L}} \text{ on } \rightarrow \boxed{\text{H}}$



For NMOS →

Gate → High → Drain { Source } Short circuit

Gate → Low → Drain { Source } Open circuit

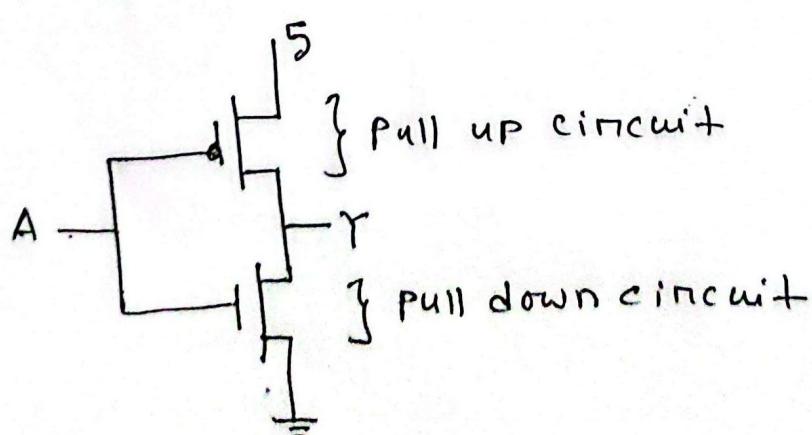


For PMOS →

Gate → High → Drain { Source } Open circuit

Gate → Low → Drain { Source } Short circuit

Not gate:



$$A \rightarrow \boxed{Y}$$

$$Y = \bar{A}$$

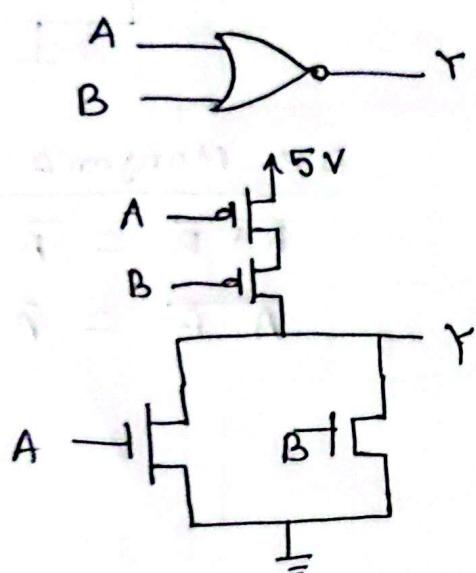
case 1 : A = 1 / High

$$Y = 0V$$

case 2 : A = 0 / Low

$$Y = 5V$$

### NOR Gate



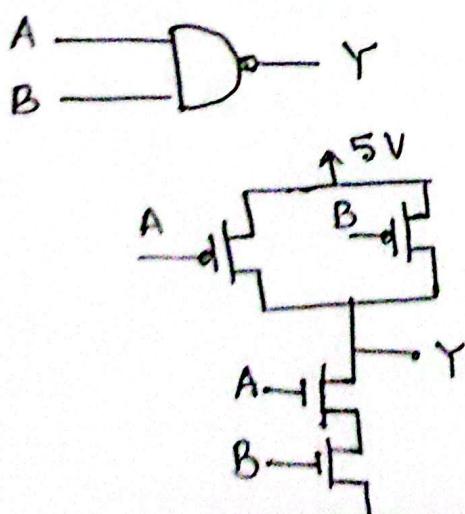
$$Y = \overline{A+B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

OR  $\rightarrow$  Parallel

AND  $\rightarrow$  Series

### NAND gate



$$Y = \overline{A \cdot B}$$

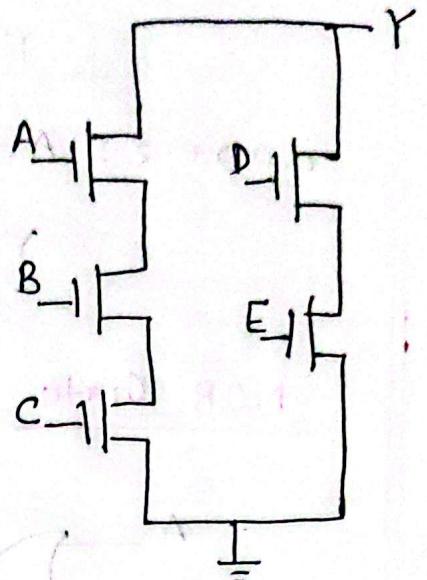
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$$Y = \overline{ABC + DE}$$

Pull down circuit

$$\bar{Y} = \overline{\overline{ABC + DE}}$$

$$\Rightarrow \bar{Y} = ABC + DE$$



Pull up circuit

$$Y = \overline{ABC + DE}$$

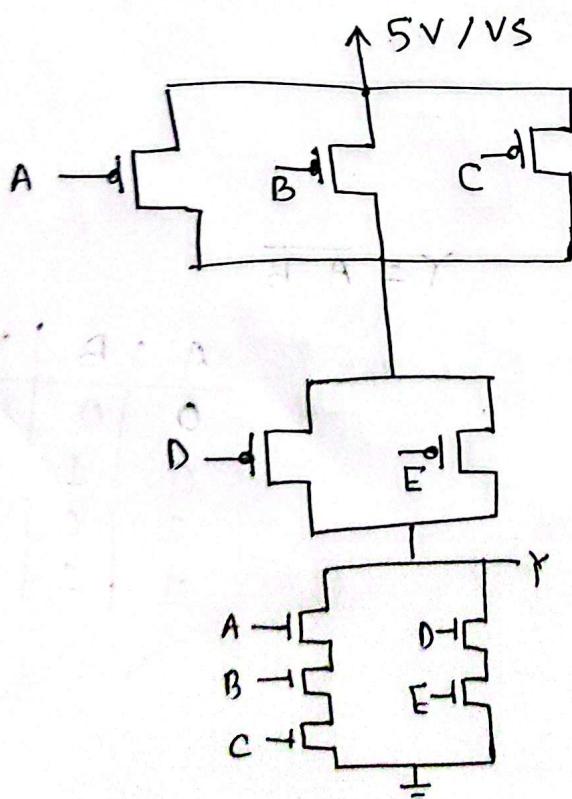
$$= \overline{ABC} \cdot \overline{DE}$$

$$Y = (\bar{A} + \bar{B} + \bar{C}) (\bar{D} + \bar{E})$$

De Morgan's Law

$$\overline{A + B} = \bar{A} \cdot \bar{B}$$

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

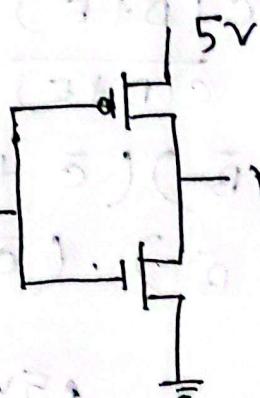
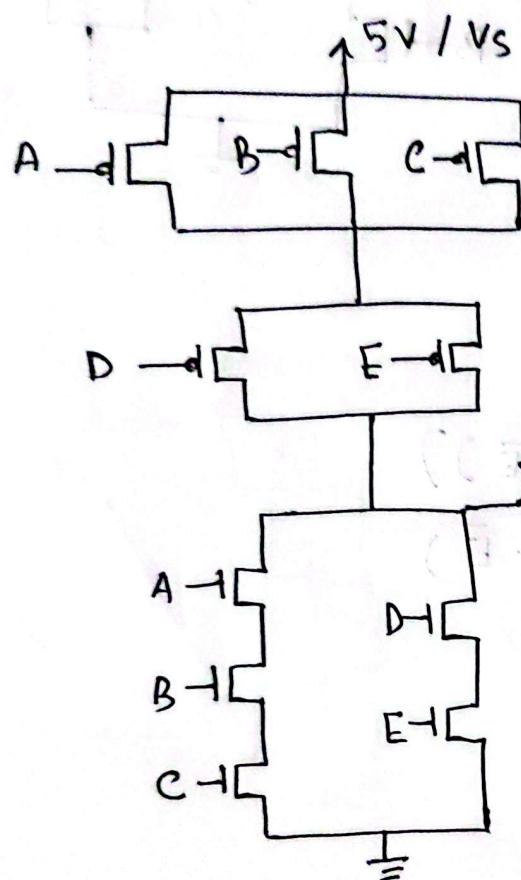


$$Y = ABC + DE$$

Assume,  $Z = \bar{Y}$

$$Z = \overline{ABC + DE}$$

Implement  $Z$



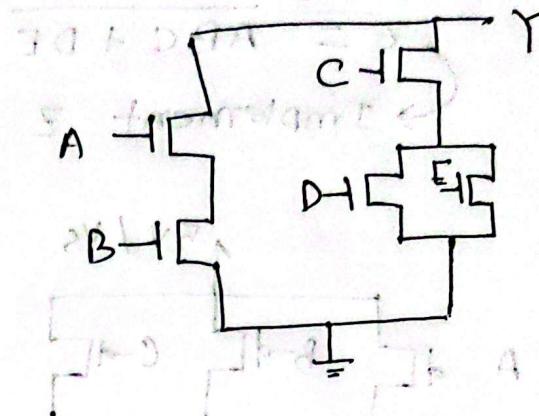
$$Y = AB + C(D+E)$$

$$\text{Assume } Z = \bar{Y} = \overline{AB + C(D+E)}$$

Pull down

$$Z = \overline{AB + C(D+E)}$$

$$\bar{Z} = AB + C(D+E)$$



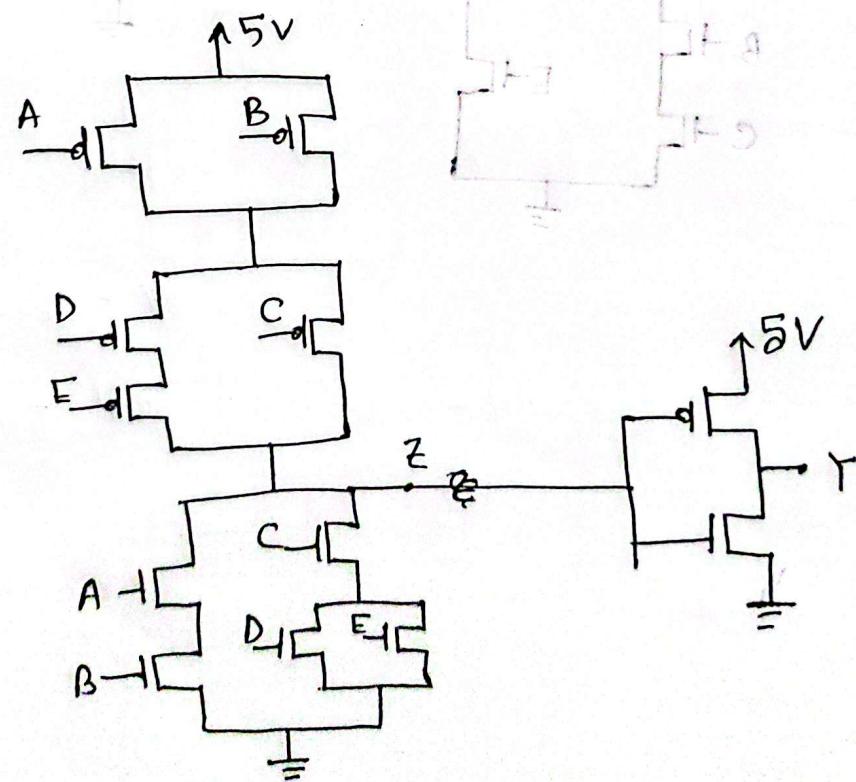
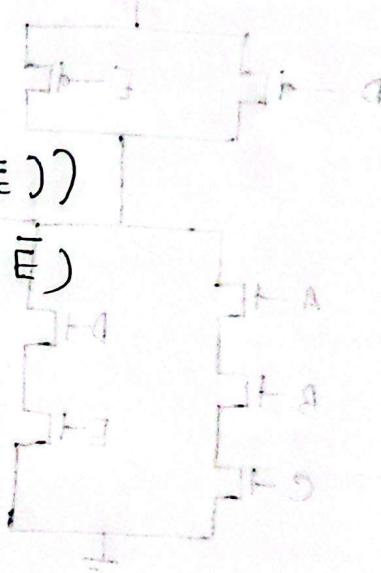
Pull up

$$Z = \overline{AB + C(D+E)}$$

$$= \overline{AB} \cdot \overline{C(D+E)}$$

$$= (\bar{A} + \bar{B})(\bar{C} + (\bar{D+E}))$$

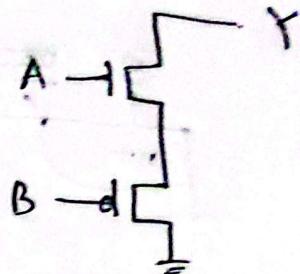
$$= (\bar{A} + \bar{B}) \cdot (\bar{C} + \bar{D} \cdot \bar{E})$$



$$Y = \bar{A} + B$$

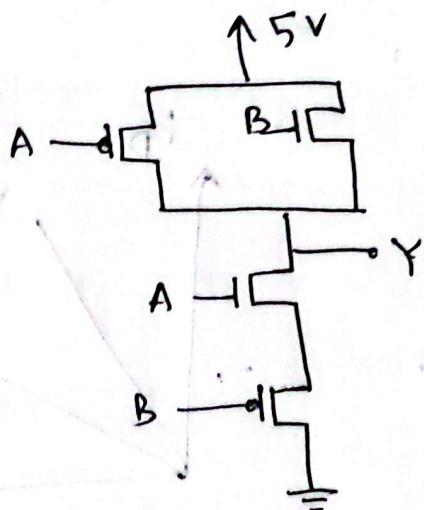
Pull down

$$\begin{aligned} Y &= \overline{\bar{A} + B} \\ &= A \cdot \bar{B} \end{aligned}$$



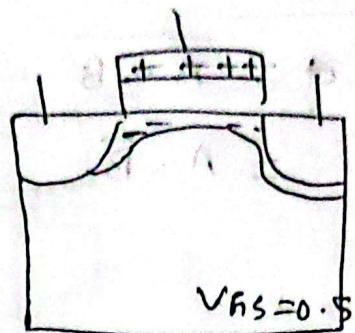
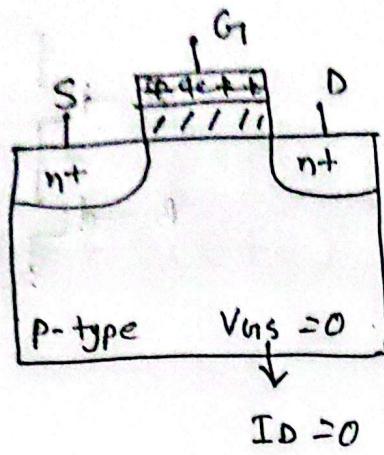
Pull up

$$Y = \bar{A} + B$$

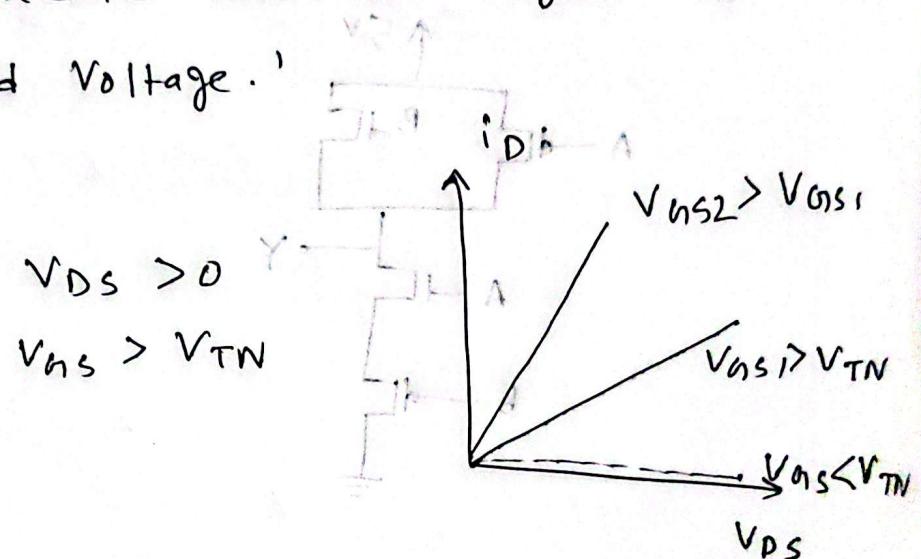
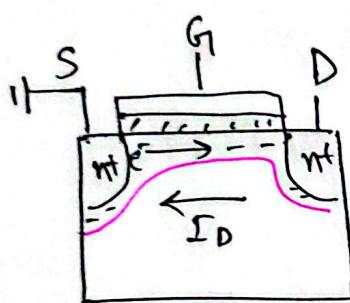


**NMOS :**

current flow (create channel)



min  $V_{GS}$  to create 'inversion layer' is called 'Threshold Voltage.'

**Triode:**

$$V_{DS} < V_{GS} - V_t$$

$$I_D = k_n [2(V_{GS} - V_t)V_{DS} - V_{DS}^2]$$

**Saturation:**

$$V_{DS} > V_{GS} - V_t$$

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2$$

$$k_n = \frac{1}{2} \mu_n C_o x (W/L)$$

## NMOS Inverter

$V_I = \text{High}$ ,  $V_O = \text{Low}$

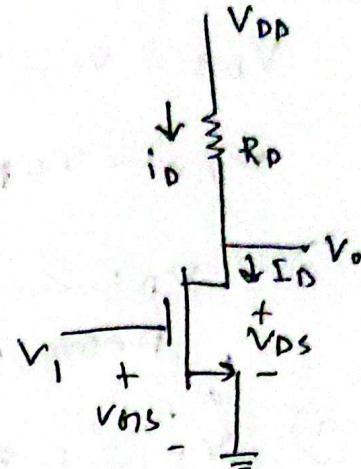
$V_I = \text{Low}$ ,  $V_O = V_{DD}$



current flow starts

$$I_{RD} = I_D$$

$$I_{RD} = \frac{V_{DD} - V_O}{R_D} = \frac{V_{DD} - V_{DS}}{R_D}$$



Problem 1  $V_{DD} = 5V$ ,  $R_D = 20k\Omega$ ,  $V_{TN} = 0.5V$ ,  $k_n = 0.3 \text{ mA/V}^2$ .

Find  $V_O$  for  $V_I = 5V$  and  $V_I = 1.5V$ .

i)  $V_I = 5V$

$$V_{GS} = V_I - 0 = 5V$$

Transistor ON

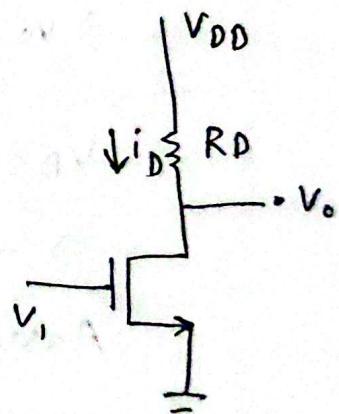
Mode: Triode

$$I_{RD} = I_D$$

$$\Rightarrow \frac{V_{DD} - V_O}{R_D} = k_n [2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2]$$

$$\Rightarrow \frac{5 - V_O}{20} = 0.3 [2(5 - 0.5) V_O - V_O^2]$$

$$\therefore V_O = 0.09, 0.02 > 5; (\text{not possible}) \quad \text{So } 0.09$$



$V_{DS} = V_O$   
 $V_{GS} \text{ is } 2.5V$   
 triode  
 $V_{GS} \text{ is } 2.5V$   
 saturation

Verify

$$V_{DS} = V_o = 0.09$$

$$V_{DS} - V_{TN} = 5 - 0.15 = 4.85$$

$$V_{DS} < V_{DS} - V_{TN}$$

∴ Assumption correct

ii)  $V_E = 1.5 \text{ V}$  (Assume Saturation)

$$I_{RD} = I_D$$

$$\Rightarrow \frac{5 - V_o}{20} = k_n (V_{DS} - V_{TN})^2$$

$$\Rightarrow \frac{5 - V_o}{20} = 0.3 (1.5 - 0.5)^2$$

$$\Rightarrow V_o = -1 \text{ V}$$

$$V_{DS} \geq V_{DS} - V_{TN}$$

$$\Rightarrow -1 \geq (1.5 - 0.5) \quad \times \text{ wrong assumption}$$

Assume triode:

$$I_{RD} = I_D$$

$$\Rightarrow \frac{5 - V_o}{20} = 0.3 [2(1.5 - 0.5)V_o - V_o^2]$$

$$\Rightarrow V_o = 0.5, 1.66$$

$$V_{DS} < V_{DS} - V_{TN}$$

$$1.66 < 1 \quad \times$$

$$\text{So } V_o = 0.5 < 1$$

Problem 2  $V_{DD} = 2.5V$ ,  $R_D = 20k\Omega$ ,  $V_{TN} = 0.5V$ ,

$$k_n = 0.3 \text{ mA/V}^2$$

Determine the transition point, minimum output voltage, maximum drain current and maximum power dissipation of an NMOS inverter with resistor load.

(i) transition

$$V_{DS} = V_{DS(\text{satn})} = V_{GS} - V_{TN}$$

$$\begin{aligned} I_D &= k_n (V_{GS} - V_{TN})^2 \\ &= k_n V_o^2 \end{aligned}$$

$$I_{RD} = \frac{2.5 - V_o}{20}$$

$$k_n V_o^2 = \frac{2.5 - V_o}{20}$$

$$\Rightarrow V_o = 0.56 ; -0.73$$

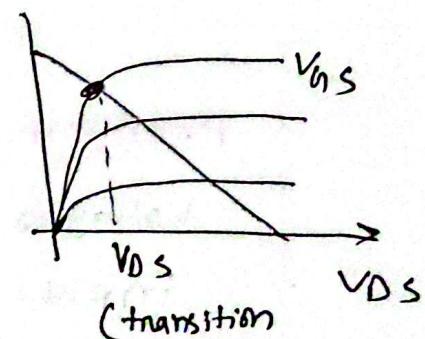
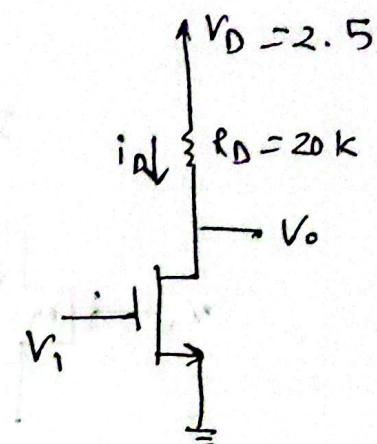
$$V_{DS} = 0.56 \text{ (transition)}$$

(ii) minimum drain current (when  $V_I = V_{DD}$ )  
(Triode)

$$\frac{2.5 - V_o}{20} = 0.3 [2(2.5 - 0.5) V_o - V_o^2]$$

$$\Rightarrow V_o \}$$

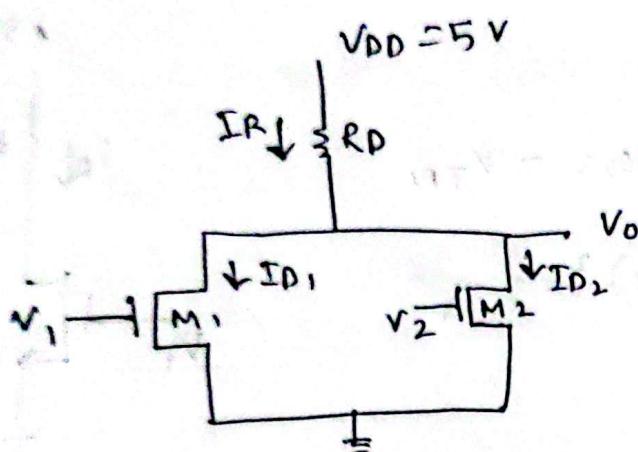
$$I_D = \frac{2.5 - V_o}{20} = I_{D\max}$$



(iii) maximum power desipation

$$P = V_{DD} \times I_{D, \max}$$

NMOS NOR



$V_1$	$V_2$	$V_o$
H	H	L
H	L	L
L	H	L
L	L	H

Problem 3 Determine the currents and voltages in a digital logic gate, for various input conditions.

$$R_D = 20\text{k}\Omega, k_n = 0.1 \text{ mA/V}^2, V_{TN} = 0.8 \text{ V}, \tau = 0$$

case 1:  $V_1 = 5 \text{ V}, V_2 = 0 \text{ V}$  /  $V_{GS} = 5 \text{ (High)}$   
 $V_1 = 0, V_2 = 5 \text{ (Low)}$   
 $\downarrow$   
 $\text{Same}$   
 $\downarrow$   
 $\text{triode}$

$$I_R = I_{D1}$$

$$\Rightarrow \frac{V_{DD} - V_o}{R_D} = k_n [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

$$\Rightarrow \frac{5 - V_o}{20} = 0.1 \times [2(5 - 0.8)V_o - V_o^2]$$

$$\therefore V_o = 8.6 \times 0.29 \text{ V}$$

$V_{GS}$  low  
 $\downarrow$   
 $\text{satn}$

Verify

$$V_{DS} < V_{DS}(\text{satn})$$

$$\Rightarrow V_{DS} < V_{GS} - V_{TN}$$

$$\Rightarrow 0.29 < 5 - 0.8$$

$$\Rightarrow 0.29 < 4.2$$

Assumption correct

$$I_R = \frac{5 - 0.29}{20} = 0.24 \text{ mA}$$

case 2:  $v_1 = v_2 = 5v$  (Triode)

$$V_{DS} = v_0 \\ V_{GS} = 5v$$

$$I_R = I_{D1} + I_{D2} = 2 \times I_{D1}$$

$$\Rightarrow \frac{5 - v_0}{20} = 2 \times 0.1 [2(5 - 0.8)v_0 - v_0^2]$$

$$\therefore v_0 = \begin{cases} 8.5v \\ 0.147v \end{cases}$$

$$V_{GS} - V_{TN} = V_{DS}(\text{satn})$$

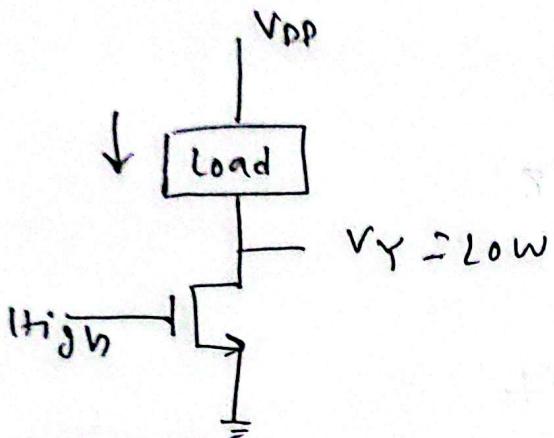
$$= 5 - 0.8 = 4.2$$

Assumption correct

$$I_R = \frac{5 - 0.147}{20}$$

$$I_{D1} = I_{D2} = \frac{I_R}{2}$$

## NMOS Inverter with Enhancement Load



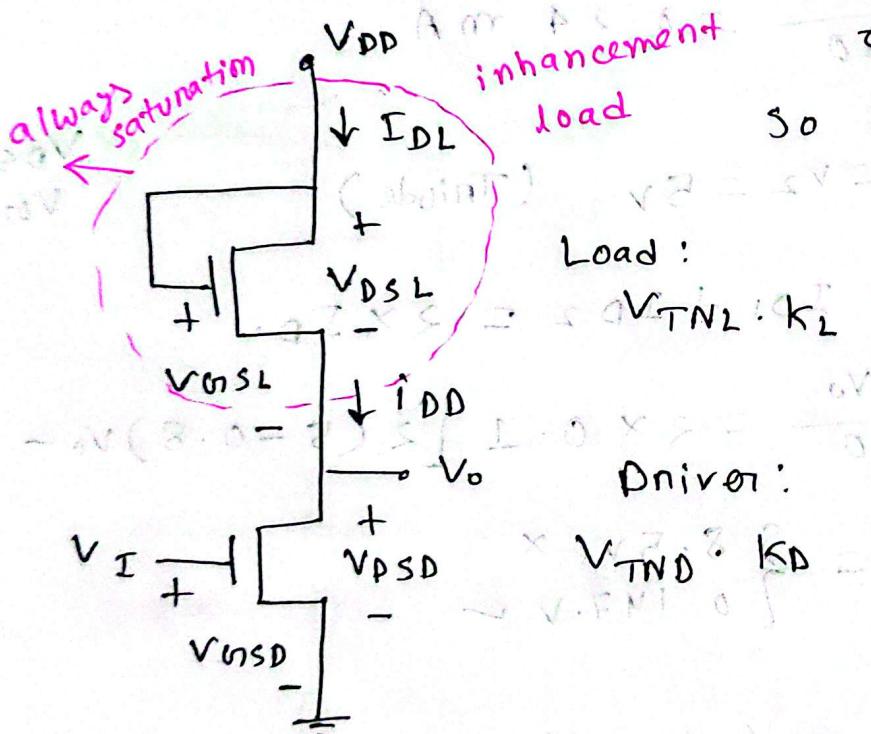
Load = resistor

resistor load factor

front (or) area ପ୍ରମାଣ

$$(R \uparrow V_o \downarrow)$$

from resistance value



$$V_{DS} > V_{GS} - V_{TN}$$

$$\Rightarrow V_{DS} > V_{DS} - V_{TN} \quad (V_{TN} > 0)$$

## NMOS Inverters with Depletion Load

$$V_{TN} = -0.5 \text{ V}$$

$$V_G = V_S \Rightarrow V_{GS} = 0$$

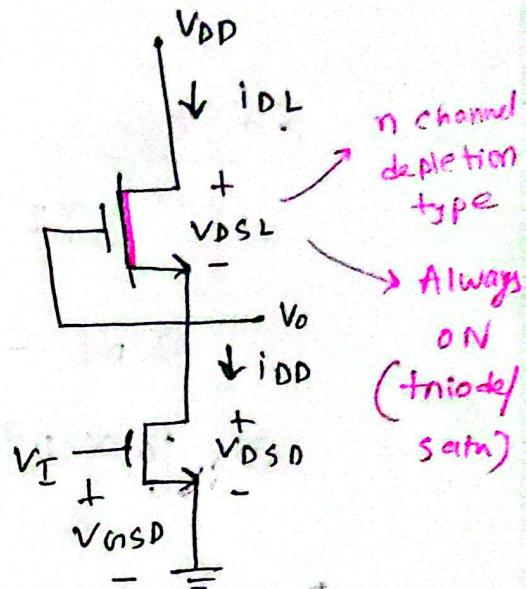
Cut off

$$V_{GS} < V_{TN} = [1 - (m_A + 1)]$$

ON (+triode, satn)

$$V_{GS} \geq V_{TN}$$

$$\Rightarrow 0 \geq -0.5$$



Problem 1  $V_{TND} = V_{TNL} = 1 \text{ V}$ ,  $k_{nD} = 50 \mu \text{A/V}^2$

$k_{nL} = 10 \mu \text{A/V}^2$ . Determine  $V_O$  for  $V_I = 5 \text{ V}$

and  $V_I = 1.5 \text{ V}$

case 1 :  $V_I = 5 \text{ V}$

$$I_{D,2} = I_{D,0}$$

$$\Rightarrow k_{nL} (V_{GS,L} - V_{TN,L})^2$$

$$= k_{nD} \left[ 2 (V_{GS,D} - V_{TN,D})^2 \right] \left[ \frac{V_{DS,D}}{V_{DS,D} - V_{GS,D}} \right]$$

$$\Rightarrow 10 \times 10^{-3} ((5 - V_O) - 1)^2 = 50 \times 10^{-3} \left[ 2(5 - 1) V_O - V_O^2 \right]$$

$$\therefore V_O = 7.45 \times 0.35 \text{ V}$$

$V_{GS,D} = 5 \text{ V}$   
 $V_{GS} \text{ high} \downarrow$   
 triode  
 load  $\Rightarrow$  satn  
 drive  $\Rightarrow$  triode

$$I_{D,D} = 10 \times 10^{-3} (5 - 0.35 - 1)^2$$

case 2

$$VI = 1.5 V$$

Driver - Satn  
Load - Satn

$$I_{DL} = I_{DD}$$

$$\Rightarrow 10 \times 10^{-3} [(5 - v_o) - 1]^2 = 50 \times 10^{-3} [(V_{DS,D} - V_{TN,D})^2]$$

$$\Rightarrow = 50 \times 10^{-3} (1.5 - 1)^2$$

$$\Rightarrow v_o = \{ 2.88, 5.11 \}$$

verify:  $V_{DS} = 1.5 V > V_{TN}$

$$V_{DS,D} = 1.5 V$$

$$V_{DS}(\text{satn}) = V_{DS} - V_{TN}$$

$$= 1.5 - 1 = 0.5 V$$

$$v_o = V_{DS} = 2.88 > V_{DS}(\text{satn})$$

Assumption correct.

### Problem 5 N.MOS NOR

$$V_{DD} = 2.5 \text{ V}, K'n = 100 \mu\text{A/V}^2,$$

$$V_{TN,D} = 0.4 \text{ V}, V_{TN,L} = -0.6 \text{ V}$$

$$(W/L)_D = 4, (W/L)_L = 1$$

$$I_{D,L} = I_{D,A} + I_{D,B}$$

$$= 2 I_{D,A}$$

$$\Rightarrow k_n' \left(\frac{w}{l}\right)_L \left[ V_{GS,L} - V_{TN,L} \right]^2$$

$$= 2 \times k_n' \left(\frac{w}{l}\right)_D \left[ 2(V_{GS,D} - V_{TN,D})^2 V_{DS,D} - V_{DS,D}^2 \right]$$

$$\Rightarrow 1 [0 - (-0.6)]^2 = 2 \times 4 [2(2.5 - 0.4) v_o - v_o^2]$$

$$\Rightarrow v_o = \begin{cases} 4.189 \\ 0.01 \text{ V} \end{cases}$$

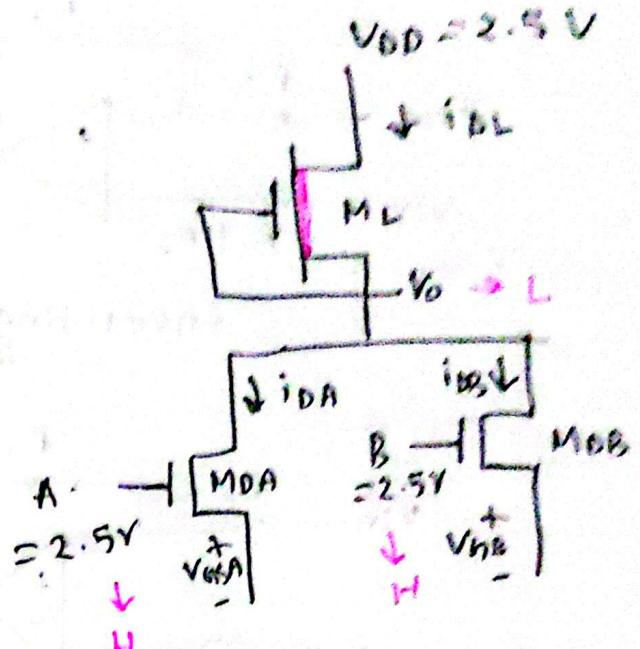
Verify: (Driver)

$$V_{DS} = v_o = 0.01 \text{ V}$$

$$V_{DS} (\text{Satn}) = 2.5 - 0.4 = 2.1 \text{ V}$$

$$(\text{Load}) \quad V_{DS} = 2.5 - 0.01 = 2.49 \text{ V}$$

$$V_{DS} (\text{Satn}) = 0 - (-0.6) = 0.6 \text{ V}$$



Driver:

$$V_{GS,D} = 2.5$$

↓  
High

(triode)

Load:

$$V_{GS,L} = 0$$

(satn)