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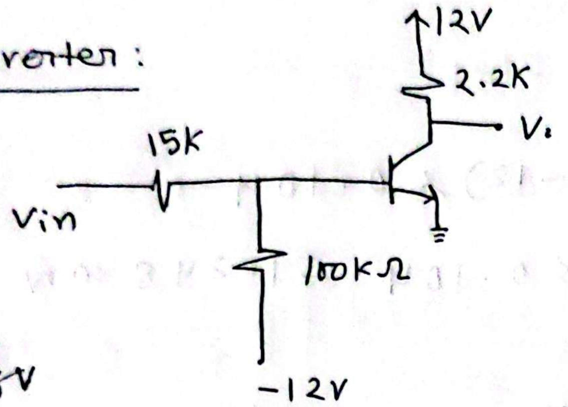
RTL (Resistor Transistor Logic)

↓

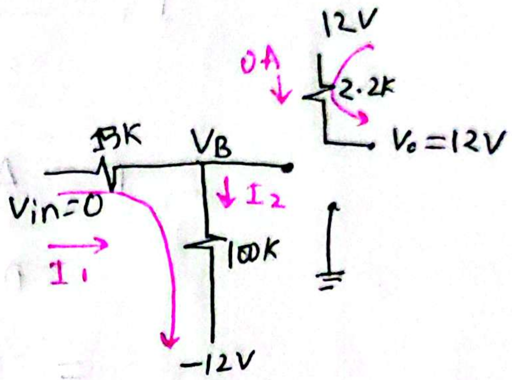
RTL Inverter (NOT Gate)

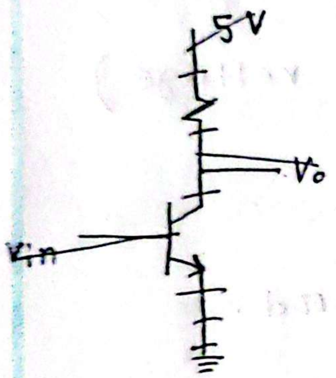
A	Y = Ā
0	1
1	0

RTL Inverter:



⇒





Case 1: Vin = 0V (low)

$V_0 \rightarrow$ High

Assume, T is in cutoff mode.

$I_E = I_B = I_C = 0$

$$\boxed{V_{BE} = V_B - V_E = V_B}$$

If $V_{BE} < 0.5V$; the T is in cutoff mode.

Nodal at V_B;

$I_1 = I_2$

$$\Rightarrow \frac{0 - V_B}{15} = \frac{V_B - (-12)}{100}$$

$\therefore V_B = -1.56\,V$

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$V_{BE} = V_B = -1.56V < 0.5V$

Assumption correct.

Power dissipation :

$$I_1 = \frac{-V_B}{15} = \frac{-(-1.56)}{15} = 0.104 \ mA$$

$$P = \Delta V I$$

$$= 0-(-12) \times 0.104$$

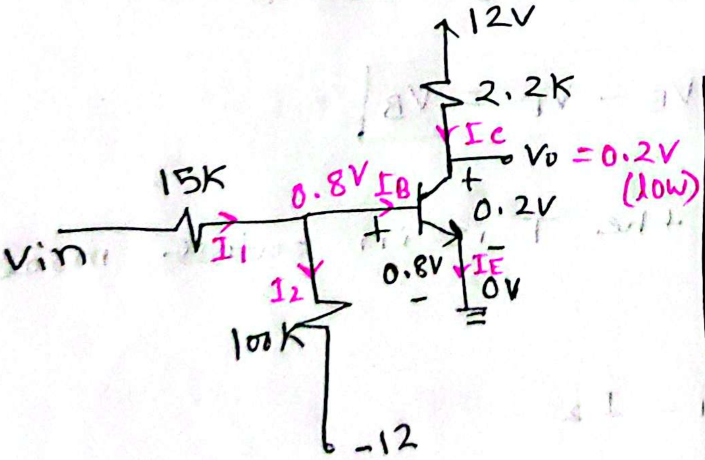
$$= 12 \times 0.104 = 1.248 \ mW$$

<u>case 2</u> : $V_{in} \rightarrow$ High $= 12V$ (supply voltage)

$V_o \rightarrow$ Low

Assume, T is in saturation mood.

$[V_{CE} = 0.2V \ ; \ V_{BE} = 0.8V]$ $\boxed{\beta_F = 30}$



T is in saturation ?

calculate I_C, I_B

Then $\beta_{forced} = \frac{I_C}{I_B}$

$\beta_{forced} < \beta_F$ [correct]

$V_{in} = 12V$, $V_o = 0.2V$

$$I_1 = \frac{12-0.8}{15} = 0.746 \text{ mA}$$

$$I_2 = \frac{0.8-(-12)}{100} = 0.128 \text{ mA}$$

$$I_1 = I_2 + I_B$$

$$\therefore I_B = I_1 - I_2 = 0.618 \text{ mA}$$

$$I_C = \frac{12-0.2}{2.2} = 5.3636 \text{ mA}$$

$$\beta_{forced} = \frac{I_C}{I_B} = \frac{5.3636}{0.618} = 8.68 < 30$$

Assumption is correct.

Power dissipation:

$$P = \Delta V I$$

$$= (12-0.8) I_1 + [0.8-(-12)] I_2 + 0.8 I_B + (12-0) I_C$$

$$= 74.85 \text{ mW}$$

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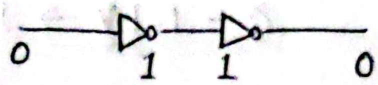
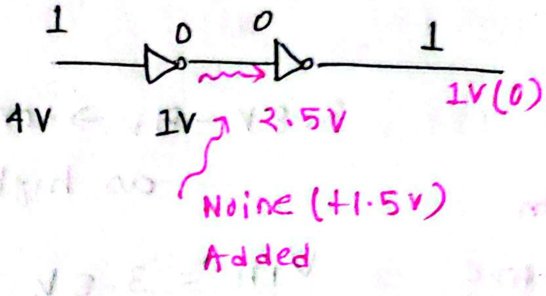
RTL Noise Margin

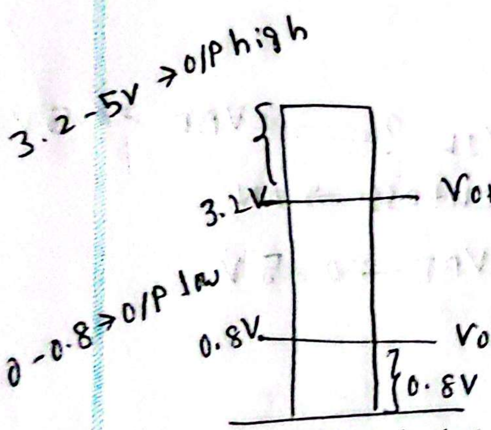


{ 0 – 2V → logic 0
2V – 5V → logic 1 }

O/P of 1st inverter → I/P of the 2nd Inverter



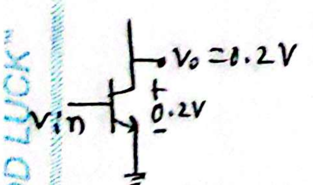
Maximum allowable noise = 1v
[noise margin]



V_{OH} = minimum O/P voltage when logic = 1

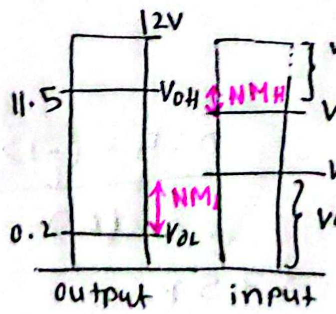
V_{OL} = maximum O/P voltage when logic = 0

O/P of 1st Inverter



O/P low → T is in Satn

$V_{OL} = 0.2V$, $V_{OH} = 11.5V$, supply voltage = 12V



voltage range which is considered as high

V_{IH}

V_{IL}

voltage range which is considered low

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How do we calculate $V_{IL} = ?$

1st

Low → High

0V → 5V

1V → 5V

$\boxed{1.1V}$ → 5V

$\left.\right\}$ cutoff

1.2V → 0V } satn

0 - 1.1V → low input range

$V_{IL} = 1.1V$

2nd

High → Low

5V → 0V

4V → 0V

$\left.\right\}$ satn

$\boxed{3.8V}$ → 0V

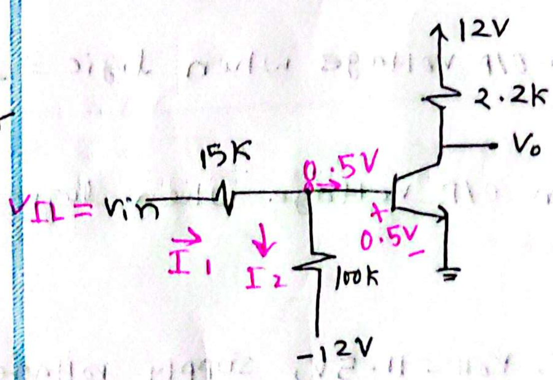
↓Active

3.75V → 5V } cutoff

3.8V - 5V → considered as high input

$V_{IH} = 3.8V$

1st



V_{IL} ?

cutoff → ON

$V_{BE} > 0.5V$

$V_{BE} = 0.5V$

$I_1 = I_2$

$$\Rightarrow \frac{V_{IL} - 0.5}{15} = \frac{0.5 - (-12)}{100}$$

$\therefore V_{IL} = 2.375V$

(0 - 2.375V) → considered as logic 0 at the input side

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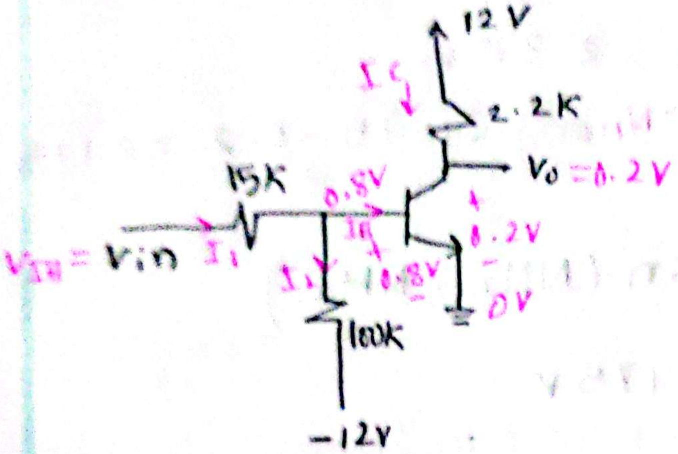
2nd

$V_{IH} = ?$

↳ Transitioned from saturation to Active mode



$\beta_{forced} < \beta_F$ [Satn]

$\beta_{forced} > \beta_F$ [Active]

$\beta_F = \beta_{Forced}$ [Transition]

$$I_C = \frac{12-0.2}{2.2} = 5.3636 \text{ mA}$$

$$\beta_{forced} = \frac{I_C}{I_B} = 30$$

$$I_B = \frac{I_C}{30} = 0.178 \text{ mA}$$

$$I_1 = I_2 + I_B$$

$$\Rightarrow \frac{V_{IH} - 0.8}{15} = \frac{0.8-(-12)}{100} + 0.178$$

$$\Rightarrow V_{IH} = 5.39V$$

5.39V − 12V → considered as logic 1 at input side

Quiz 1 : DL + RTL
Sunday

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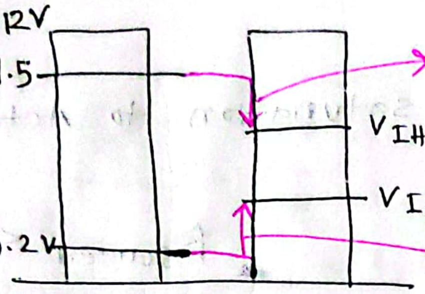


$V_{OH} = 11.5$

$0.2 \times 6.11 = 6.31V$
↓
high range

$V_{OL} = 0.2V$

$NM_H = 11.5 - 5.39 = 6.11V$

$V_{IH} = 5.39V$

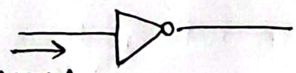
$V_{IL} = 2.375V$

$NM_L = 2.375 - 0.2 = 2.175V$

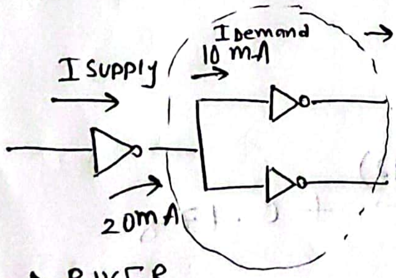
Noise Margin $= \min(NM_L, NM_H)$

$= 2.175V$

FANOUT



10mA
↓
Required current (Properly function)



Fanout → maximum no of gate can be connected to the output

I_{supply} = current supplied by DRIVER

I_{demand} = current required for the load to ...

$$\text{Fanout} = \frac{I_{supply}}{I_{demand}}$$

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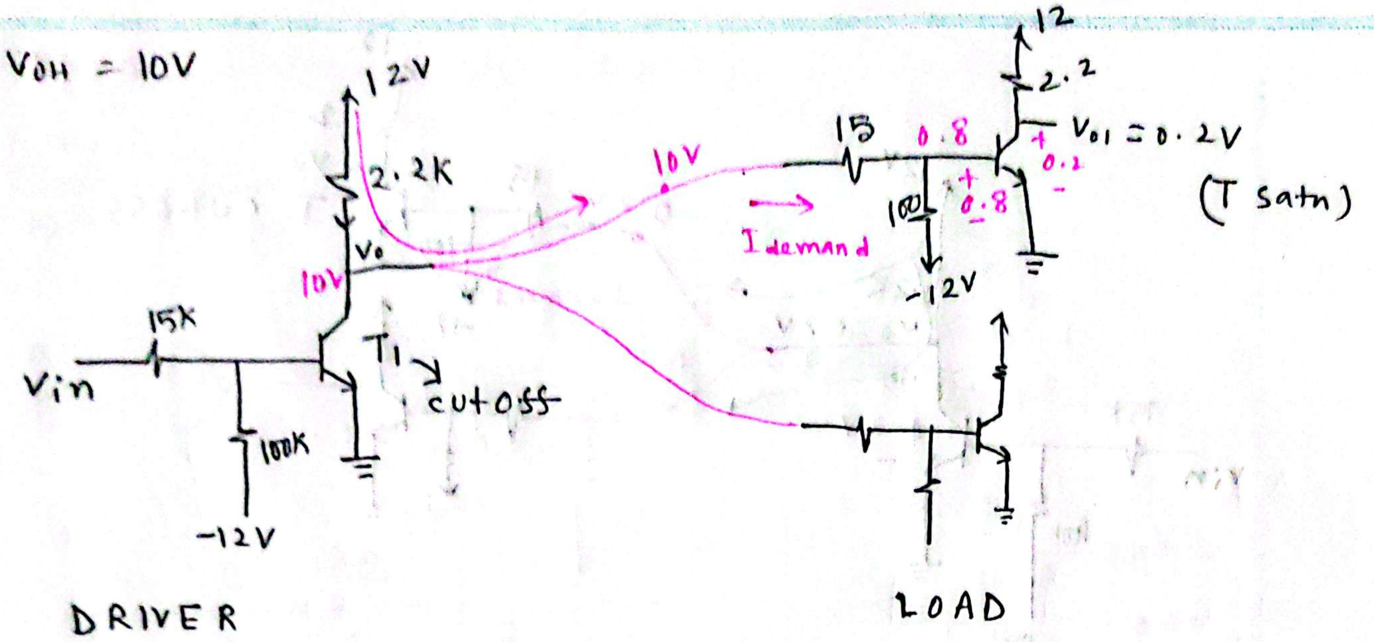
$V_{OH} = 10V$



Driver Transistor → cutoff, load circuit transistors → satn

Case 01 : Vin = Low , $V_o = 10V$
↳ cutoff

$$I_c = \frac{12-10}{2.2} = 0.91 \text{ mA} = I_{supply}$$

$$\cancel{For}\ I_{demand} = \frac{10-0.8}{15} = 0.613 \text{ mA}$$

$$\text{Fanout} = \frac{I_{supply}}{I_{demand}} = \frac{0.91}{0.613} = (1.43)\ \text{floor} = 1$$

* There would be resistor connected to input terminal and the resistor is connected to the transistor → RTL circuit

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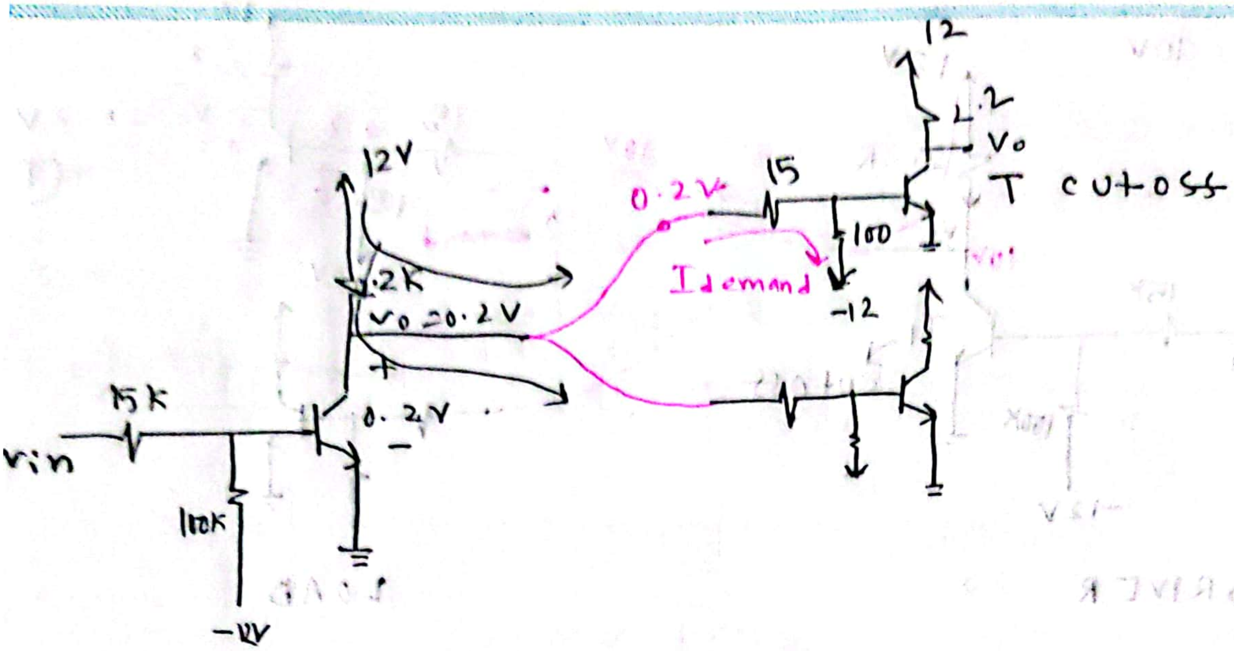

load circuit transistors → cut off

case 2

V_{in} = High , V_o = Low , V_{OL} = 0.2 V

T → saturation

$$I_c = \frac{12 - 0.2}{2.2} = 5.36 \text{ mA} = I_{supply}$$

$$I_{demand} = \frac{0.2 - (-12)}{115} = 0.1086 \text{ mA}$$

$$\text{Fanout} = \frac{I_{supply}}{I_{demand}} = 50.566 \approx 50$$

∴ Maximum Fanout = min (1, 50) = 1

power = $P_1 + 50 \times P_2$

P_1 = driver এর power dissipation

P_2 = load " " "