CSE460
Practice Sheet

CMOS Logic

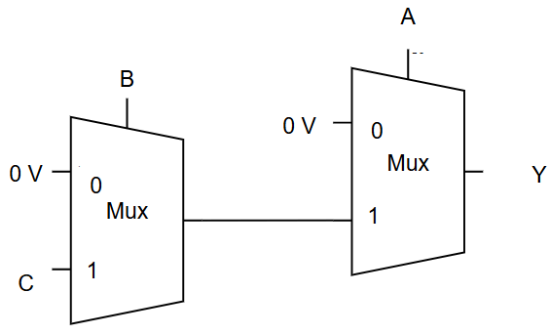
Q-1. Suppose you want to design a circuit that includes three inputs (x_1, x_2, x_3), and one output (f). Following is the truth table of the desired circuit.

x_1	x_2	x_3	f
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	d

Find the logic expression using k-map and implement the logic expression using only 2x1 mux (Don't use any logic gate; you can use more than one 2x1 mux).

Q-2. Implement an XNOR gate using a single 2x1 mux.

Q-3. Form a truth table and identify the logic expression of the given circuit.



Q-4: Compare the number of required transistors for implementing a 2x1 mux using CMOS and transmission gates. (Show both implementation diagram)

Q-5. Design a 4x1 Mux using minimum number of nmos pass transistors. You are only given the input signals s, D0, D1, D2, D3. Using the 4x1 Mux, design a 8x1 Mux(you cannot use any other Mux).

Q-6. Take a room light control system for example. The light should turn ON automatically only:

- if the main power switch is ON
- and either the wall switch is ON or a person is detected by the motion sensor

Take the inputs as following:

- **A** = Main power switch (1 = ON, 0 = OFF)
- **B** = Wall switch (1 = ON, 0 = OFF)
- **C** = Motion sensor (1 = detects movement, 0 = no movement).

(a) Find the expression for output **f** (1 = Light ON, 0 = Light OFF).
(b) Design the circuit using transmission gates.

Q-7. For the following truth table:

X1	X2	X3	X4	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	d
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	d

A) Find the expression for f using K-map.
B) Now, design the circuit using CMOS logic.

Q-8. Implement the following function using only transmission gate logic:

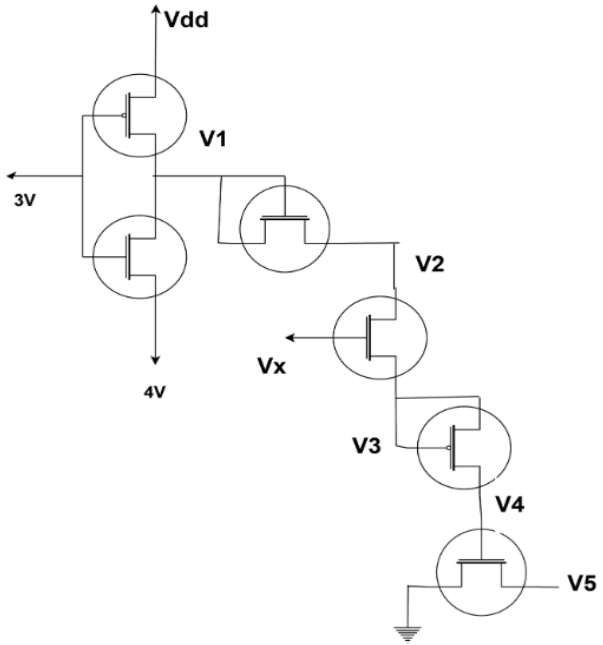
$$f = A \cdot \overline{B} \cdot C + D$$

Q-9. Write truth table of a 4 to 1 mux whose select pins are A, B and Input lines are I_0 ,I_1 , I_2 , I_3

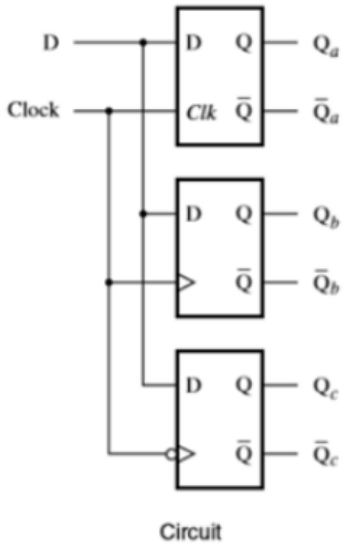
Q-10. Find the simplified output logic expression Y=F(A,B,C) using **karnaugh's map** rule

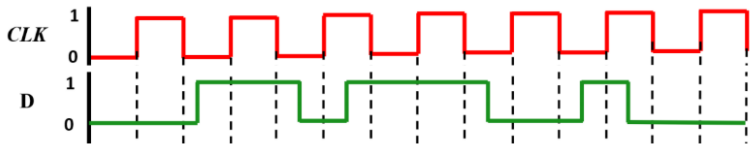
AB / C	00	01	11	10
0	1	0	0	1
1	1	1	0	1

Q-11. Find out the voltages at V1, V2, V3, V4 , V5 when VDD=4V,and Vx= 3V, Vtn= 0.5V , |Vtp|= 0.2V

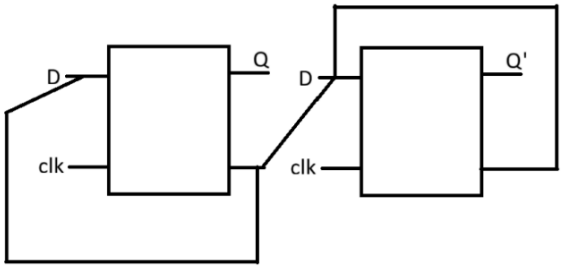


Q-12: For the following circuit, draw Qa, Qb and Qc:





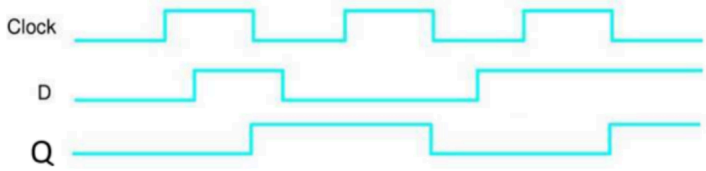
Q-13. The input (D) output(Q) relationship of the device in figure is given below



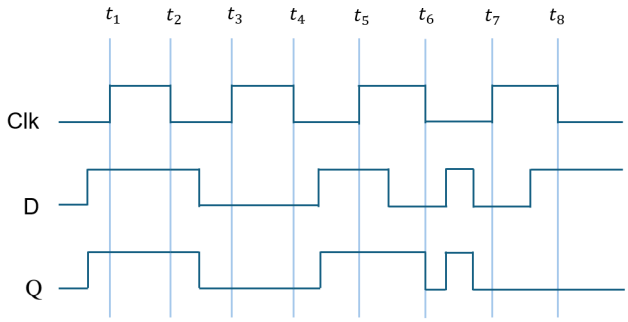
(a) Identify the block device from given waveform below

(b) Draw output Q', initially assume D on the left device to be 0

(c) What function does the circuit perform?

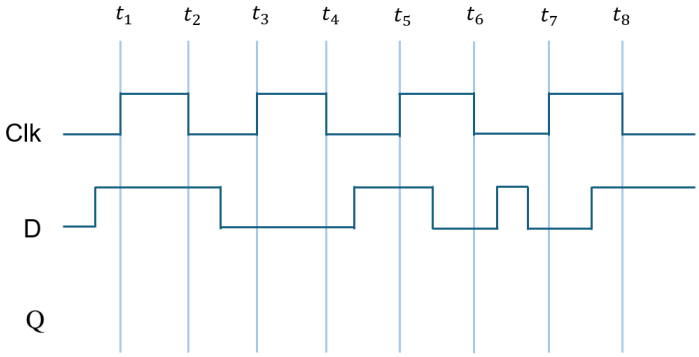


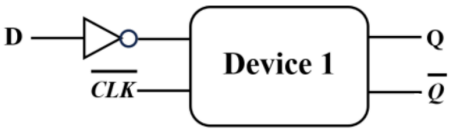
Q-14.



(a) Identify Device-1 and implement it using transmission gates.

(b) Draw the output waveform based on the following circuit:





Q-15: **Identify** Device 1 and **draw** the waveforms in the grid given above for the right circuit of Fig. 1. **Determine** if the circuit is a negative-edge/level-triggered or positive-edge/level-triggered flip-flop/latch?

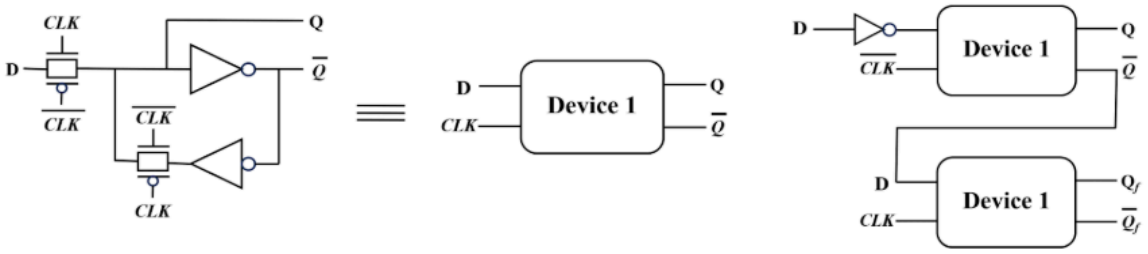
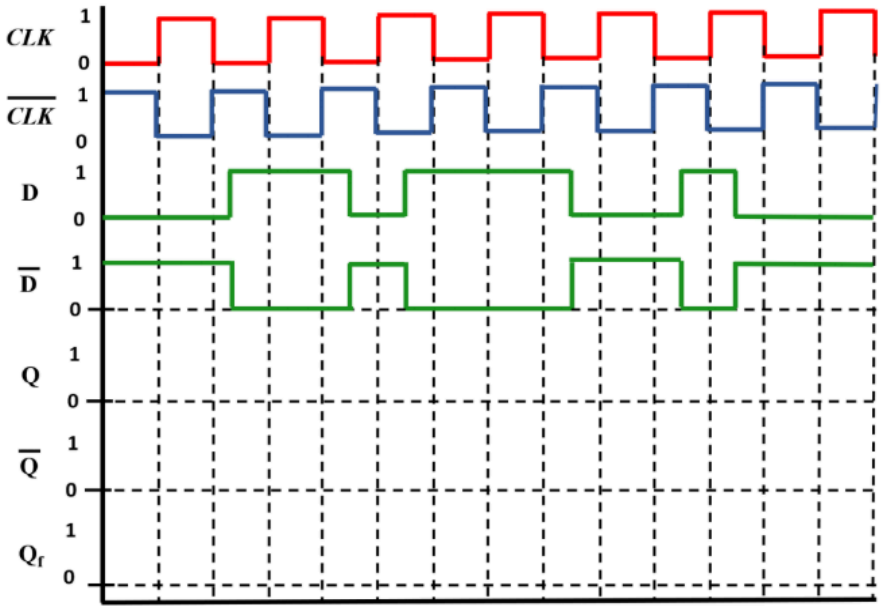


Figure 1: Circuit on the left is represented by the block **Device 1.** Circuit on the right uses this **Device 1**.



Q-16.

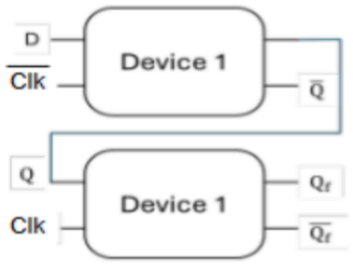


Figure: 1

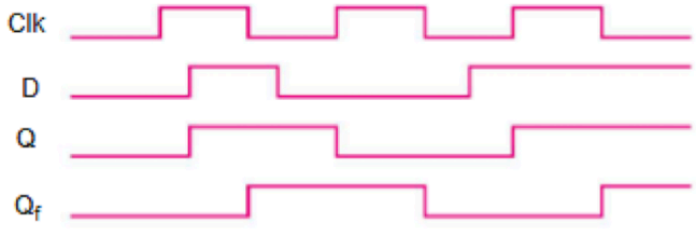


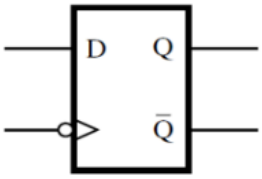
Figure: 2

Figure 2 shows the output waveshape of the device implemented in **Figure 1**.

A. **Identify** the circuit implemented in **Figure 1** from the timing diagram of **Figure 2**. Also identify **Device 1** shown in **Figure 1**.

B. **Draw** the circuit of **Device 1** using transmission gates.

Q-17.



D Flip-flop

Figure 1.1

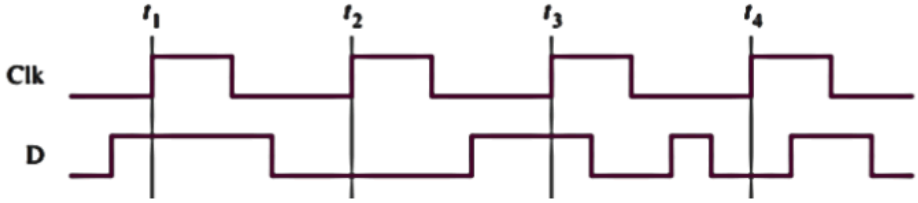


Figure 1.2

(a)	State the difference between D Latch and D Flip-Flop. Implement the D Flip-Flop (Given in the above Figure) using D Latch.
(b)	Draw the output of the D Flip-Flop when Clk and D of Figure 1.2 are applied to the D Flip-Flop.

Finite State Machine (FSM)

Q-1.

Design a finite state machine (FSM) for a car alarm system. The system has two binary inputs: y, indicating the lock status of the car door (**y = 1 if unlocked, y = 0 if locked**) and x, indicating the door status (**x = 1 if the door is open, x = 0 if closed**). The output z is used to control the alarm: z = 1 when the alarm is active, and z = 0 otherwise. The alarm should be triggered (z = 1) if the door is opened (x = 1) while it is still locked (y = 0) **for two consecutive clock cycles**. An example is shown below:

y	1	0	1	0	0	0	1	1	0	0	0	0	1	0
x	0	0	1	1	1	0	1	0	1	1	1	0	0	1
z	0	0	0	0	**1**	0	0	0	0	**1**	**1**	0	0	0

(a)	**Determine** the type of **FSM** that would be needed for the given problem and **design** the state diagram for the corresponding FSM.	[2]
(b)	**Derive** the state-assigned table using the **Binary encoding** from your state diagram in (a).	[2]
(c)	**Find** the expression for the **next state** and the **output** for the FSM using **KMAP.**	[3]
(d)	**Calculate** the number of flip-flops required for the circuit implementation and **draw** the circuit for this FSM.	[3]

Q-2: Design an FSM (mealy) that detects either ’10’ or ’1011’. Provide

- State diagram
- State Assigned table
- The final circuit using logic gates and FF

Q-3: A system has one input, A, and two outputs, X and Y.

The output X should be **1** if the input A has been **0** for **three consecutive cycles**.

The output Y should be **1** if the input sequence **010** occurs consecutively. For example,

A	1	0	0	0	0	1	0	0	1	0	1	0	0	0
X	0	0	0	0	1	1	0	0	0	0	0	0	0	0
Y	0	0	0	0	0	0	0	1	0	0	1	0	1	0

(a) Draw the state diagram for the corresponding FSM.

(b) Derive the state-assigned table from the state diagram.

(c) Find the expression for the next state and the output for the FSM using KMAP.

Q-4: A sequential circuit has two inputs, w1 and w2, and an output, z. Its function is to compare the input sequences on the two inputs. If w1 = w2 during any four consecutive clock cycles, the circuit produces z = 1; otherwise, z = 0. For example

w1	0	1	1	0	1	1	1	0	0	0	1	1	0	1
w2	1	1	1	0	1	0	1	0	0	0	1	1	1	0
z	0	0	0	0	1	0	0	0	0	1	1	1	0	0

Draw the **state diagram** of the corresponding FSM.

Q-5:

Suppose you want to design an FSM that will detect sequences of alphabet. There will be four different types of possible input alphabets (A, B, C, D). When the sequence of the alphabets is **AACC**, the output of the FSM will be high (1), otherwise it will remain low (0).

Input (w)	A	B	A	A	C	C	A	C
Output (z)	0	0	0	0	0	1	0	0

(a)	**Identify** the type of FSM and **draw** the state diagram of the FSM.	[6]
(b)	Make a **state assigned table** using the gray encoding.	[5]
(c)	**Find** the expression of the output (z) using the state assigned table from (b).	[4]