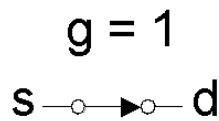
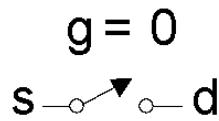
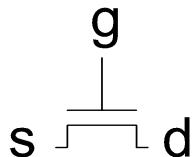


Signal Strength

- *Strength* of signal
 - How close it approximates ideal voltage source
- V_{DD} and GND rails are strongest 1 and 0
- nMOS pass strong 0
 - But degraded or weak 1
- pMOS pass strong 1
 - But degraded or weak 0
- Thus **nMOS are best for pull-down network**
- And, **pMOS are best for pull-up network**

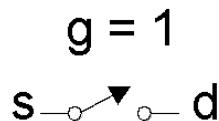
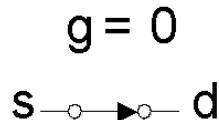
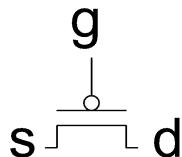
Pass Transistors

- Transistors can be used as switches



Input $g = 1$ Output
0 → strong 0

$g = 1$
1 → degraded 1

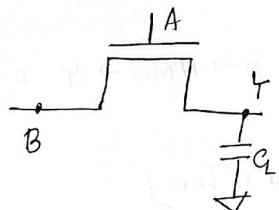


Input $g = 0$ Output
0 → degraded 0

$g = 0$
1 → strong 1

Pass transistor

N-MOS pass transistor:



not exactly AND
due to Z

A	B	Y = A · B
0	0	0
0	1	0
1	0	0 → good '0'
1	1	1 → Bad '1'

For NMOS → Source is at lower potential
Drain is at higher potential

reason = ??

Source to Drain
 e^- is sent by
repulsion of Source end
hence Source is at (+ve) potential.

Case 1: $A = 1, B = 0$:

here, B = lower potential than Y hence its ~~not~~ source now.

C_L discharges through MOS to GND at B point.

for NMOS, $V_{gs} > V_{th}$ to be ON. Hence, C_L ie Y

Node can be fully discharged in this case \rightarrow Good 0.
always $V_{gs} = 5 - 0 = 5V > V_{th}$

Case 2: $A = 1, B = 1$:

Now, B is at (+5V) ie highest potential hence its now the drain end. Y is the source now.

C_L starts getting charged from $B \rightarrow$ NMOS \rightarrow Y node.

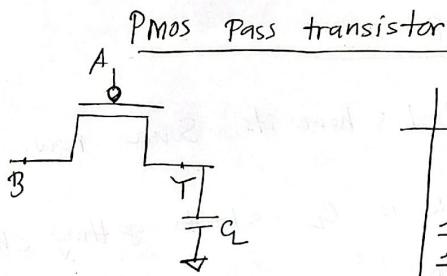
But, as $V_{gs} > V_{th}$ [let $V_{th} = 1V$ here]

$$\Rightarrow V_g - V_s > 1 \Rightarrow V_s < (5 - 1)$$

$$\Rightarrow V_s < 4V$$

Hence, the source ie Y node can rise upto 4V only in ON state so, 4V instead of 5V

Bad 1



not exactly AND due to 2 state

A	B	Y = $\bar{A} \cdot B$
0	0	0 → GND
0	1	1 → Drain
1	0	2
1	1	2

PMOS ON condition: $V_{sg} > |V_{tp}|$

Also, for PMOS \rightarrow source is at Higher potential to repel holes from S \rightarrow D end

\rightarrow Drain is at lower potential

case 1 : A = 0, B = 0:

here, B = Drain end hence if C_L is already charged beforehand it starts discharging to GND at B node. As for PMOS \rightarrow

$$V_{sg} > |V_{tp}| \quad [k_t, |V_{tp}| = 1V]$$

$$\Rightarrow V_s > (1 - 0) V$$

Hence, the Y node is source node will stop discharging when its slightly higher than 1V.



Bad 0 hence

case 2 : A = 0, B = 1:

Now, B = High potential \Rightarrow hence its Source now.

As A=0, the Y node ie C_L starts getting charged due to (+5V) at B node.

Y node = Drain now

$V_{sg} > |V_{tp}| \rightarrow$ always maintained no matter whatever voltage appears at Y node. but always now $V_{sg} = (5 - 0)$

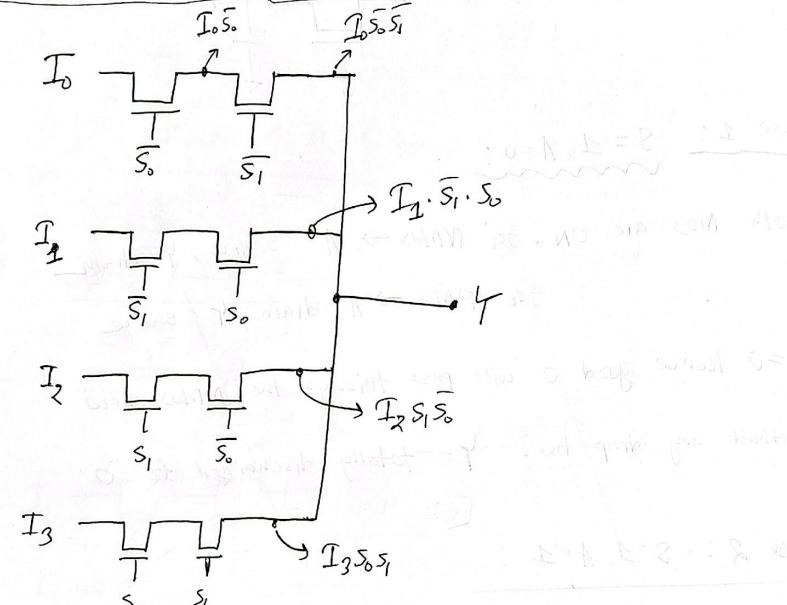


Hence Y node capacitance can fully get charged to +5V so good 1 ensured

4 to 1 Mux using NMOS Pass T

$$Y = \bar{S}_0 \bar{S}_1 D_0 + S_0 \bar{S}_1 D_1 + \bar{S}_0 S_1 D_2 + S_0 S_1 D_3$$

 basic expression

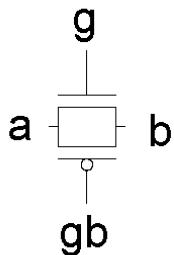


→ NMOS needed = 8

Also, passes 1 poorly as seen earlier [V_{th} drop]

Transmission Gates

- Pass transistors produce **degraded** outputs
- *Transmission gates* pass both 0 and 1 well



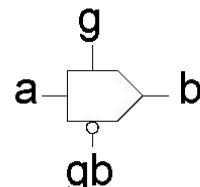
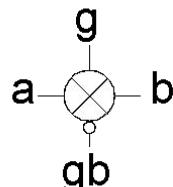
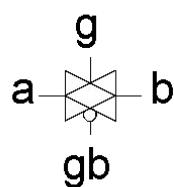
$g = 0, gb = 1$
a → b

$g = 1, gb = 0$
a → b

Input Output

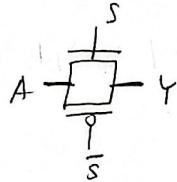
$g = 1, gb = 0$
0 → strong 0

$g = 1, gb = 0$
1 → strong 1

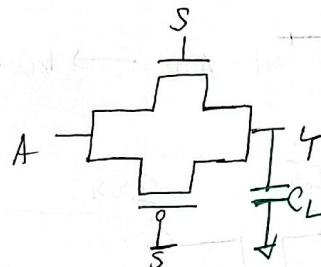


Transmission Gate (TG)

Symbol →



Internal components →



Case 1: $S = 1, A = 0$:

Both MOS are ON. For NMOS $\rightarrow A = \text{Source}, Y = \text{drain}$

for PMOS $\rightarrow A = \text{drain}, Y = \text{source}$

$A = 0$ hence good 0 will pass through the NMOS now

Without any drop loss, $Y = \text{totally discharged to '0'}$

case 2: $S = 1, A = 1$:

Both MOS = ON \rightarrow for NMOS $\rightarrow A = \text{drain}, Y = \text{source}$

for PMOS $\rightarrow A = \text{Source}, Y = \text{drain}$

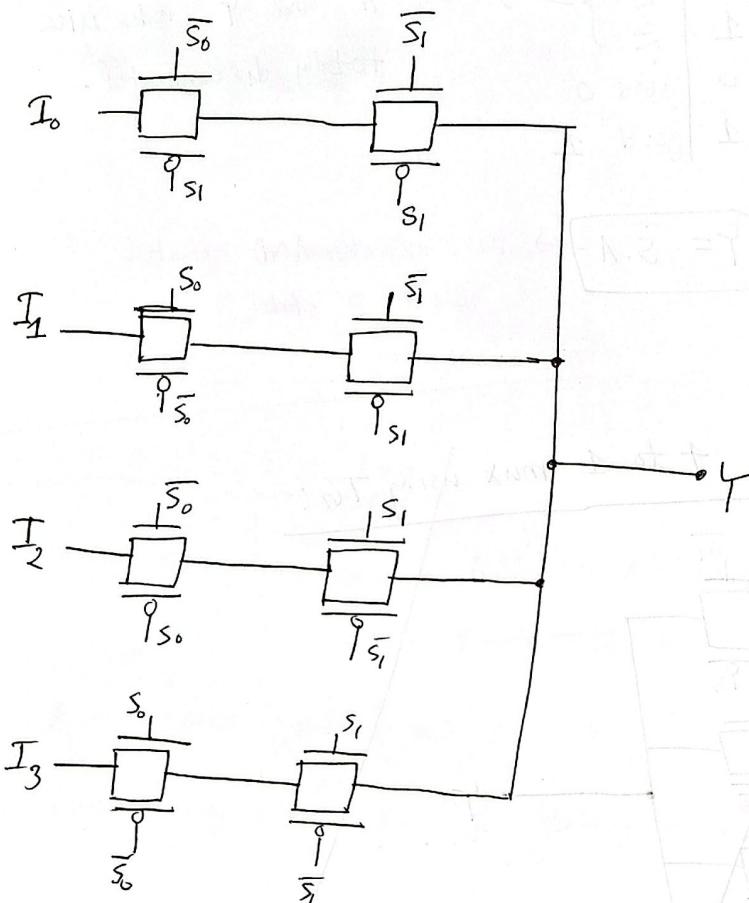
To pass 1 from A to Y, PMOS will participate and charges C_L to (+5V) exactly.

S	A	Y
0	0	Z
0	1	Z
1	0	good 0
1	1	good 1

Coz A and Y nodes are totally disconnected.

\hookrightarrow SOP $\Rightarrow Y = S \cdot A$ → not exactly AND operation due to Z state

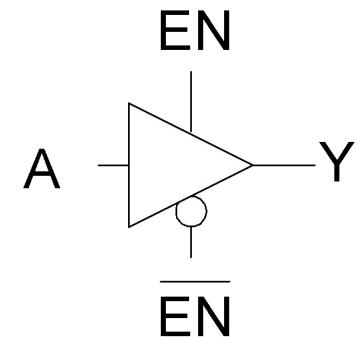
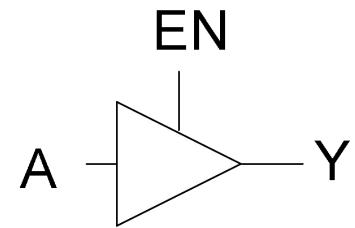
4 to 1 mux using TG



Tristates

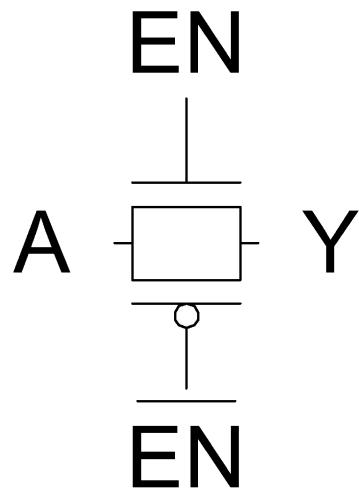
- *Tristate buffer* produces Z when not enabled

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1



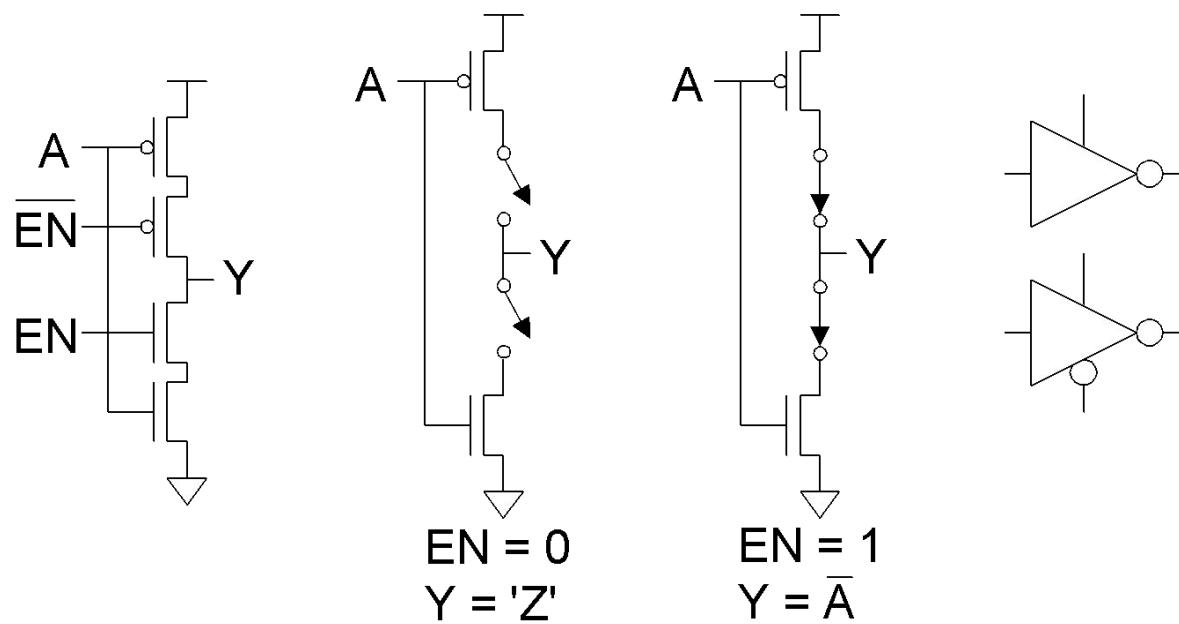
Nonrestoring Tristate

- Transmission gate acts as tristate buffer
 - Only two transistors
 - But *nonrestoring*
 - Noise on A is passed on to Y



Tristate Inverter

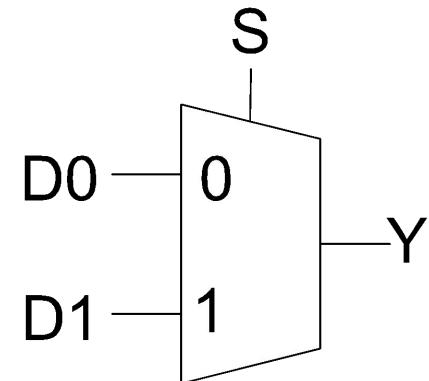
- Tristate inverter produces restored output
 - Violates conduction complement rule
 - Because we want a Z output



Multiplexers

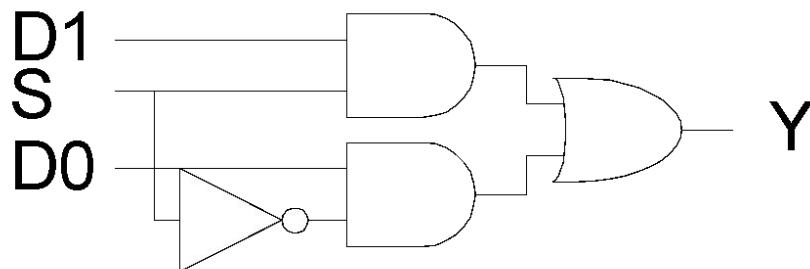
- 2:1 multiplexer chooses between two inputs

S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

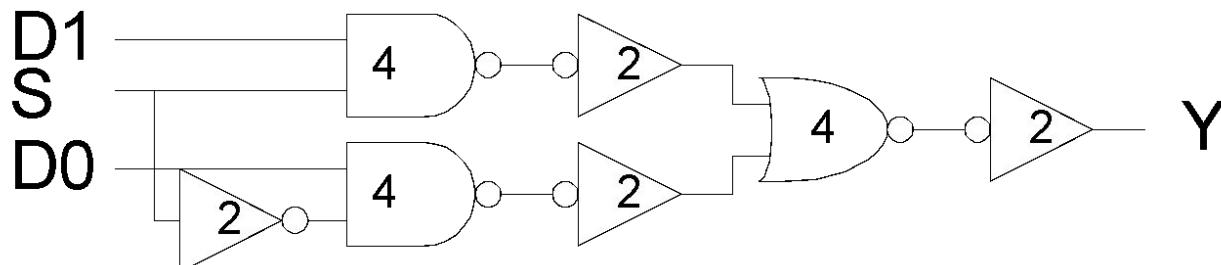


Gate-Level Mux Design

- $Y = SD_1 + \bar{S}D_0$ (too many transistors)
- How many transistors are needed? = **20** (2 for S_{bar} , 6*2 for AND, finally 6 for OR)

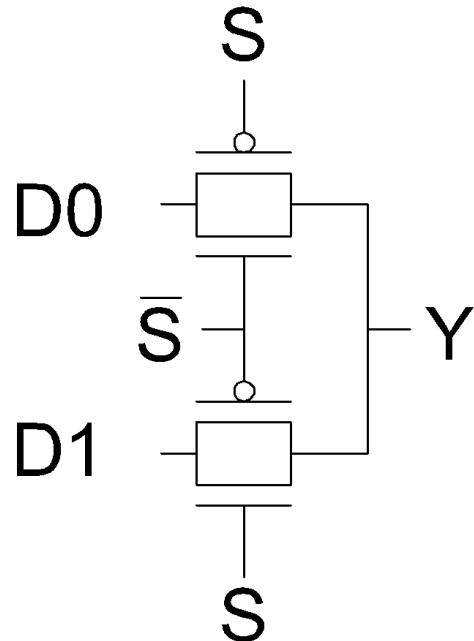


these are transistor count

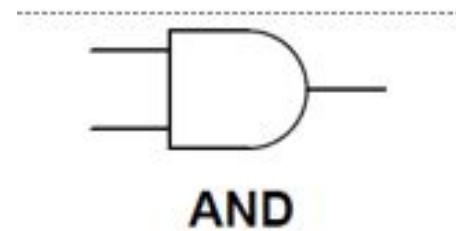
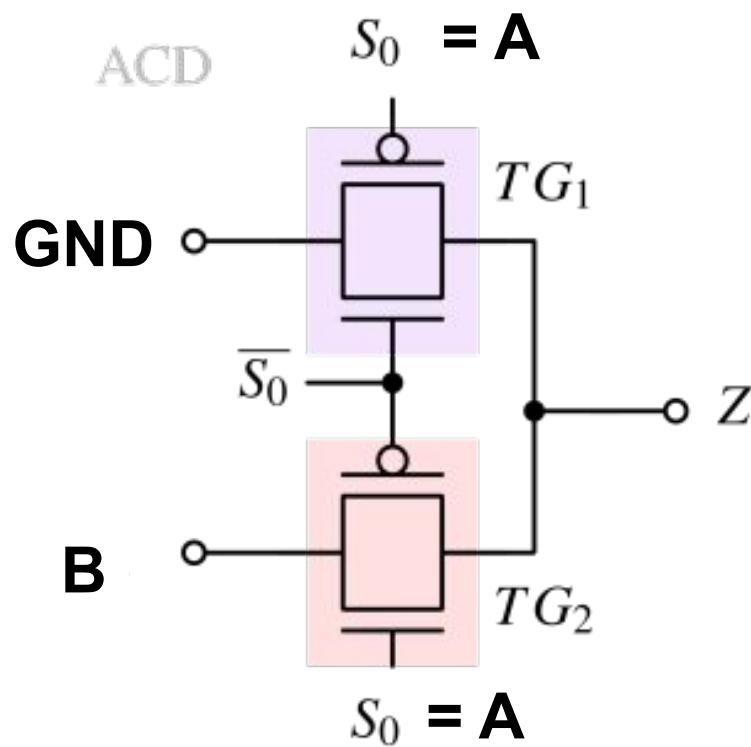


Transmission Gate Mux

- Nonrestoring mux uses two transmission gates
 - Only 4 transistors << 20 in prev slide

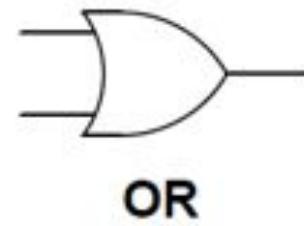
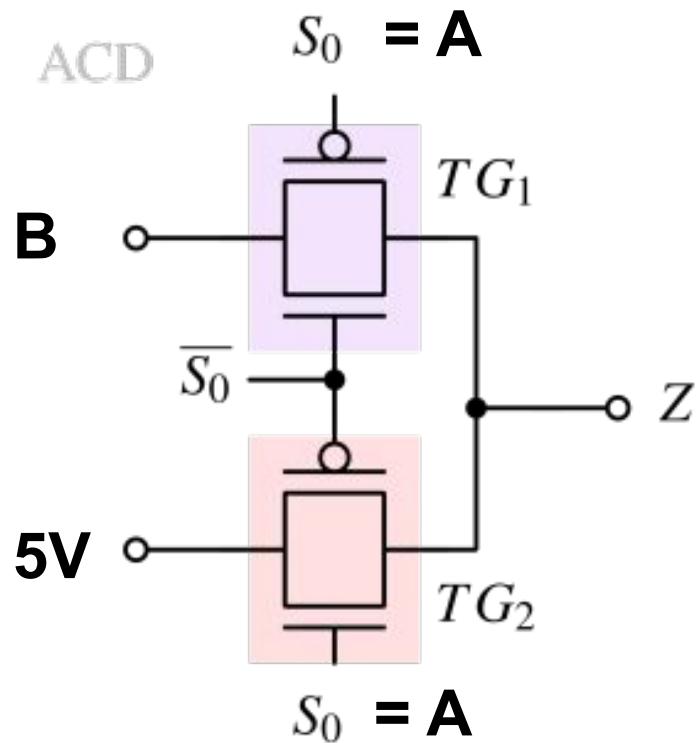


Logic Gate using TG



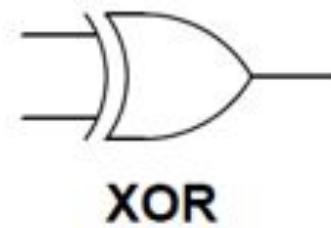
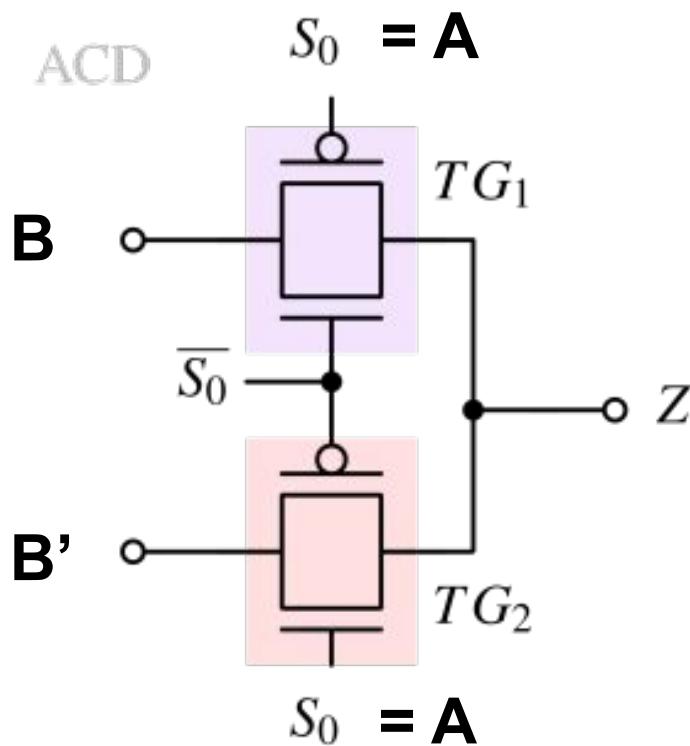
A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Logic Gate using TG



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

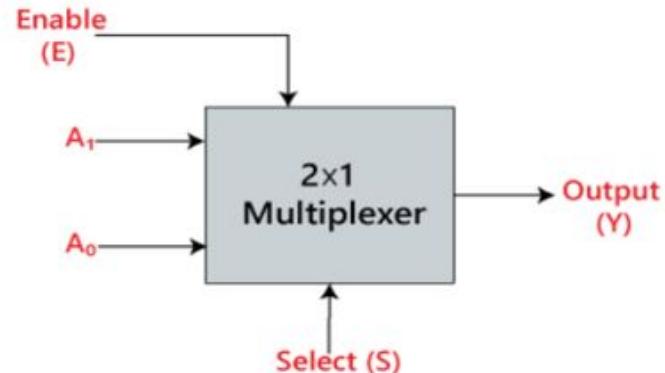
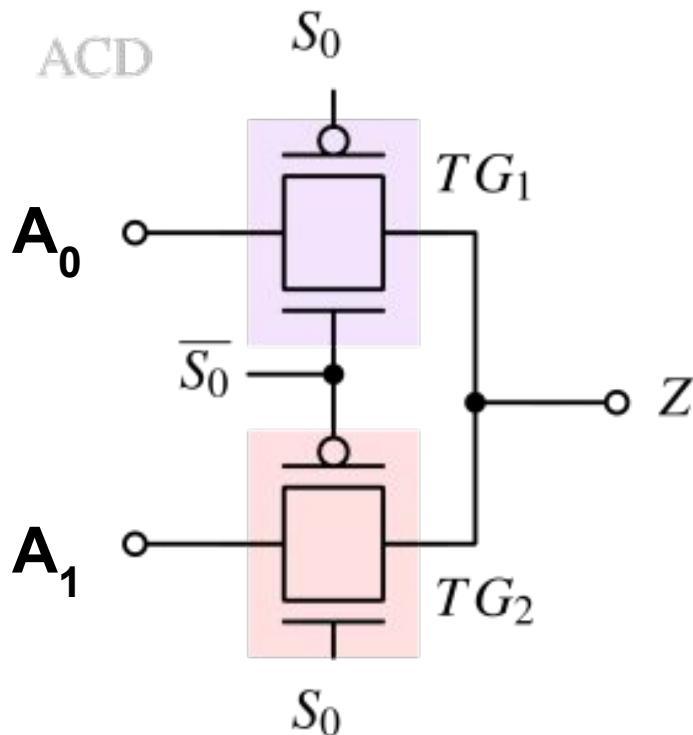
Logic Gate using TG



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

2:1 MUX using TG

Block Diagram:



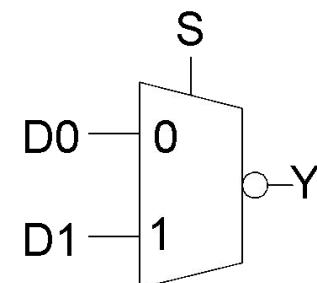
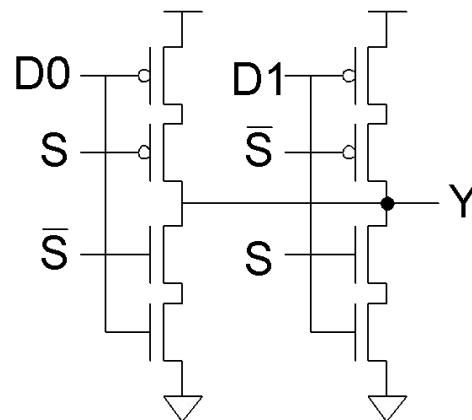
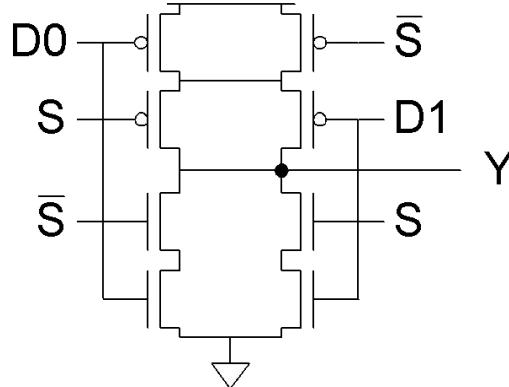
INPUTS	Output
S_0	Y
0	A_0
1	A_1

The logical expression of the term Y is as follows:

$$Y = S_0' \cdot A_0 + S_0 \cdot A_1$$

Inverting Mux

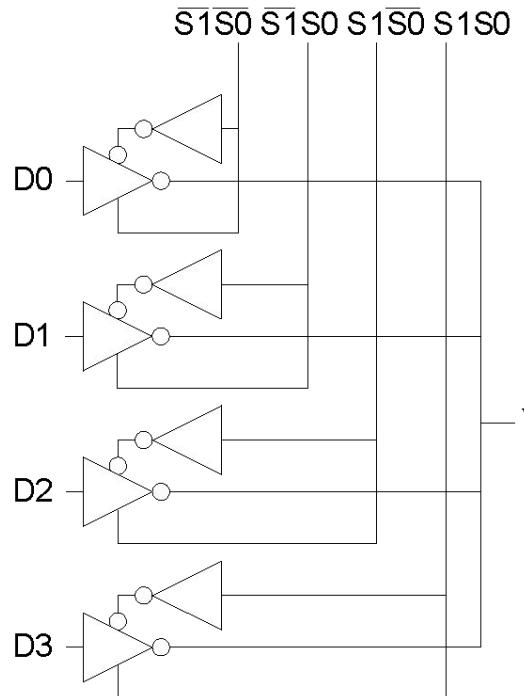
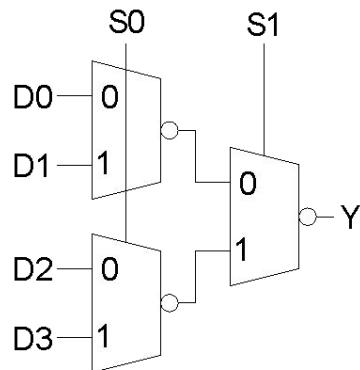
- Inverting multiplexer
 - Use compound AOI22
 - Or pair of tristate inverters
 - Essentially the same thing
- Noninverting multiplexer adds an inverter



4:1 Multiplexer

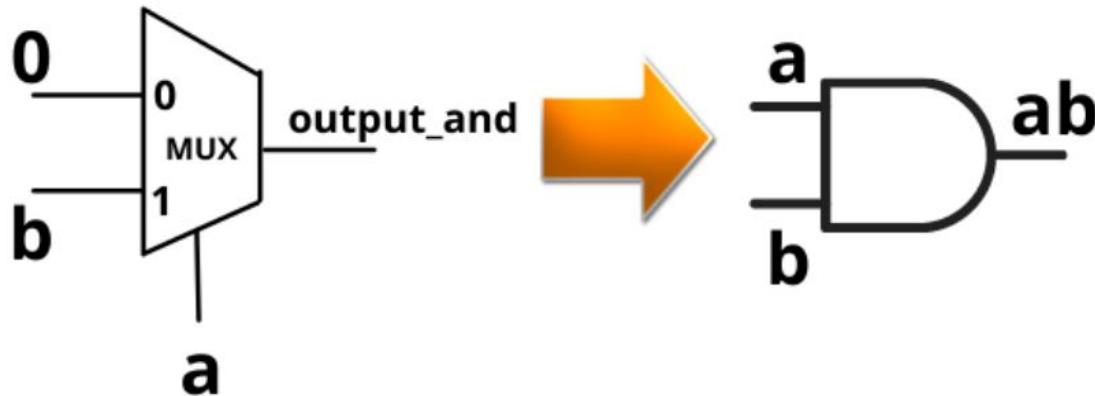
4:1 Multiplexer

- 4:1 mux chooses one of 4 inputs using two selects
 - Two levels of 2:1 muxes
 - Or four tristates

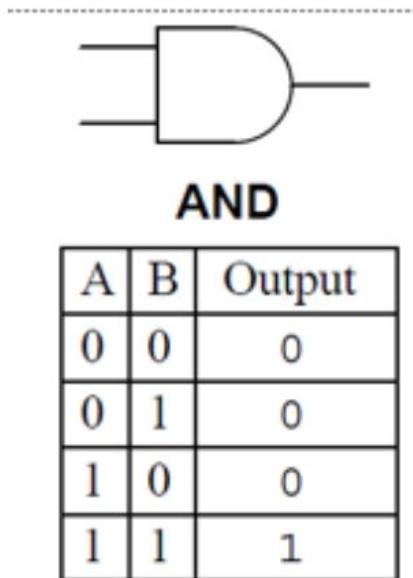


Logic Gates using Multiplexer

And Gate Using 2:1 MUX



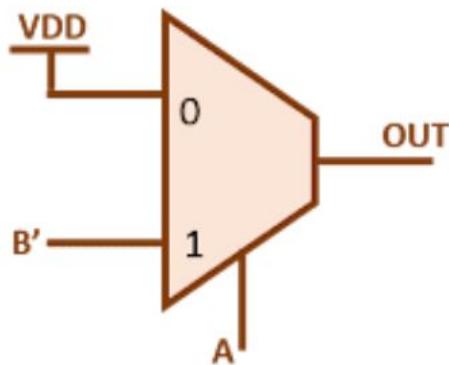
$$\begin{aligned} B &\rightarrow I_1 \\ A &\rightarrow S \\ I_0 &\rightarrow 0 \text{ V} \end{aligned}$$



Logic Gates using Multiplexer

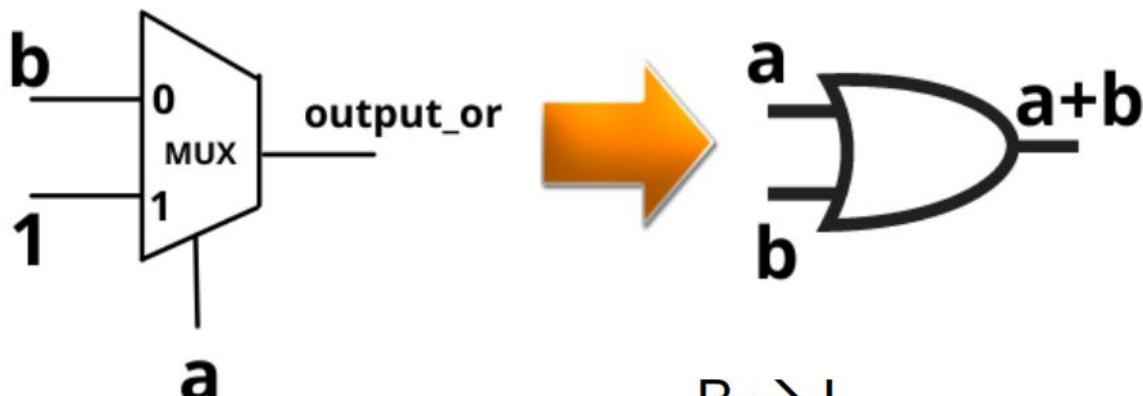
NAND Gate using MUX

A	B	OUT	
0	0	1	OUT = 1 when A = 0
0	1	1	
1	0	1	
1	1	0	OUT = B' when A = 1

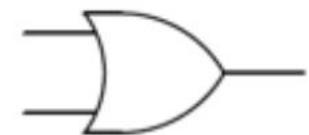


Logic Gates using Multiplexer

OR Gate Using 2:1 MUX



$$\begin{aligned} B &\rightarrow I_0 \\ A &\rightarrow S \\ I_1 &\rightarrow 5V \end{aligned}$$



OR

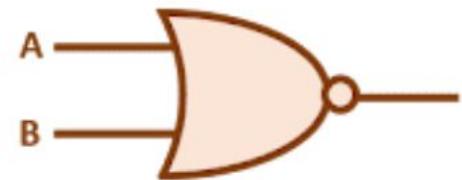
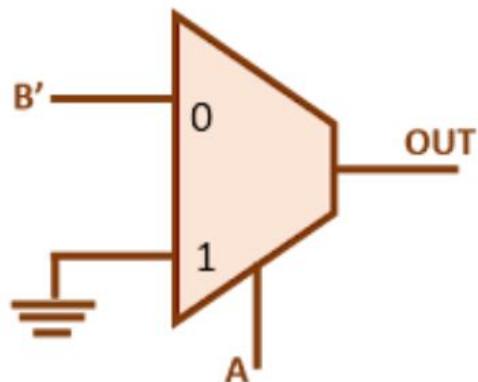
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

Logic Gates using Multiplexer

NOR Gate using MUX

A	B	OUT	
0	0	1	
0	1	0	
1	0	0	
1	1	0	

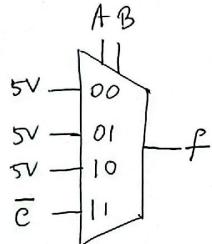
OUT = B' when A = 0
OUT = 0 when A = 1



NAND-3 gate implementation using one mux only

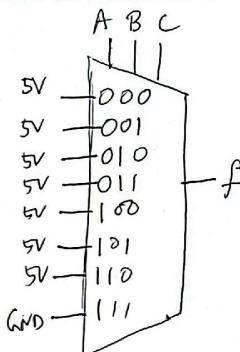
Way 1: Using a 4:1 mux:

hint: take MUXs as
select pins

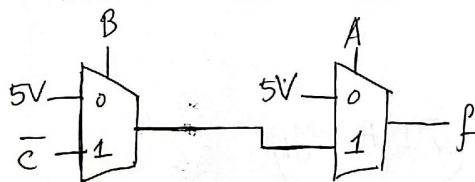


A	B	C	f
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Way 2: Using one 8:1 mux:



using two 1:2:1 muxs only:



Difference between combinational and sequential circuits

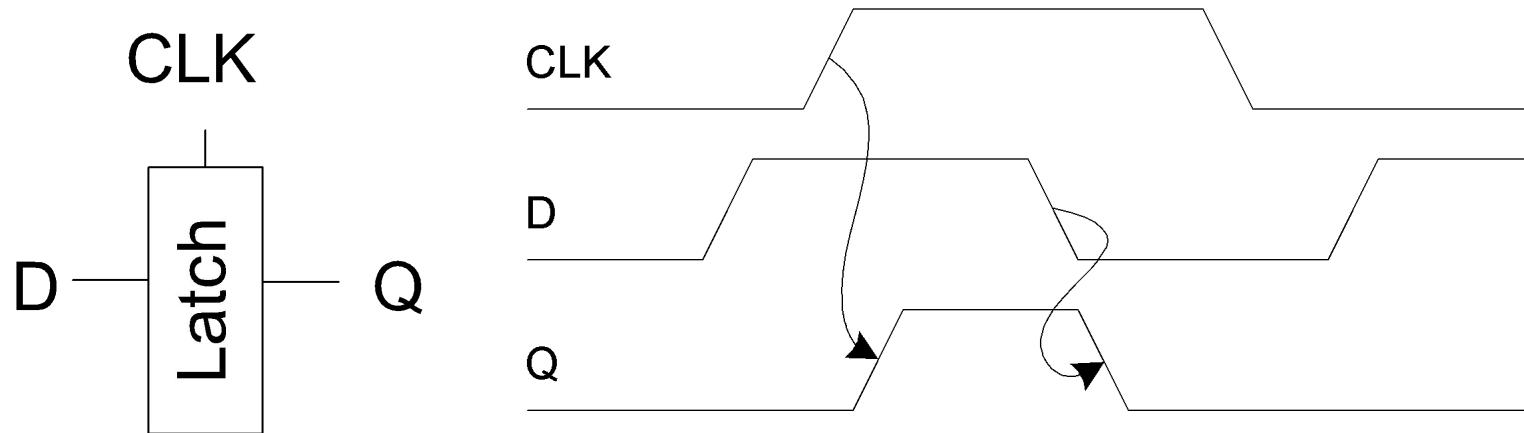
Combinational Circuit	Sequential Circuit
This output is solely dependent on the current input.	This output is affected by both current and previous input.
The process is quick.	The process is slow.
It is intended to be simple.	When compared to combinational circuits, it is more efficiently designed.
There is no feedback from input to output.	A feedback path exists between input and output.
This is not dependent on time.	This is time-sensitive.
Basic building blocks: Logical gates	Basic building blocks: Flip-flops
Used for both arithmetic and boolean operations.	Mostly used for data storage.
Combinational circuits are incapable of storing any state.	Sequential circuits can store any state or retain previous states.
Combinational circuits do not require triggering because they lack a clock.	Sequential circuits require triggering because they are clock dependent.
These circuits lack a memory element.	Memory elements are used in these circuits.
It is simple to use and manage.	It is difficult to use and handle.

Combinational circuits are built with logic gates such as AND, OR, NOT, NAND, and NOR. These logic gates serve as the foundation for combinational circuits.

Sequential circuits are built with counters, shift registers, latches, etc.

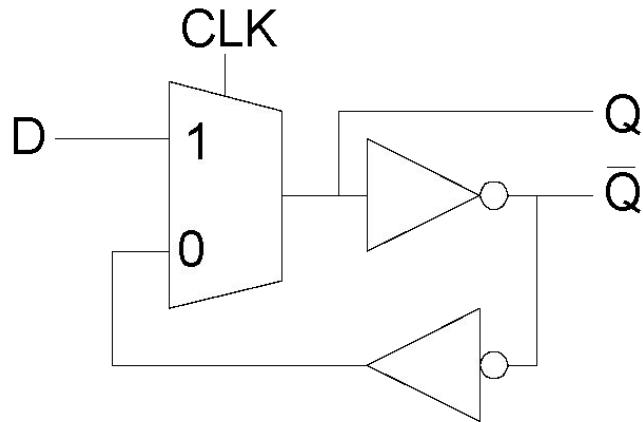
D Latch

- When $\text{CLK} = 1$, latch is *transparent*
 - D flows through to Q like a buffer
- When $\text{CLK} = 0$, the latch is *opaque*
 - Q holds its old value independent of D
- a.k.a. *transparent latch* or *level-sensitive latch*



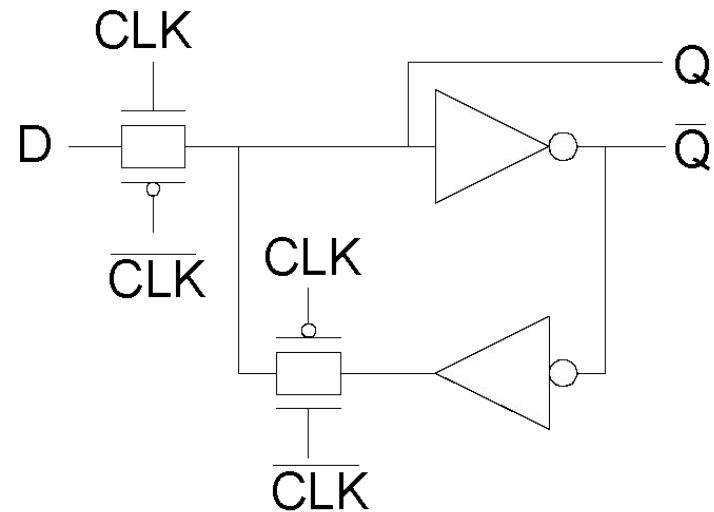
D Latch Design using MUX

- Multiplexer chooses D or old Q

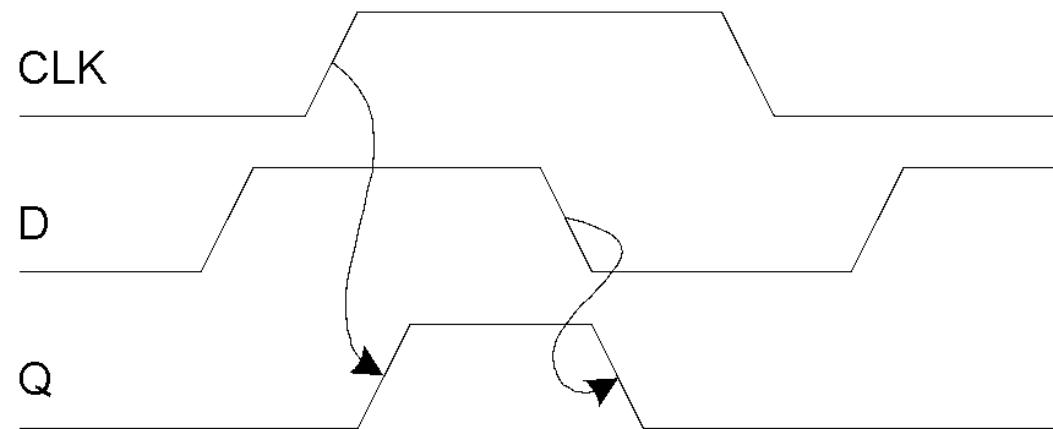
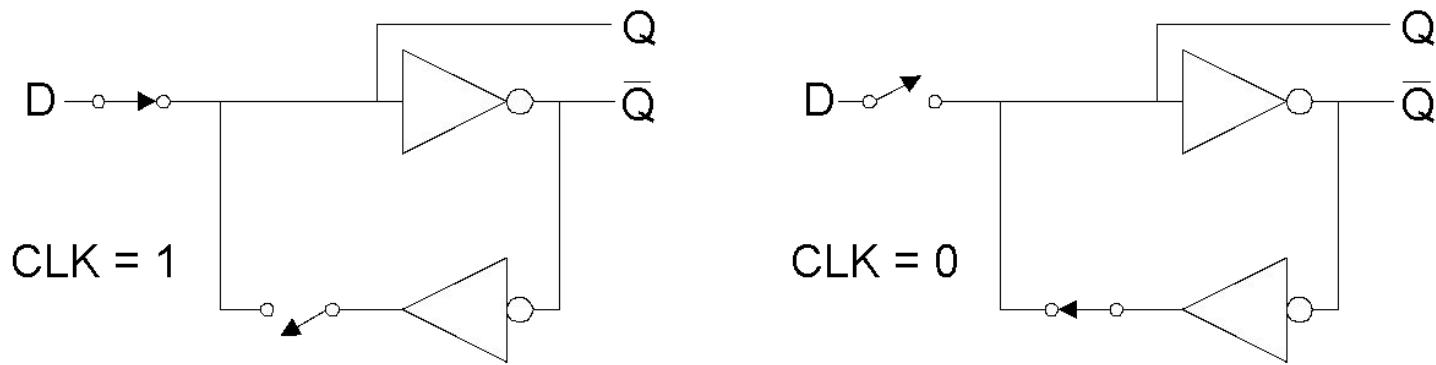


+ve D Latch Design using Transmission gate

It's a Positive level triggered D-Latch



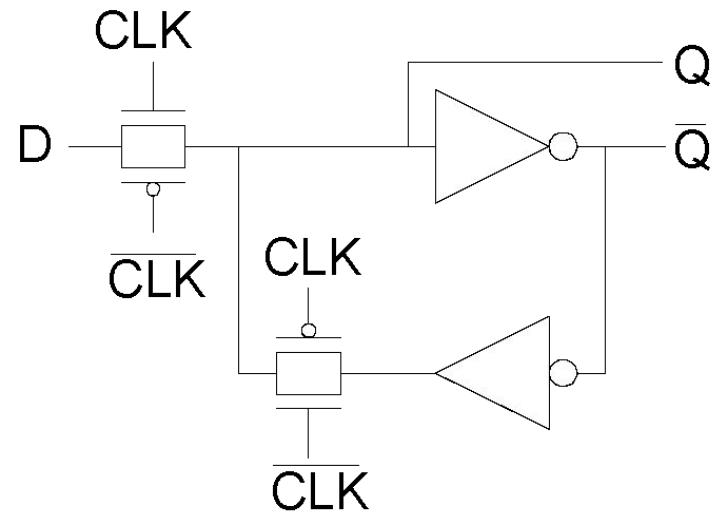
+ve D Latch Operation



-ve D Latch Design using Transmission gate

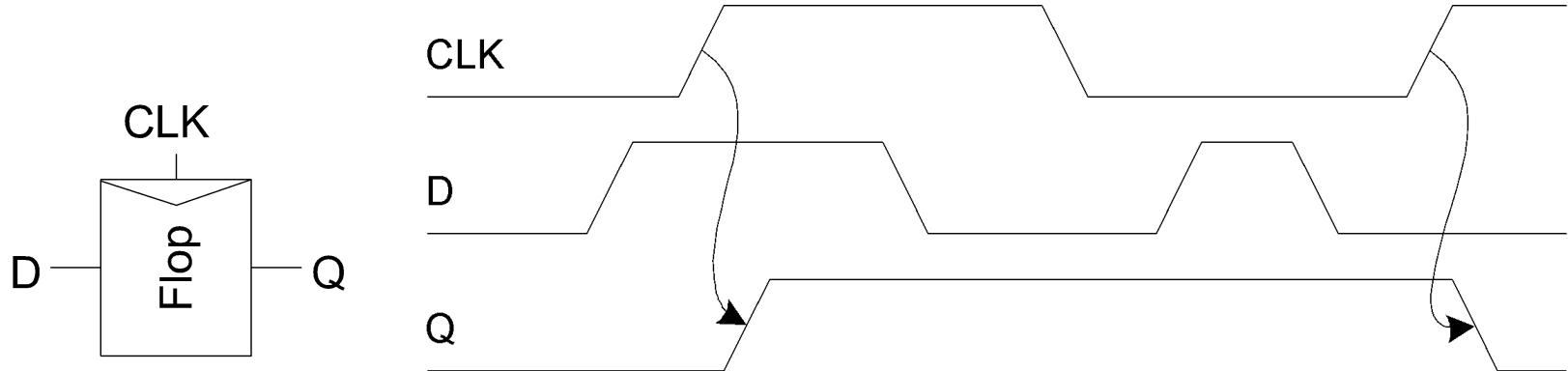
It's a Negative level triggered D-Latch.

Replaced CLK with CLK_bar.



D Flip-flop

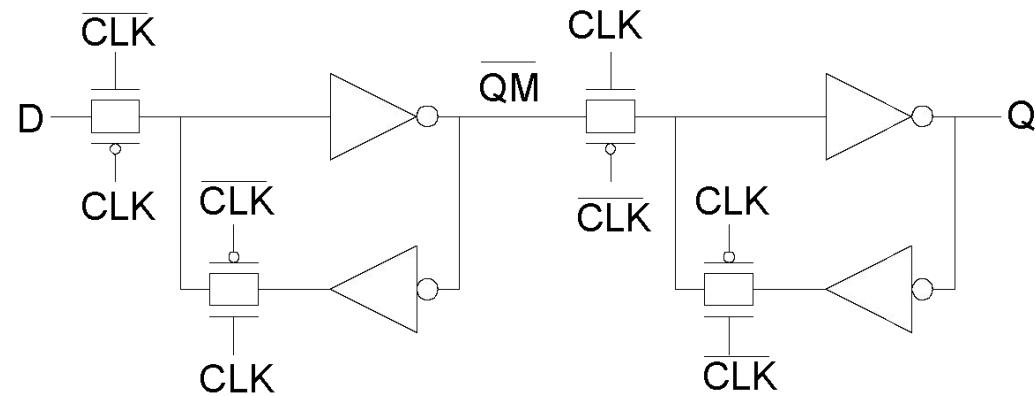
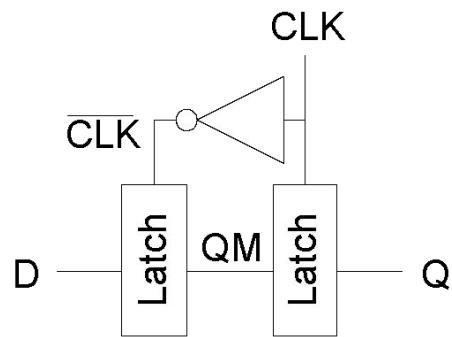
- When CLK rises, D is copied to Q
- At all other times, Q holds its value
- a.k.a. *positive edge-triggered flip-flop, master-slave flip-flop*



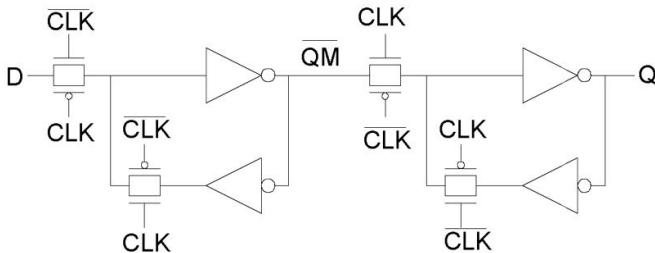
+ve edge triggered D Flip-flop Design

by cascading -ve Latch with +ve Latch in series

- Built from master and slave D latches



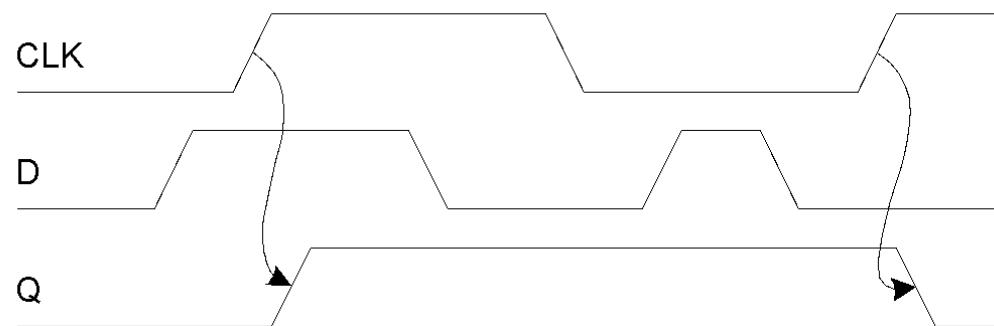
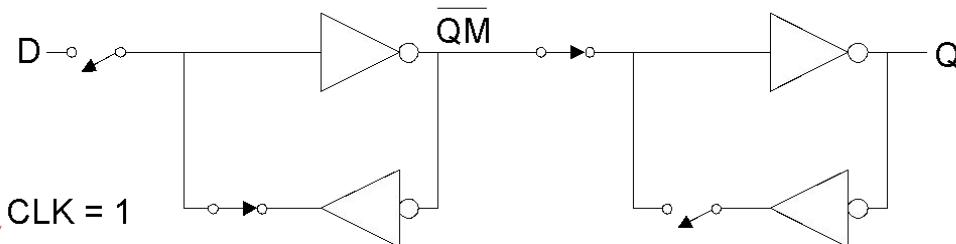
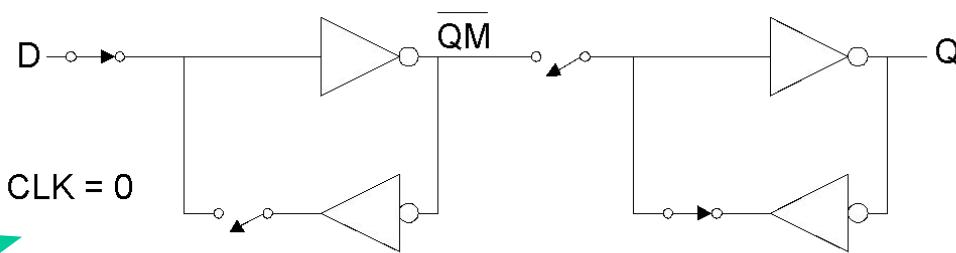
D Flip-flop Operation



When $\text{CLK}=0$: Q retains its old value and $\overline{\text{QM}} = \overline{\text{D}}$ is being continuously set unless $\text{CLK}=1$

When $\text{CLK}=1$: D gets disconnected from $\overline{\text{QM}}$ hence $\overline{\text{QM}} = \overline{\text{D}}$ is sent directly to Inveter to Q point.

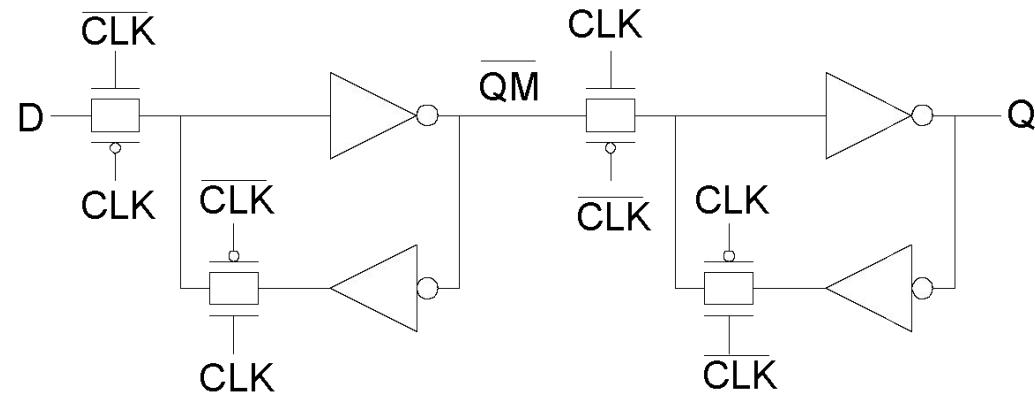
Also, after $\text{CLK}=1$ is set, Q can't follow D anymore as D is isolated from $\overline{\text{QM}}$.



-ve edge triggered D Flip-flop Design

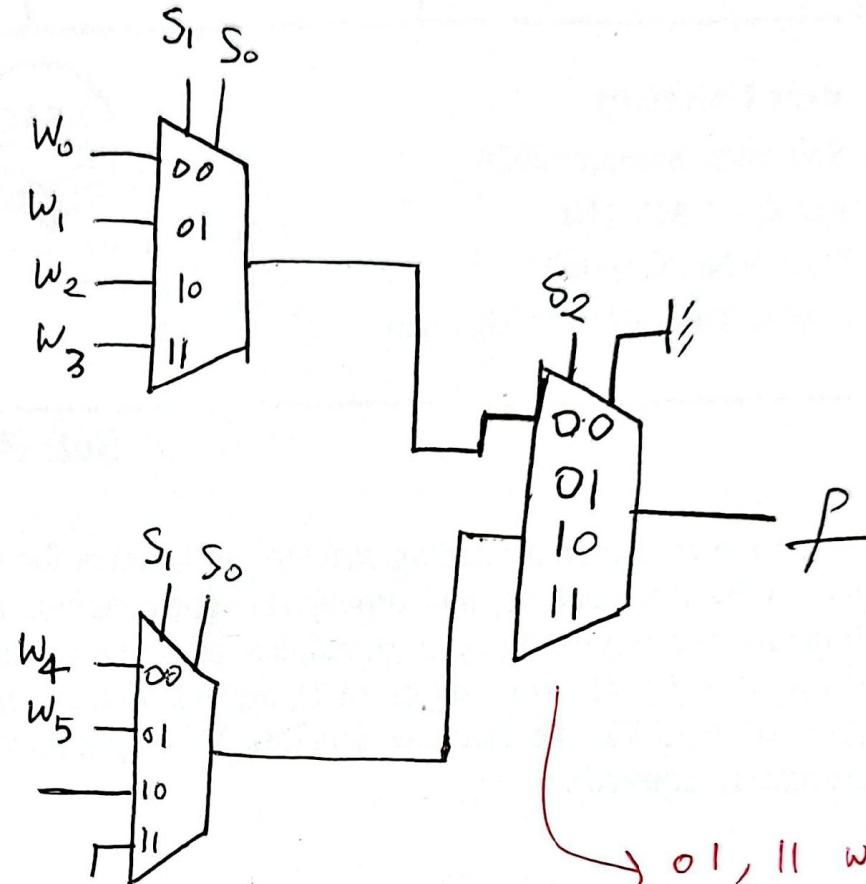
by cascading +ve Latch with -ve Latch in series

- Built from master and slave D latches



Design 6:1 mux using 4:1 mux

S_2	S_1	S_0	f
0	0	0	w_0
0	0	1	w_1
0	1	0	w_2
0	1	1	w_3
1	0	0	w_4
1	0	1	w_5



keep 10,11 disconnected

→ 01, 11 will never
be selected due to
GND connection at
LSB select pin

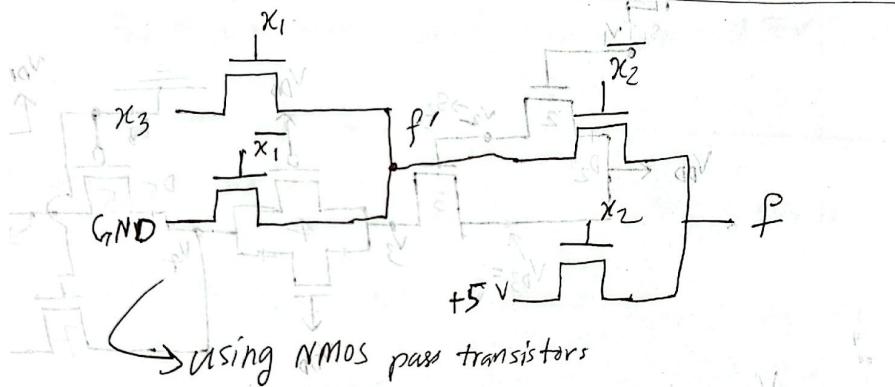
Implement boolean expression using Pass Transistor and Transmission gate

$$f = x_2 + x_1 x_3 \rightarrow \begin{array}{l} \text{implement using pass T} \\ \text{and } T^H \end{array}$$

x_1	x_3	f_1	
0	0	0	
0	1	0	
1	0	0	
1	1	1	

$\left. \begin{array}{l} \\ \\ \\ \end{array} \right\}$ always GND
 $\left. \begin{array}{l} \\ \\ \\ \end{array} \right\}$ $x_3 \rightarrow \text{copy}$

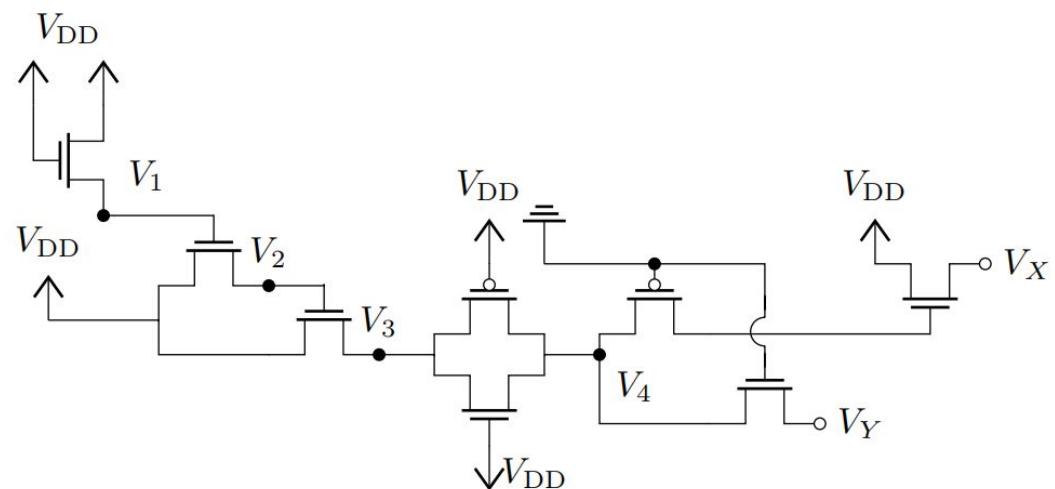
x_2	f'	f
0	0	0
0	1	1
1	0	1
1	1	1



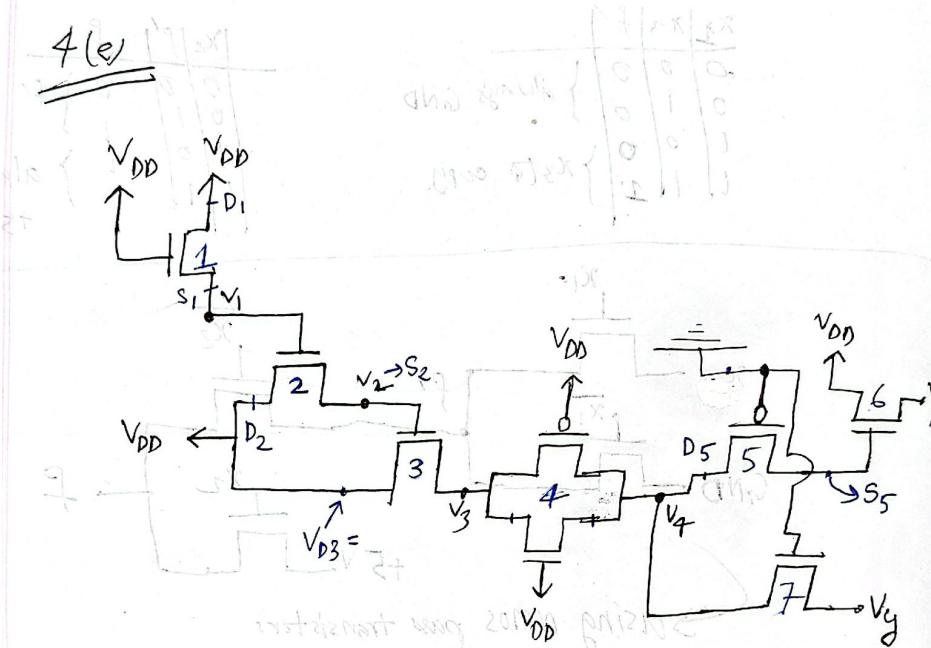
Using TG :

Pass Transistor math

[5 marks] In the adjacent figure, the supply voltage (V_{DD}) is 5 V. The threshold voltages for the pMOS and nMOS transistors are both set at $V_{tn} = |V_{tp}| = 0.1$ V. Determine the voltages V_1 , V_2 , V_3 , and V_4 as well as the output voltages V_X and V_Y . [Z is also a valid output.]



Summer 24 → set 2



$$V_{th} = |V_{tp}| = 0.1V; V_{DD} = 5V \text{ (given)}$$

$$\begin{aligned} \textcircled{1} \rightarrow & \text{ ON; } V_1 = (V_{s,max} \text{ or } V_g - V_{th}) = V_{D1} \text{ or pass} \\ & = 5 - 0.1 = 4.9V \end{aligned}$$

$$\begin{aligned} \textcircled{2} \rightarrow & \text{ ON as } V_g - V_{th} = 4.9 - 0.1 > 0V \\ \text{ now, } & V_{s2} \text{ ie } V_{s,max} = V_{g2} - V_{th} = 4.9 - 0.1 \\ & = 4.8V \end{aligned}$$

hence $V_{D2} = 5V \rightarrow$ gets degred. dcl. as $V_2 < V_{D2}$

$$V_2 = 4.8V \quad |_{V_2 < 5V}$$

\rightarrow (3) $\rightarrow V_{g3} = 4.8V > 0.1V$ hence on.

$$V_{3, \max} \text{ can be } \approx V_{g3} - V_{th} = 4.7V$$

$$V_{D3} = 5V \text{ here hence } \rightarrow V_3 = V_{S3} = 4.7V$$

(4) \rightarrow pMOS of T_6 is disabled only NMOS is

ON. and $V_2 = 5V$

$$\text{as } V_{g4} = 5V \text{ here and, } V_{f, \max} = V_{DD} - 0.1$$

$$\text{select } V_{D4} = 1.0 - F.A. \times 5V \approx 0.9V \Rightarrow (4.9)V$$

$$\text{as } V_{D4} = V_3 = 4.7V < 4.9V \rightarrow V_3 \text{ easily}$$

passes without degradation

\downarrow

$$V_4 > 0 = 5V \Rightarrow V_4 = 4.7V$$

⑤ \rightarrow PMOS always ON and for NMOS \rightarrow

$$V_{sg} > |V_{tp}| \quad (V_{tp}) = 5V$$

$$\Rightarrow V_{s, \min} = V_g + |V_{tp}| \rightarrow V_{s, \min} \text{ for}$$

$$V_{ss} = V_T + g_{nd} I = 4.7V$$

$$V_{tp} = 5V \leftarrow \text{constant} \quad \text{and } V_D = 5V$$

⑥ $\rightarrow V_{g6}$ of NMOS = $4.7V - 0.1V$ hence

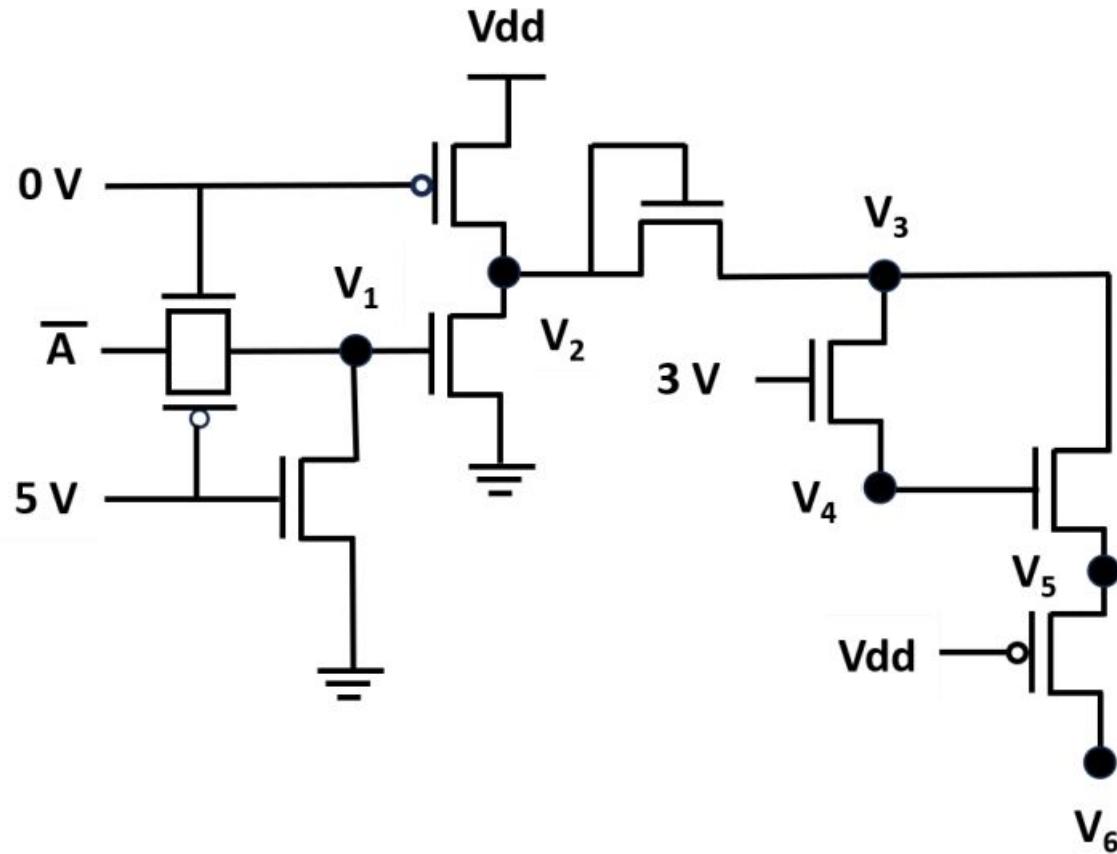
ON. $V_{D6} = 5V$ but $V_{D6} = 0V$

$V_{s6, \max}$ ie $V_{x, \max} = 4.7 - 0.1 = 4.6V$ possible

hence $V_{s6} = V_x = 4.6V$

⑦ \rightarrow NMOS always off as $V_g = 0 < V_{th}$

hence, $V_y = \text{floating} = 2$



For the circuit, $V_{dd} = 4\text{ V}$ and $V_{tn} = |V_{tp}| = 0.2\text{ V}$. Determine V_1 , V_2 , V_3 , V_4 , V_5 , and V_6 .

(d) $V_1 = 0\text{ V}$, $V_2 = 4\text{ V}$, $V_3 = 3.8\text{ V}$, $V_4 = 2.8\text{ V}$, $V_5 = 2.6\text{ V}$, $V_6 = 2$

Transmission gates are used to execute different types of combinational and sequential logic circuits like below:

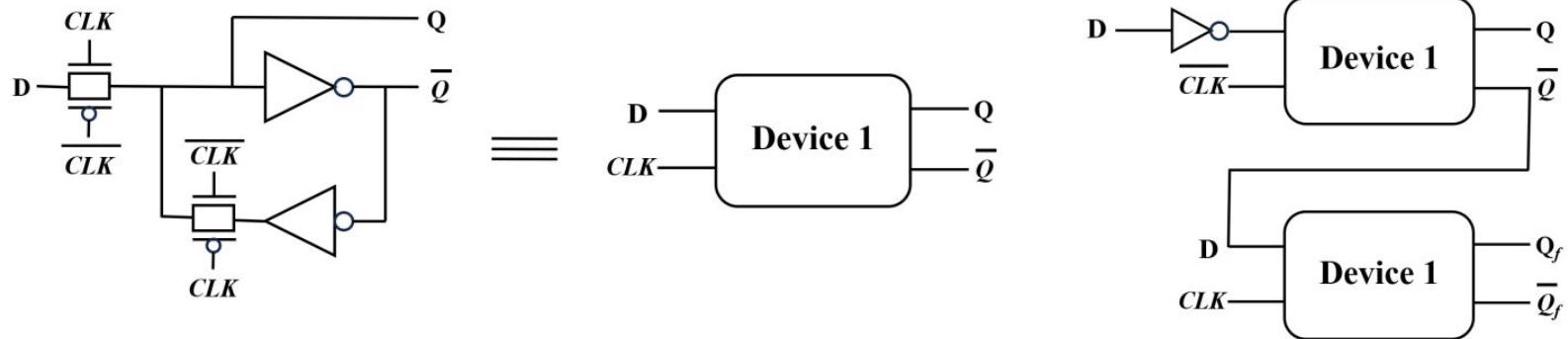
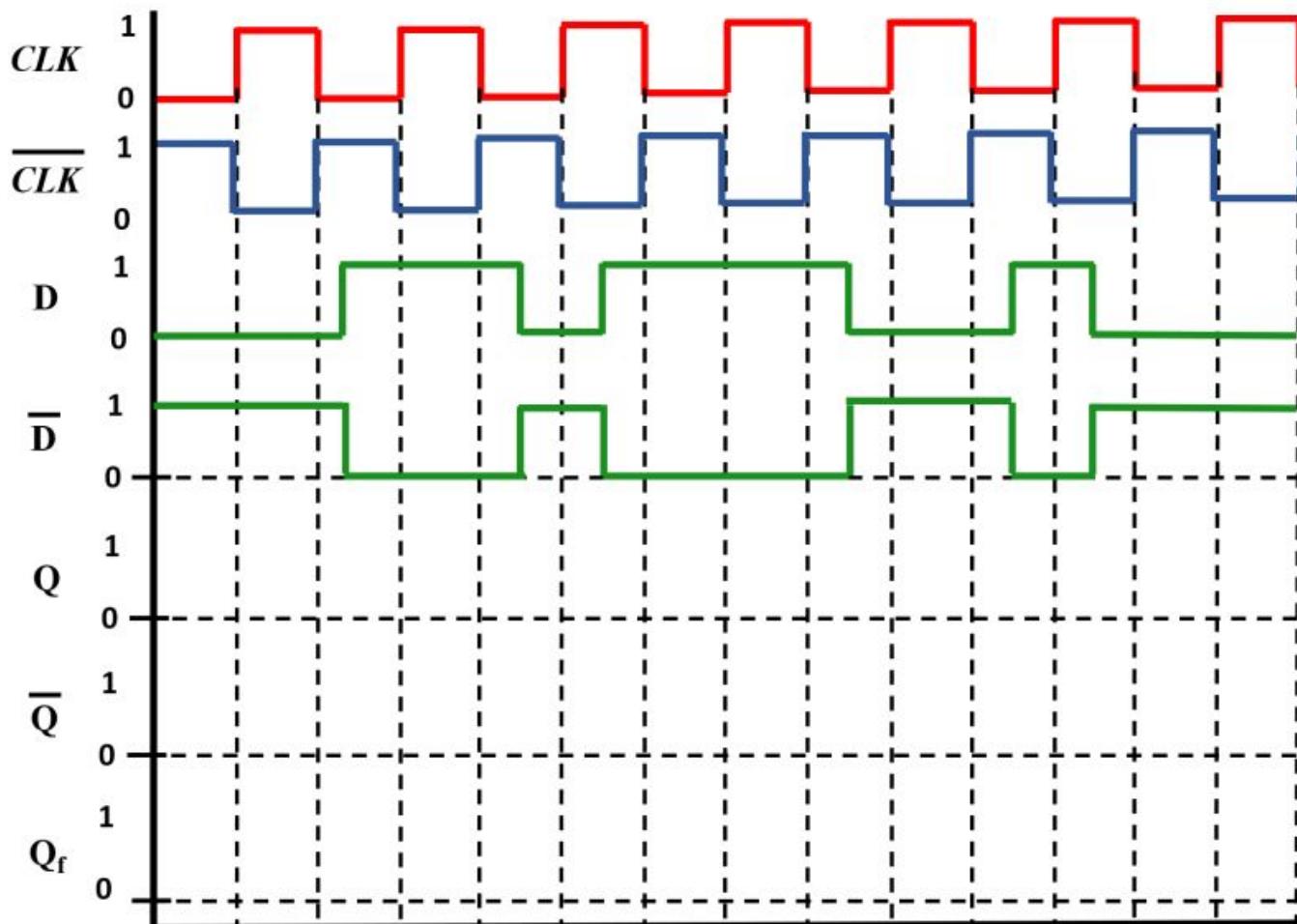


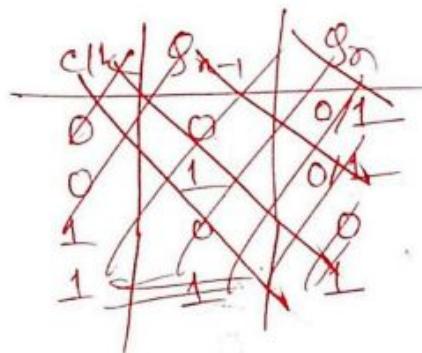
Figure 1: Circuit on the left is represented by the block **Device 1**. Circuit on the right uses this **Device 1**.



- (b) Identify Device 1 in Fig. 1 (Negative-edge/level-triggered or positive-edge/level-triggered flip-flop/latch) with a proper **characteristic table**. 2
- (c) Draw the waveforms in the grid given above for the right circuit of Fig. 1. Determine if the circuit is a negative-edge/level-triggered or positive-edge/level-triggered flip-flop/latch?

b

Device-1 is a positive level triggered latch.



clk	D	Q _{n-1}	Q
0	0	0	0
0	1	1	1
1	0	0	0
1	1	1	1

c) positive-edge triggered flip-flop.

