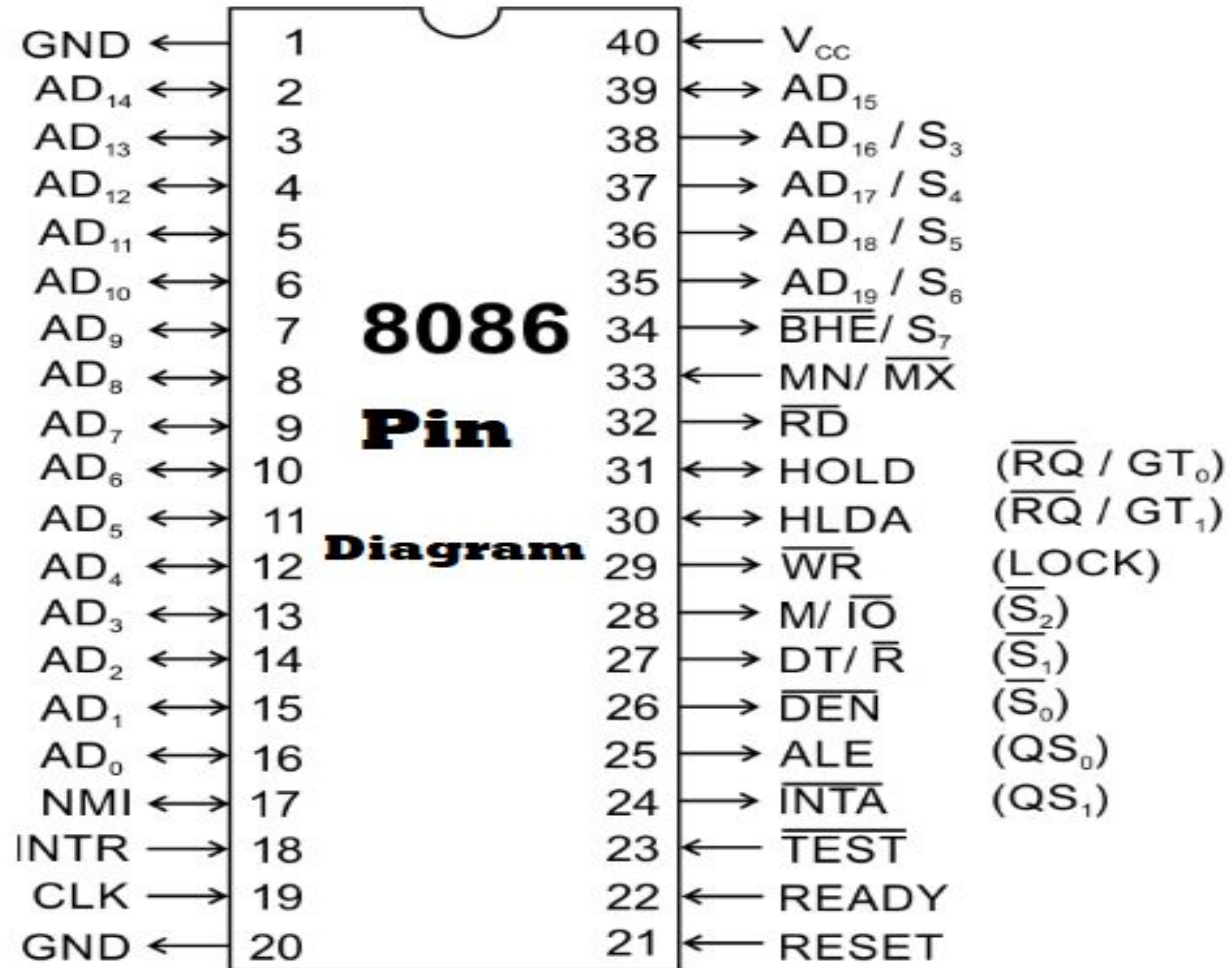


# 8086 Bus Timing Diagram :

## Pins and Signals

Classe-23

# 8086 Pin Diagram

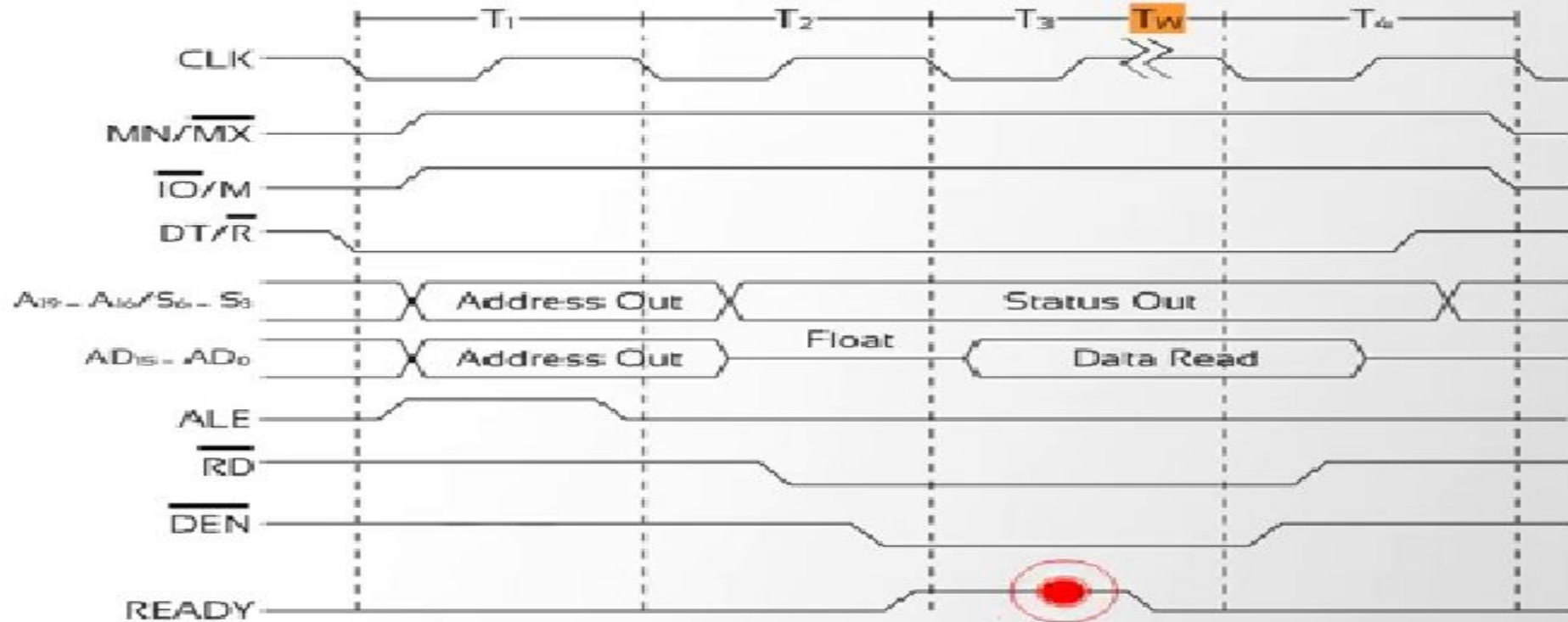


# 8086 Status Signals

Status Inputs			CPU Cycles	8288 Command
$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$		
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}, \quad \overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Instruction Fetch	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}, \quad \overline{AMWC}$
1	1	1	Passive	None

Bus Status Codes

# 8086 Bus Timing Diagram



Once the Ready line is pulled low, the processor enters a Wait State and it will continue to be in Wait State till the Ready line is pulled high.

# 8086 Bus Timing Diagram

## Use of the Ready line:

Ready line is pulled high when the external peripheral device is ready.



The processor reads information of the data bus.



Enables the signal to read data from the memory device at that point of time.

# 8086: Mode of Operation

## Minimum Mode

- Single Processor mode: No additional Co-processor can be connected.
- 8086 responsible for generating all control signals for Memory and I/O.
- Used to design systems used in simple applications.

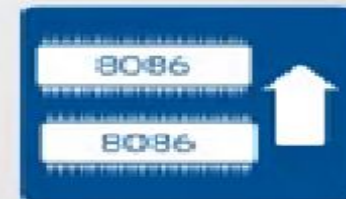
## Maximum Mode

- Multiprocessor mode: Additional Co-processors can be connected.
- External Bus controller is responsible for generating all control signals for Memory and I/O.
- Used for complex and large applications.



Minimum Mode

Versus



Maximum Mode

# Reference

Microprocessors and Microcomputer-Based System Design, Mohamed Rafiquzzaman,

Chapter-3

- 3.7.1 (overview) & 3.7.2.