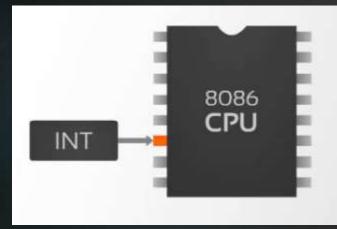
# 8086 Microprocessor Interrupts



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#### **Introduction**

- > The meaning of 'interrupts' is to break the sequence of operation.
- While the Microprocessor is executing a program, an 'interrupt' breaks the normal sequence of execution of instructions, diverts its execution to some other program called Interrupt Service Routine (ISR).

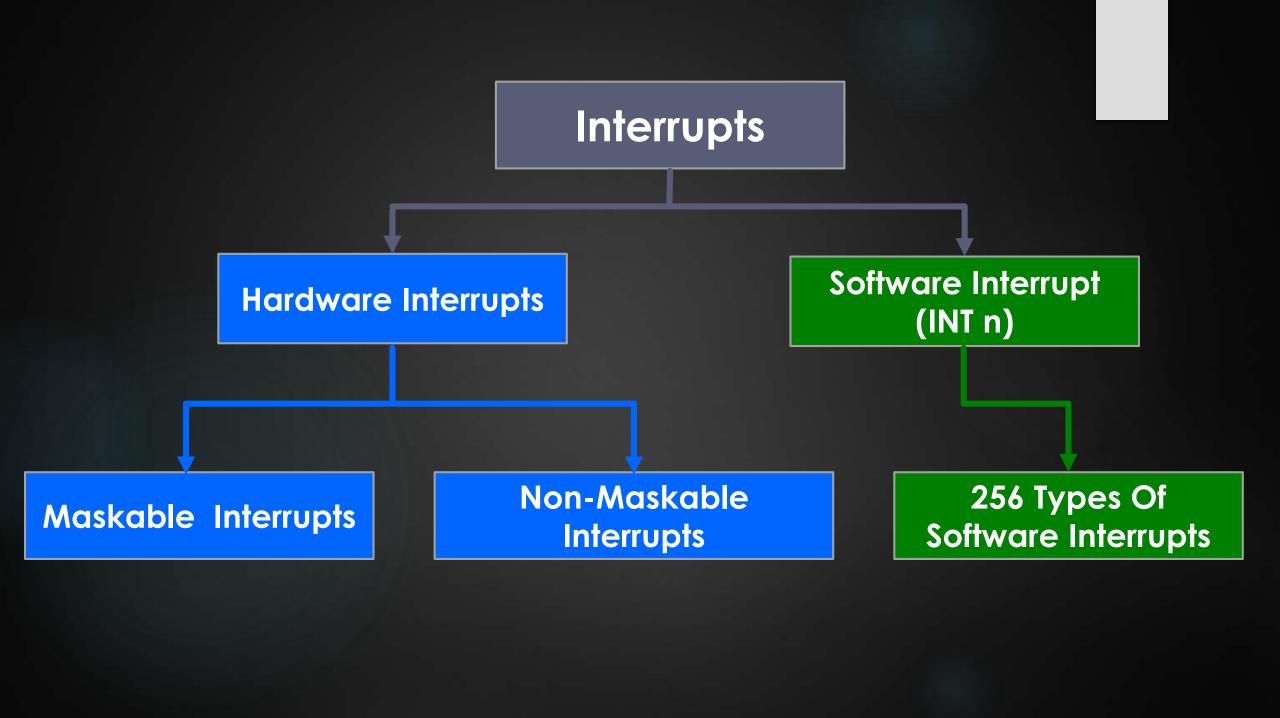
After executing, control returns the back again to the main program.

## <u>Interrupt</u>

- Keeping moving until interrupted by the sensor.
- > Interrupt received then do pre-defined operation.
- After finishing the interrupt service return to normal operation i.e keep moving forward again.

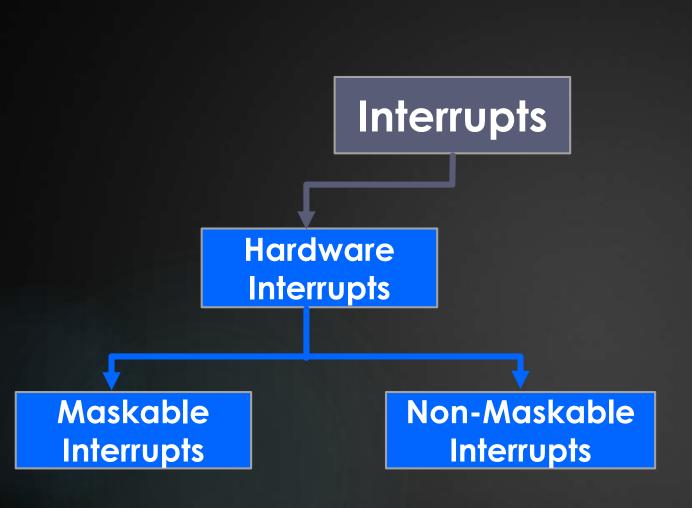
#### The processor can be interrupted in the following ways

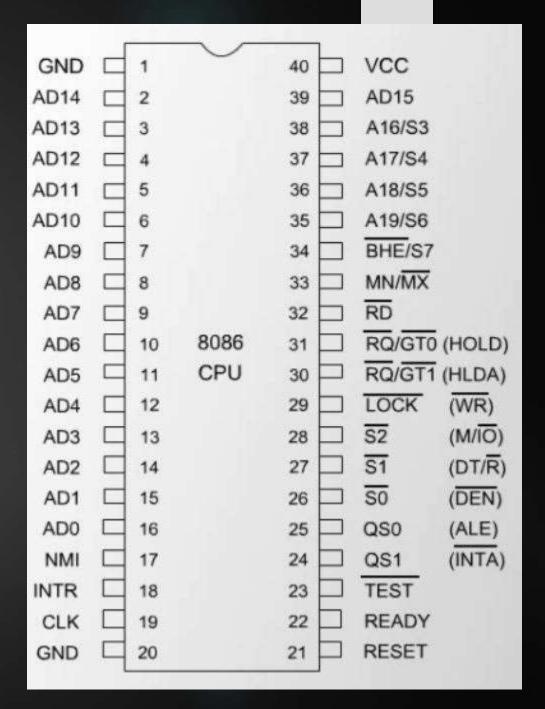
- i) by an external signal generated by a peripheral,
- ii) by an internal signal generated by a special instruction in the program,
- iii) by an internal signal generated due to an exceptional condition which occurs while executing an instruction.

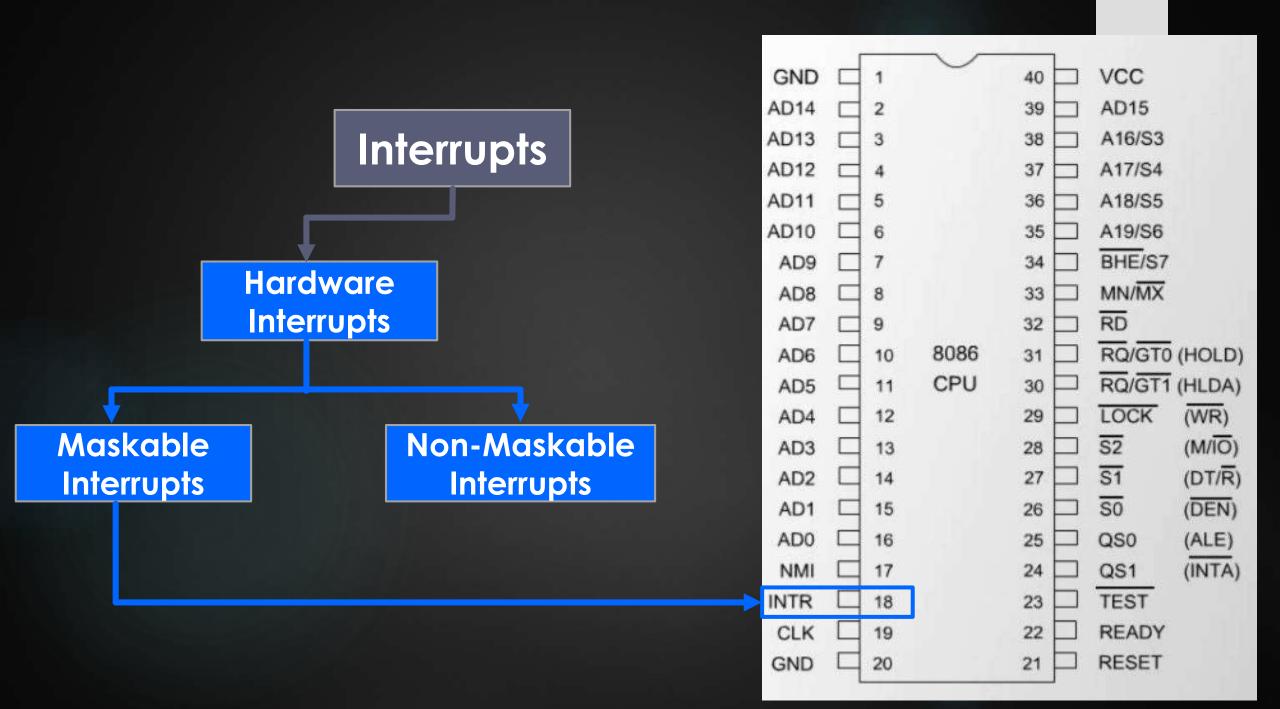


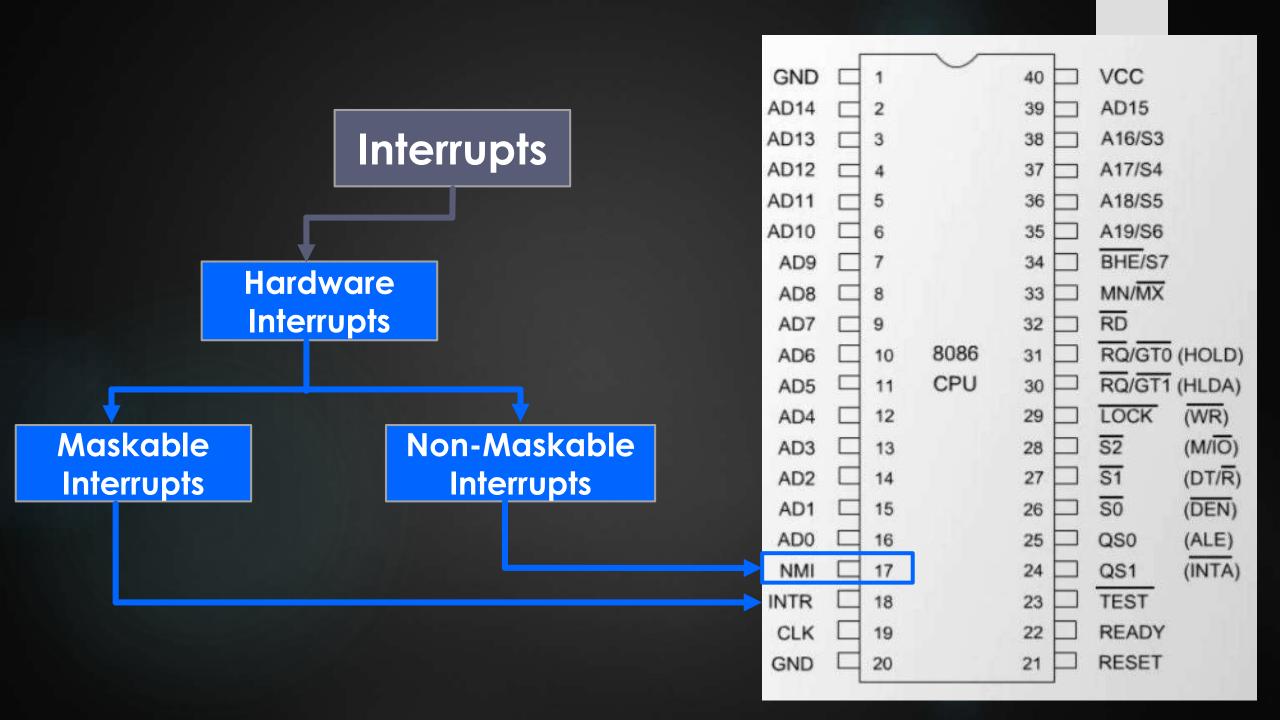
## **Hardware Interrupts**

The interrupts initiated by external hardware by sending an appropriate signal to the interrupt pin of the processor is called hardware interrupt. The 8086 processor has two interrupt pins INTR and NMI. The interrupts initiated by applying appropriate signal to these pins are called hardware interrupts of 8086.









#### **Hardware Interrupts**

Used to handle external hardware peripherals, such as key boards, mouse, hard disks, floppy disks, DVD drivers, and printers.

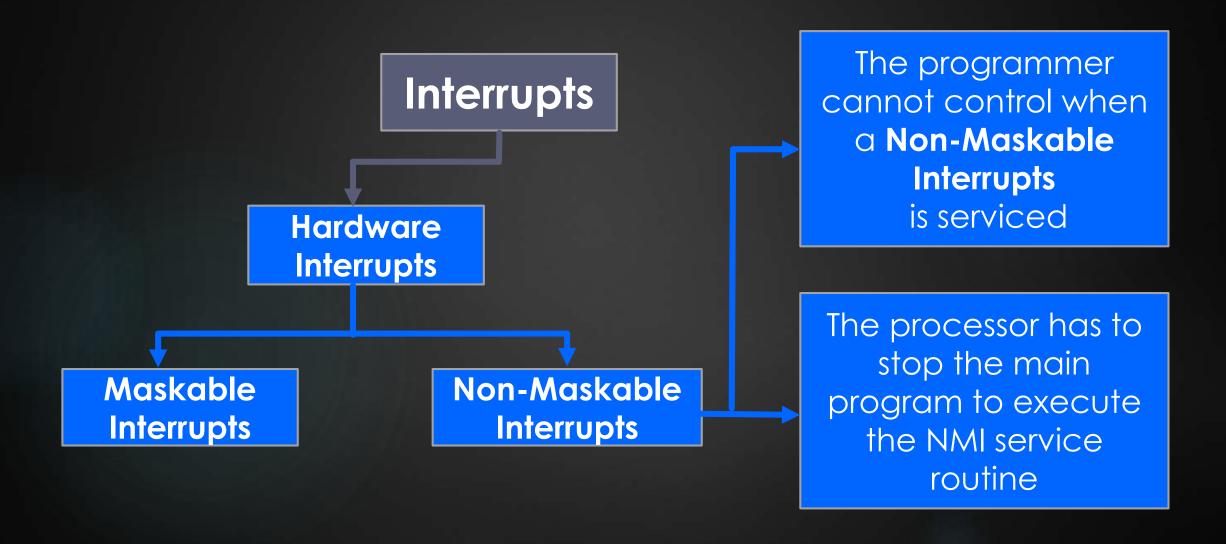


#### Maskable & Non-Maskable Interrupts

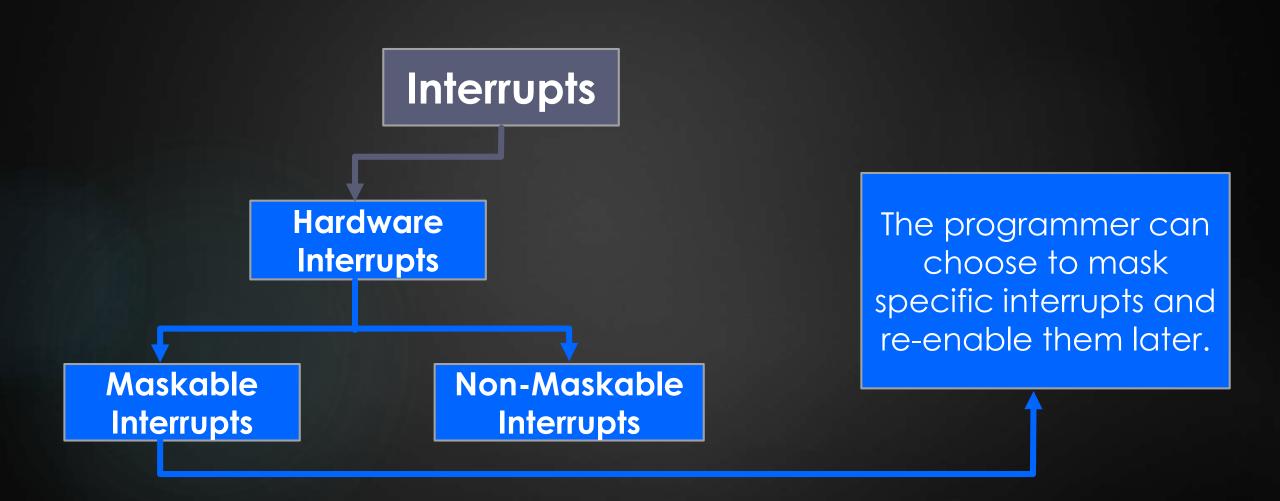
The processor has the facility for accepting or rejecting hardware interrupts. Programming the processor to reject an interrupt is referred to as masking or disabling and programming the processor to accept an interrupt is referred to as unmasking or enabling. In 8086 the interrupt flag (IF) can be set to one to unmask or enable all hardware interrupts and IF is cleared to zero to mask or disable a hardware interrupts except NMI. The interrupts whose request can be either accepted or rejected by the processor are called maskable interrupts.

The interrupts whose request has to be definitely accepted (or cannot be rejected) by the processor are called non-maskable interrupts. Whenever a request is made by non-maskable interrupt, the processor has to definitely accept that request and service that interrupt by suspending its current program and executing an ISR. In 8086 processor all the hardware interrupts initiated through INTR pin are maskable by clearing interrupt flag (IF). The interrupt initiated through NMI pin and all software interrupts are non-maskable.

#### Maskable & Non-Maskable Interrupts



### Maskable & Non-Maskable Interrupts



#### Non-Maskable Interrupts

Used during power failure

Used during critical response time

Used during non-recoverable hardware errors

Used watchdog interrupt

Used during memory parity errors

#### **Software Interrupts**

The software interrupts are program instructions. These instructions are inserted at desired locations in a program. While running a program, if software interrupt instruction is encountered then the processor initiates an interrupt. The 8086 processor has 256 types of software interrupts. The software interrupt instruction is INT n, where n is the type number in the range 0 to 255.

## Software Interrupt (INT n)

Used by operating systems to provide hooks into various function

Used as a communication mechanism between different parts of the program

## 8086 INTERRUPT TYPES 256 INTERRUPTS OF 8086 ARE DIVIDED IN TO 3 GROUPS

#### 1. TYPE 0 TO TYPE 4 INTERRUPTS-

These Are Used For Fixed Operations And Hence Are Called Dedicated Interrupts

#### 2. TYPE 5 TO TYPE 31 INTERRUPTS

Not Used By 8086,reserved For Higher Processors Like 80286 80386 Etc

#### 3. TYPE 32 TO 255 INTERRUPTS

Available For User, called User Defined Interrupts These Can Be H/W Interrupts And Activated Through Intr Line Or Can Be S/W Interrupts.

- ➤ Type 0 Divide Error Interrupt

  Quotient Is Large Cant Be Fit In Al/Ax Or Divide By Zero
- ➤ Type –1 Single Step Interrupt

  Used For Executing The Program In Single Step Mode By Setting Trap Flag
- ➤ Type 2 Non Maskable Interrupt

  This Interrupt Is Used For Execution Of NMI Pin.
- ➤ Type 3 Break Point Interrupt

  Used For Providing Break Points In The Program
- ➤ Type 4 Over Flow Interrupt

  Used To Handle Any Overflow Error.

## **Conclusion**

The CPU executes program, as soon as a key is pressed, the Keyboard generates an interrupt. The CPU will response to the interrupt – read the data. After that returns to the original program. So by proper use of interrupt, the CPU can serve many devices at the "same time"

## Reference

- □Net
- "Advanced microprocessor & peripherals" by K.M Bhurchandi & A.K Ray



#### **Related Articles**

Difficulty Level: Medium • Last Updated: 17 Aug, 2018

An interrupt is a condition that halts the microprocessor temporarily to work on a different task and then return to its previous task. Interrupt is an event or signal that request to attention of CPU. This halt allows peripheral devices to access the microprocessor.

Whenever an interrupt occurs the processor completes the execution of the current instruction and starts the execution of an Interrupt Service Routine (ISR) or Interrupt Handler. ISR is a program that tells the processor what to do when the interrupt occurs. After the execution of ISR, control returns back to the main routine where it was interrupted.

In 8086 microprocessor following tasks are performed when microprocessor encounters an interrupt:

- The value of flag register is pushed into the stack. It means that first the value of SP (Stack Pointer) is decremented by 2 then the value of flag register is pushed to the memory address of stack segment.
- 2. The value of starting memory address of CS (Code Segment) is pushed into the stack.
- 3. The value of IP (Instruction Pointer) is pushed into the stack.
- 4. IP is loaded from word location (Interrupt type) \* 04.
- 5. CS is loaded from the next word location.
- 6. Interrupt and Trap flag are reset to 0.

The different types of interrupts present in 8086 microprocessor are given by:

#### 1. Hardware Interrupts -

Hardware interrupts are those interrupts which are caused by any peripheral device

by sending a signal through a specified pin to the microprocessor. There are two hardware interrupts in 8086 microprocessor. They are:

- (A) NMI (Non Maskable Interrupt) It is a single pin non maskable hardware interrupt which cannot be disabled. It is the highest priority interrupt in 8086 microprocessor. After its execution, this interrupt generates a TYPE 2 interrupt. IP is loaded from word location 00008 H and CS is loaded from the word location 0000A H.
- (B) INTR (Interrupt Request) It provides a single interrupt request and is activated by I/O port. This interrupt can be masked or delayed. It is a level triggered interrupt. It can receive any interrupt type, so the value of IP and CS will change on the interrupt type received.
- 2. **Software Interrupts –** These are instructions that are inserted within the program to generate interrupts. There are 256 software interrupts in 8086 microprocessor. The instructions are of the format INT type where type ranges from 00 to FF. The starting address ranges from 00000 H to 003FF H. These are 2 byte instructions. IP is loaded from type \* 04 H and CS is loaded from the next address give by (type \* 04) + 02 H. Some important software interrupts are:
  - (A) *TYPE 0* corresponds to division by zero (0).
  - (B) *TYPE 1* is used for single step execution for debugging of program.
  - (C) TYPE 2 represents NMI and is used in power failure conditions.
  - (D) *TYPE 3* represents a break-point interrupt.
  - (E) TYPE 4 is the overflow interrupt.

#### Refer for - Interrupts in 8085 microprocessor

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