CSE 4621
Microprocessor and Interfacing

Class-22

Tri-state Logic

Tri-state Logic

- In digital electronics three-state, tri-state, or 3-state logic
  - allows an output port to assume a high impedance state in addition to the 0 and 1 logic levels,
  - **effectively removing the output from the circuit.**

Tri-state Logic

- To understand the concept and need for tri-state devices one must understand the **concept of a ‘bus’.**
- Bus is typically a set of parallel connections on which several devices are connected together.
- Imagine a bus were many devices are connected on parallel.
- If one of the device’s output is connected to the bus and the rest have their inputs on the it, then there is no problem.

Tri-state Logic

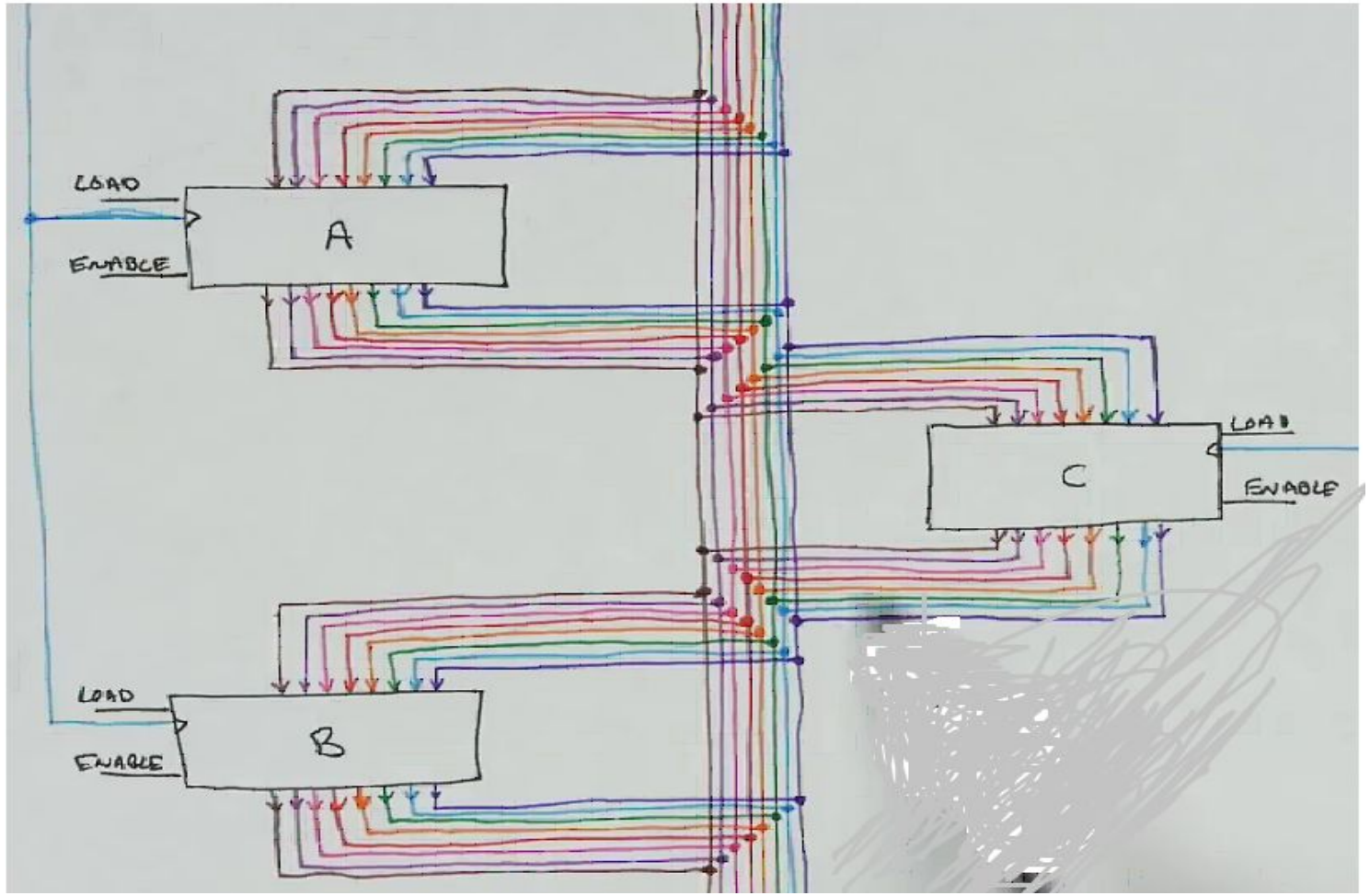


Figure: Typical Bus System, on which several devices are connected together.

Tri-state Logic

- But what happens **when multiple devices have their outputs connected to it.**
- For example two or more logic gates' output is connected together. One of the device might output a logic '1' and simultaneously the other might output a '0'. **Leading to short circuit currents** and pulling the potential of the line to some indeterminate state.

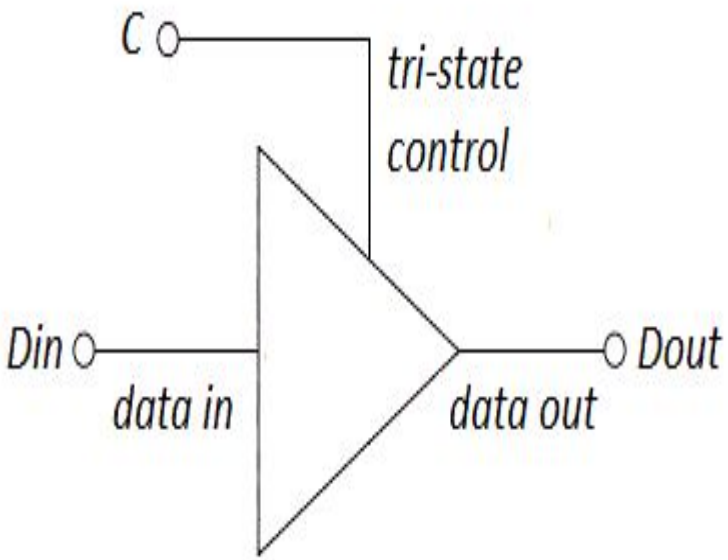
Tri-state Logic

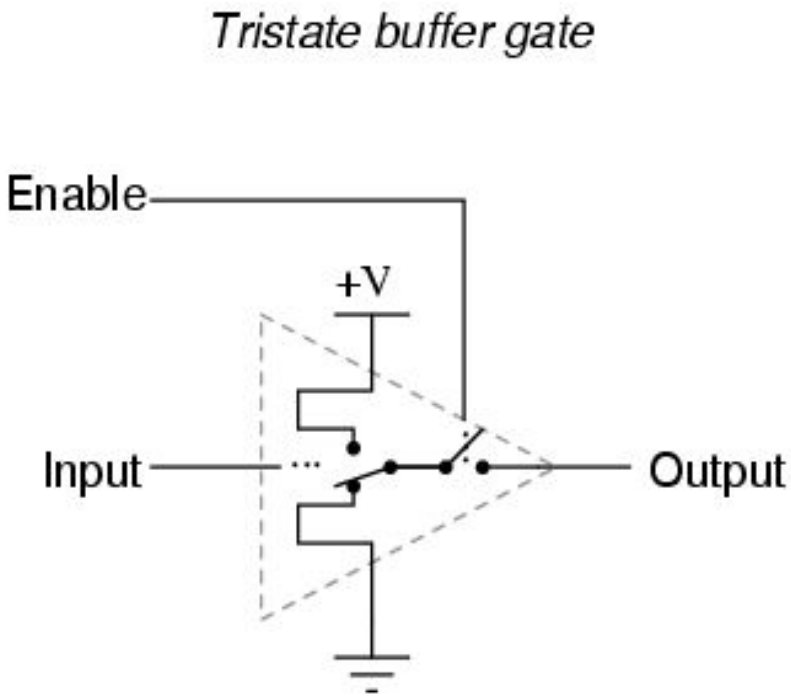
- Under such a scenario how do we connect multiple devices (eg. multiple RAMs etc) **irrespective of the inputs, the output will either be in '1' or '0'.**
- **That is where tri-state comes into picture.**

Tri-state Logic

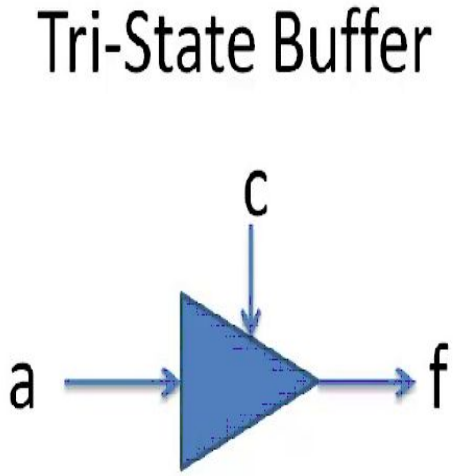
- **All the devices will have tri-state drives at their output.**
- Now when enabled, the outputs can either be ‘1’ or ‘0’ but when disabled they go into a third state
  - **i.e. tri-state, where they can neither source or sink.**
- Such outputs can be connected in parallel and they will not affect the existing condition of the bus.

Tri-state Logic

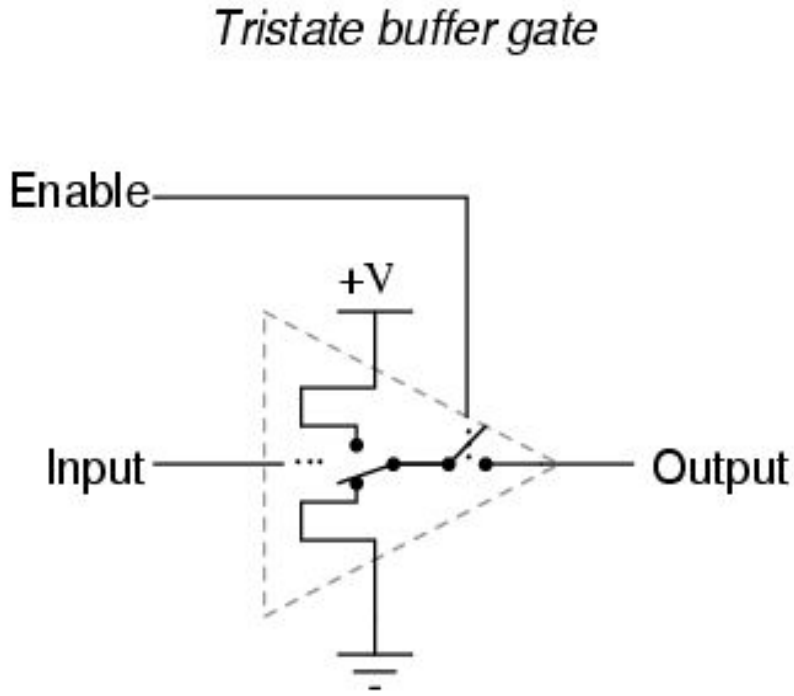




Tri-state Logic



c	a	f
0	0	Z
0	1	Z
1	0	0
1	1	1



Tri-state Logic

- When we connect multiple memory devices together on the data bus then the only device which is being addressed will enable the output buffers out of tri-state in response to the read signal.

Reference:

- https://youtu.be/faAjse109Q8
- https://www.quora.com/What-does-tristate-mean-in-8085-microprocessor