

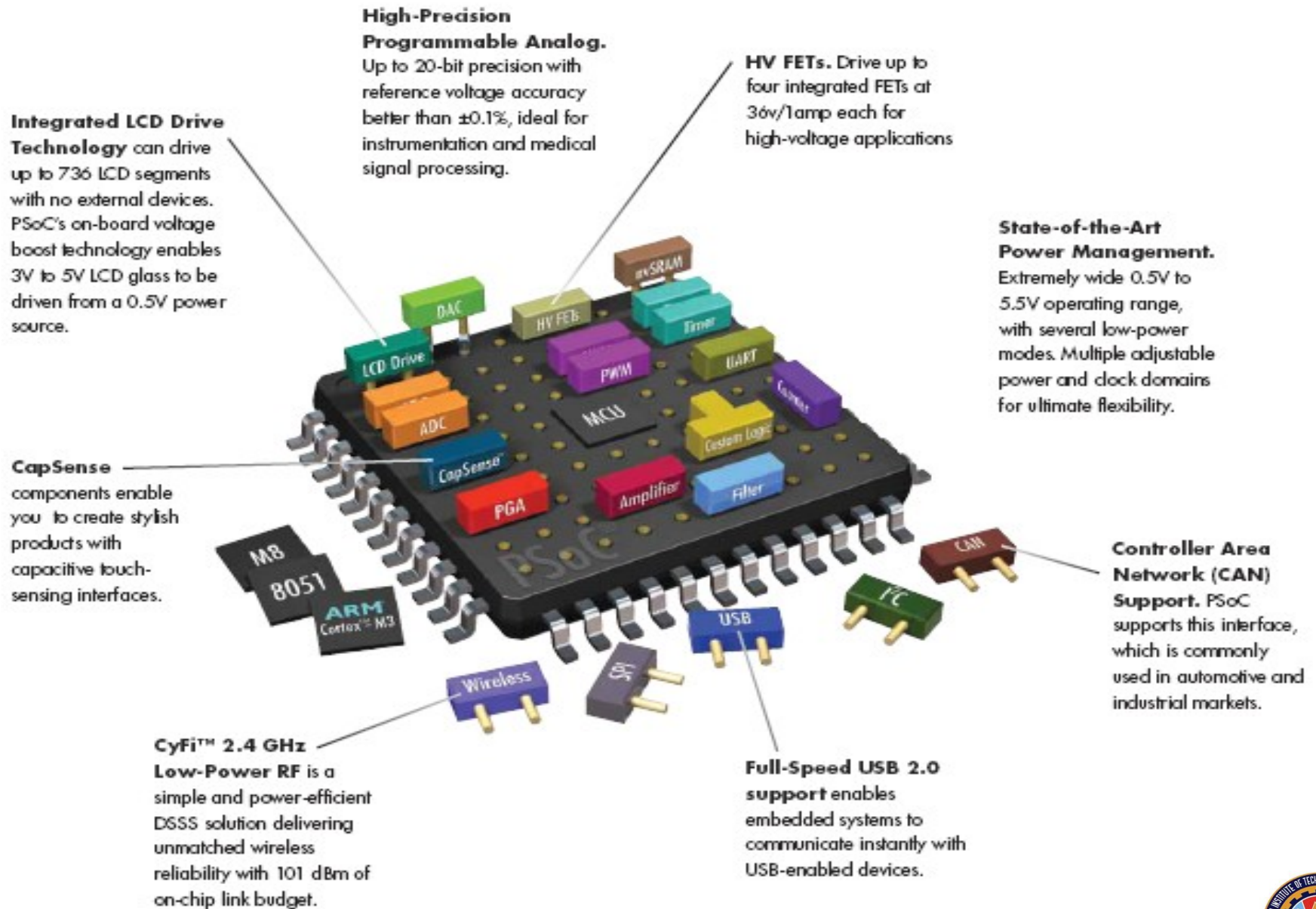
# What is a PSoC ?

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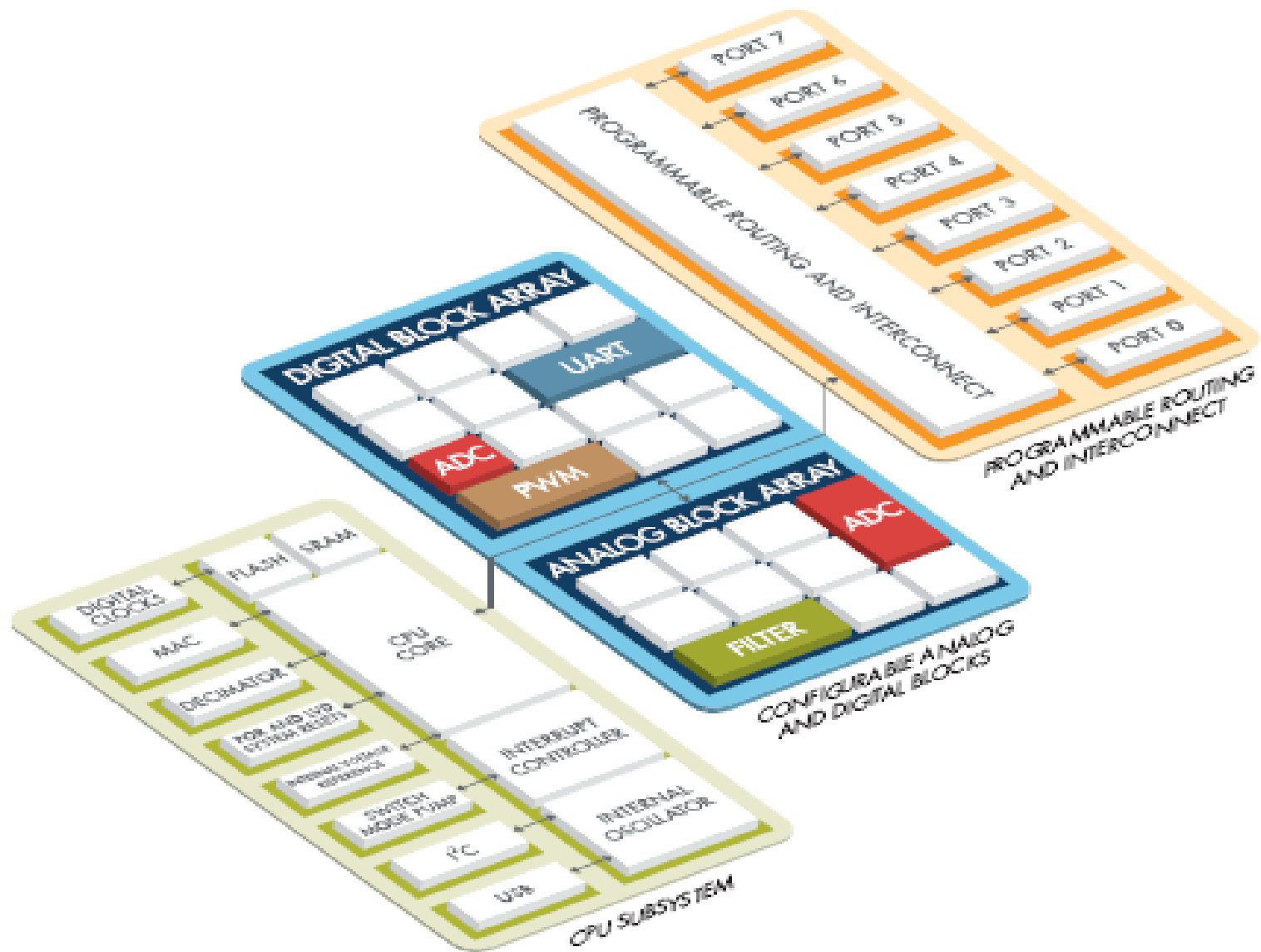
PSoC combines:

- the familiarity of a microcontroller
- the configurability of an CPLD
- the capabilities of an Mixed –Signal Array

# PSoC: Functionalities



# PSoC: Functional Blocks



# Functions Enabled by PSoC

## ☐ Environmental sensing

- Pressure
- Humidity
- Current
- Airflow
- Acceleration
- Tilt
- Pyroelectric Infrared (PIR)
- Light
- Voltage
- Temperature
- Inductive
- Gas
- Liquid level

## ☐ Touch Sensing

- CapSense capacitive sensing (buttons, sliders)
- Touchscreens
- Trackpads
- Proximity sensing

## ☐ Fan/Motor Control

- AC motor
- DC motor
- Fan
- Fuel pump
- Instrument gauges

# Functions Enabled by PSoC

## ☐ Communications interfaces

- Wireless radio control
- LIN bus
- Optical cable conversion
- Dual Tone Multi-Frequency (DTMF) dialer
- USB 2.0

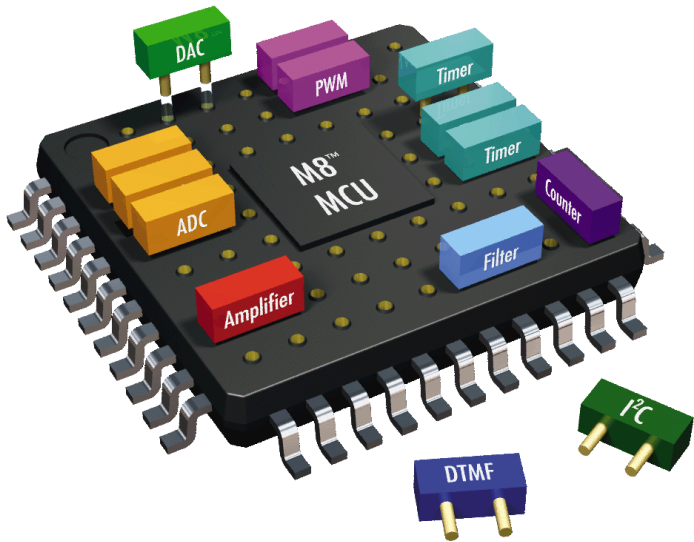
## ☐ Other

- Magnetic cord read/write
- Mechanical buttons or other inputs
- LCD display/drive control
- LED drive

## ☐ Power Control

- Battery charging
- Voltage & current
- System power
- AC power metering
- Lighting

# What is PSoC 1?



## Inputs

- Each pin can sink 25mA
- Programmable filters
- Flexible sensor interface I/O
- 3 types of ADCs, up to 4

## Processing

- Fast M8 Microcontroller Core
- Multiply Accumulate

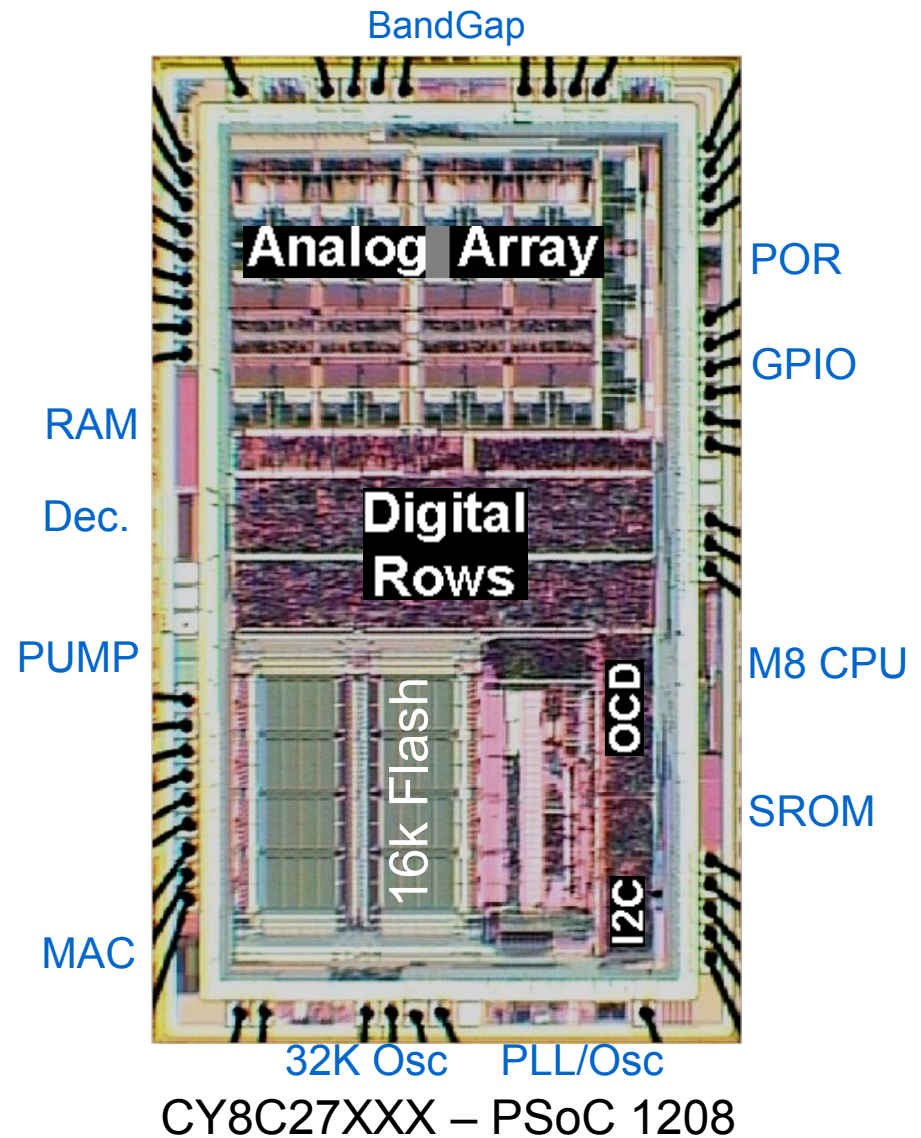
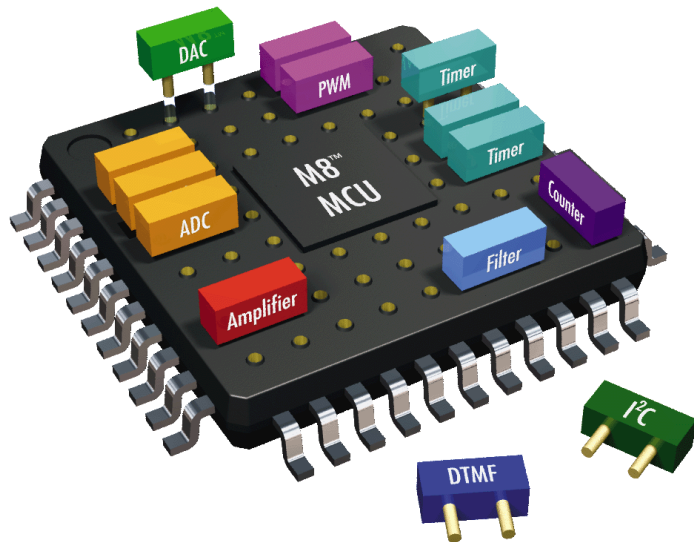
## Outputs

- Each pin can source 10mA
- Up to 16 PWMs, Timers, Counters
- Up to 9-bit DACs, 14-bit ADCs

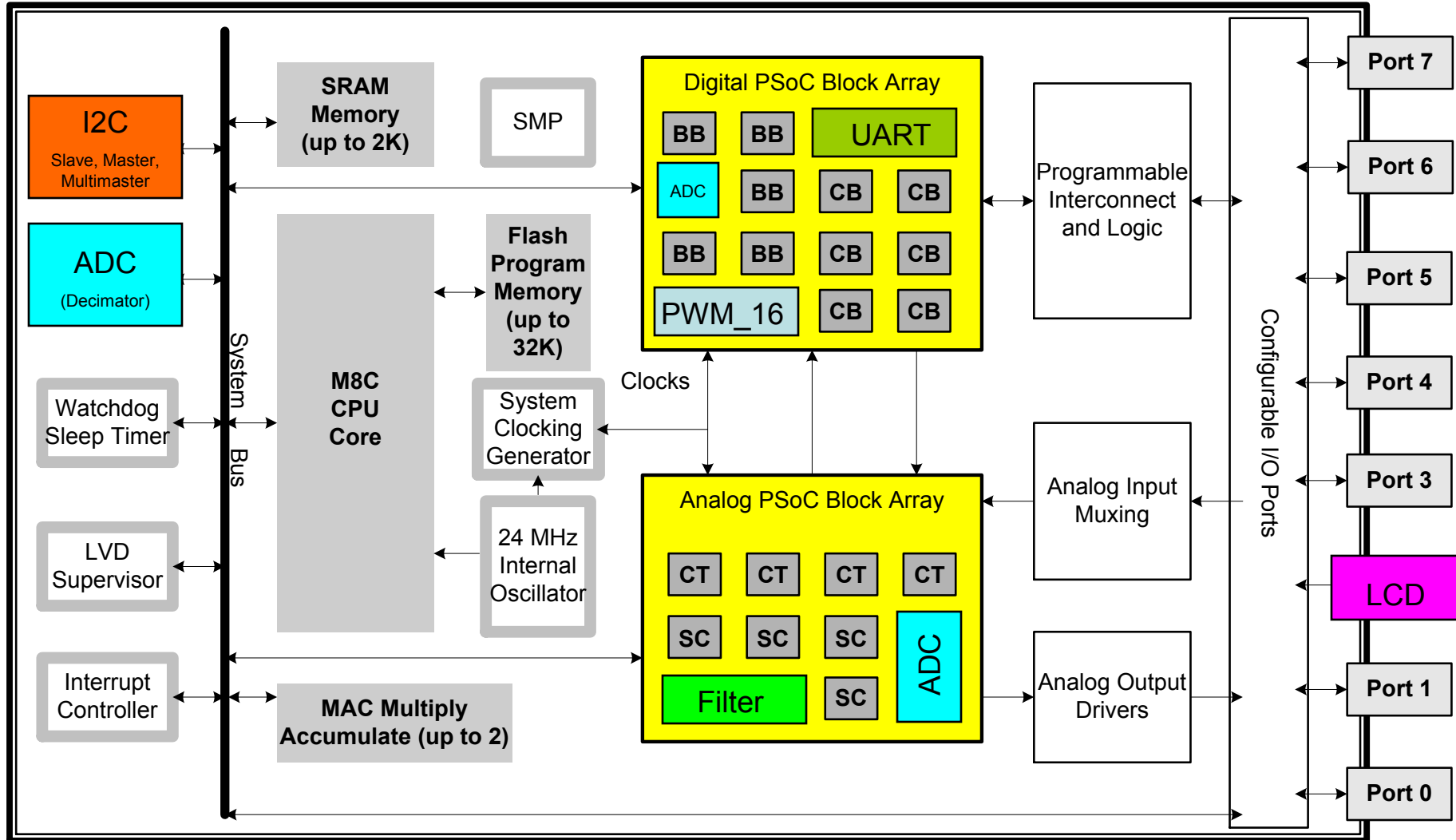
## Support Functions

- EEPROM
- Sleep Options
- Watch Dog Timer
- Low voltage detect

# PSoC Die

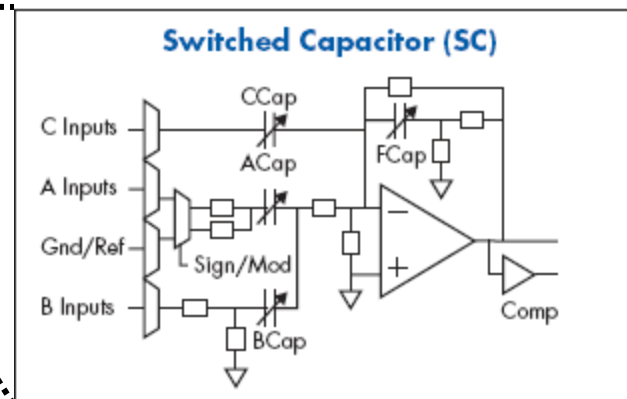
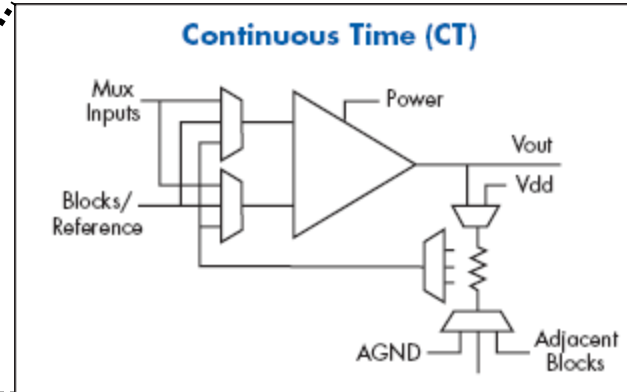
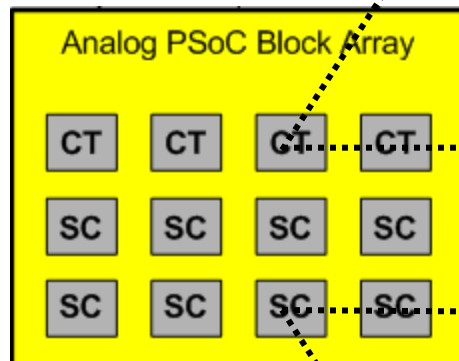


# PSoC 1 Architecture



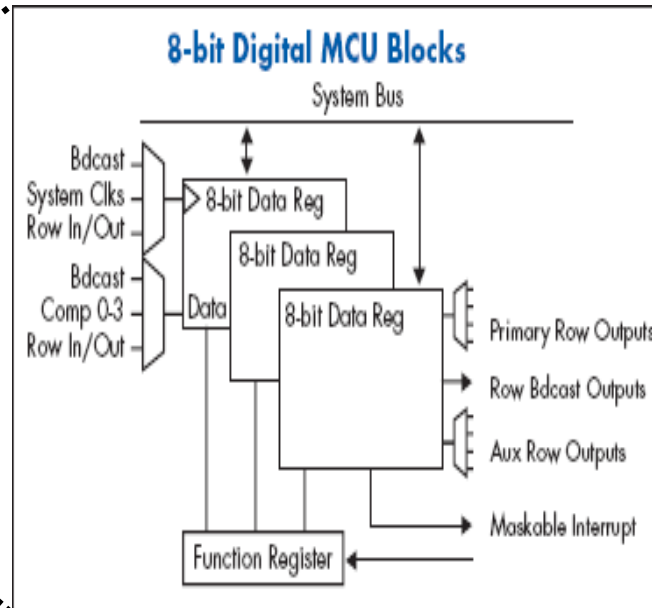
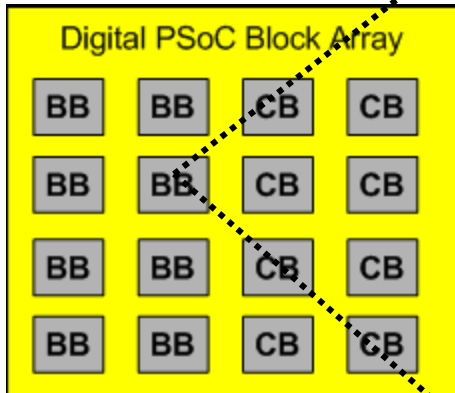


# Analog Functions (Subset)



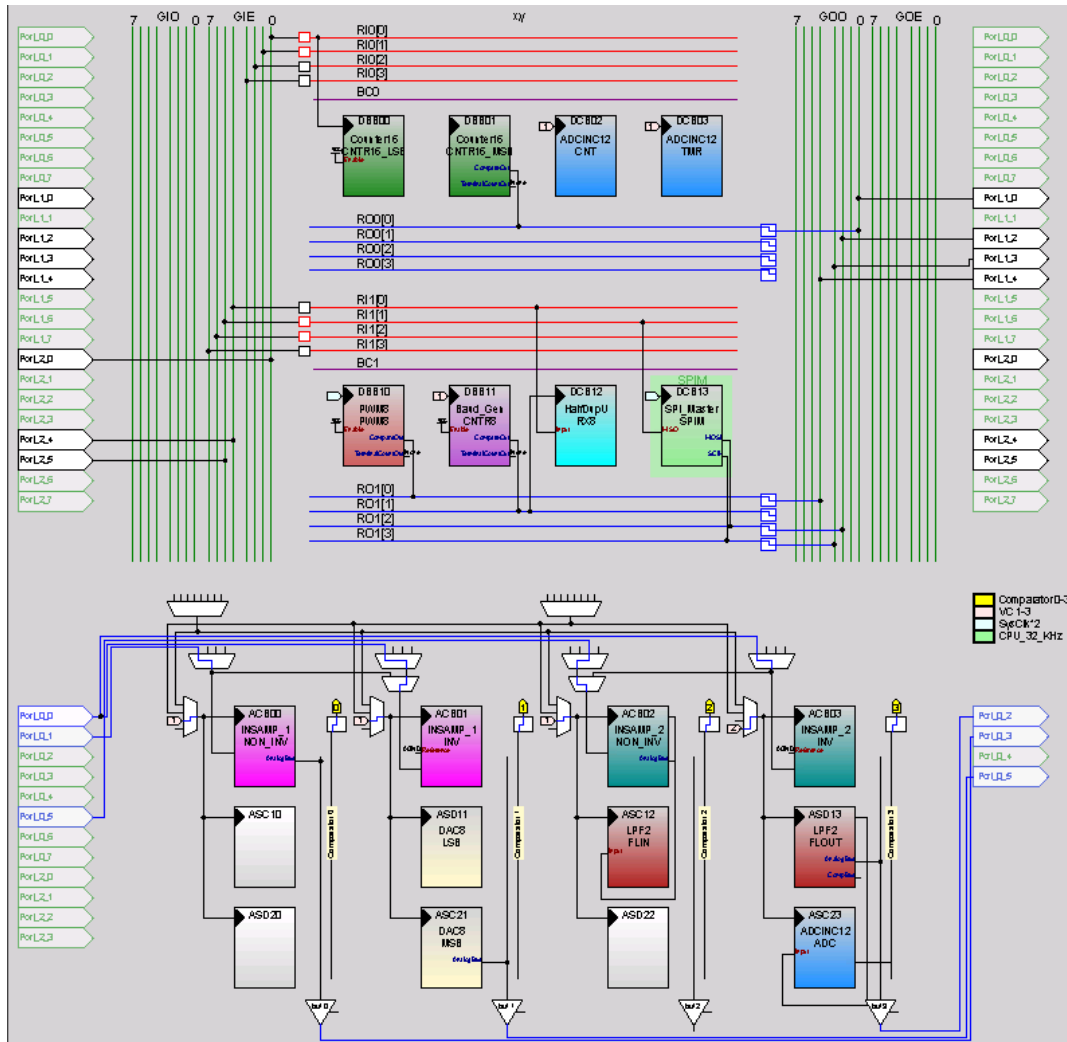
- ADC
  - Incremental 6-14 bits
  - Delta Sigma 6-13 bits
- DAC
  - 6, 8, and 9 bit
  - 6 and 8 bit multiplying
- Filters
  - 2-pole Low-pass
  - 2-pole Band-pass
- DTMF Dialer
- Modulator
- Peak Detector
- V to I Converter
- Amplifiers
  - Programmable Gain
  - Instrumental
  - Inverting
- Comparators
  - Programmable
  - Hysteresis
  - Zero-Crossing
- CapSense

# Digital Functions (subset)



- Timer  
8, 16, 24, 32 bit
- Counter  
8, 16, 24, 32 bit
- PWM  
8, 16, 24, 32 bit
- Dead Band Generator  
8, 16, 24, 32 bit
- Pseudo Random Source
- Cyclic Redundancy Check
- Communication Interface
  - I2C Master
  - I2C Slave
  - SPI Master
  - SPI Slave
  - Full Duplex UART
  - Tx, Rx
  - Full Speed USB v2.0

# Interconnection Scheme



- Define connections between pins and function blocks
- Define connections between function blocks
- Define clock paths
- Change connections dynamically too!

# User Modules

Pre-configured and Pre-characterized Digital and Analog PSoC Blocks

Greatly simplifies and shortens coding process

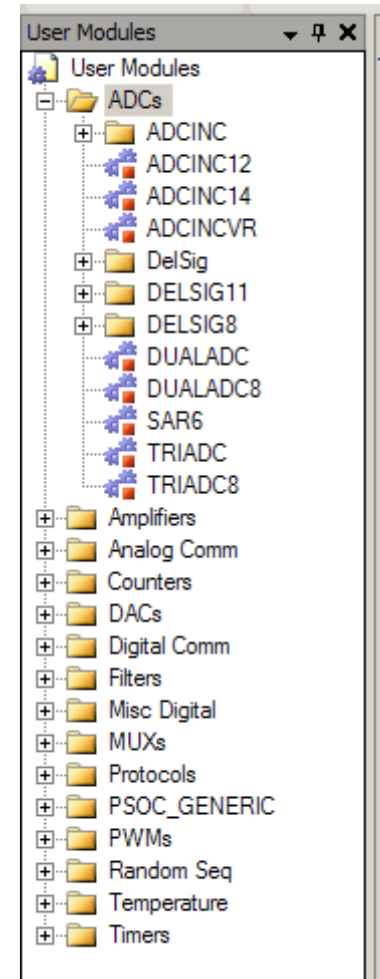
Analogous to On-chip Peripherals

- ADCs, DACs, PGAs, Filters
- Timers, Counters, PWMs
- UART, SPI, I2C

Defines the Register Bits for Initial Configuration  
Selected via Double Click in IDE

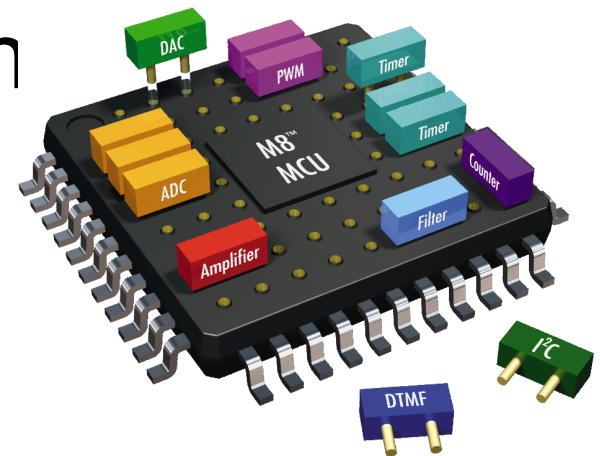
User Modules Include

- Application Programmer Interfaces (APIs)
- Interrupt Service Routines (ISRs)
- Specific UM Data Sheets



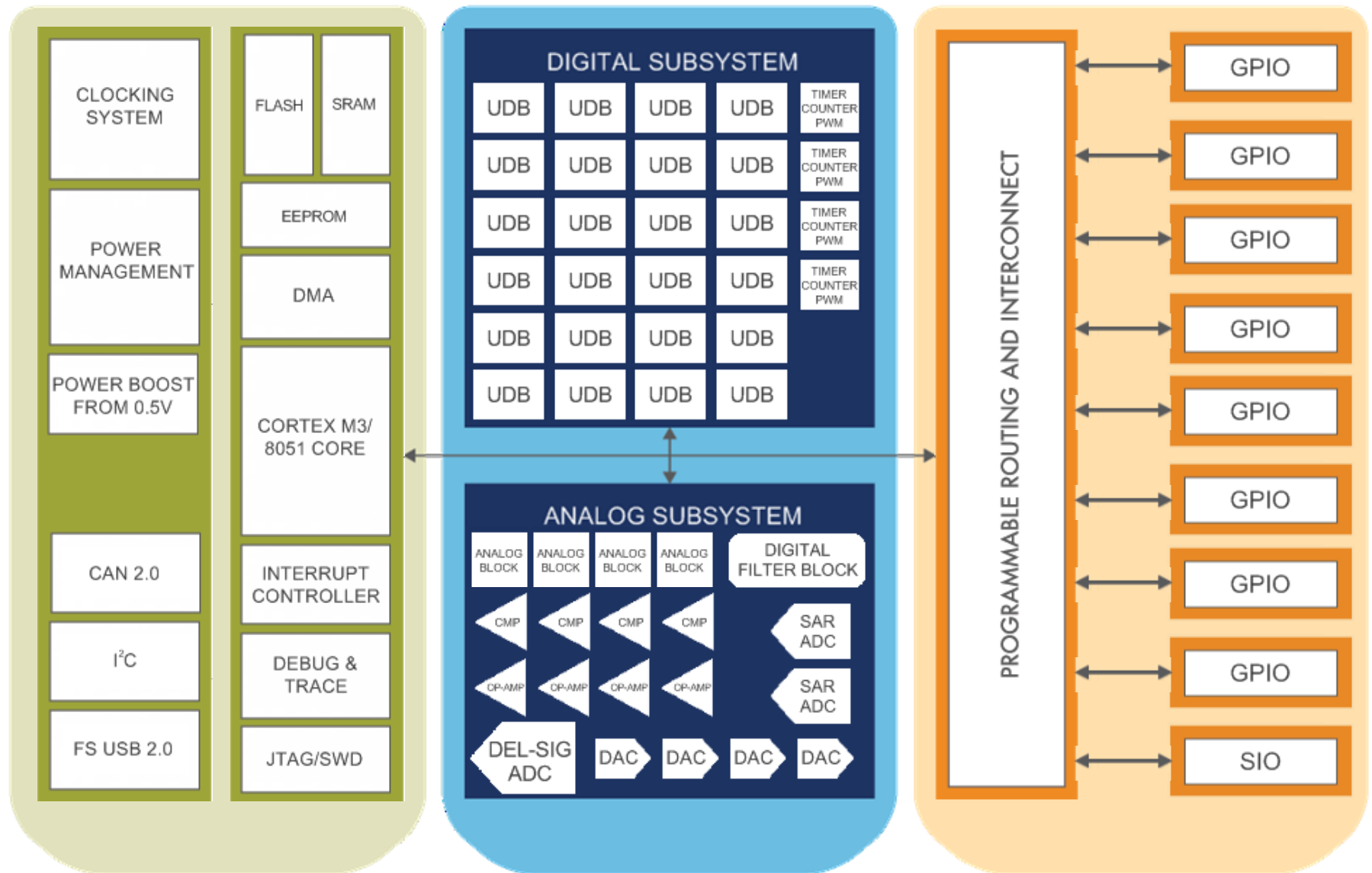
# Additional Features

- Comprehensive Design Tools
- Intuitive Resource Placement
- Easy Routing
- Powerful Logic
- Dynamic Reconfiguration

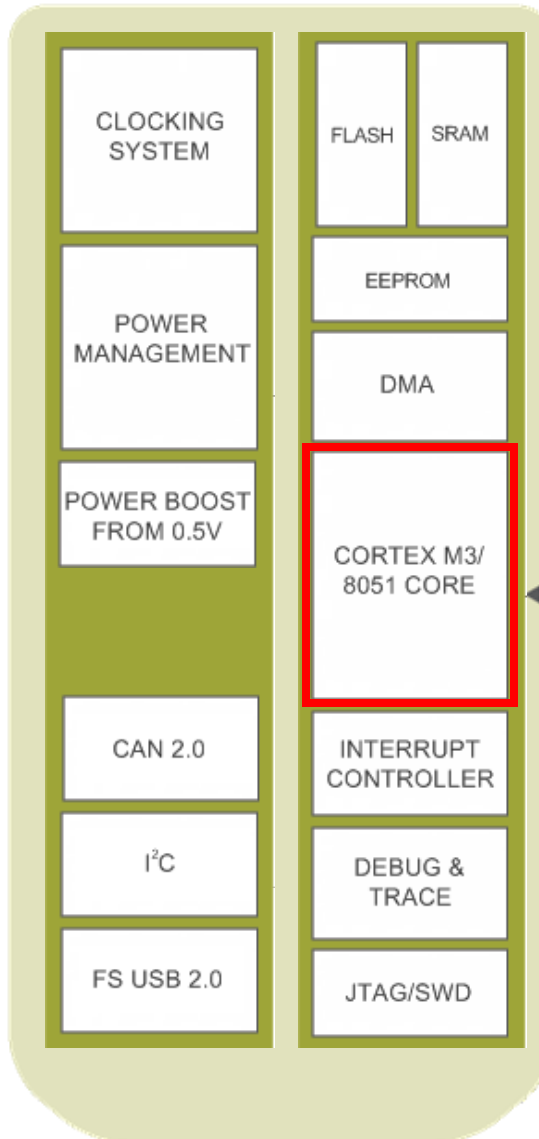


# **PSoC 3 / PSoC 5 101: Architecture Overview**

# PSoC 3 / PSoC 5 Platform Architecture



# CPU Subsystem



## ARM Cortex-M3

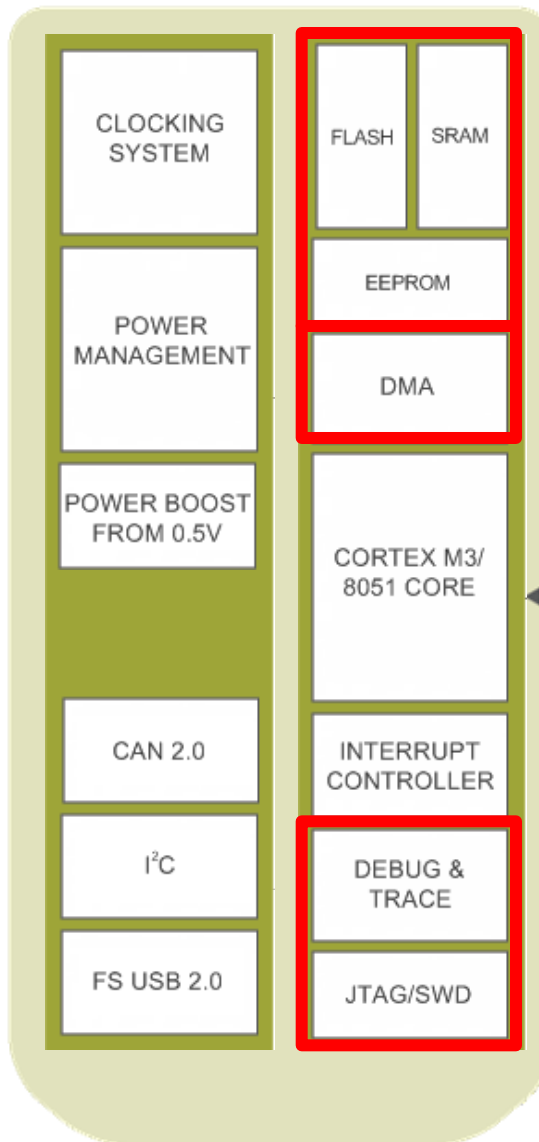
- Industry's leading embedded CPU company
- Broad support for middleware and applications
- Up to 80 MHz; 100 DMIPS
- Enhanced v7 ARM architecture:
  - Thumb2 Instruction Set
  - 16- and 32-bit Instructions (no mode switching)
  - 32-bit ALU; Hardware multiply and divide
- Single cycle 3-stage pipeline; Harvard architecture

## 8051

- Broad base of existing code and support
- Up to 67 MHz; 33 MIPS
- Single cycle instruction execution



# CPU Subsystem



## High Performance Memory

- Flash memory with ECC
- High ratio of SRAM to flash
- EEPROM

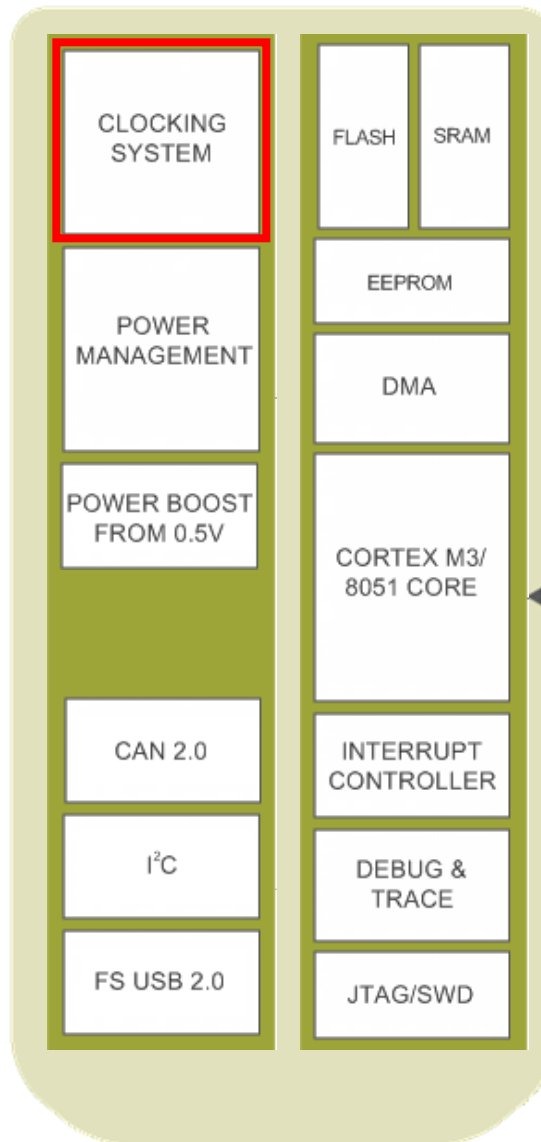
## Powerful DMA Engine

- 24-Channel Direct Memory Access
- Access to all Digital and Analog Peripherals
- CPU and DMA simultaneous access to independent SRAM blocks

## On-Chip Debug and Trace

- Industry standard JTAG/SWD (Serial Wire Debug)
- On chip trace
- NO MORE ICE

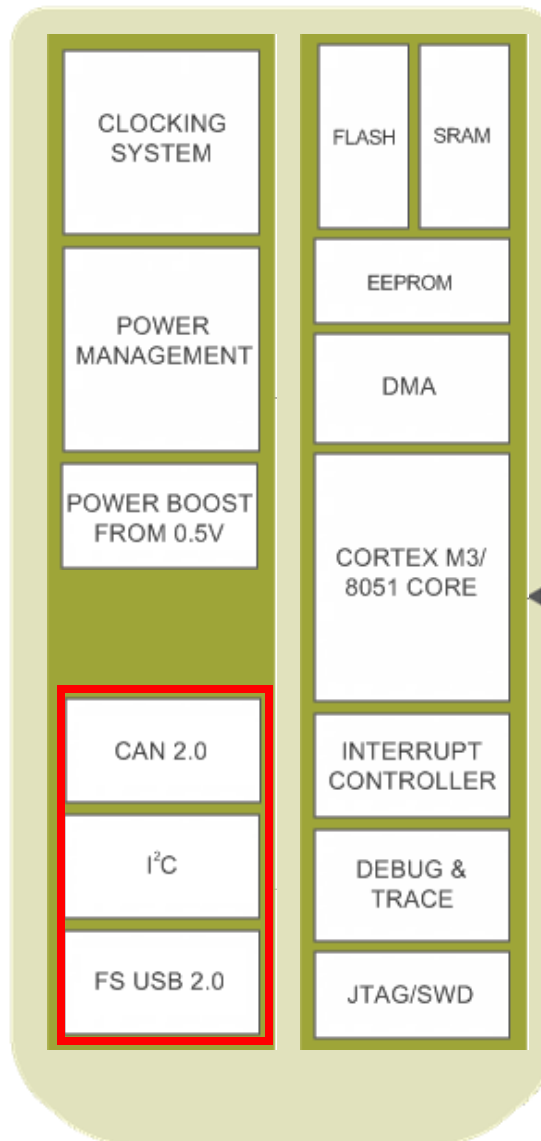
# CPU Subsystem



## Clocking System

- Many Clock Sources
  - Internal Main Oscillator
  - External clock crystal input
  - External clock oscillator inputs
  - Clock doubler output
  - Internal low speed oscillator
  - External 32 kHz crystal input
  - Dedicated 48 MHz USB clock
  - PLL output
- 16-bit Clock Dividers
  - 8 Digital
  - 4 Analog
- PSoC Creator Configuration Wizard
- PSoC Creator auto-derive clocking source/dividers

# CPU Subsystem



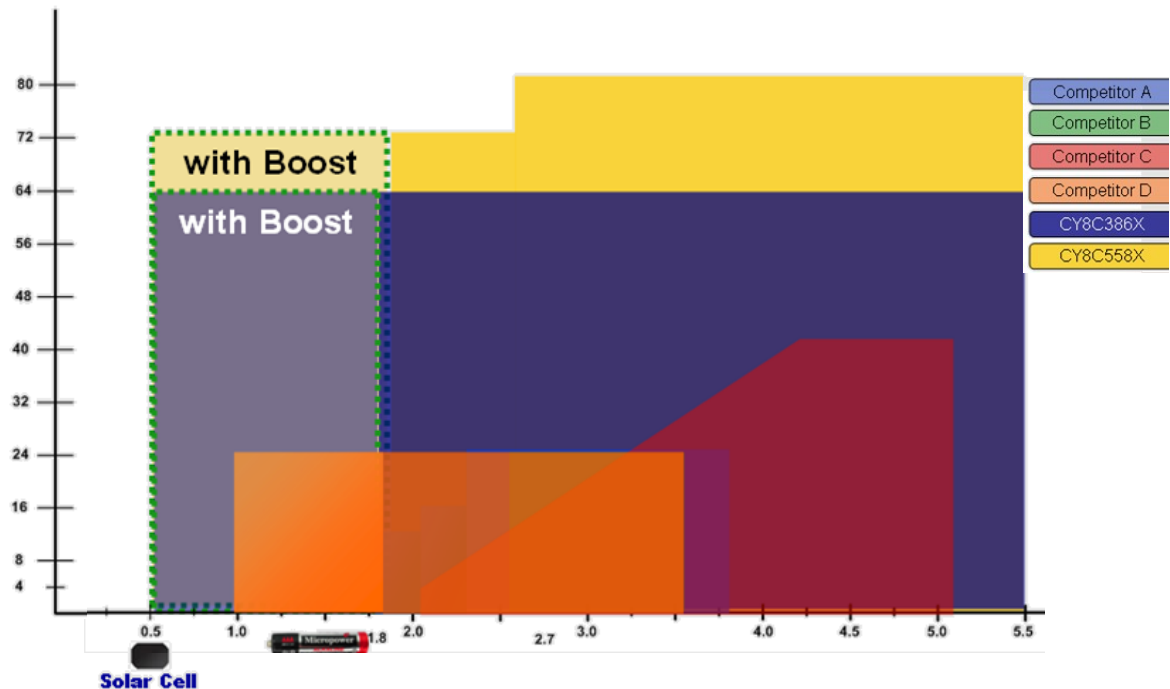
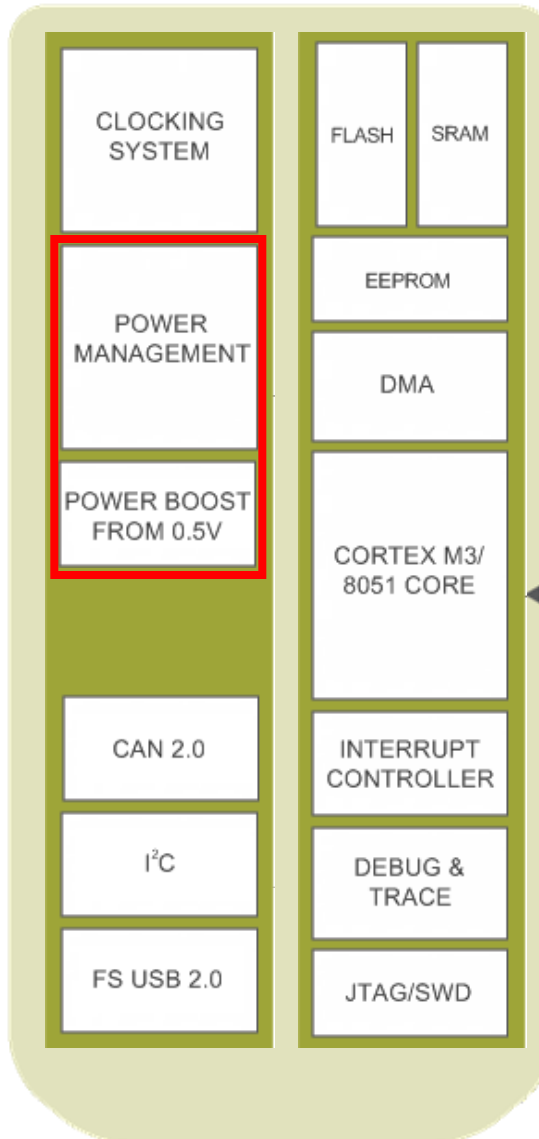
## Dedicated Communication Peripherals

- **Full Speed USB device**
  - 8 bidirectional data end points + 1 control end point
  - No external crystal required
  - Drivers in PSoC Creator for HID class devices
- **Full CAN 2.0b**
  - 16 RX buffers and 8 TX buffers
- **I2C master or slave**
  - Data rate up to 400 kbps
  - Additional I2C slaves may be implemented in UDB array
- New peripherals will be added as family members are added to the platform: Ethernet, HS USB, USB Host...

# CPU Subsystem

## Power Management

- Industry's Widest Operating Voltage
  - 0.5V to 5.5V with full analog/digital capability
- High Performance at 0.5V
  - PSoC 3 @ 67 MHz; PSoC 5 @ 72 MHz
- 3 Power Modes (Active, Sleep and Hibernate)



# Designed for Low Power/Low Voltage

## Highly configurable clock tree

Flexible, automated clock gating.

## On-board DMA Controller

Direct memory transfer between peripherals offloads CPU operation, lowering power consumption

## Cached Operations

Execution from flash memory is improved by caching instructions (PSoC 5 only)

## Precise CPU frequencies

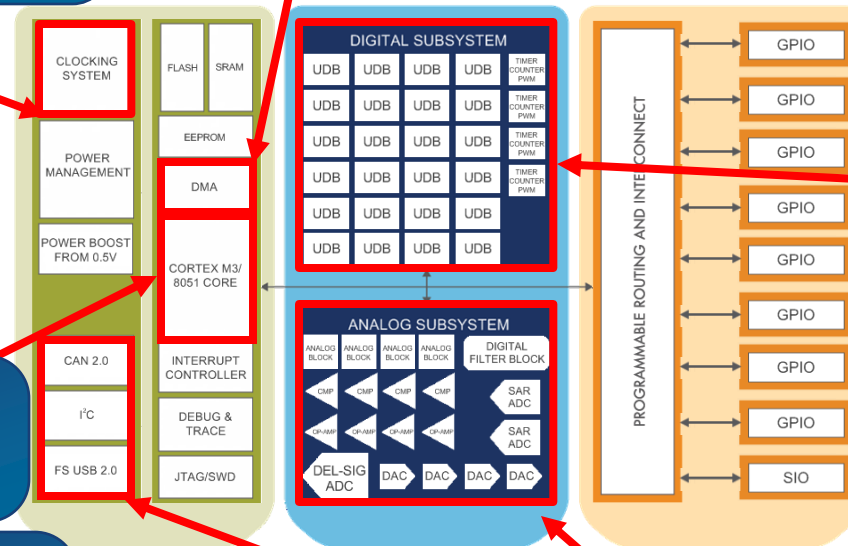
PLL allows 4,032 different frequencies; tunable power consumption

## Universal Digital Blocks

Implement features in hardware that reduce CPU processing requirements, lowering power consumption

## Integrated Analog, Digital and Communication Peripherals

Reduce external component counts and lower overall system power consumption



# Low Power Modes

Power mode	Current (PSoC 3)	Current (PSoC 5)	Code execution	Digital resources available	Analog resources available	Clock sources available	Wakeup sources	Reset sources
Active	1.2 mA @ 6MHz	2 mA @ 6MHz	Yes	All	All	All	N/A	All
Sleep	1 uA	2 uA	No	I2C	Comparator	Low Speed and 32 kHz Osc	IO, I2C, RTC, sleep timer, comparator	XRES, LVD, WDR
Hibernate	200 nA	300 nA	No	None	None	None	IO	XRES, LVD

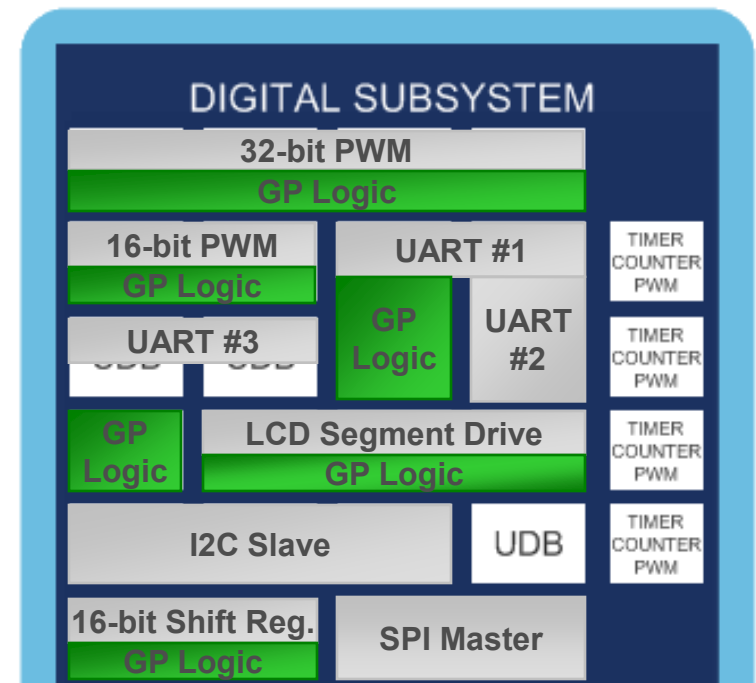
## Power Management Enabled in PSoC Creator

- Provides easy to use control APIs for quick power management
- Allows code and register manipulation for in-depth control

# Digital Subsystem

## Universal Digital Block Array (UDBs)

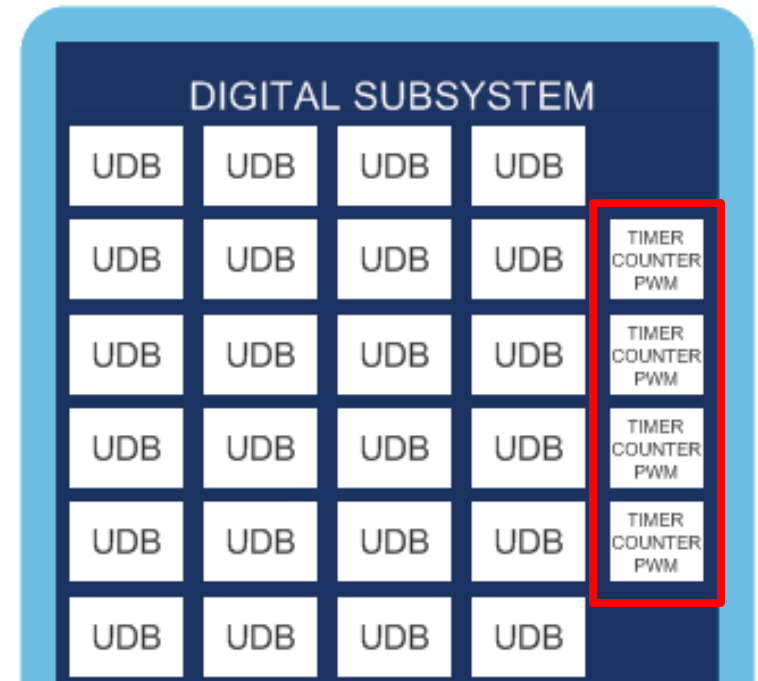
- Flexibility of a PLD integrated with a CPU
- Provides hardware capability to implement components from a rich library of pre-built, documented, and characterized components in PSoC Creator
- PSoC Creator will synthesize, place, and route components automatically.
- Fine configuration granularity enables high silicon utilization
- DSI routing mesh allows any function in the UDBs to communicate with any other on-chip function/GPIO pin with 8- to 32-bit data buses



# Digital Subsystem

## Optimized 16-bit Timer/Counter/PWM Blocks

- Provides nearly all of the features of a UDB based timer, counter, or PWM
- PSoC Creator provides easy access to these flexible blocks
- Each block may be configured as either a full featured 16-bit Timer, Counter, or PWM
- Programmable options
  - Clock, enable, reset, capture, kill from any pin or digital signal on chip
  - Independent control of terminal count, interrupt, compare, reset, enable, capture, and kill synchronization
- Plus
  - Configurable to measure pulse widths or periods
  - Buffered PWM with dead band and kill

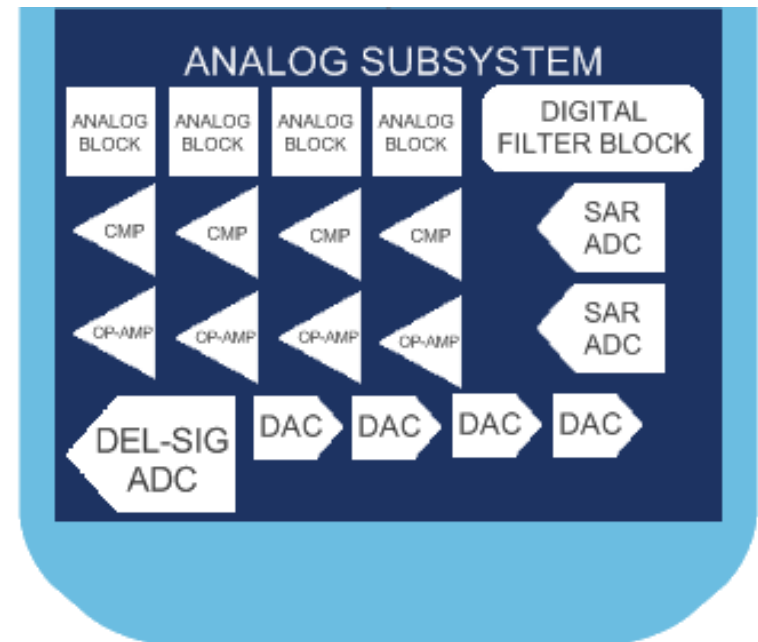




# Analog Subsystem

## Configurable Analog System

- Flexible Routing: All GPIO are Analog Input/Output
- +/- 0.1% Internal Reference Voltage
- Delta-Sigma ADC: Up to 20-bit resolution
  - 16-bit at 48 ksp/s or 12-bit at 192 ksp/s
- SAR ADC: 12-bit at 1 Msps
- DACs: 8 – 10-bit resolution, current and voltage mode
- Low Power Comparators
- Opamps (25 mA output buffers)
- Programmable Analog Blocks
  - Configurable PGA (up to x50), Mixer, Trans-Impedance Amplifier, Sample and Hold
- Digital Filter Block: Implement HW IIR and FIR filters
- CapSense Touch Sensing enabled



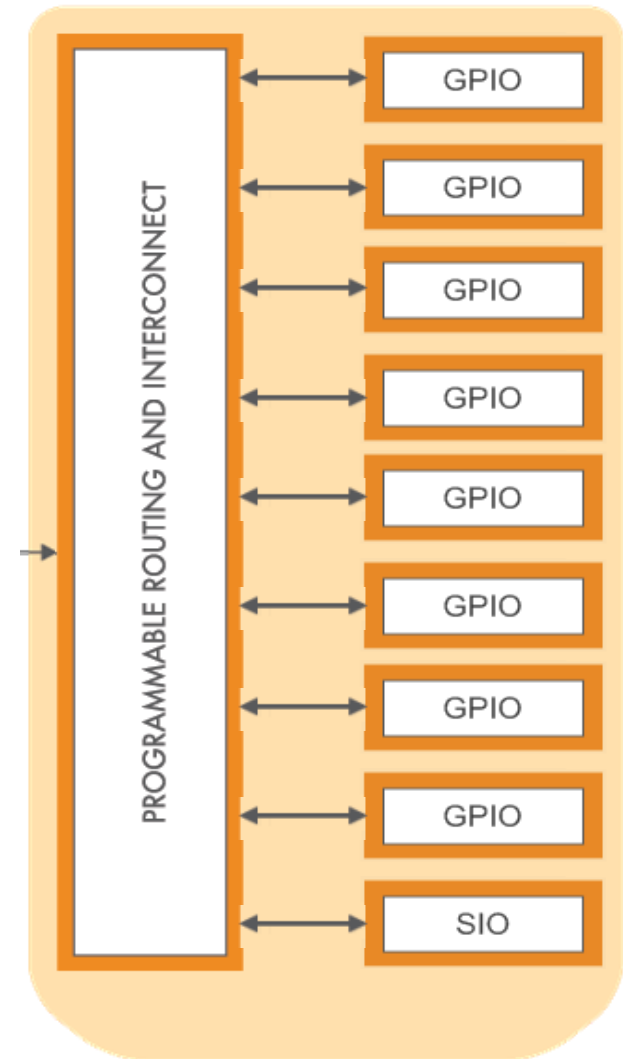
# Programmable Routing/Interconnect

## Input / Output System

- Three types of I/O
  - GPIO, SIO, USBIO
- Any GPIO to any peripheral routing
- Wakeup on analog, digital or I2C match
- Programmable slew rate reduces power and noise
- 8 different configurable drive modes
- Programmable input threshold capability for SIO
- Auto and custom/lock-able routing in PSoC Creator

## Up to 4 separate I/O voltage domains

- Interface with multiple devices using one PSoC 3 / PSoC 5 device



# Supported Compilers

- Free Bundled compiler options

- PSoC 3: Cypress-Edition Keil™ CA51 Compiler Kit
- PSoC 5: GNU/CodeSourcery Sourcery G++™ Lite
- No code size restrictions, not board-locked, no time limit
- Fully integrated including full debugging support



- Upgrade, more optimization/compiler-support options

- PSoC 3: Keil CA51™ Compiler Kit
- PSoC 5: Keil RealView® Microcontroller Development Kit
- Higher levels of optimization
- Direct support from the compiler vendor

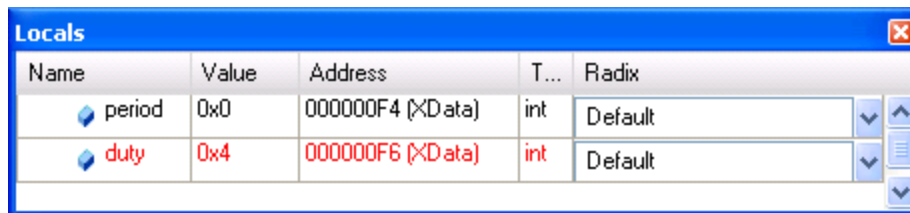
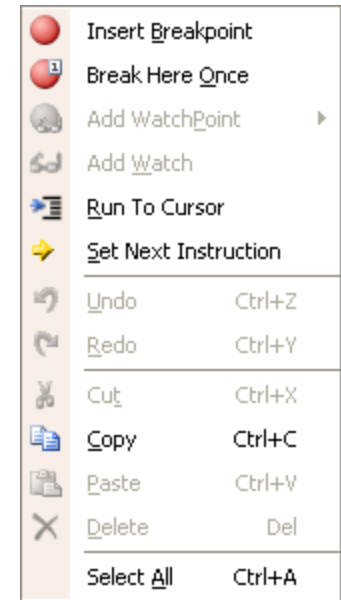


- Upgrade Compiler Pricing

- Set and managed by our 3rd party partner, Keil
- Already own these compilers? No need to buy another license!
- Keil CA51 Compiler Kit ~\$2,000
- Keil RealView MDK ~\$3,000-5,000

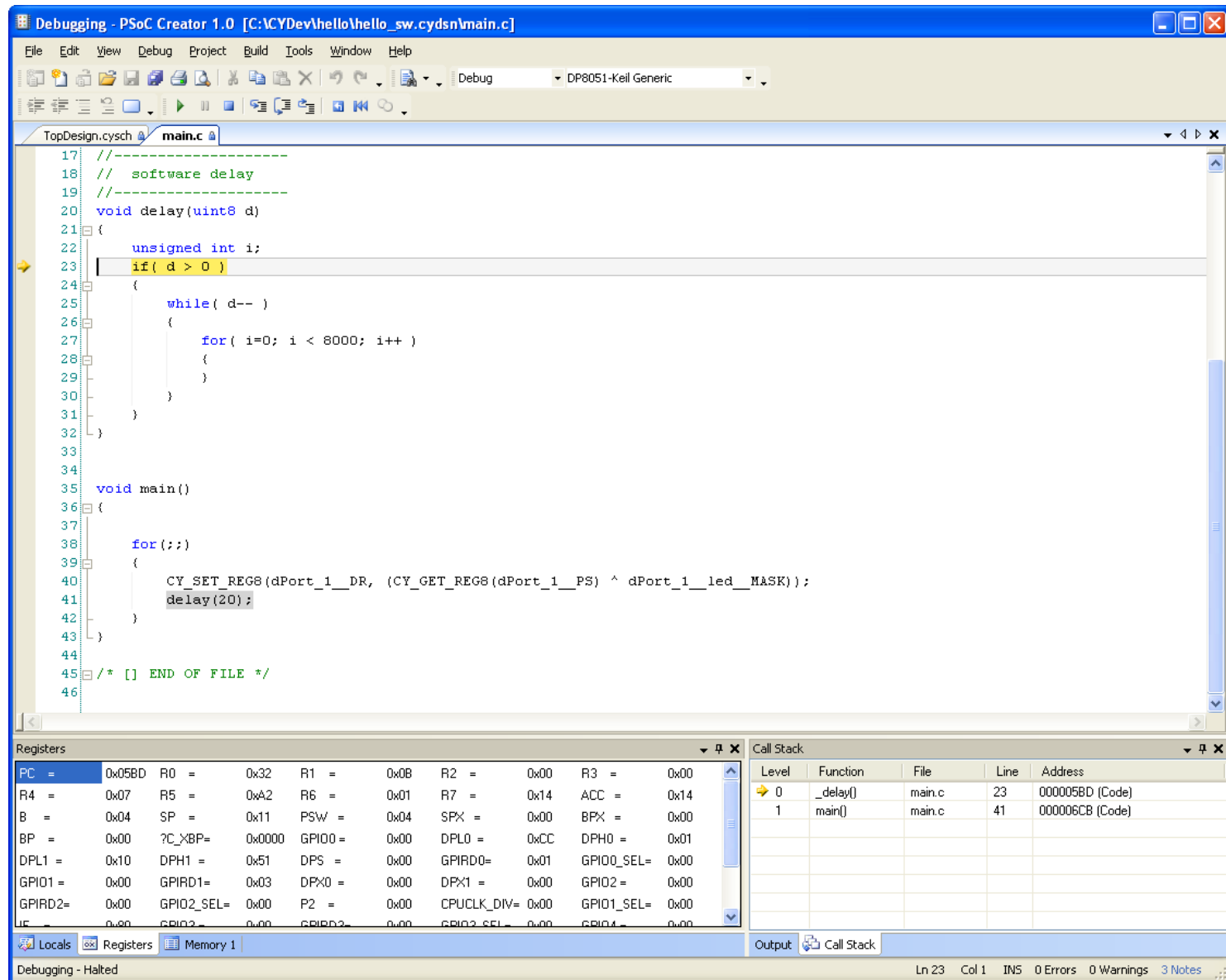
# Integrated Debugger

- JTAG and SWD connection
- All devices support debug
- MiniProg3 programmer / debugger
- Control execution with menus, buttons and keys
- Full set of debug windows
  - Locals, register, call stack, watch (4), memory (4)
  - C source and assembler
  - Components
- Set breakpoints in Source Editor



Name	Value	Address	T...	Radix
period	0x0	000000F4 (XData)	int	Default
duty	0x4	000000F6 (XData)	int	Default

# Debugger Windows



Debugging - PSoC Creator 1.0 [C:\CYDev\hello\hello\_sw.cydsn\main.c]

File Edit View Debug Project Build Tools Window Help

Debug DP8051-Keil Generic

TopDesign.cysch main.c

```
17 //-----
18 // software delay
19 //-----
20 void delay(uint8 d)
21 {
22     unsigned int i;
23     if( d > 0 )
24     {
25         while( d-- )
26         {
27             for( i=0; i < 8000; i++ )
28             {
29             }
30         }
31     }
32 }
33
34
35 void main()
36 {
37
38     for(;;)
39     {
40         CY_SET_REG8(dPort_1_DR, (CY_GET_REG8(dPort_1_PS) ^ dPort_1_led_MASK));
41         delay(20);
42     }
43 }
44
45 /* [] END OF FILE */
46
```

Registers

Register	Value
PC	0x05BD
R0	0x32
R1	0x08
R2	0x00
R3	0x00
R4	0x07
R5	0xA2
R6	0x01
R7	0x14
ACC	0x14
B	0x04
SP	0x11
PSW	0x04
SPX	0x00
BFX	0x00
BP	0x00
?C_XBP	0x0000
GPI00	0x00
DPL0	0xCC
DPH0	0x01
DPL1	0x10
DPH1	0x51
DPS	0x00
GPIRD0	0x01
GPI00_SEL	0x00
GPI01	0x00
GPIRD1	0x03
DPX0	0x00
DPX1	0x00
GPI02	0x00
GPIRD2	0x00
GPI02_SEL	0x00
P2	0x00
CPUCLK_DIV	0x00
GPI01_SEL	0x00
UF	0x00
GPI03	0x00
GPIRD3	0x00
GPI03_SEL	0x00
GPI04	0x00

Call Stack

Level	Function	File	Line	Address
0	_delay()	main.c	23	000005BD (Code)
1	main()	main.c	41	000006CB (Code)

Locals Registers Memory 1

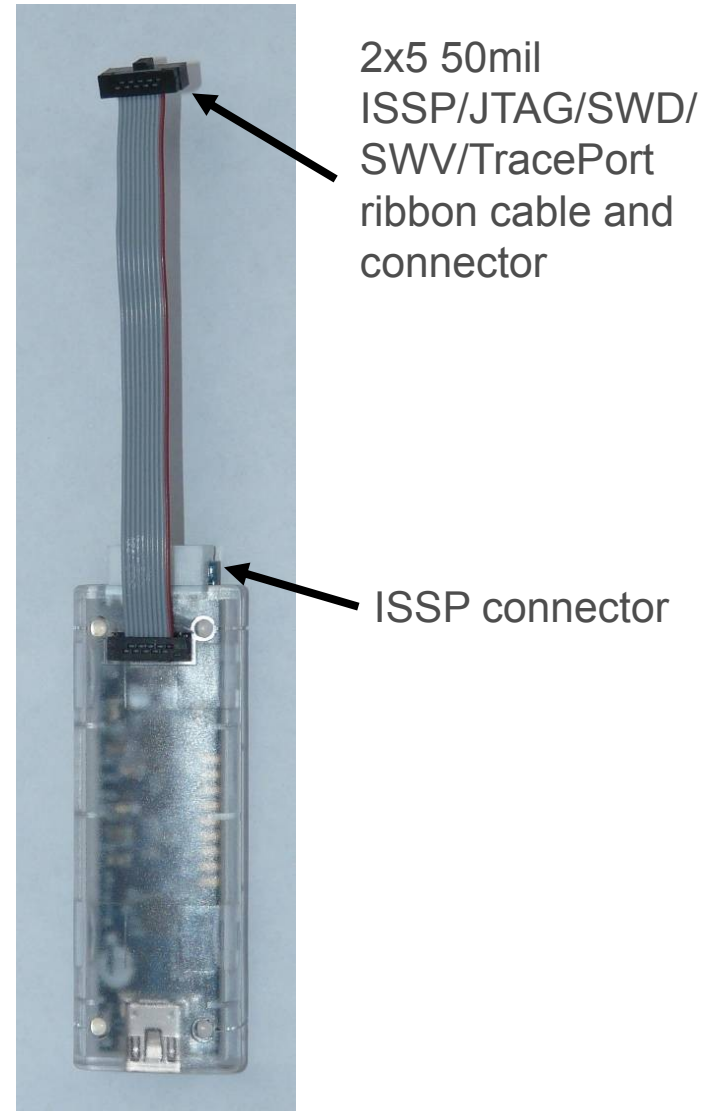
Debugging - Halted

Ln 23 Col 1 INS 0 Errors 0 Warnings 3 Notes

# MiniProg3

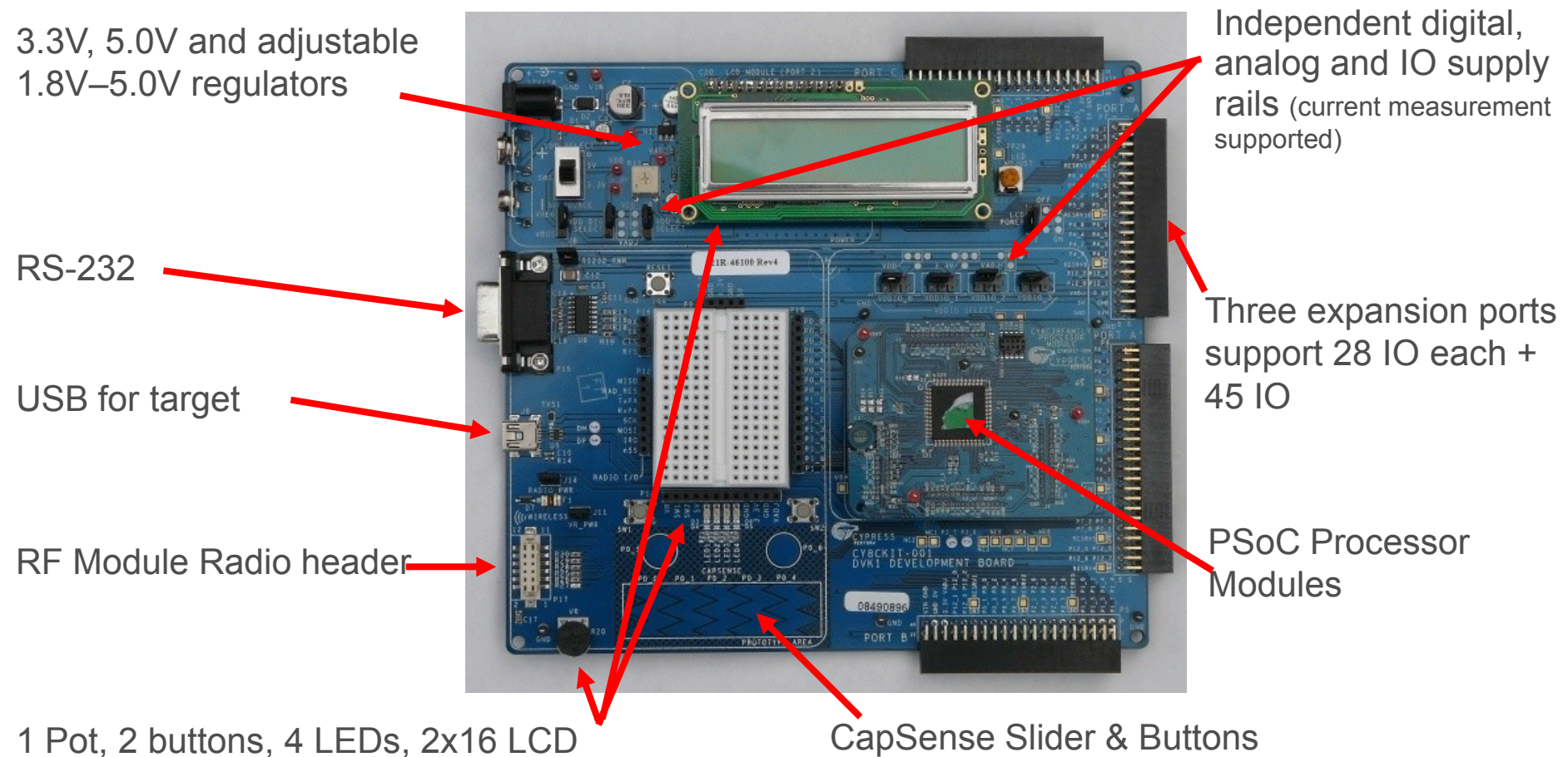
- Program PSoC 1 devices
- Program/Debug PSoC 3 / PSoC 5 devices
- Standard 50mil connector
- nTRST/XRES pin is used as the device reset (XRES) by default
- nTRST is JTAG specific and rarely used

Features	MiniProg	MiniProg3
ISSP connector (5-pin)	Yes	Yes
Issp protocol (PSoC1)	Yes	Yes
JTAG/SWD connector with ribbon cable	No	Yes
JTAG/SWD protocol	No	Yes
SWV protocol	No	Yes
ARM Cortex M3 trace port	No	Yes
Match ISSP, JTAG, SWD voltage to IOs	No	Yes
Target Supply (100ma limit)	5.0V	1.8V-5.0V
USB bus speed	Full	High



# PSoC Development Kit (CY8CKIT-001)

- Supports all PSoC architectures via processor modules
- Integrated support of all required and optional chip connections
- MiniProg3 should not supply power to PSoC Development Kit



# PSoC Architecture Comparison

Features	PSoC 1	PSoC 3	PSoC 5
Interface	SPI, UART, GPIO, FS-USB, I2C	PSoC1 + CAN, I2S	Same as PSoC 3
Inputs	Sensors, CapSense, Touchscreen, Analog	PSoC1 + Precision Analog	PSoC1 + High speed Analog
Outputs	LED control, Motor control, Analog buffers	PSoC1 + LCD segment drive, LED drive, advanced motor control	PSoC1 + QVGA LCD control
Processing	M8 24 MHz	8051 67 MHz	ARM® Cortex -M3™ 80 MHz



# PSoC 1 Architecture

	Features	PSOC 1
Configurable Analog / Digital	ADC	1 Delta-Sigma (6- to 14-bit)
	Sample Rate	Up to 31 KSPS (8-bit)
	Reference Voltage Accuracy	±1.53%
	DACs	Up to 2 (6- to 8-bit)
	PGA	x1 to x48
	LCD Segment Drive	Control
	Integrate Programmable Logic	No
	CapSense & Touchscreen	Up to 44 Buttons and 8 Sliders

# PSoC 1 Architecture

	Features	PSOC 1
CPU Subsystem	CPU	M8C
	CPU Performance	24 MHz, 4 MIPS
	Flash	4 KB to 32 KB
	SRAM	256B to 2 KB
	Operating Range	1.7V to 5.25V
	Power Consumption (Active@6MHz)	Active:2mA, Sleep:3uA
	Connectivity Resources	FS USB 2.0, I2C, SPI, UART

# PSoC 1 Architecture

	Features	PSOC 1
Programmable Interconnect	Routing & Matrix	Manual Routing, Configurable
	# IO	Up to 64
Tools	Software Development Tools	PSoC Designer and 3rd party compilers
	In-Circuit Emulation and Debug	Requires ICE Cube and FlexPods (Bond Out)

# PSoC 3 & 5 Architecture

Features	PSOC 3	PSOC 5
ADC	1 Delta-Sigma (12- to 20-bit)	1 Delta-Sigma (12- to 20-bit); 2-SAR ADC (12-bit)
Sample Rate	192 KSPS (12-bit)	192 KSPS (12-bit) Delta-Sigma; 1 MSPS (12-bit) SAR ADC
Reference Voltage Accuracy	Industrial $\pm 0.1\%$	Industrial $\pm 0.1\%$
DACs	Up to 4 (8-bit)	Up to 2 (8-bit) and 1 (12-bit)
PGA	x1 to x50	x1 to x50
LCD Segment Drive	Control + Drive (736 segments)	Control + Drive (736 segments)
Integrate Programmable Logic	Yes	Yes
CapSense & Touchscreen	Up to 62 Buttons and 12 Sliders	Up to 62 Buttons and 12 Sliders

# PSoC 3 & 5 Architecture

Features	PSOC 3	PSOC 5
CPU	Advanced 8051 (1CPI)	ARM Cortex-M3
CPU Performance	67 MHz, 33 MIPS	80 MHz, 100 DMIPS
Flash	8 KB to 64 KB	32 KB to 256 KB
SRAM	2 KB to 8 KB	16 KB to 64 KB
Operating Range	0.5V to 5.5V	0.5V to 5.5V
Power Consumption (Active@6MHz)	Active:1mA, Sleep:1uA, Hibernate:200nA)	Active:2mA, Sleep:2uA, Hibernate:300nA
Connectivity Resources	FS USB 2.0, I2C, SPI, UART, CAN, LIN, I2S	FS USB 2.0, I2C, SPI, UART, CAN, LIN, I2S

# PSoC 3 & 5 Architecture

Features	PSOC 3	PSOC 5
Routing & Matrix	Automatic; Any pin anywhere	Automatic; Any pin anywhere
# IO	Up to 72	Up to 72
Software Development Tools	PSoC Creator and 3rd party Compilers/IDEs	PSoC Creator and 3rd party Compilers/IDEs
In-Circuit Emulation and Debug	On-chip JTAG, Debug and Trace	On-chip JTAG, Debug and Trace

# Bibliography

- ❑ Cypress Semiconductor Power Point Slides
- ❑ Cypress Semiconductor Product Brochure