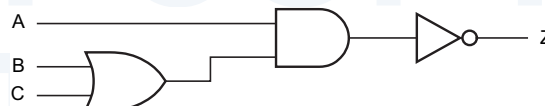


- 3.56 For each of the following resistive loads, determine whether the output drive specifications of the 74LS00 over the commercial operating range are exceeded. (Refer to Table 3-12, and use $V_{OLmax} = 0.5$ V and $V_{CC} = 5.0$ V.)
- (a) $470\ \Omega$ to V_{CC} (b) $330\ \Omega$ to V_{CC} and $470\ \Omega$ to GND
 - (c) $10\ K\Omega$ to GND (d) $390\ \Omega$ to V_{CC} and $390\ \Omega$ to GND
 - (e) $600\ \Omega$ to V_{CC} (f) $510\ \Omega$ to V_{CC} and $510\ \Omega$ to GND
 - (g) $4.7\ K\Omega$ to GND (h) $220\ \Omega$ to V_{CC} and $330\ \Omega$ to GND
- 3.57 Compute the LOW-state and HIGH-state DC noise margins for each of the following cases of a TTL output driving a TTL-compatible CMOS input, or vice versa.
- (a) 74HCT driving 74LS (b) 74VHCT driving 74AS
 - (c) 74LS driving 74HCT (d) 74S driving 74VHCT
- 3.58 Compute the maximum fanout for each of the following cases of a TTL-compatible CMOS output driving multiple inputs in a TTL logic family. Also indicate how much “excess” driving capability is available in the LOW or HIGH state for each case.
- (a) 74HCT driving 74LS (b) 74HCT driving 74S
 - (c) 74VHCT driving 74AS (d) 74VHCT driving 74LS
- 3.59 For a given load capacitance and transition rate, which logic family in this chapter has the lowest dynamic power dissipation?

Exercises

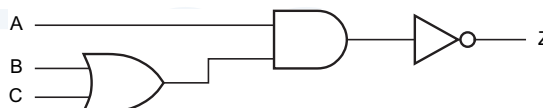
- 3.60 Design a CMOS circuit that has the functional behavior shown in Figure X3.60. (Hint: Only six transistors are required.)

Figure X3.60



- 3.61 Design a CMOS circuit that has the functional behavior shown in Figure X3.61. (Hint: Only six transistors are required.)

Figure X3.61



- 3.62 Draw a circuit diagram, function table, and logic symbol in the style of Figure 3-19 for a CMOS gate with two inputs A and B and an output Z, where $Z = 1$ if $A = 0$ and $B = 1$, and $Z = 0$ otherwise. (Hint: Only six transistors are required.)
- 3.63 Draw a circuit diagram, function table, and logic symbol in the style of Figure 3-19 for a CMOS gate with two inputs A and B and an output Z, where

- $Z = 0$ if $A = 1$ and $B = 0$, and $Z = 1$ otherwise. (*Hint:* Only six transistors are needed.)
- 3.64 Draw a figure showing the logical structure of an 8-input CMOS NOR gate, assuming that at most 4-input gate circuits are practical. Using your general knowledge of CMOS electrical characteristics, select a circuit structure that minimizes the NOR gate's propagation delay for a given area of silicon, and explain why this is so.
 - 3.65 The circuit designers of TTL-compatible CMOS families presumably could have made the voltage drop across the "on" transistor under load in the HIGH state as little as it is in the LOW state, simply by making the p -channel transistors bigger. Why do you suppose they didn't bother to do this?
 - 3.66 How much current and power are "wasted" in Figure 3-32(b)?
 - 3.67 Perform a detailed calculation of V_{OUT} in Figures 3-34 and 3-33. (*Hint:* Create a Thévenin equivalent for the CMOS inverter in each figure.)
 - 3.68 Consider the dynamic behavior of a CMOS output driving a given capacitive load. If the resistance of the charging path is double the resistance of the discharging path, is the rise time exactly twice the fall time? If not, what other factors affect the transition times?
 - 3.69 Analyze the fall time of the CMOS inverter output of Figure 3-37, assuming that $R_L = 1 \text{ k}\Omega$ and $V_L = 2.5 \text{ V}$. Compare your answer with the results of Section 3.6.1 and explain.
 - 3.70 Repeat Exercise 3.68 for rise time.
 - 3.71 Assuming that the transistors in an FCT CMOS three-state buffer are perfect, zero-delay on-off devices that switch at an input threshold of 1.5 V, determine the value of t_{PLZ} for the test circuit and waveforms in Figure 3-24. (*Hint:* You have to determine the time using an RC time constant.) Explain the difference between your result and the specifications in Table 3-3.
 - 3.72 Repeat Exercise 3.70 for t_{PHZ} .
 - 3.73 Using the specifications in Table 3-6, estimate the "on" resistances of the p -channel and n -channel transistors in 74AC-series CMOS logic.
 - 3.74 Create a $4 \times 4 \times 2 \times 2$ matrix of worst-case DC noise margins for the following CMOS interfacing situations: an (HC, HCT, VHC, or VHCT) output driving an (HC, HCT, VHC, or VHCT) input with a (CMOS, TTL) load in the (LOW, HIGH) state; Figure X3.74 illustrates. (*Hints:* There are 64 different combinations to examine, but many give identical results. Some combinations yield negative margins.)
 - 3.75 In the LED example in Section 3.7.5, a designer chose a resistor value of 300Ω , and found that the open-drain gate was able to maintain its output at 0.1 V while driving the LED. How much current flows through the LED, and how much power is dissipated by the pull-up resistor in this case?
 - 3.76 Consider a CMOS 8-bit binary counter (Section 8.4) clocked at 16 MHz. For the purposes of computing dynamic power dissipation, what is the transition frequency of least significant bit? Of the most significant bit? For the purposes of

Figure X3.74

Output	Input							
	HC		HCT		VHC		VHCT	
HC	CL	TL	CL	TL	CL	TL	CL	TL
	CH	TH	CH	TH	CH	TH	CH	TH
HCT	CL	TL	CL	TL	CL	TL	CL	TL
	CH	TH	CH	TH	CH	TH	CH	TH
VHC	CL	TL	CL	TL	CL	TL	CL	TL
	CH	TH	CH	TH	CH	TH	CH	TH
VHCT	CL	TL	CL	TL	CL	TL	CL	TL
	CH	TH	CH	TH	CH	TH	CH	TH

Key:

CL = CMOS load, LOW

CH = CMOS load, HIGH

TL = TTL load, LOW

TH = TTL load, HIGH

determining the dynamic power dissipation of the eight output bits, what frequency should be used?

- 3.77 Using only AND and NOR gates, draw a logic diagram for the logic function performed by the circuit in Figure 3-55.
- 3.78 Calculate the approximate output voltage at Z in Figure 3-56, assuming that the gates are HCT-series CMOS.
- 3.79 Redraw the circuit diagram of a CMOS 3-state buffer in Figure 3-48 using actual transistors instead of NAND, NOR, and inverter symbols. Can you find a circuit for the same function that requires a smaller total number of transistors? If so, draw it.
- 3.80 Modify the CMOS 3-state buffer circuit in Figure 3-48 so that the output is in the High-Z state when the enable input is HIGH. The modified circuit should require no more transistors than the original.
- 3.81 Using information in Table 3-3, estimate how much current can flow through each output pin when the outputs of two different 74FCT257Ts are fighting.
- 3.82 A computer system made by the Green PC Company had ten LED “status OK” indicators, each of which was turned on by an open-collector output in the style of Figure 3-52. However, in order to save a few cents, the logic designer connected the anodes of all ten LEDs together and replaced the ten, now parallel, 300- Ω pull-up resistors with a single 30- Ω resistor. This worked fine in the lab, but a big problem was found after volume shipments began. Explain.
- 3.83 Show that at a given power-supply voltage, an FCT-type I_{CCD} specification can be derived from an HCT/ACT-type C_{PD} specification, and vice versa.
- 3.84 If both V_Z and $V_{_B}$ in Figure 3-65(b) are 4.6 V, can we get $V_C = 5.2$ V? Explain.
- 3.85 Modify the program in Table 3-10 to account for leakage current in the OFF state.
- 3.86 Assuming “ideal” conditions, what is the minimum voltage that will be recognized as a HIGH in the TTL NAND gate in Figure 3-75 with one input LOW and the other HIGH?
- 3.87 Assuming “ideal” conditions, what is the maximum voltage that will be recognized as a LOW in the TTL NAND gate in Figure 3-75 with both inputs HIGH?
- 3.88 Find a commercial TTL part that can source 40 mA in the HIGH state. What is its application?

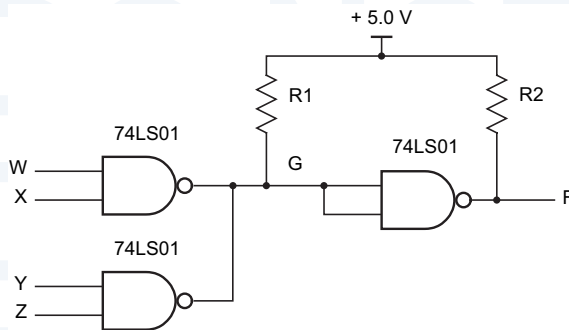


Figure X3.92

- 3.89 What happens if you try to drive an LED with its cathode grounded and its anode connected to a TTL totem-pole output, analogous to Figure 3-53 for CMOS?
- 3.90 What happens if you try to drive a 12-volt relay with a TTL totem-pole output?
- 3.91 Suppose that a single pull-up resistor to +5 V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much HIGH-state DC noise margin are you providing in this case?
- 3.92 The circuit in Figure X3.92 uses open-collector NAND gates to perform “wired logic.” Write a truth table for output signal F and, if you’ve read Section 4.2, a logic expression for F as a function of the circuit inputs.
- 3.93 What is the maximum allowable value for $R1$ in Figure X3.92? Assume that a 0.7 V HIGH-state noise margin is required. The 74LS01 has the specs shown in the 74LS column of Table 3-11, except that I_{OHmax} is $100\ \mu A$, a leakage current that flows *into* the output in the HIGH state.
- 3.94 A logic designer found a problem in a certain circuit’s function after the circuit had been released to production and 1000 copies of it built. A portion of the circuit is shown in Figure X3.94 in black; all of the gates are 74LS00 NAND gates. The logic designer fixed the problem by adding the two diodes shown in color. What do the diodes do? Describe both the logical effects of this change on the circuit’s function and the electrical effects on the circuit’s noise margins.

Figure X3.94

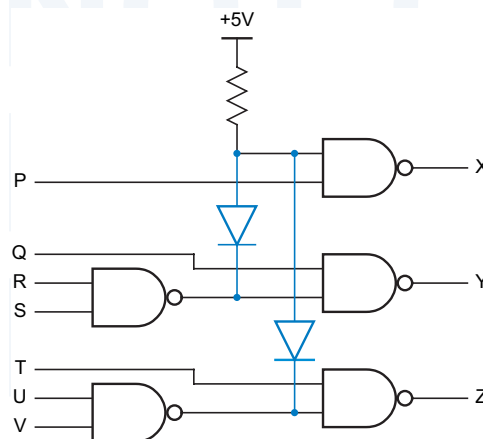
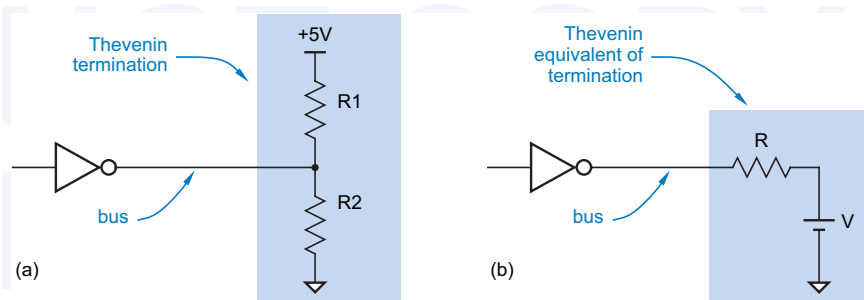


Figure X3.95



- 3.95 A Thévenin termination for an open-collector or three-state bus has the structure shown in Figure X3.95(a). The idea is that, by selecting appropriate values of $R1$ and $R2$, a designer can obtain a circuit equivalent to the termination in (b) for any desired values of V and R . The value of V determines the voltage on the bus when no device is driving it, and the value of R is selected to match the characteristic impedance of the bus for transmission-line purposes (Section 12.4). For each of the following pairs of V and R , determine the required values of $R1$ and $R2$.
- (a) $V = 2.75$, $R = 148.5$ (b) $V = 2.7$, $R = 180$
 (c) $V = 3.0$, $R = 130$ (d) $V = 2.5$, $R = 75$
- 3.96 For each of the $R1$ and $R2$ pairs in Exercise 3.95, determine whether the termination can be properly driven by a three-state output in each of the following logic families: 74LS, 74S, 74ACT. For proper operation, the family's I_{OL} and I_{OH} specs must not be exceeded when $V_{OL} = V_{OLmax}$ and $V_{OH} = V_{OHmin}$, respectively.
- 3.97 Suppose that the output signal F in Figure 3.92 drives the inputs of two 74S04 inverters. Compute the minimum and maximum allowable values of $R2$, assuming that a 0.7 V HIGH-state noise margin is required.
- 3.98 A 74LS125 is a buffer with a three-state output. When enabled, the output can sink 24 mA in the LOW state and source 2.6 mA in the HIGH state. When disabled, the output has a leakage current of $\pm 20 \mu A$ (the sign depends on the output voltage—plus if the output is pulled HIGH by other devices, minus if it's LOW). Suppose a system is designed with multiple modules connected to a bus, where each module has a single 74LS125 to drive the bus, and one 74LS04 to receive information on the bus. What is the maximum number of modules that can be connected to the bus without exceeding the 74LS125's specs?
- 3.99 Repeat Exercise 3.97, this time assuming that a single pull-up resistor is connected from the bus to +5 V to guarantee that the bus is HIGH when no device is driving it. Calculate the maximum possible value of the pull-up resistor, and the number of modules that can be connected to the bus.
- 3.100 Find the circuit design in a TTL data book for an actual three-state gate, and explain how it works.
- 3.101 Using the graphs in a TTL data book, develop some rules of thumb for derating the maximum propagation delay specification of LS-TTL under nonoptimal conditions of power-supply voltage, temperature, and loading.

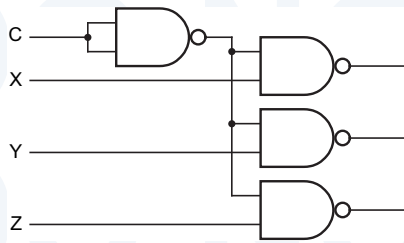


Figure X3.102

- 3.102 Determine the total power dissipation of the circuit in Figure 3.102 as function of transition frequency f for two realizations: (a) using 74LS gates; (b) using 74HC gates. Assume that input capacitance is 3 pF for a TTL gate and 7 pF for a CMOS gate, that a 74LS gate has an internal power dissipation capacitance of 20 pF, and that there is an additional 20 pF of stray wiring capacitance in the circuit. Also assume that the X, Y, and Z inputs are always HIGH, and that input C is driven with a CMOS-level square wave with frequency f . Other information that you need for this problem can be found in Tables 3-5 and 3-11. State any other assumptions that you make. At what frequency does the TTL circuit dissipate less power than the CMOS circuit?
- 3.103 It is possible to drive one or more 74AC or 74HC inputs reliably with a 74LS TTL output by providing an external resistor to pull the TTL output all the way up to V_{CC} in the HIGH state. What are the design issues in choosing a value for this pull-up resistor?

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