Introduction to Data Converters

DAC
INTRODUCTION

Digital-Analog Converters

- Characteristics:
  - Can be asynchronous or synchronous
  - Primary active element is the op amp
  - Conversion time can vary from fast (one clock period, T) to slow ($2^{\text{No. of bits}} * T$)

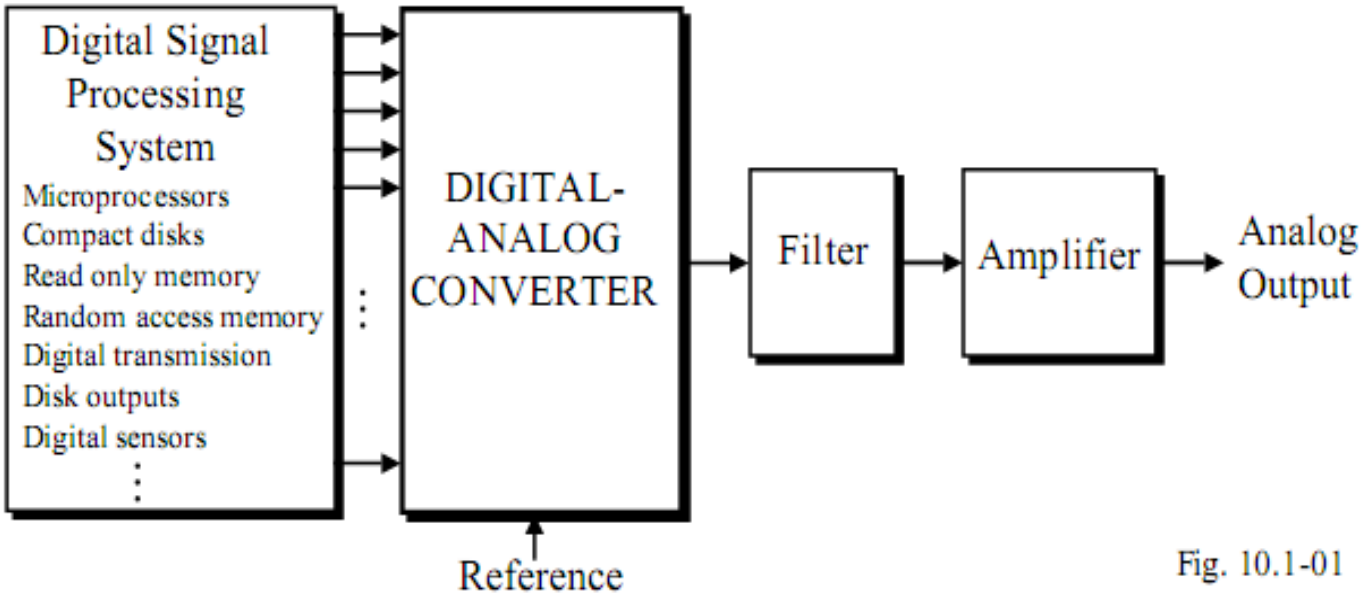
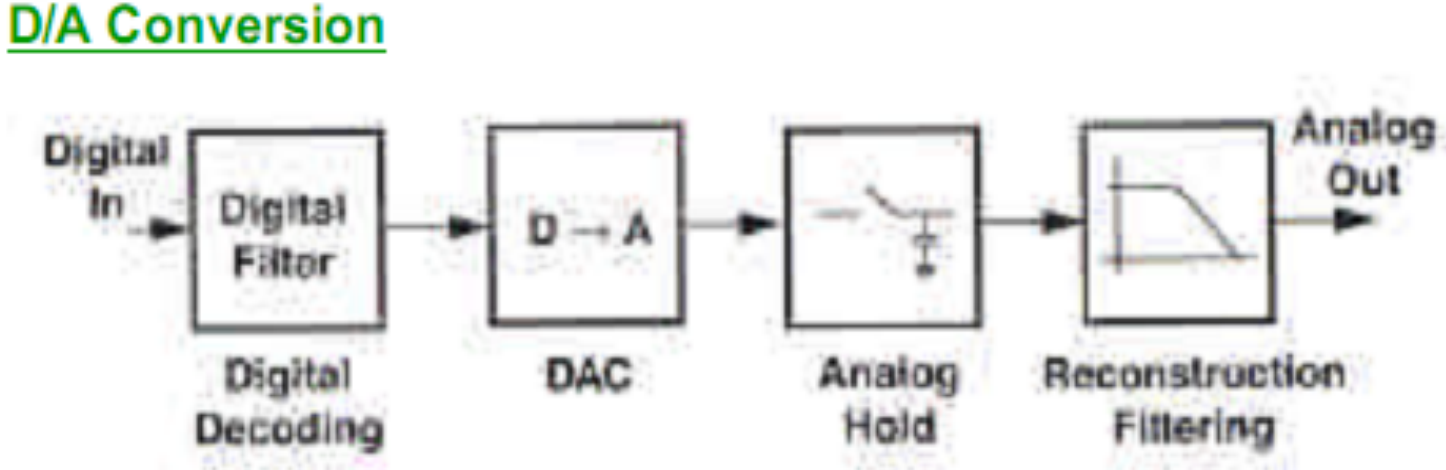
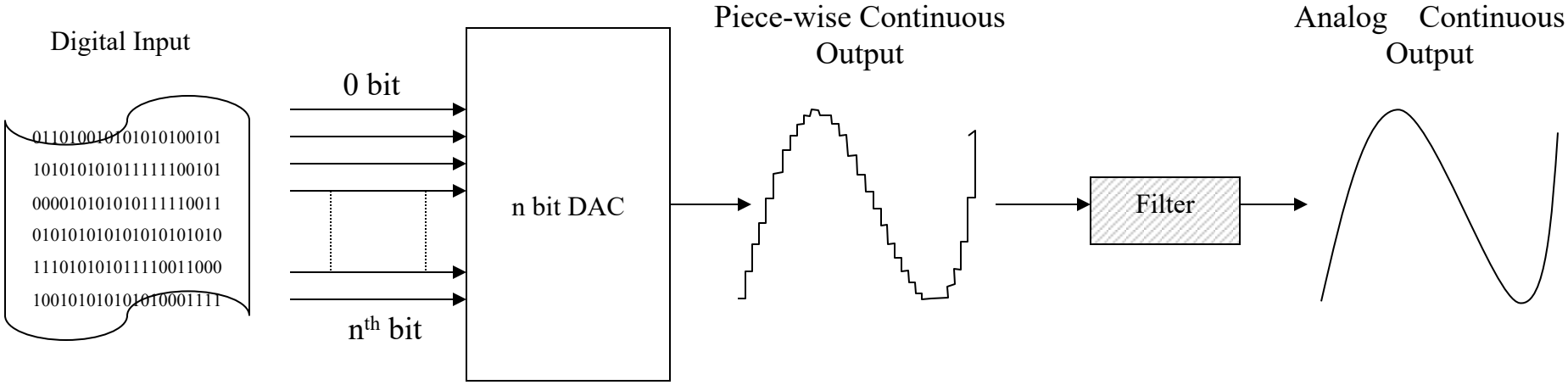


Fig. 10.1-01

Common Applications

- Used when a continuous analog signal is required.
- Signal from DAC can be smoothed by a Low pass filter





Block Diagram of a DAC

Block Diagram of a Digital-Analog Converter

Typical Output

DACs capture and hold a number, convert it to a physical signal, and hold that value for a given sample interval. This is known as a zero-order hold and results in a piecewise constant output.

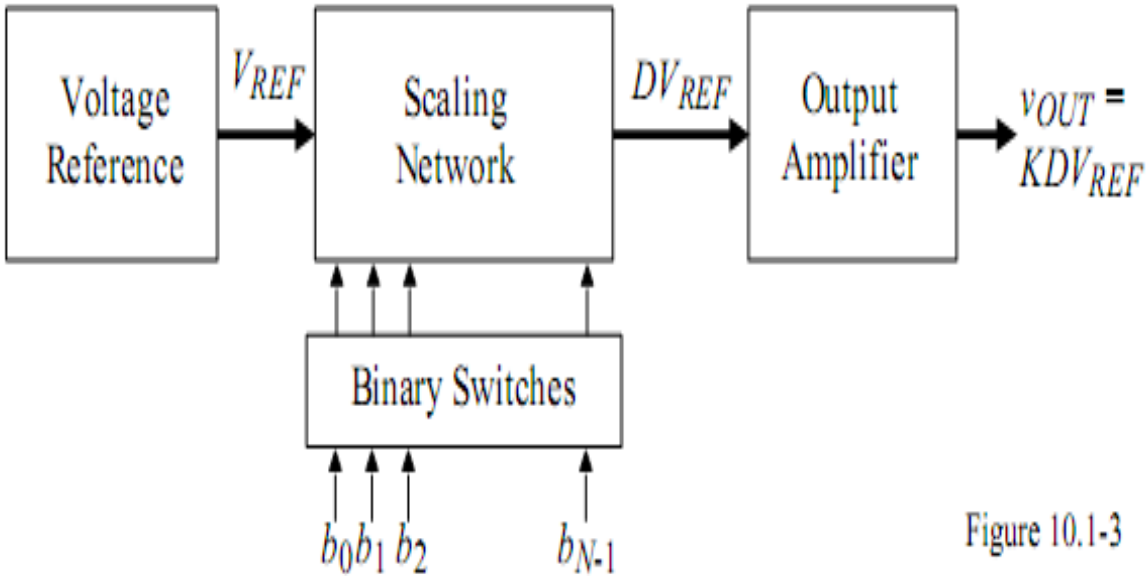
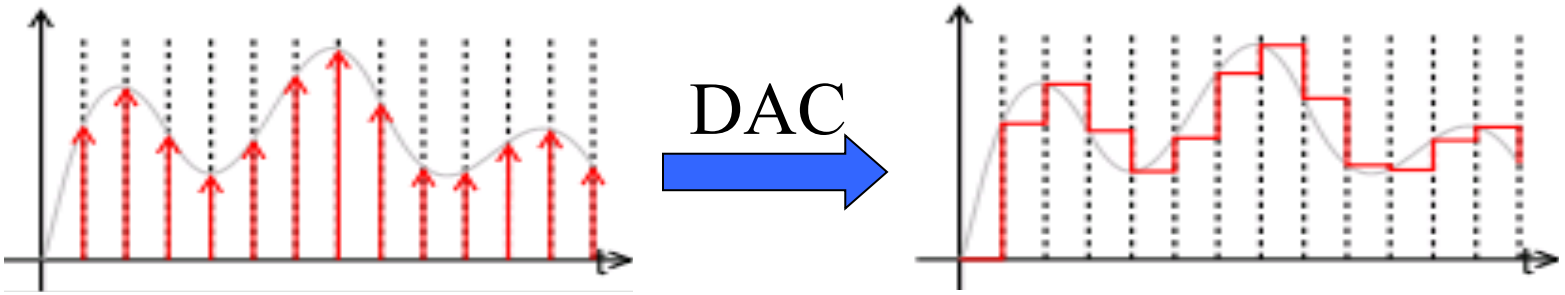


Figure 10.1-3



Ideally Sampled Signal

Output typical of a real, practical DAC due to sample & hold

Reference Voltage (Applied to ADC as well)

- Determines Characteristic of DACs
  - Set externally or Generated inside DAC
- V_{ref} sets maximum DAC output voltage (if not amplified)
- Full scale output voltage:

$$E_{o(fs)} = \frac{V_{ref}(2^n - 1)}{2^n}$$

- V_{ref} determines analog output voltage changes to steps taken by 1 LSB of digital input signal (resolution)

$$X = k \cdot A \cdot B$$

X = analog output

k = Constant

A = V_{ref} analog

B = Binary (digital) input

Input-Output Characteristics

- Ideal input-output characteristics of a 3-bit DAC
- Each binary number sampled by the DAC corresponds to a different output level.

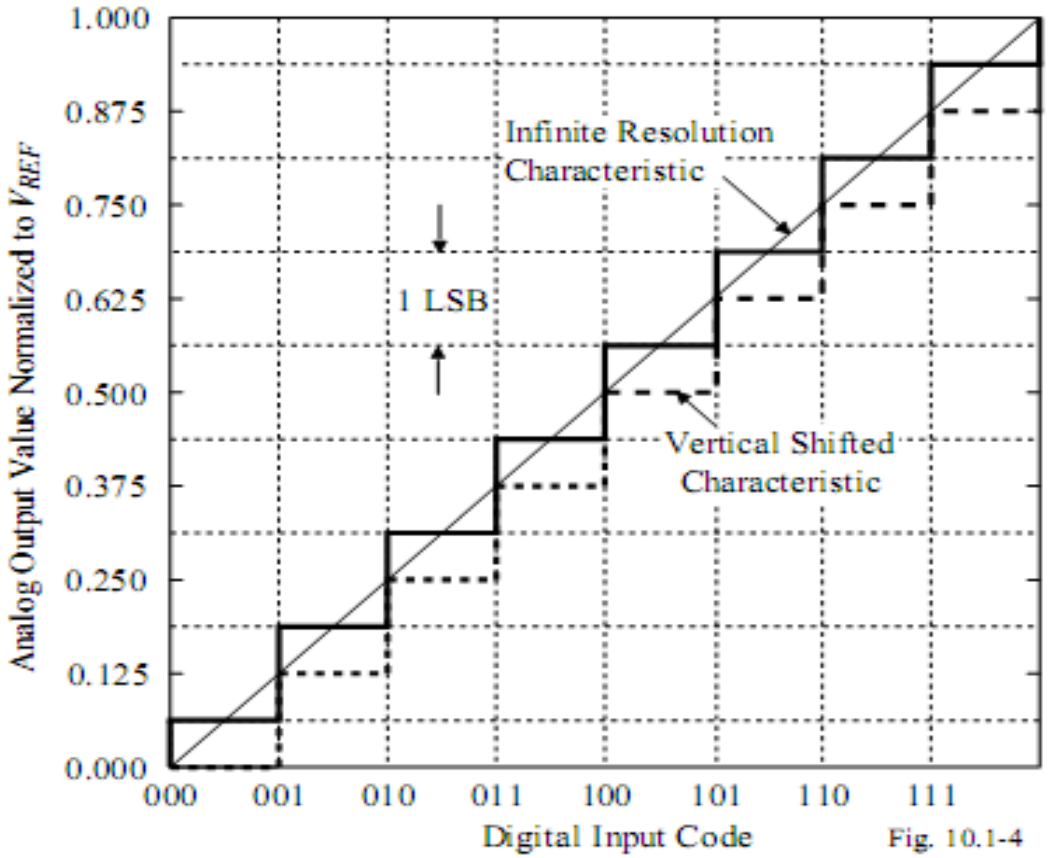


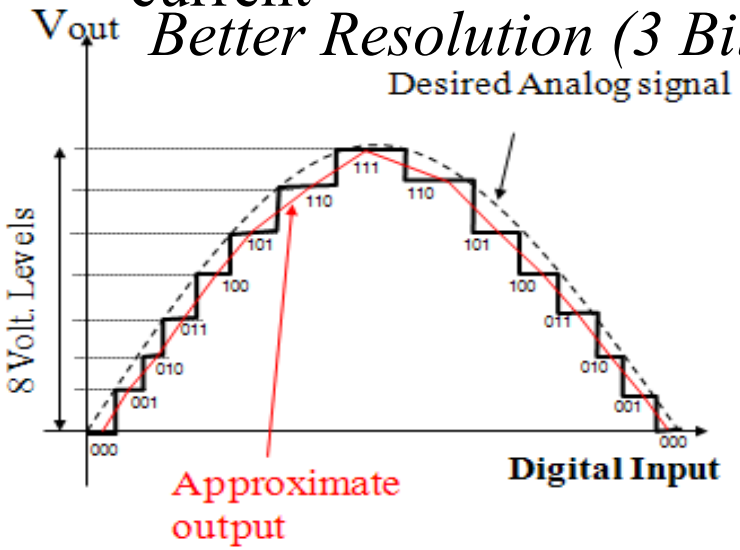
Fig. 10.1-4

Resolution Errors

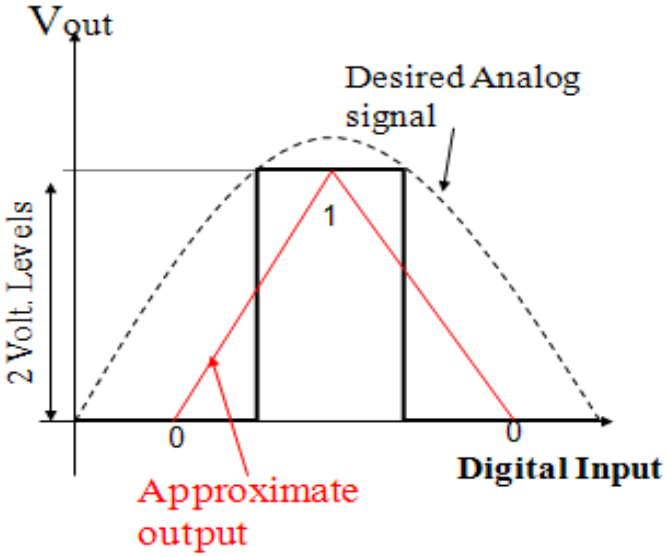
- Inherent errors associated with resolution $= \frac{\text{Ref Voltage}}{2^{\#\ of\ bits}}$
  - More Bits => Less Error & Greater Resolution
  - Less Bits => More Error & Less Resolution
  - Q: How does very high resolution affect measurements?

    A: LSB may be in noise range and not produce an output; it may be difficult to find an op-amp to amplify such small current

Better Resolution (3 Bit)

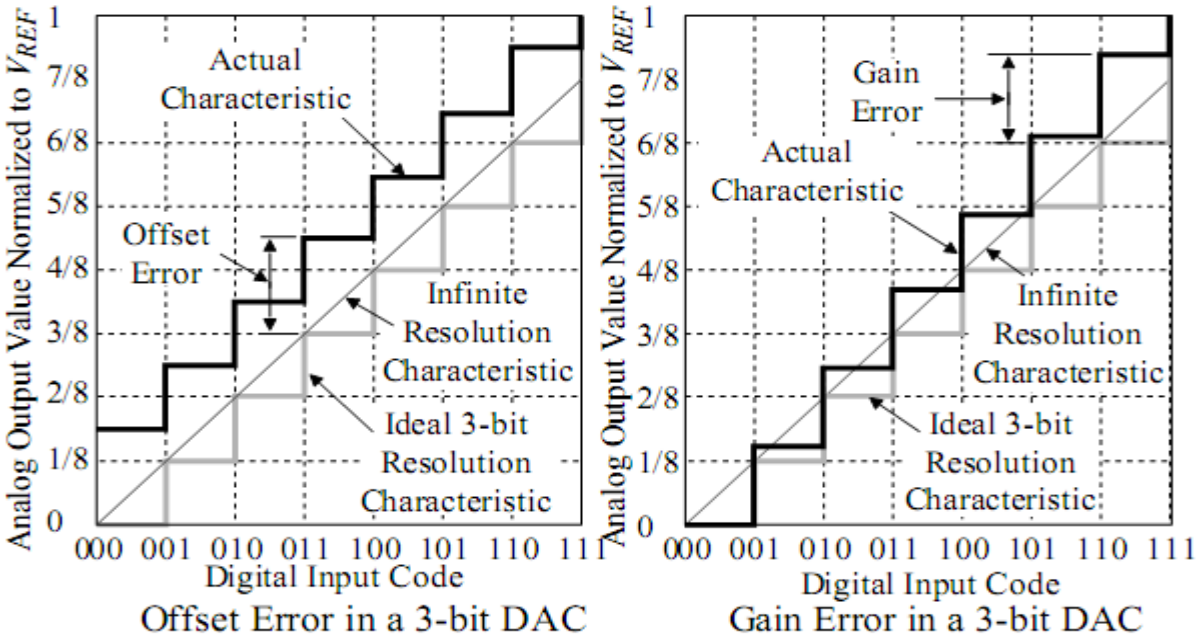


Poor Resolution (1 Bit)



Offset and Gain Errors

- An offset error is a constant difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured at any vertical jump.
- A gain error is the difference between the slope of the actual finite resolution and the ideal finite resolution characteristic measured at the right-most vertical jump.



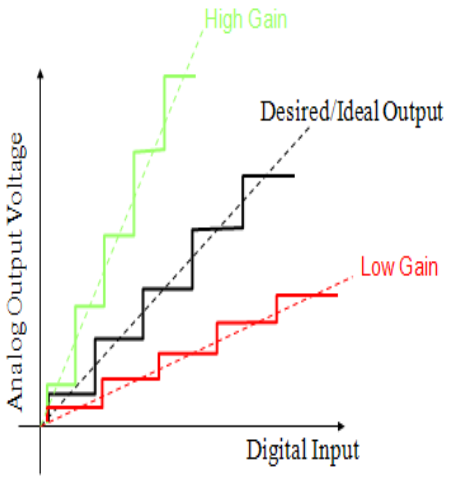
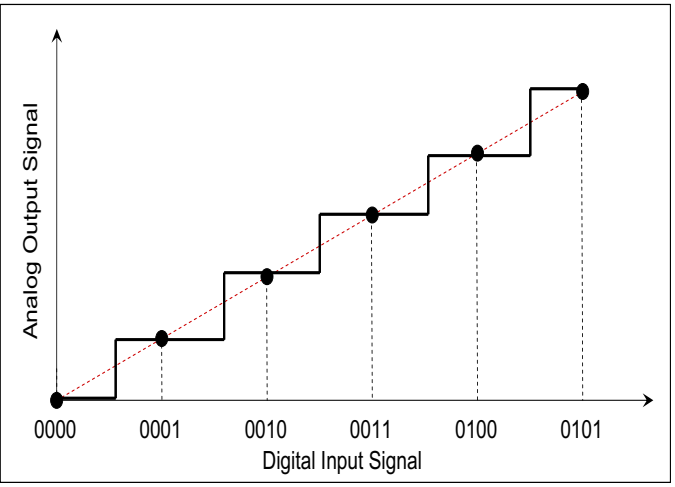


Fig. 10.1-6

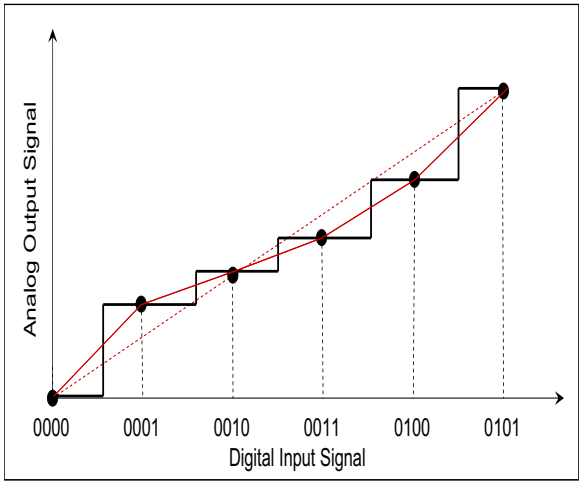
*This error may be detected when all input bits are low

DAC Linearity

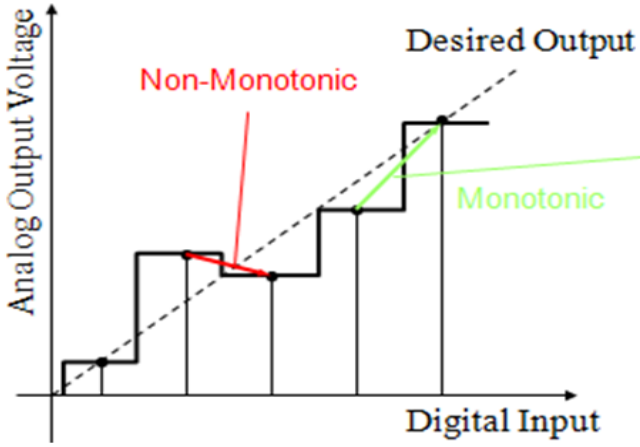
- The difference between the desired analog output and the actual output over the full range of expected values
- Does the DAC analog output vary linearly with digital input signal?
- Can the DAC behavior follow a constant Transfer Function relationship?
- Ideally, proportionality constant – linear slope
- Increase in input → increase in output → monotonic
- Integral non-linearity (INL) & Differential non-linearity (DNL)



Linear

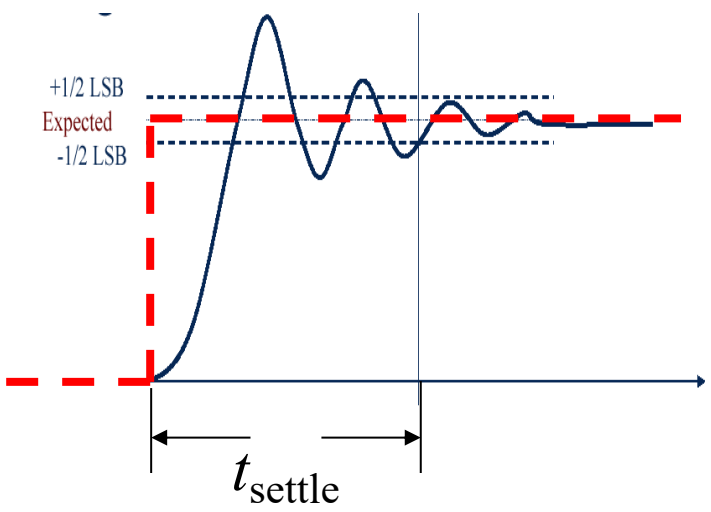


Non-Linear



Settling Time and Overshoot

- The interval between a command to update (change) its output value and the instant it reaches its final value, within a specified percentage ($V_{LSB} = \pm$ ½ LSB)
  - Settling time generally determines maximum operating frequency of DAC (Faster DACs have shorter settling time)
  - One of the principal limiting factors of any commercial DAC is the settling time of the op-amp
  - Electronic switching → fast
- Ideal DAC output would be sequence of impulses → Instantaneous update
- Causes:
  - Slew rate of output amplifier
  - Amount of amplifier ringing and signal overshoot



Summary: Types of DAC Errors

- Gain Error
- Offset Error
- Full Scale Error
- Non-Monotonic Output Error
- Differential Nonlinearity Error
- Integral Nonlinearity Error
- Settling Time and Overshoot Error
- Resolution Error
- Sources of Errors

Summary: Sources of Errors

- Deviation of voltage sources from nominal values
- Variations and tolerances on resistance values
- Non-ideal operational amplifiers
- Other non-ideal circuit components, temperature dependence, etc.

DAC
IN DETAILS

PARALLEL DIGITAL-ANALOG CONVERTERS

- Classification of Digital-Analog Converters

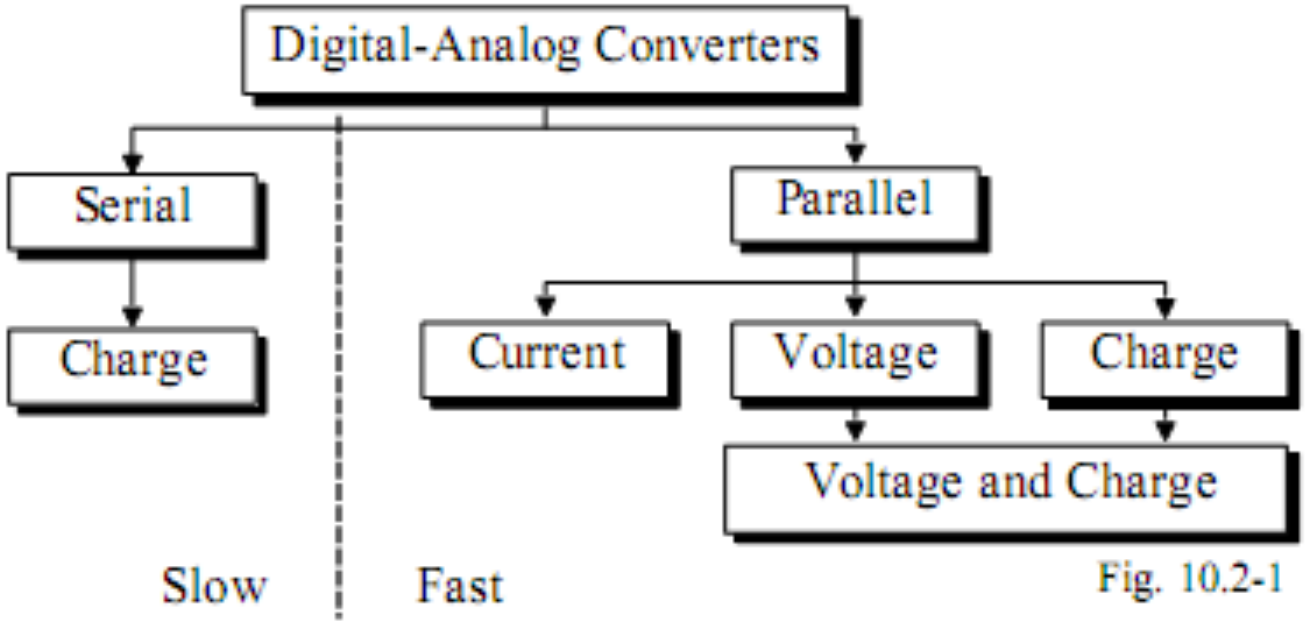


Fig. 10.2-1

DAC Architecture

Kelvin-Varley divider	Accurate, monotonous. Mainly as building block in integrated DACs
Thermometer DAC	Monotonous. Limited number of bits
Binary weighted ladder	Very common, but subject to glitches
R-2R ladder	Widely used. Not very power efficient
Σ-Δ	Linear, accurate, but complex.

Mixed architectures:

- Segmented DAC
- Interpolating DAC

Variants:

- Multiplying DACs
- Current or voltage output
- Differential or single-ended

CURRENT SCALING DAC

General Current Scaling DACs

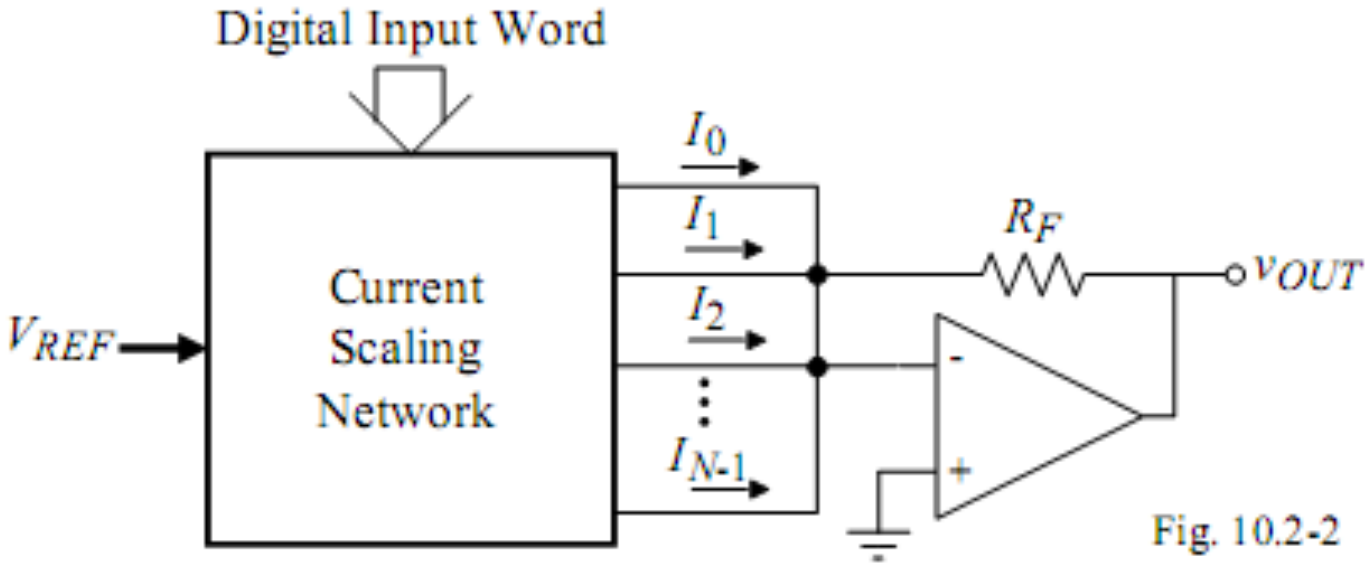


Fig. 10.2-2

The output voltage can be expressed as

$$V_{OUT} = -R_F(I_0 + I_1 + I_2 + \cdots + I_{N-1})$$

where the currents I_0, I_1, I_2, ... are binary weighted currents.

Binary-Weighted Resistor DAC

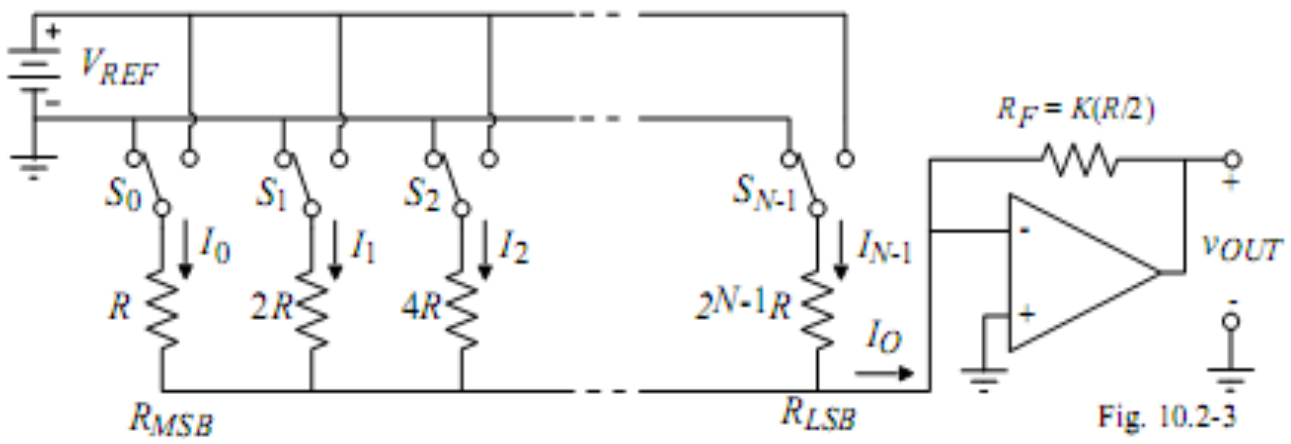


Fig. 10.2-3

Comments:

1.) R_F can be used to scale the gain of the DAC. If $R_F = KR/2$, then

$$v_{OUT} = -R_F I_O = \frac{-KR}{2}\left(\frac{b_0}{R} + \frac{b_1}{2R} + \frac{b_2}{4R} + \cdots + \frac{b_{N-1}}{2^{N-1}R}\right)V_{REF} \Rightarrow v_{OUT} = -K\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-1}}{2^N}\right)V_{REF}$$

where b_i is 1 if switch S_i is connected to V_{REF} or 0 if switch S_i is connected to ground.

2.) Component spread value $= \dfrac{R_{MSB}}{R_{LSB}} = \dfrac{R}{2^{N-1}R} = \dfrac{1}{2^{N-1}}$

3.) Attributes:

Insensitive to parasitics ⇒ fast	Large component spread value
Trimming required for large values of N	Nonmonotonic

Binary Weighted Resistor

- Advantages
  - Simple
  - Fast
- Disadvantages
  - Need large range of resistor values (2048:1 for 12-bit) with high precision in low resistor values
  - Need very small switch resistances
  - Op-amp may have trouble producing low currents at the low range of a high precision DAC

R-2R Ladder Implementation of the Binary Weighted Resistor DAC

Use of the R-2R concept to avoid large element spreads:

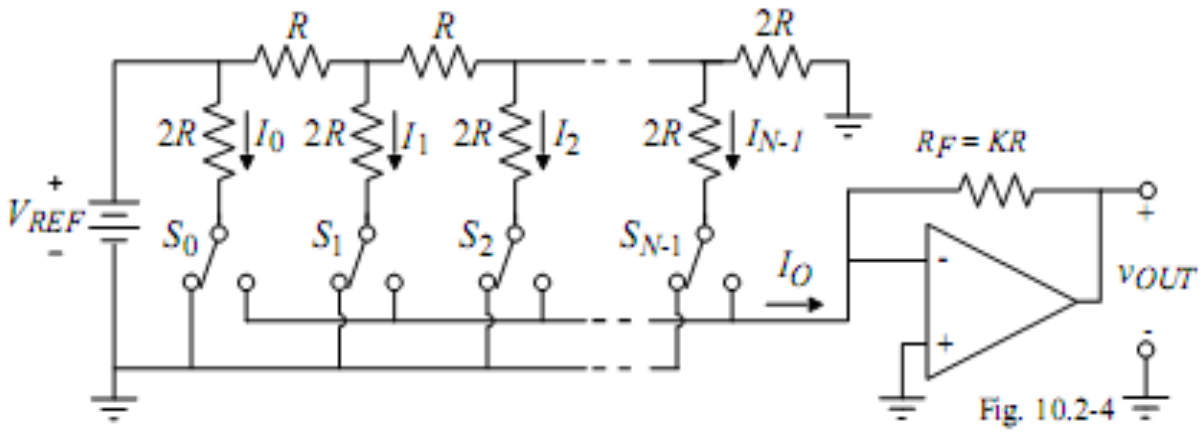


Fig. 10.2-4

How does the R-2R ladder work?

"The resistance seen to the right of any of the vertical $2R$ resistors is $2R$."

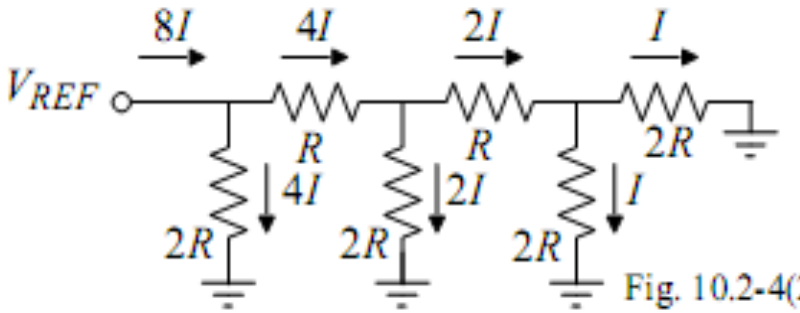


Fig. 10.2-4(2R-R)

Attributes:

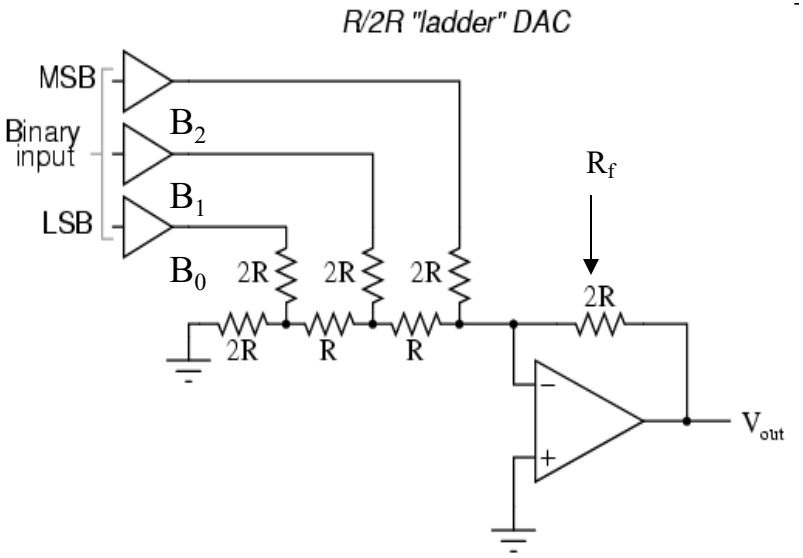
- Not sensitive to parasitics

(currents through the resistors never change as S_i is varied)

- Small element spread. Resistors made from same unit ($2R$ consist of two in series or R consists of two in parallel)
- Not monotonic

R-2R Ladder

- Circuit may be analyzed using Thevenin's theorem (replace network with equivalent voltage source and resistance)
- Final result is:



$$V_{\text{out}} = -V_{\text{ref}} \frac{R_f}{R} \sum_{i=0}^{n-1} \frac{B_i}{2^{n-i}}$$

Compare to binary weighted circuit:

$$V_{\text{out}} = -V_{\text{ref}} \frac{R_f}{R} \sum_{i=0}^{n-1} \frac{B_i}{2^{(n-1)-i}}$$

R-2R Ladder

- Resolution

$$|V_{\min}| = \frac{R_f |V_{ref}|}{R2^n}$$

- If $R_f = R$ then resolution is $\dfrac{|V_{ref}|}{2^n}$

and max V_{out} is $|V_{\max}| = |V_{ref}|\left(1 - \dfrac{1}{2^n}\right)$

R-2R Ladder

- Advantages:
  - Only 2 resistor values
  - Lower precision resistors acceptable
- Disadvantages
  - Slower conversion rate

General comments

- Circuits as shown produce only unipolar output
- Replacing ground with $-V_{ref}$ will allow V_{out} to be positive or negative

General Voltage Scaling Digital Analog Converter

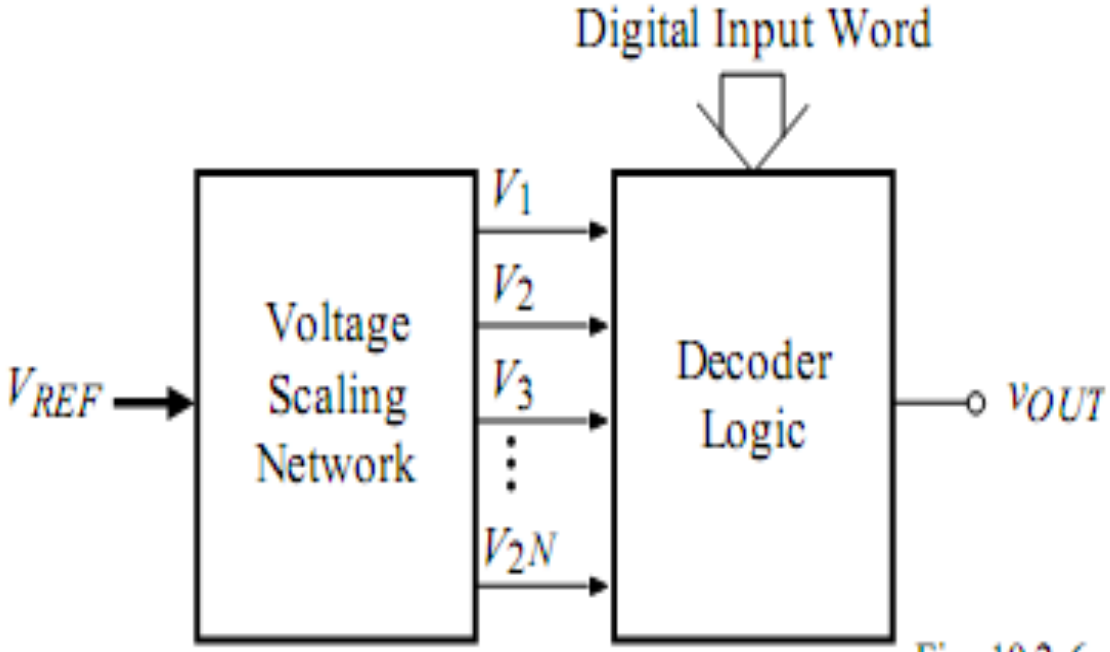


Fig. 10.2-6

Operation:

Creates all possible values of the analog output then uses a decoding network to determine which voltage to select based on the digital input word.

3-Bit Voltage Scaling Digital-Analog Converter

The voltage at any tap can be expressed as: $v_{OUT} = \frac{V_{REF}}{8}(n - 0.5) = \frac{V_{REF}}{16}(2n - 1)$

Attributes:

- Guaranteed monotonic
- Compatible with CMOS technology
- Large area if N is large
- Sensitive to parasitics
- Requires a buffer
- Large current can flow through the resistor string.

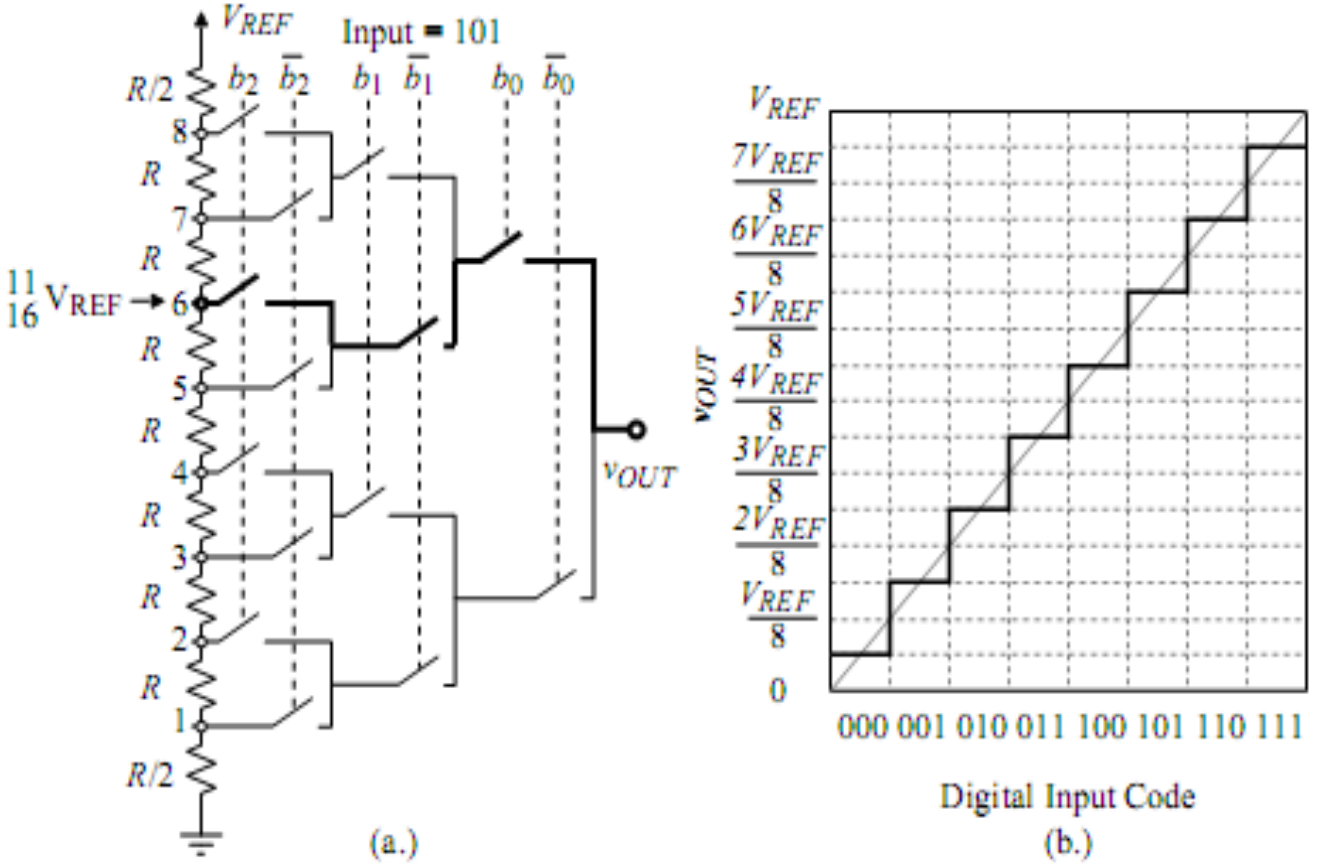


Figure 10.2-7 - (a.) Implementation of a 3-bit voltage scaling DAC. (b.) Input-output characteristics of Fig. 10.2-7(a.)

Alternate Realization of the 3-Bit Voltage Scaling DAC

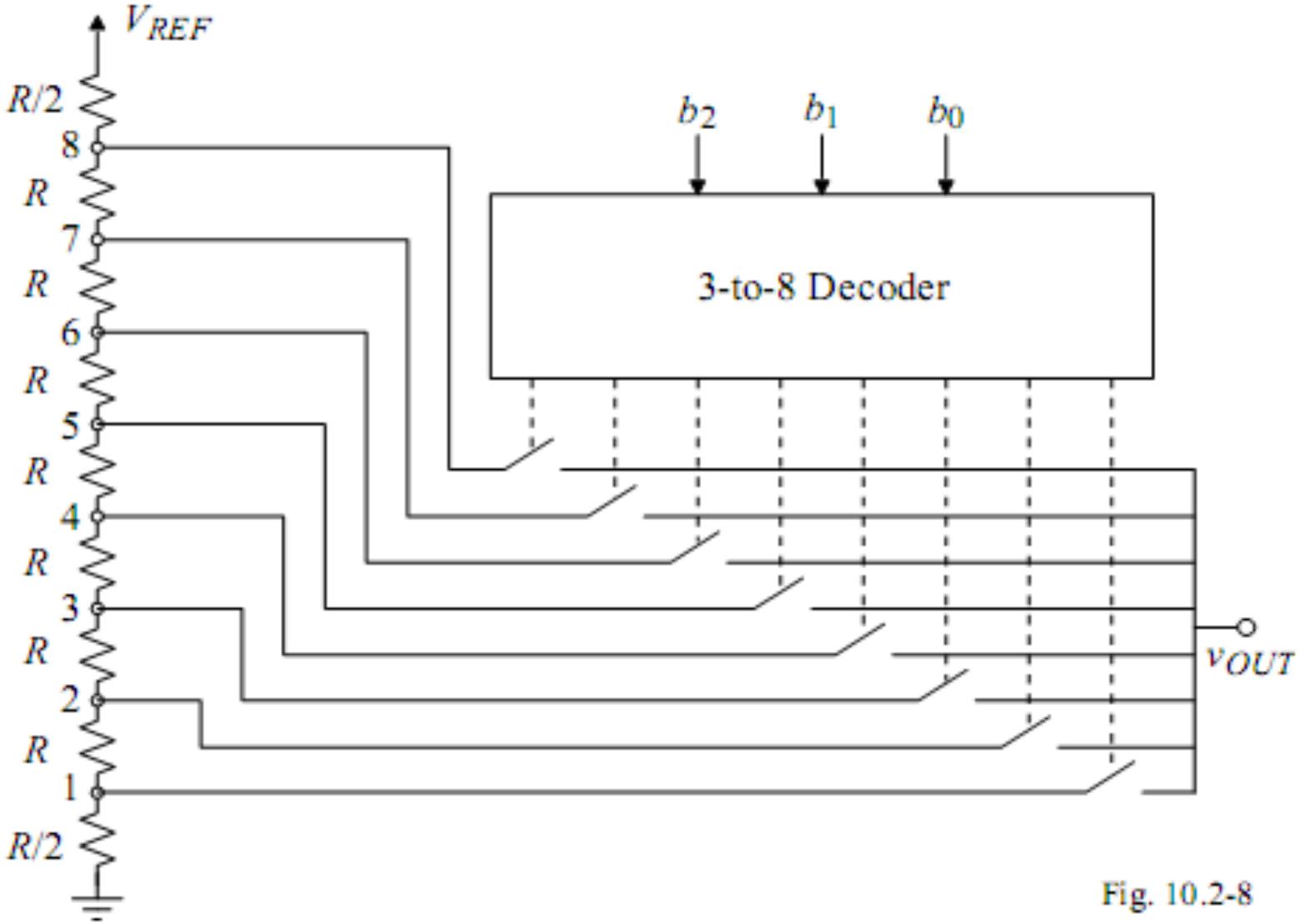


Fig. 10.2-8

Example 10.2-1 - Accuracy Requirements of a Voltage-Scaling DAC

If the resistor string of a voltage scaling digital-analog converter is a 5 μm wide polysilicon strip having a relative accuracy of ±1%, what is the largest number of bits that can be resolved and keep the worst case *INL* within ±0.5 LSB? For this number of bits, what is the worst case *DNL*?

Solution

From the previous page, we can write that

$$2^{n-1}\left(\frac{\Delta R}{R}\right) = 2^{n-1}\left(\frac{1}{100}\right) \le \frac{1}{2}$$

This inequality can be simplified

$$2^n \le 100$$

which has a solution of $n = 6$.

The value of the *DNL* for $n = 6$ is found from the previous page as

$$DNL = \frac{\pm 1}{100}\, LSBs = \pm 0.01 LSBs$$

(This is the reason the resistor string is monotonic.)

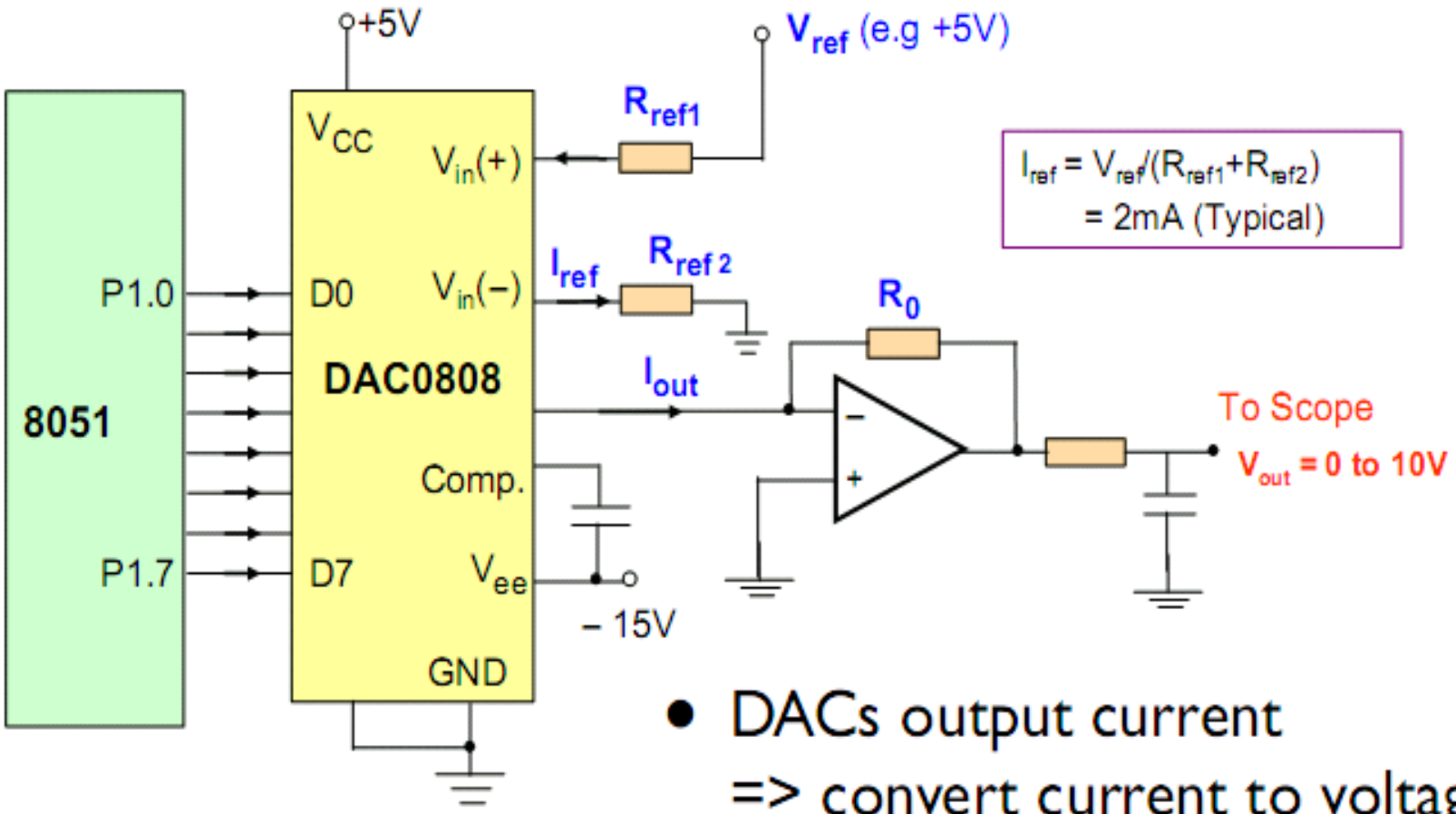
Summary of the Parallel DAC Performance

DAC Type	Advantage	Disadvantage
Current Scaling	Fast, insensitive to switch parasitics	Large element spread, nonmonotonic
Voltage Scaling	Monotonic, equal resistors	Large area, sensitive to parasitic capacitance
Charge Scaling	Fast, good accuracy	Large element spread, nonmonotonic

SUMMARY OF THE PERFORMANCE OF DACs

DAC	Figure	Primary Advantage	Primary Disadvantage
Current-scaling, binary weighted resistors	10.2-3	Fast, insensitive to parasitic capacitance	Large element spread, nonmonotonic
Current-scaling, R-2R ladder	10.2-4	Small element spread, increased accuracy	Nonmonotonic, limited to resistor accuracy
Current-scaling, active devices	10.2-5	Fast, insensitive to switch parasitics	Large element spread, large area
Voltage-scaling	10.2-7	Monotonic, equal resistors	Large area, sensitive to parasitic capacitance
Charge-scaling, binary weighted capacitors	10.2-10	Best accuracy	Large area, sensitive to parasitic capacitance
Binary weighted, charge amplifier	10.2-12	Best accuracy, fast	Large element spread, large area
Current-scaling subDACs using current division	10.3-3	Minimizes area, reduces element spread which enhances accuracy	Sensitive to parasitic capacitance, divider must have $\pm 0.5LSB$ accuracy
Charge-scaling subDACs using charge division	10.3-4	Minimizes area, reduces element spread which enhances accuracy	Sensitive to parasitic capacitance, slower, divider must have $\pm 0.5LSB$ accuracy
Binary weighted charge amplifier subDACs	10.3-6	Fast, minimizes area, reduces element spread which enhances accuracy	Requires more op amps, divider must have $\pm 0.5LSB$ accuracy
Voltage-scaling (*MSBs*), charge-scaling (*LSBs*)	10.3-7	Monotonic in *MSBs*, minimum area, reduced element spread	Must trim or calibrate resistors for absolute accuracy
Charge-scaling (*MSBs*), voltage-scaling (*LSBs*)	10.3-8	Monotonic in *LSBs*, minimum area, reduced element spread	Must trim or calibrate resistors for absolute accuracy
Serial, charge redistribution	10.4-1	Simple, minimum area	Slow, requires complex external circuits
Pipeline, algorithmic	10.4-3	Repeated blocks, output at each clock after N clocks	Large area for large number of bits
Serial, iterative algorithmic	10.4-4	Simple, one precise set of components	Slow, requires additional logic circuitry

DAC 808



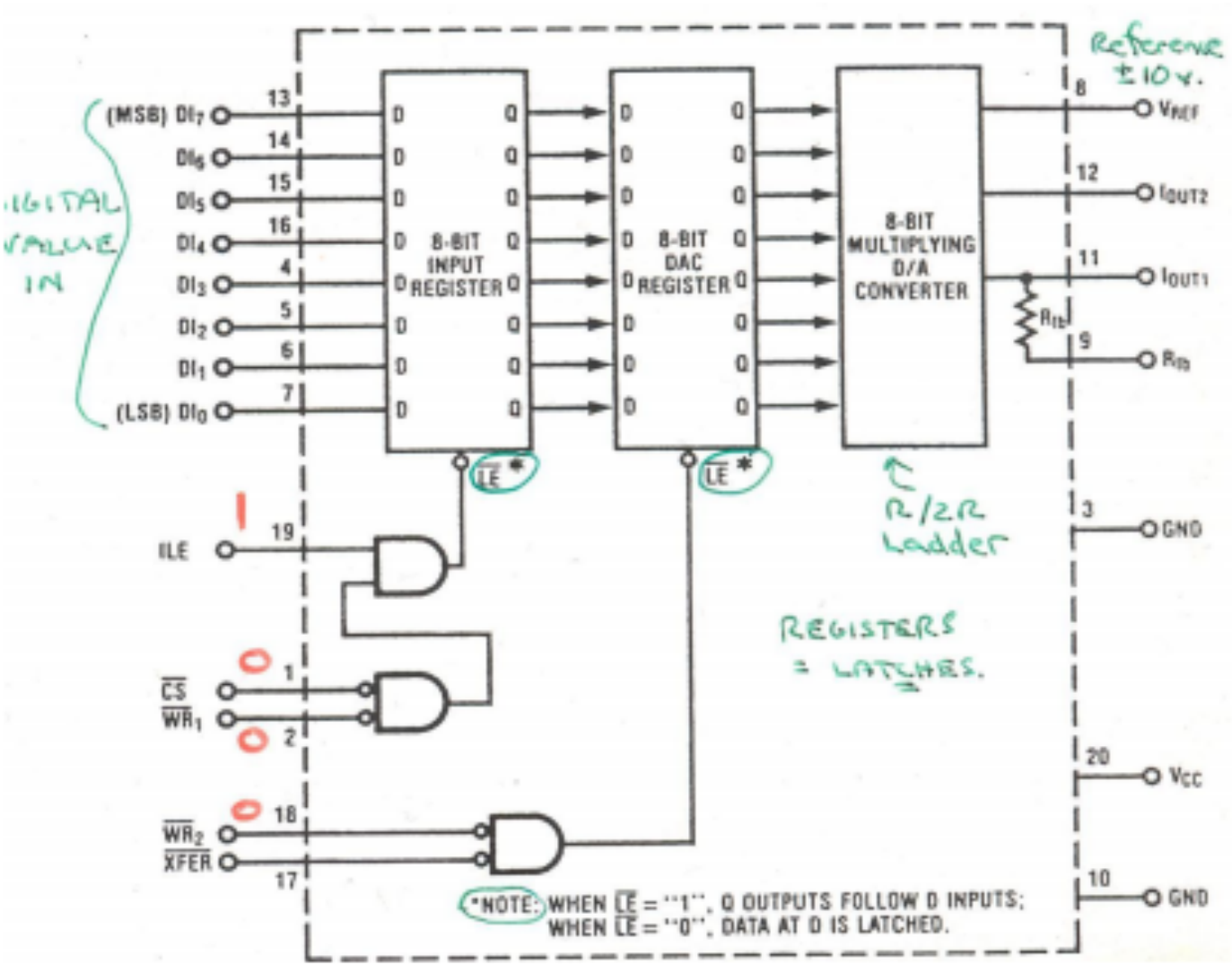
$I_{ref} = V_{ref}/(R_{ref1}+R_{ref2})$
= 2mA (Typical)

- DACs output current
  => convert current to voltage

Output voltage, $V_{out} = I_{out} \times R_o$

$$I_{out} = I_{ref}\left(\frac{D_7}{2}+\frac{D_6}{4}+\frac{D_5}{8}+\frac{D_4}{16}+\frac{D_3}{32}+\frac{D_2}{64}+\frac{D_1}{128}+\frac{D_0}{256}\right)$$

DAC 0831 8-bit D/A converter

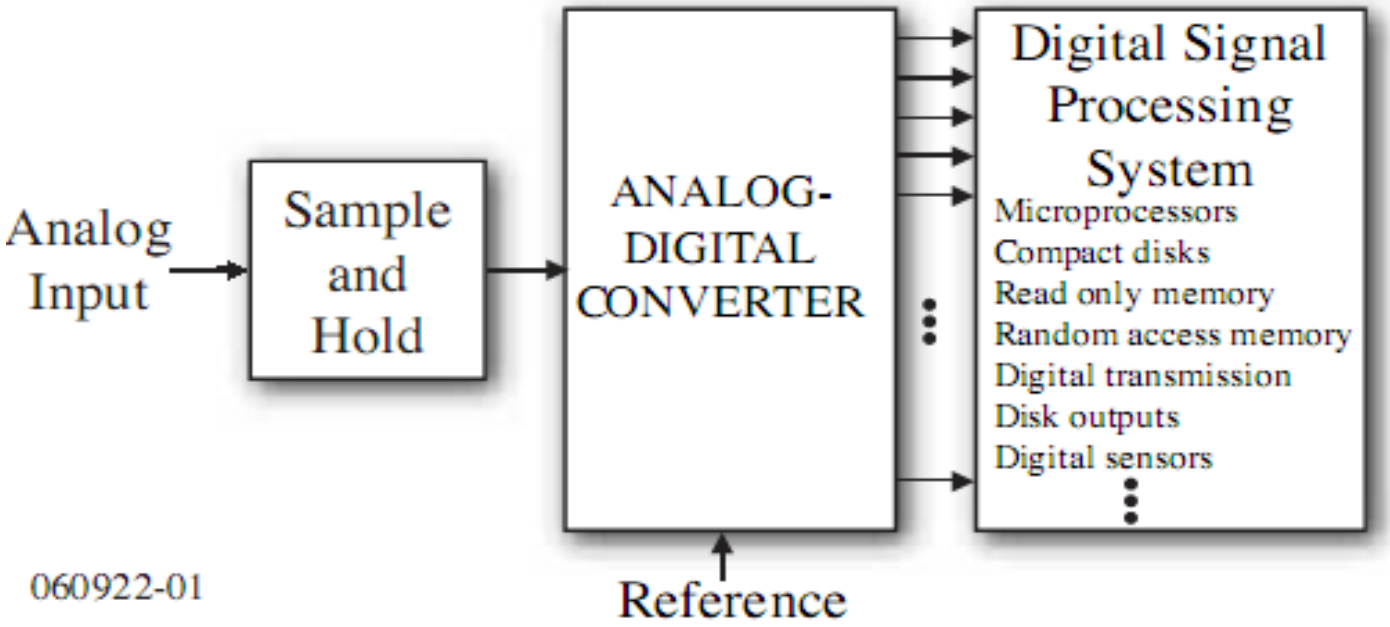


Input latches can be made transparent

ADC
INTRODUCTION

Analog-Digital Converters

- Characteristics:
  - Can only be synchronous (the analog signal must be sampled and held during conversion)
  - Primary active element is the comparator
  - Conversion time can vary from fast (one clock period, T) to slow ($2^{\text{No. of bits}} * T$)



Analog to digital conversion

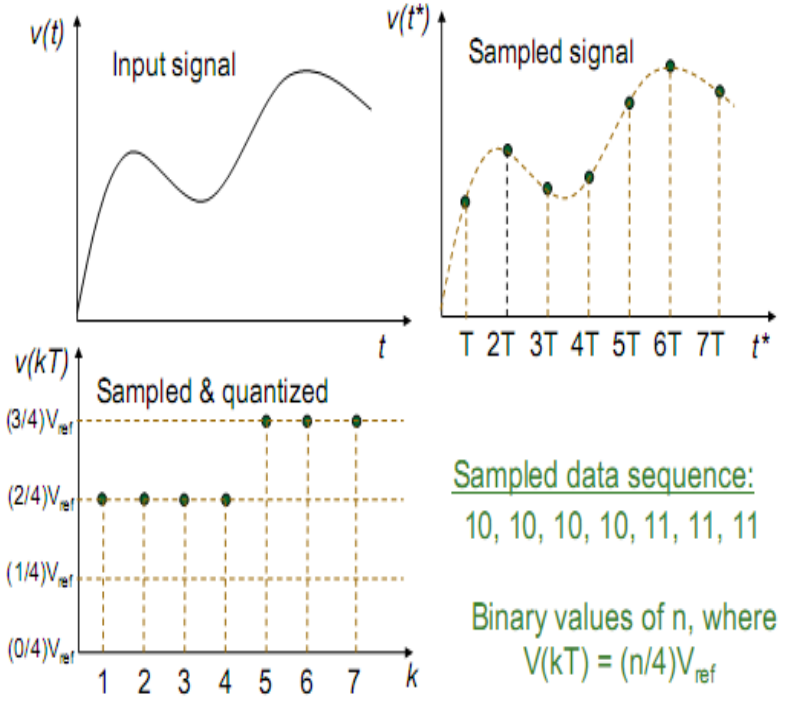
- Given: continuous-time electrical signal

  v(t), t >=0

- Desired: sequence of discrete numeric values that represent the signal at selected sampling times :

  v(0), v(T), v(2T),…v(nT)

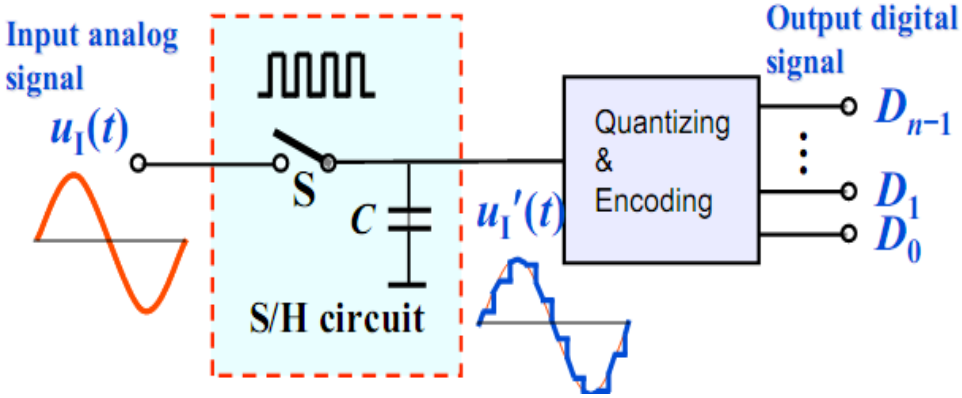
  – T = "sampling time": v(t) "sampled" every T seconds
  – n = sample number
  – v(nT) = value of v(t) measured at the n^{th} sample time and quantized to one of 2^k discrete levels

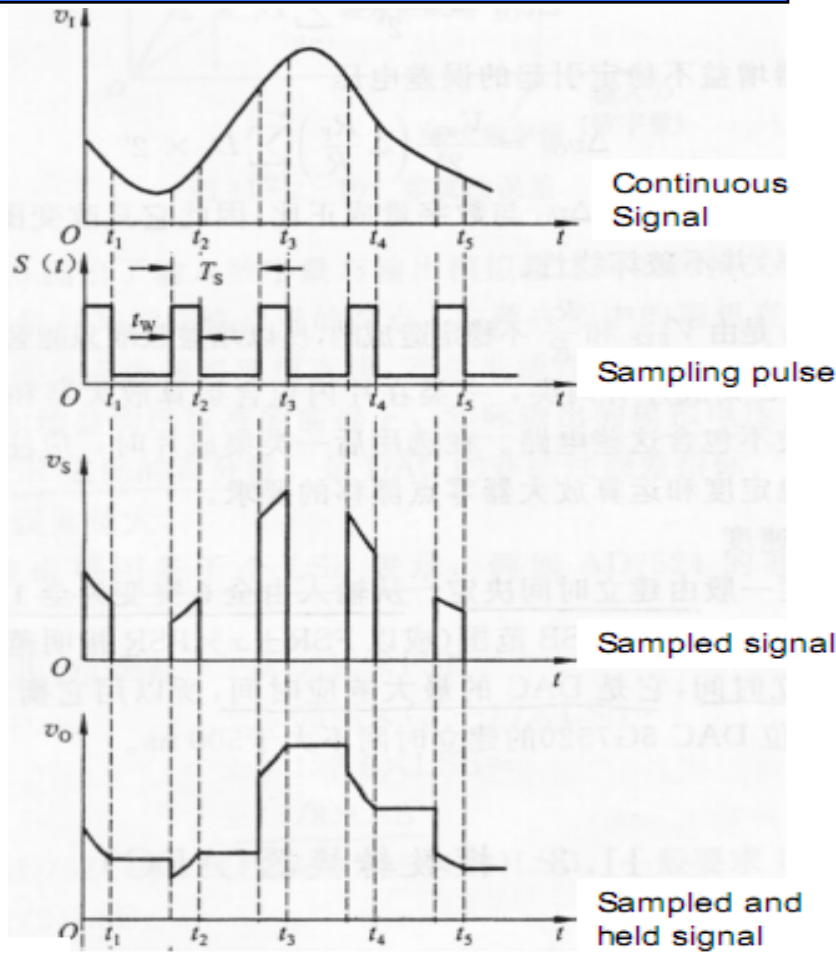


Analog to digital conversion

2 steps

- Sampling and Holding (S/H)
  - Holding signal benefits the accuracy of the A/D conversion
- Quantizing and Encoding (Q/E)



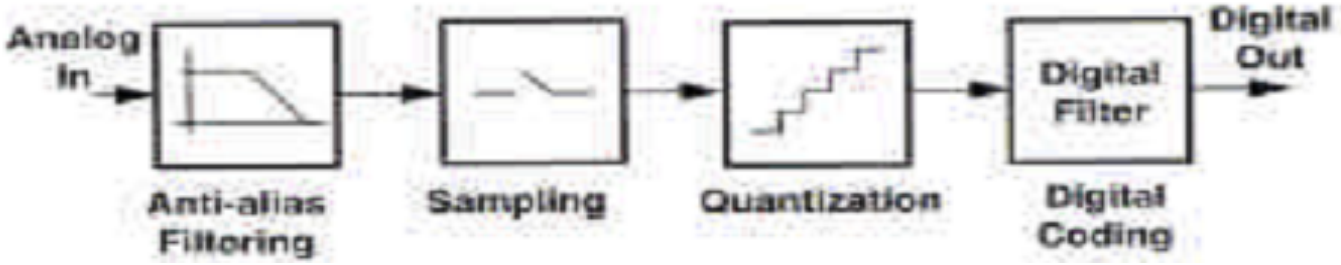


A/D conversion parameters

- Sampling rate, F (sampling interval T = 1/F)
  - Nyquist rate ≥ 2 x (highest frequency in the signal) to reproduce sampled signals
- Precision (# bits in sample value)
  - k = # of bits used to represent samples
  - "precision": each step represents (1/2k)*Vrange
  - "accuracy": degree to which converter discerns proper level (error when rounding to nearest level)
- More difficult than D/A conversion
- Tradeoffs:
  - Precision (# bits)/Accuracy/Speed (of conversion)/Linearity/Unipolar vs. bipolar input/Encoding method for output/Cost
  - Often built around digital to analog converters

CHARACTERIZATION OF ADCs INTRODUCTION

A/D Conversion



General Block Diagram of an Analog-Digital Converter

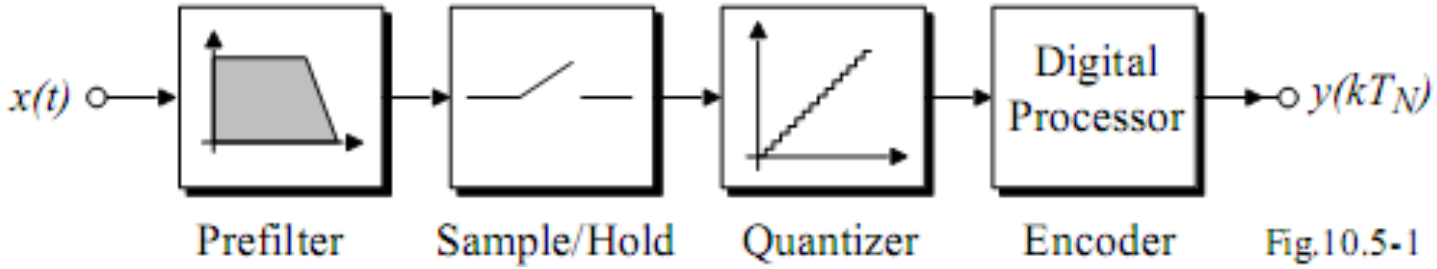


Fig.10.5-1

- Prefilter - Avoids the aliasing of high frequency signals back into the baseband of the ADC
- Sample-and-hold - Maintains the input analog signal constant during conversion
- Quantizer - Finds the subrange that corresponds to the sampled analog input
- Encoder - Encoding of the digital bits corresponding to the subrange

Classification of ADCs

Analog-digital converters can be classified by the relationship of f_B and $0.5f_S$ and by their conversion rate.

- *Nyquist ADCs* - ADCs that have f_B as close to $0.5f_S$ as possible.
- *Oversampling ADCs* - ADCs that have f_B much less than $0.5f_S$.

Table 10.5-1 - Classification of Analog-to-Digital Converter Architectures

Conversion Rate	Nyquist ADCs	Oversampled ADCs
Slow	Integrating (Serial)	Very high resolution <14-16 bits
Medium	Successive Approximation1-bit Pipeline Algorithmic	Moderate resolution <10-12 bits
Fast	Flash Multiple-bit Pipeline Folding and interpolating	Low resolution < 6-8 bits

Input-Output Characteristics

Ideal input-output characteristics of a 3-bit ADC

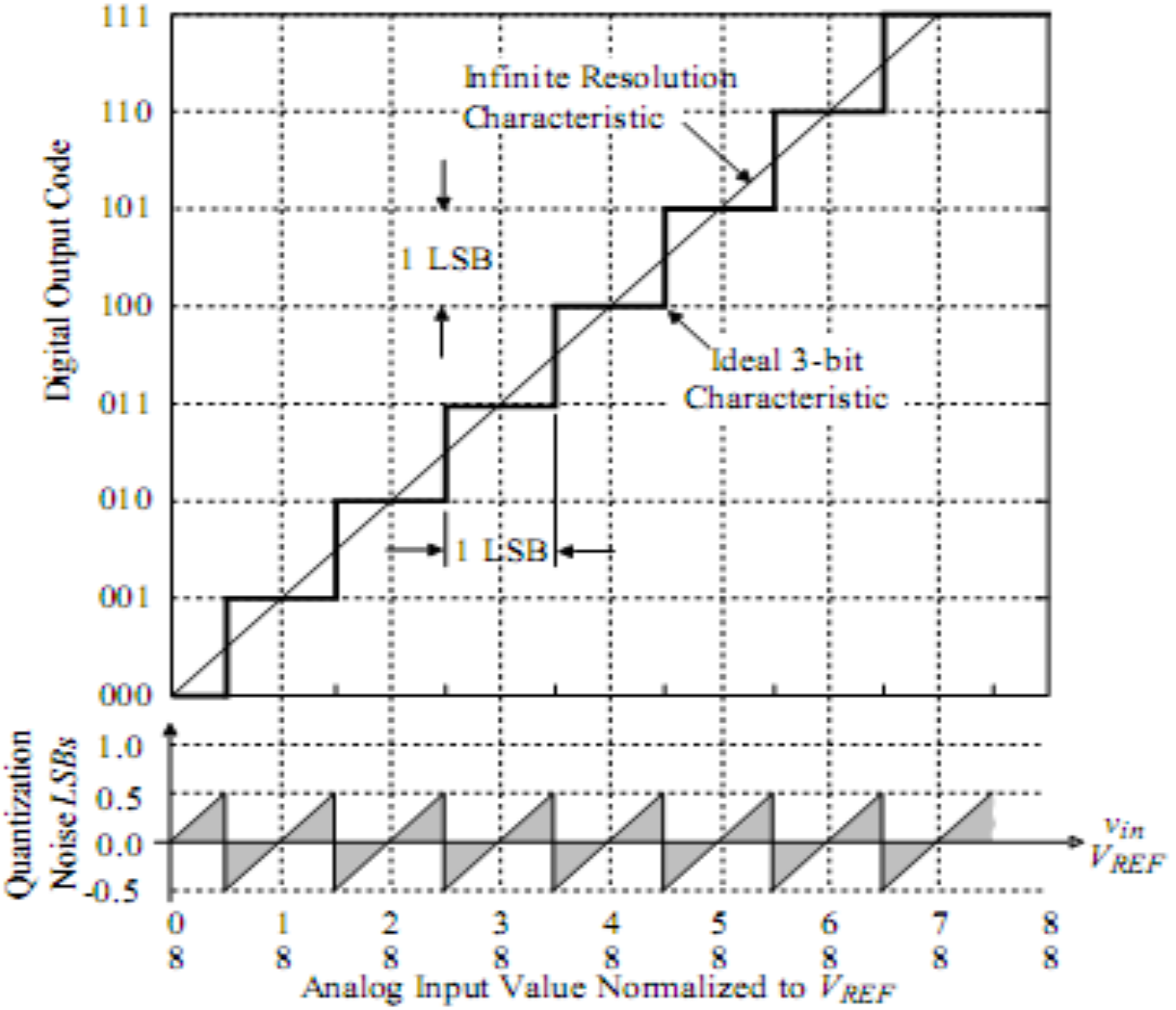


Figure 10.5-3 Ideal input-output characteristics of a 3-bit ADC.

Definitions related to ADCs

- The *dynamic range, signal-to-noise ratio (SNR)*, and the *effective number of bits (ENOB)* of the ADC are the same as for the DAC
- *Resolution* of the ADC is the smallest analog change that distinguishable by an ADC.
- *Quantization Noise* is the $\pm 0.5LSB$ uncertainty between the infinite resolution characteristic and the actual characteristic.
- *Offset Error* is the difference between the ideal finite resolution characteristic and actual finite resolution characteristic
- *Gain Error* is the difference between the ideal finite resolution characteristic and actual finite resolution characteristic measured at full-scale input. This difference is *proportional* to the analog input voltage.

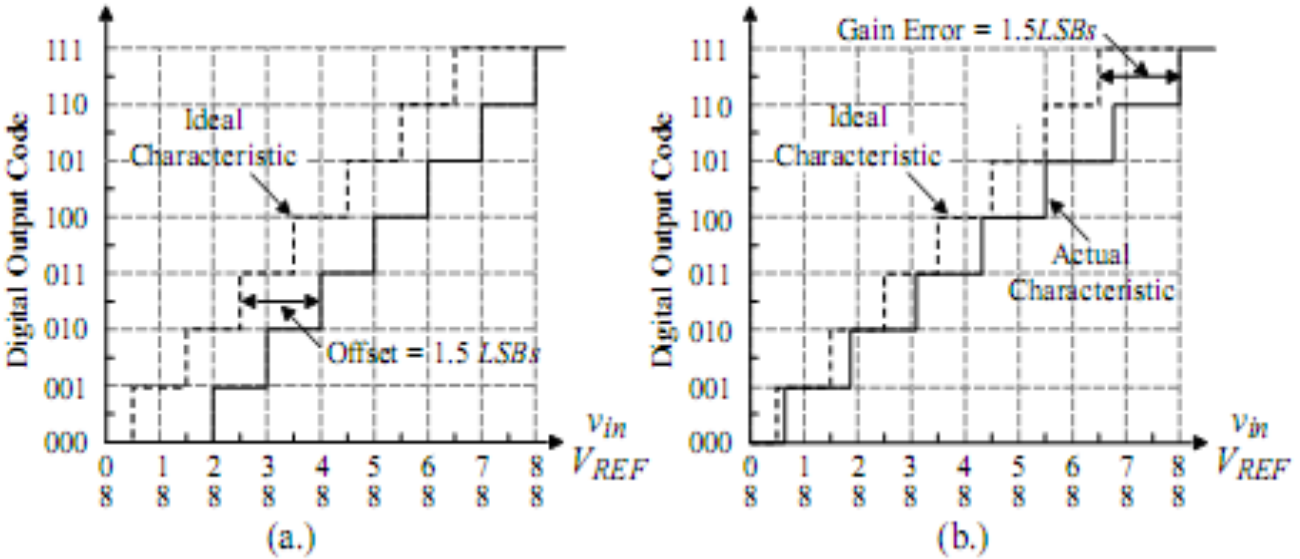


Figure 10.5-4 - (a.) Example of offset error for a 3-bit ADC. (b.) Example of gain error for a 3-bit ADC.

Resolution

Resolution:

The smallest change in analog signal that will result in a change in the digital output.

$$\Delta V = V_r/2^N$$

V_r = Reference voltage range

N = Number of bits in digital output.

2^N = Number of states.

ΔV = Resolution

The resolution represents the quantization error inherent in the conversion of the signal to digital form

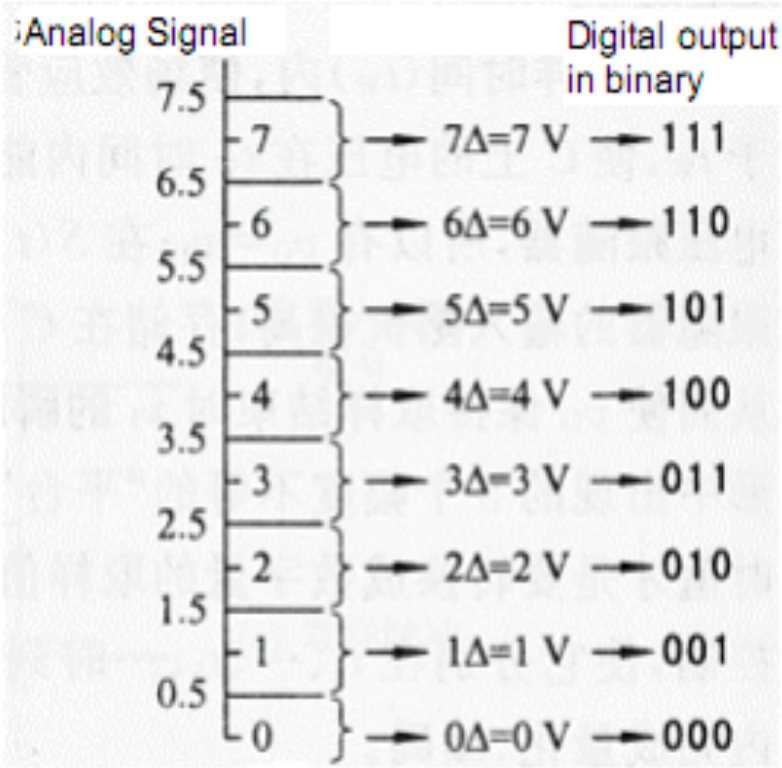
Quantizing and Encoding

- Quantizing:

  Partitioning the reference signal range into a number of discrete quanta, then matching the input signal to the correct quantum.

- Encoding:

Assigning a unique digital code to each quantum, then allocating the digital code to the input signal.



$$\Delta V = 1\,V$$

$$\text{Maximum Quantization error} = \pm\frac{1}{2}\Delta V = \pm 0.5\,V$$

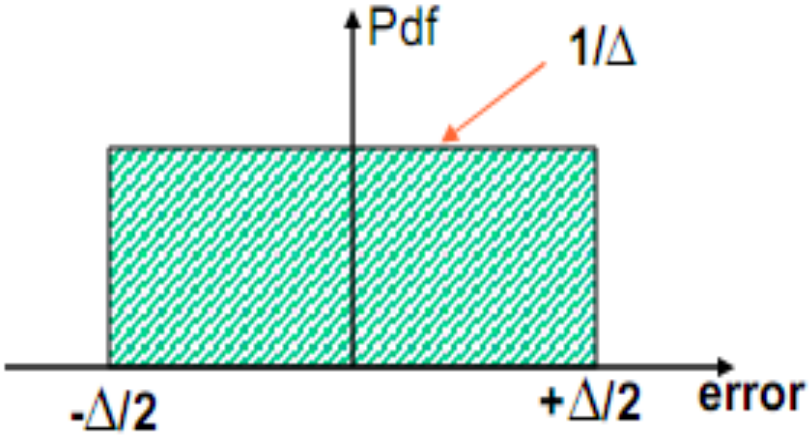
Digital Output Codes

Table 10.5-2 - Digital Output Codes used for ADCs

Decimal	Binary	Thermometer	Gray	Two's Complement
0	000	0000000	000	000
1	001	0000001	001	111
2	010	0000011	011	110
3	011	0000111	010	101
4	100	0001111	110	100
5	101	0011111	111	011
6	110	0111111	101	010
7	111	1111111	100	001

Quantization Error PDF

- Uniformly distributed from $-\Delta/2 \ldots +\Delta/2$ provided that
  - Busy input
  - Amplitude is many LSBs
  - No overload
- Not Gaussian!



- Zero mean
- Variance

$$\overline{e^2} = \int_{-\Delta/2}^{+\Delta/2} \frac{e^2}{\Delta} de = \frac{\Delta^2}{12}$$

- Spectral density white if the joint pdf of the input at different sample times is smooth

Ref: W. R. Bennett, "Spectra of quantized signals," Bell Syst. Tech. J., vol. 27, pp. 446-72, July 1988.

B. Widrow, "A study of rough amplitude quantization by means of Nyquist sampling theory," IRE Trans. Circuit Theory, vol. CT-3, pp. 266-76, 1956.

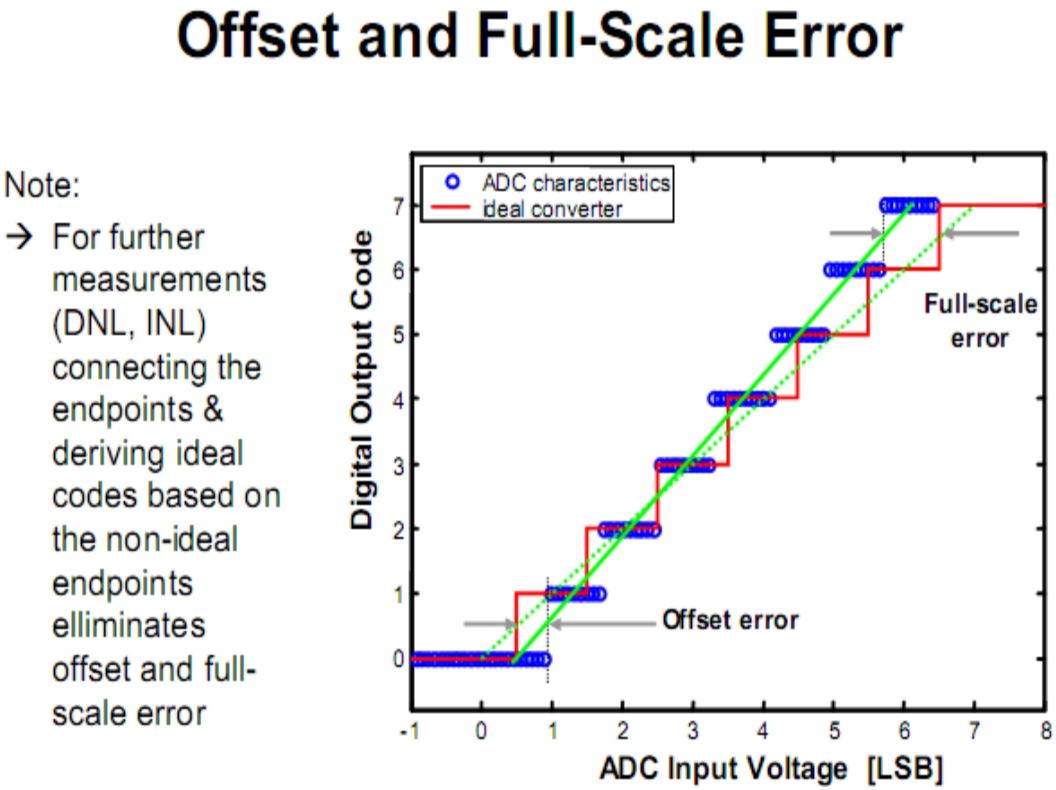
Offset and Full Scale Errors

- Alternative specification in

  % Full Scale = 100% * (LSB value)/ 2^N
- Gain error can be extracted from offset & full scale error
- Non-trivial to build a converter with extremely good gain/offset specs
- Typically gain/offset is most easily compensated by the digital pre/post-processor
- More interesting: Linearity -> DNL, INL

Note:

→ For further measurements (DNL, INL) connecting the endpoints & deriving ideal codes based on the non-ideal endpoints elliminates offset and full-scale error



Sample-and-Hold Circuit

Waveforms of a sample-and-hold circuit:

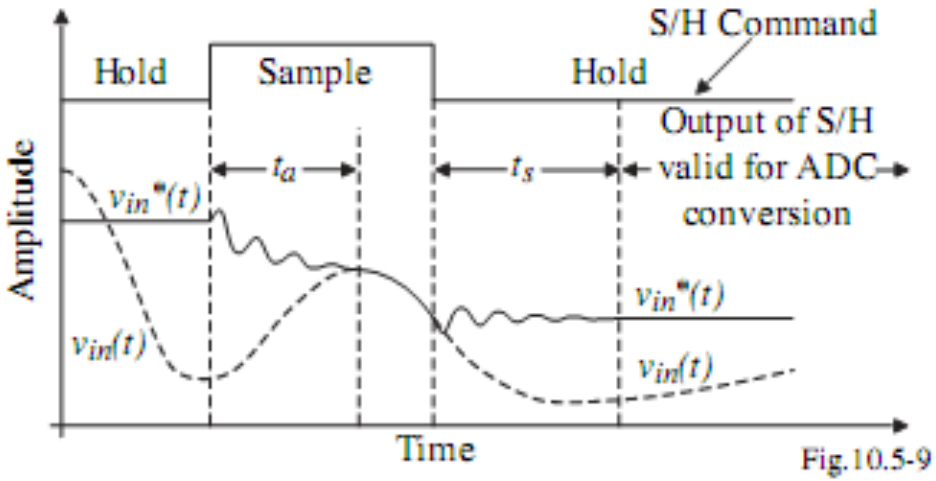


Fig.10.5-9

Definitions:

- *Acquisition time* (t_a) = time required to acquire the analog voltage
- *Settling time* (t_s) = time required to settle to the final held voltage to within an accuracy tolerance

$$\therefore \quad T_{sample} = t_a + t_s \quad \rightarrow \quad \text{Maximum sample rate} = f_{sample}(\max) = \frac{1}{T_{sample}}$$

Other consideratons:

- *Aperture time* = the time required for the sampling switch to open after the S/H command is initiated
- *Aperture jitter* = variation in the aperture time due to clock variations and noise

Types of S/H circuits:

- No feedback - faster, less accurate
- Feedback - slower, more accurate

Open-Loop, Buffered S/H Circuit

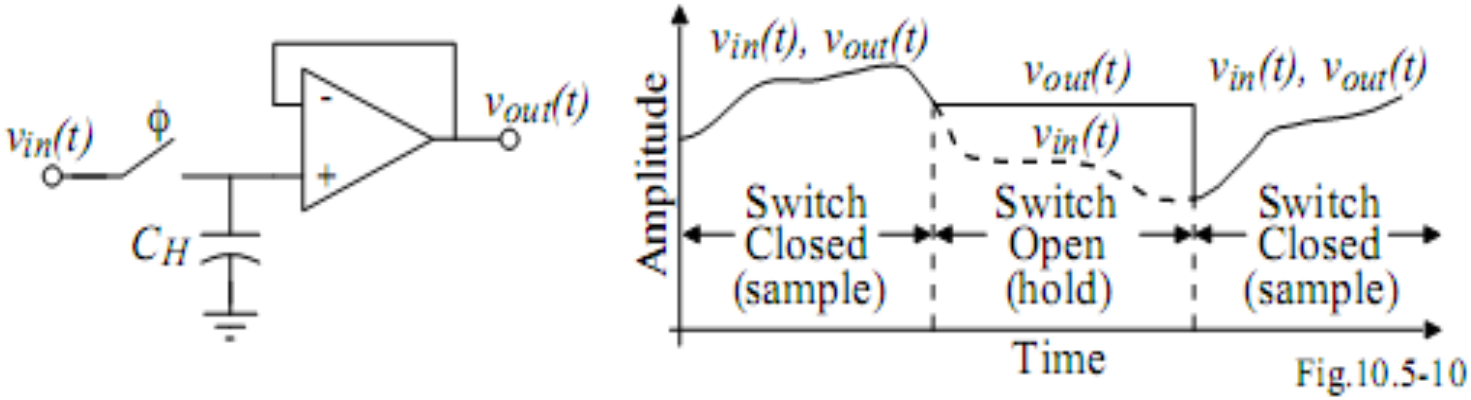


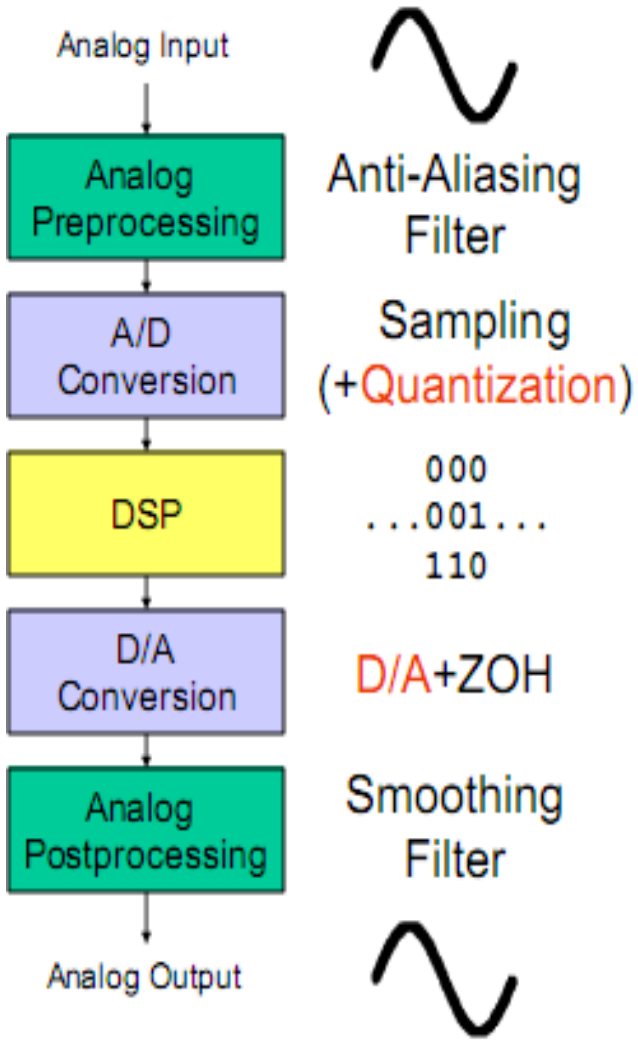
Fig.10.5-10

Attributes:

- Fast, open-loop
- Requires current from the input to charge C_H
- DC voltage offset of the op amp and the charge feedthrough of the switch will create dc errors

Summary

- Sampling theorem $f_s > 2f_{max}$, usually dictates anti-aliasing filter
- If theorem is met, CT signal can be recovered from DT without loss of information
- ZOH and smoothing filter reconstruct CT from DT signal
- Oversampling helps reduce order & complexity of anti-aliasing & smoothing filters



ADC
IN DETAILS

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MODERATE SPEED ADCs

Moderate Speed ADC Topics

- Serial ADCs - require $2^N T$ for conversion where T = period of the clock
  - Types:
    - Single-slope
    - Dual-slope
- Successive approximation ADCs – require NT for conversion where T = the clock period
- 1-bit per stage, pipeline ADCs – require T for conversion after a delay of NT
- Iterative ADCs – require NT for conversion
- Self-calibration techniques

Single-Slope ADCs

Single-Slope ADC

Block diagram:

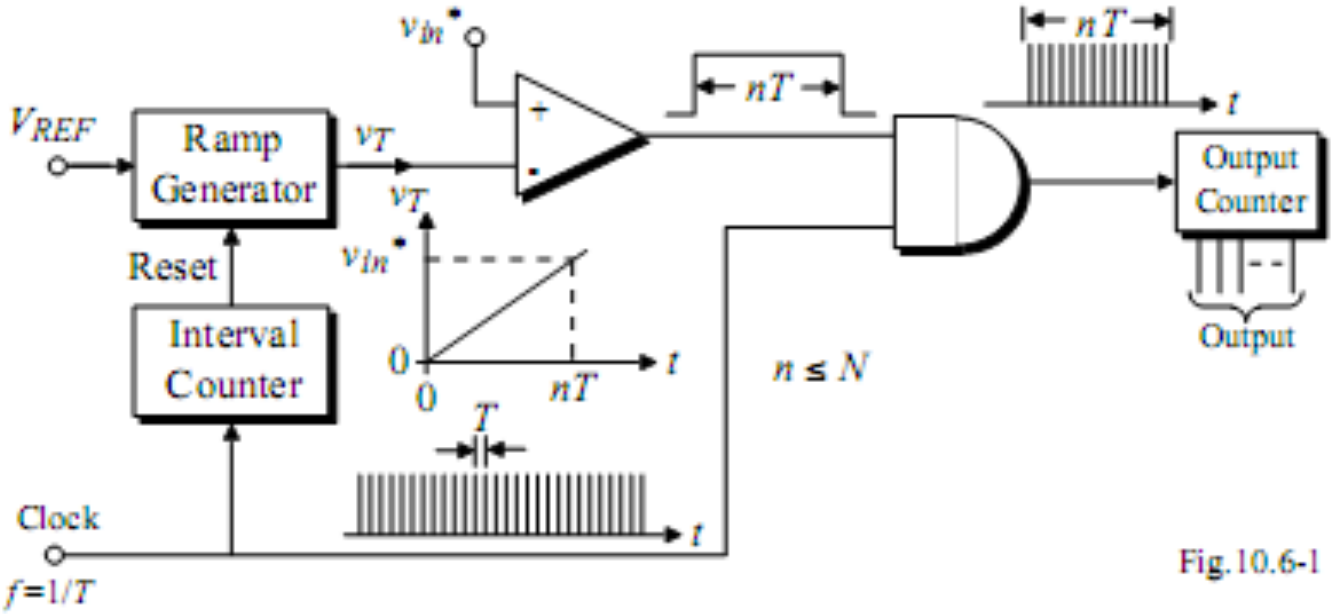


Fig.10.6-1

Attributes:

- Simplicity of operation
- Subject to error in the ramp generator
- Long conversion time $\le 2^N T$

Dual-Slope ADCs

Block diagram:

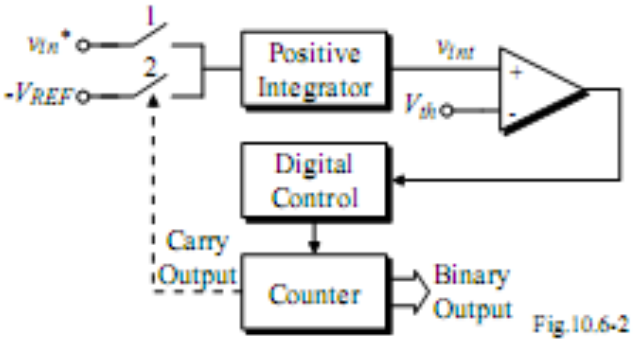


Fig.10.6-2

Waveforms:

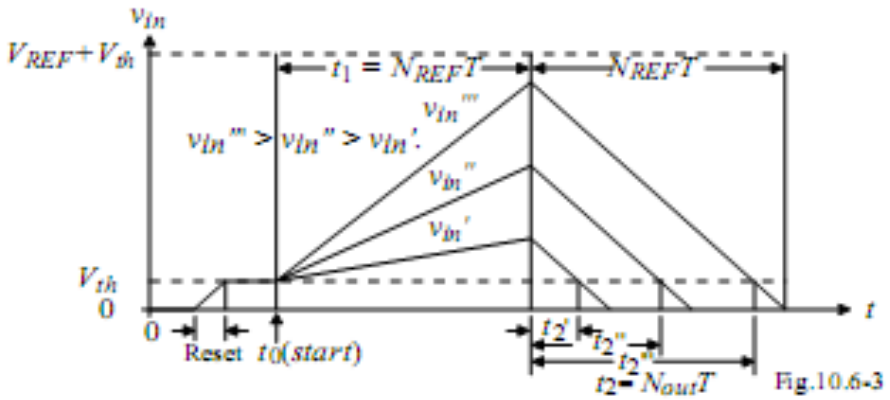


Fig.10.6-3

Operation:

1.) Initially $v_{int} = 0$ and v_{in} is sampled and held ($v_{IN}^* > 0$).

2.) Reset the positive integrator by integrating a positive voltage until $v_{int}(0) = V_{th}$.

3.) Integrate v_{in}^* for N_{REF} clock cycles to get,

$$v_{int}(t_1) = K\int_0^{N_{REF}T} v_{in}^*\,dt + v_{int}(0) = KN_{REF}Tv_{in}^* + V_{th}$$

4.) After N_{REF} counts, the carry output of the counter closes switch 2 and -V_{REF} is applied to the positive integrator. The output of the integrator at $t = t_1+t_2$ is,

$$v_{int}(t_1+t_2) = v_{int}(t_1)+K\int_{t_1}^{N_{out}T}(-V_{REF})dt = V_{th} \rightarrow KN_{REF}Tv_{in}^*+V_{th} - KN_{out}TV_{REF} = V_{th}$$

5.) Solving for N_{out} gives, $N_{out} = N_{REF}(v_{in}^*/V_{REF})$

Comments: Conversion time $\le 2(2^N)T$ and the operation is independent of V_{th} and K.

Dual Slope A/D Converter

PROS

- Conversion result is insensitive to errors in the component values.
- Fewer adverse affects from
- “noise”
- High Accuracy

CONS

- Slow
- Accuracy is dependent on the use of precision external components
- Cost

Introduction

Successive Approximation Algorithm:

1.) Start with the *MSB* bit and work toward the *LSB* bit.

2.) Guess the *MSB* bit as 1.

3.) Apply the digital word 10000.... to a DAC.

4.) Compare the DAC output with the sampled analog input voltage.

5.) If the DAC output is greater, keep the guess of 1. If the DAC output is less, change the guess to 0.

6.) Repeat for the next *MSB*.

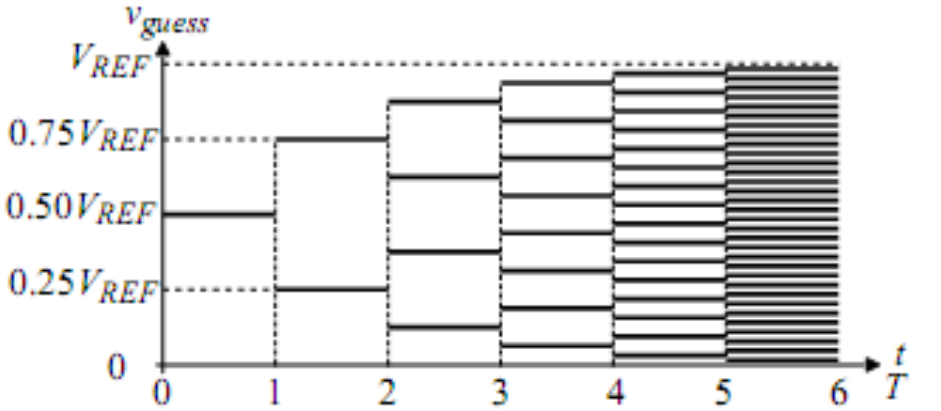


Fig.10.7-2

Block Diagram of a Successive Approximation ADC

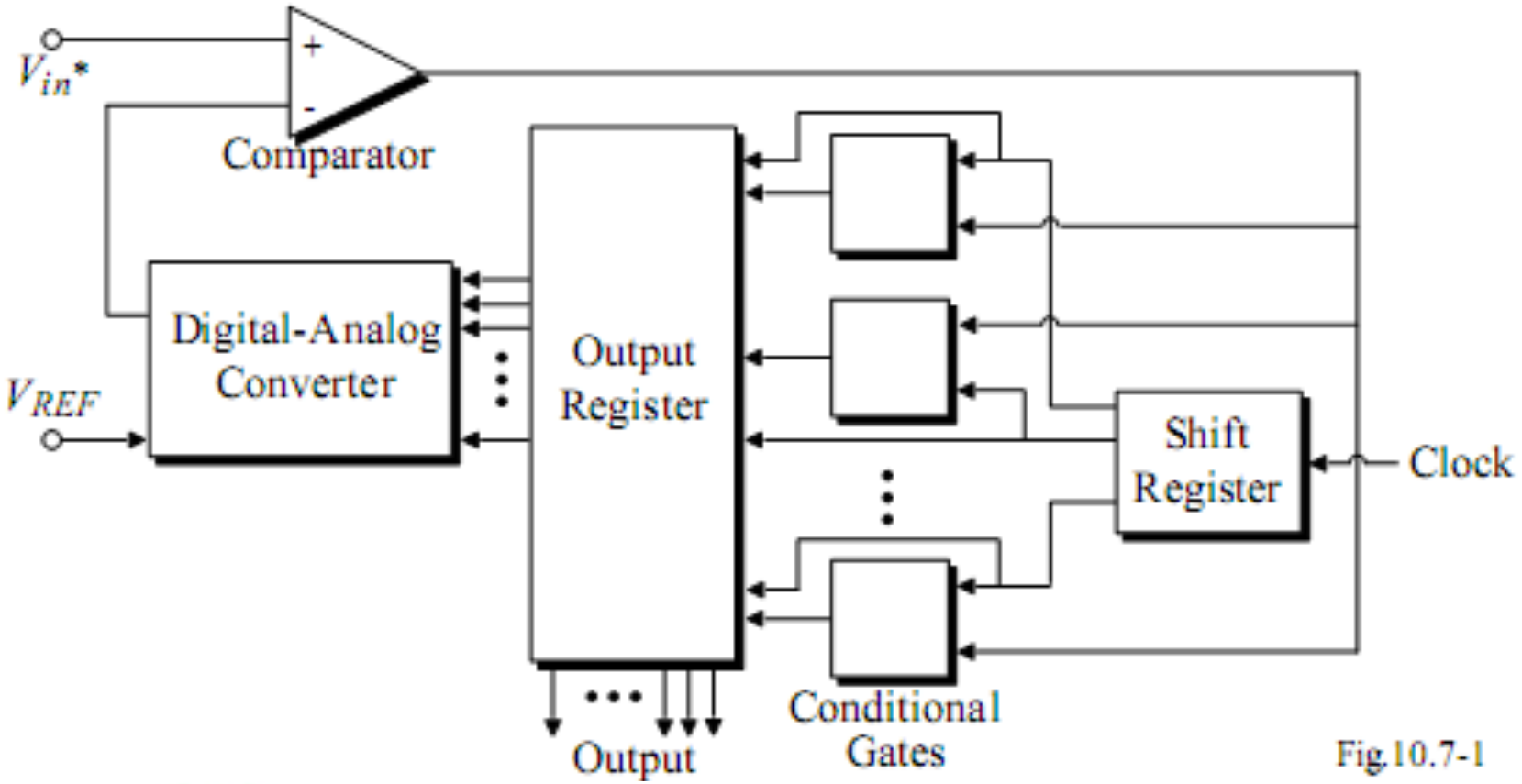
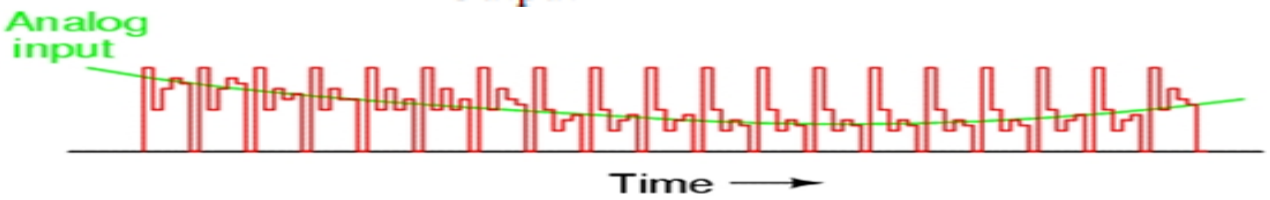
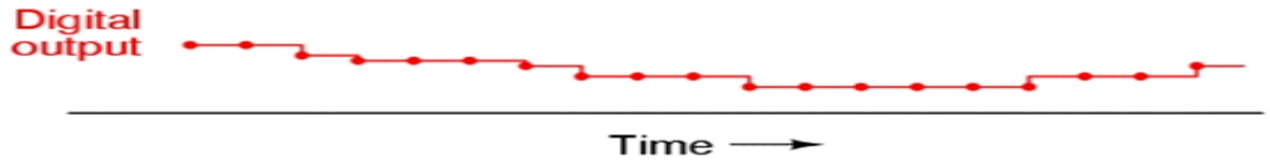


Fig.10.7-1





Successive Approximation Example

Example

- 10 bit ADC
- Vin= 0.6 volts (from analog device)
- V_{ref}=1 volts
- Find the digital value of Vin

Bit	Voltage
9	.5
8	.25
7	.125
6	.0625
5	.03125
4	.015625
3	.0078125
2	.00390625
1	.001952125
0	.0009765625

$N=2^n$ (N of possible states)
N=1024
Vmax-Vmin/N = 1 Volt/1024 = 0.0009765625V of Vref (resolution)

Successive Approximation

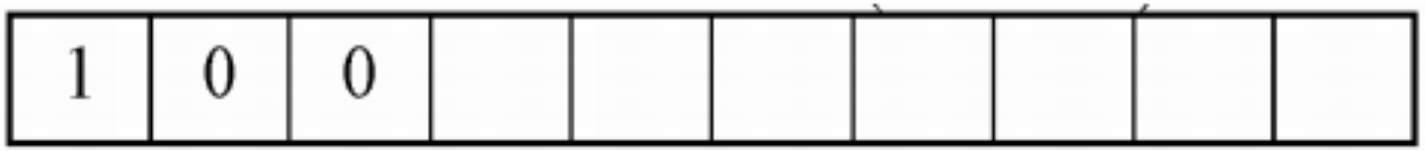
- MSB (bit 9)
  - Divided V_{ref} by 2
  - Compare $V_{ref}/2$ with V_{in}
  - If V_{in} is greater than $V_{ref}/2$, turn MSB on (1)
  - If V_{in} is less than $V_{ref}/2$, turn MSB off (0)
  - V_{in} =0.6V and V=0.5
  - Since V_{in}>V, MSB = 1 (on)

Bit	Voltage
9	.5
8	.25
7	.125
6	.0625
5	.03125
4	.015625
3	.0078125
2	.00390625
1	.001952125
0	.0009765625

1									

Successive Approximation

- Next Calculate MSB-1 (bit 8)
  - Compare V_{in}=0.6 V to V=V_{ref}/2 + V_{ref}/4= 0.5+0.25 =0.75V
  - Since 0.6<0.75, MSB is turned off
- Calculate MSB-2 (bit 7)
  - Go back to the last voltage that caused it to be turned on (Bit 9) and add it to V_{ref}/8, and compare with V_{in}
  - Compare V_{in} with (0.5+V_{ref}/8)=0.625
  - Since 0.6<0.625, MSB is turned off



Successive Approximation

- Calculate the state of MSB-3 (bit 6)
  - Go to the last bit that caused it to be turned on (In this case MSB-1) and add it to $V_{ref}/16$, and compare it to V_{in}
  - Compare V_{in} to $V = 0.5 + V_{ref}/16 = 0.5625$
  - Since 0.6>0.5625, MSB-3=1 (turned on)

MSB	MSB-1	MSB-2	MSB-3	…					
1	0	0	1						

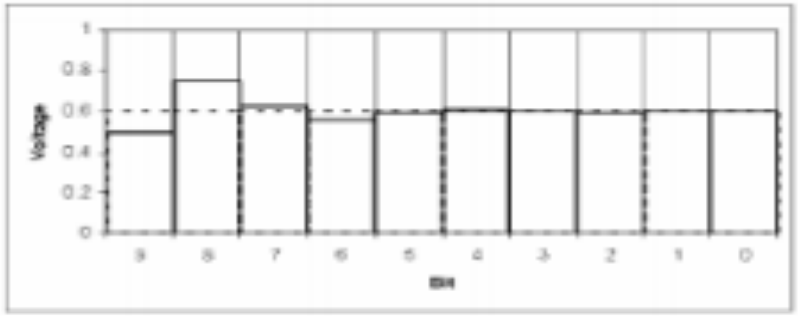
Successive Approximation ADC

- This process continues for all the remaining bits.

•Digital Results:

MSB	MSB-1	MSB-2	MSB-3	…					LSB
1	0	0	1	1	0	0	1	1	0

•Results: $\frac{1}{2}+\frac{1}{16}+\frac{1}{32}+\frac{1}{256}+\frac{1}{512}=.599609375\ \text{V}$



Successive Approximation A/D Converter

PROS

- Capable of high speed and reliable
- Medium accuracy compared to other ADC
- Good tradeoff between speed and cost
- Capable of outputting the binary number in serial (one bit at a time) format

CONS

- Higher resolution successive approximation, ADC's will be slower
- Speed limited to ~5Msps

Summary of Moderate Speed ADCs

Type of ADC	Advantage	Disadvantage
Serial ADC	High resolution	Slow
Voltage-scaling, charge-scaling successive approximation ADC	High resolution	Requires considerable digital control circuitry
Successive approximation using a serial DAC	Simple	Slow
Pipeline algorithmic ADC	Fast after initial latency of NT	Accuracy depends on input
Iterative algorithmic ADC	Simple	Requires other digital circuitry

Successive approximation ADCs also can be calibrated extending their resolution 2-4 bits more than without calibration.

HIGH SPEED ADCs INTRODUCTION

Characteristics of High-Speed ADCs

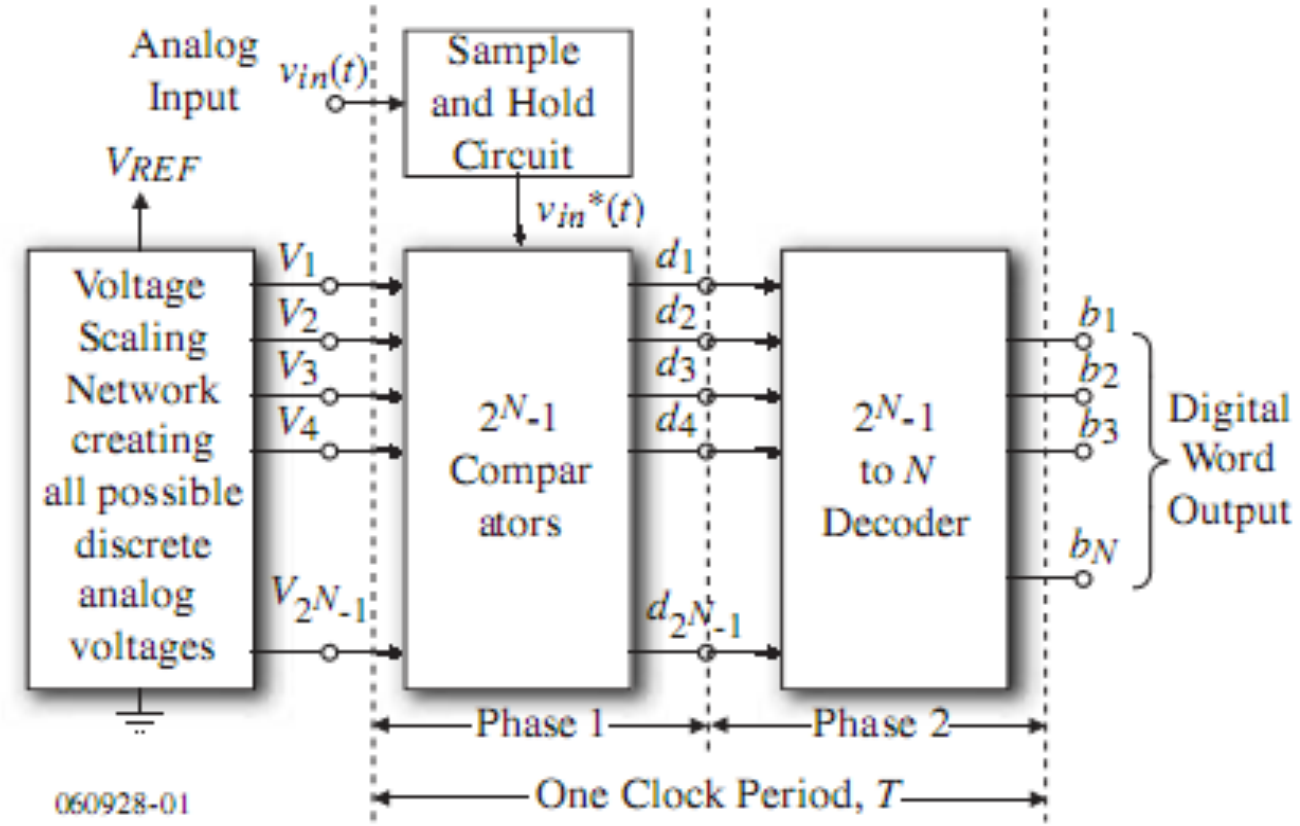
Conversion time is T where T is a clock period.

Types:

- Parallel or Flash ADCs
- Interpolating/averaging ADCs
- Folding ADCs
- Speed-Area Tradeoffs
  - Multiple-Bit, Pipeline ADCs
  - Digital Error Correction
  - Time-Interleaved ADCs

PARALLEL/FLASH ADCs

Parallel/Flash ADC Architecture



- The notation, $v_{in}^*(t)$, means the signal is sampled and held.
- The sample and hold function can be incorporated into the comparators
- The digital words designated as d_i form a thermometer code

A 3-bit, parallel ADC

General Comments:

- Fast, in the first phase of the clock the analog input is sampled and applied to the comparators. In the second phase, the digital encoding network determines the correct output digital word.
- Number of comparators required is 2^N-1 which can become large if N is large
- The offset of the comparators must be less than $\pm V_{REF}/2^{N+1}$
- Errors occur as "bubbles" in the thermometer code and can be corrected with additional circuitry
- Typical sampling frequencies can be as high as 1000MHz for 6-bits in sub-micron CMOS technology.

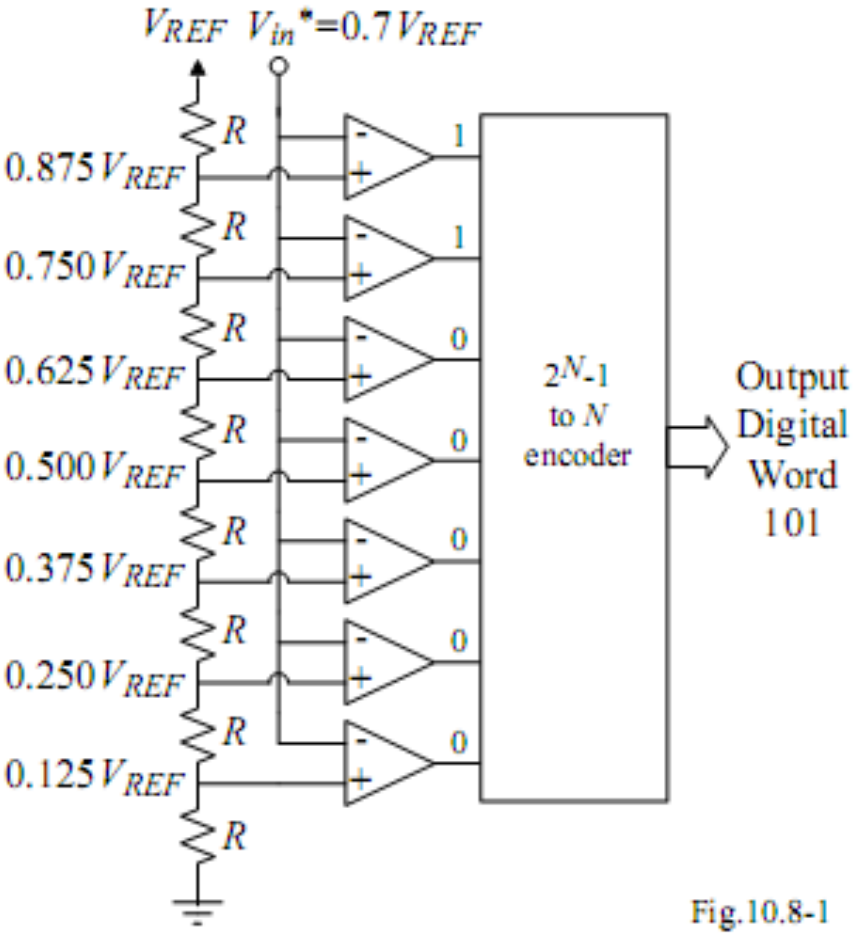


Fig.10.8-1

Example 10.7-1 - Comparator Bandwidth Limitations on the Flash ADC

The comparators of a 6-bit, flash ADC have a dominant pole at 10^4 radians/sec, a dc gain of 10^4 a slew rate of 10V/μs, and a binary output voltage of 1V and 0V. Assume that the conversion time is the time required for the comparator to go from its initial state to halfway to its final state. What is the maximum conversion rate of this ADC if V_{REF} = 1V? Assume the resistor ladder is ideal.

Solution:

The output of the *i*-th comparator can be found by taking the inverse Laplace transform of,

$$\mathcal{L}^{-1}\left[\text{Vout}(s) = \left(\frac{A_o}{(s/10^4)+1}\right)\cdot\left(\frac{V_{in}^* - V_{Ri}}{\text{s}}\right)\right] \quad \rightarrow \quad v_{out}(t) = A_o(1 - e^{-10^4 t})(V_{in}^* - V_{Ri}).$$

The worst case occurs when

$$V_{in}^* - V_{Ri} = 0.5V_{LSB} = V_{REF}/2^7 = 1/128$$

$$\therefore \quad 0.5\text{V} = 10^4(1 - e^{-10^4 T})(1/128) \rightarrow 64\text{x}10^{-4} = 1 - e^{-10^4 T}$$

$$\text{or,} \quad e^{10^4 T} = 1 - 64\text{x}10^{-4} = 0.9936 \rightarrow T = 10^{-4}\ln(1.0064) = 0.6421\,\mu\text{s}$$

$$\therefore \quad \text{Maximum conversion rate} = \frac{1}{0.6421\,\mu\text{s}} = 1.557\text{x}10^6 \text{ samples/second}$$

Checking the slew rate shows that it does not influence the maximum conversion rate.

$$\text{SR} = 10\text{V}/\mu\text{s} \rightarrow \frac{\Delta V}{\Delta T} = 10\text{V}/\mu\text{s} \rightarrow \Delta V = 10\text{V}/\mu\text{s}(0.6421\,\mu\text{s}) = 6.421\text{V} > 1\text{V}$$

Flash A/D Converter

PROS

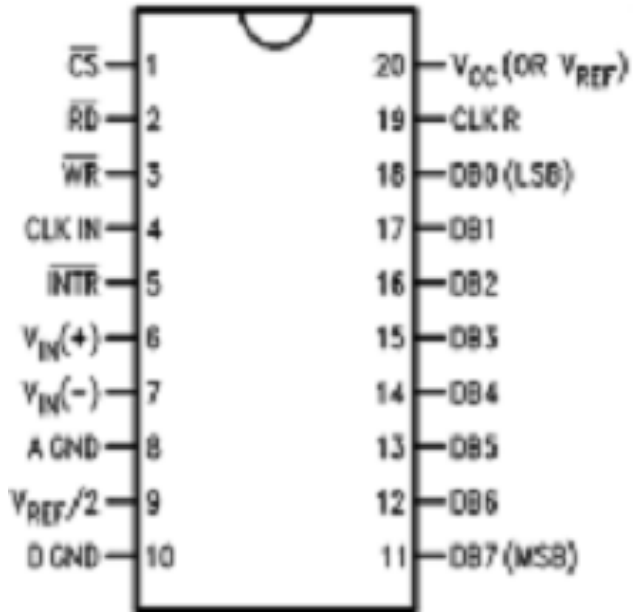
- Very Fast (Fastest)
- Very simple operational theory
- Speed is only limited by gate and comparator propagation delay

CONS

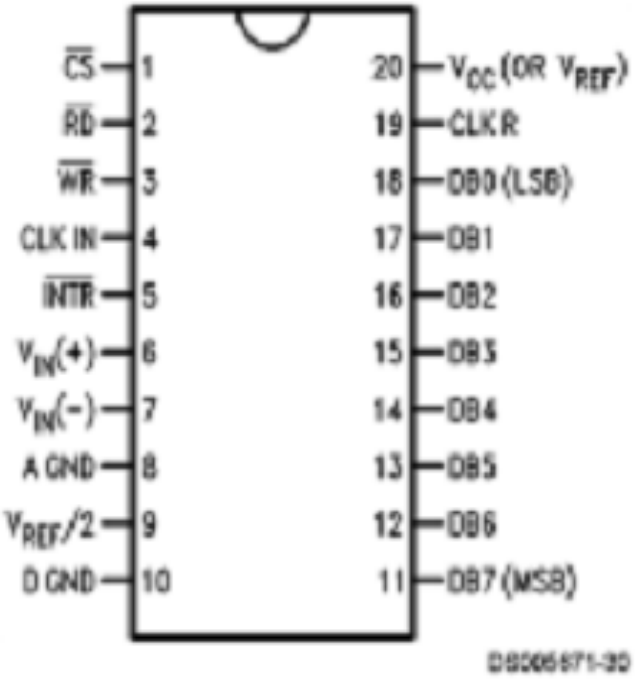
- Expensive
- Prone to produce glitches in the output
- Each additional bit of resolution requires twice the comparators => cost

National Semiconductor ADC0804

- Successive approximation A/D converter
  - 8-bit data: precision = (1/256)Vrange
  - Accuracy: 1 LSB
  - Conversion time: 100μs
  - Input voltage range: 0 to 5v
  - Built-in reference (Vcc/2)
  - Can also use external reference: Vref/2
  - Microprocessor bus compatible



ADC0804 pin diagram



Source: National Semiconductor Data Sheet

DB7-0: data bus interface

CS*: chip select (address)

RD*: read enable (IOR*)

- CS* & RD* active puts data on DB7-0.
- Otherwise, DB7-0 tri-stated

WR*: write enable (IOW*)

- CS* & WR* active triggers new conversion

INTR*: interrupt

- Set to 1 at start of conversion
- Set to 0 when conversion finished
- Set to 1 when data rea

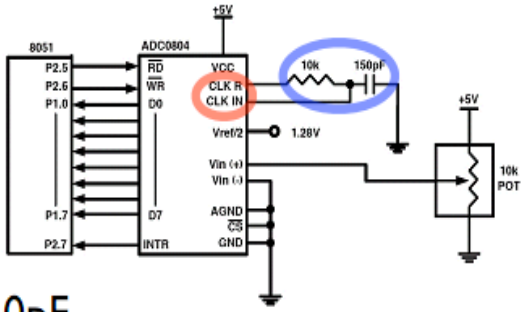
$V_{IN}(+), V_{IN}(-)$ – analog input voltage

CLK IN, CLK R – clock components

Vref/2 – reference voltage (1/2 Vcc if open)

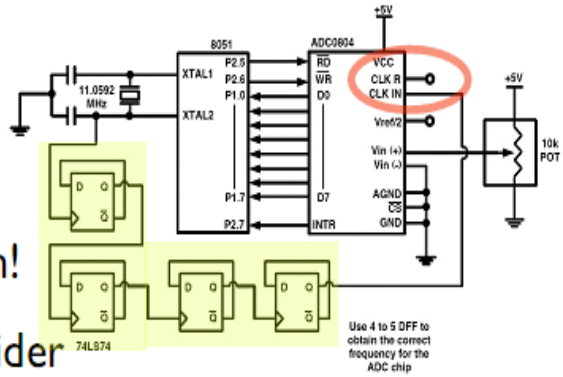
CLK IN and CLK R

- As internal clock
  - Set the R, C value
    $f = 1/(1.1\ RC)$
  - R = 10KΩ, C = 150pF
    $f = 1/(1.1*10^{4}*150*10^{-12})$
    = 606060.6 => 606KHz,
    or 1.65μs cycle time
- Can also take external clock



External clocking scheme for ADC0804

- Could use the same crystal as for 8051
- Issue: freq too high!
- Solution: clock divider
  - cascaded D-flipflops:
    next one is clocked by the prev's Q,
    each feeds /Q to its own D

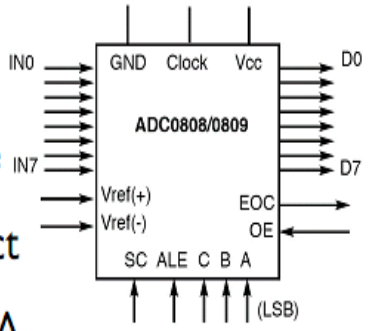


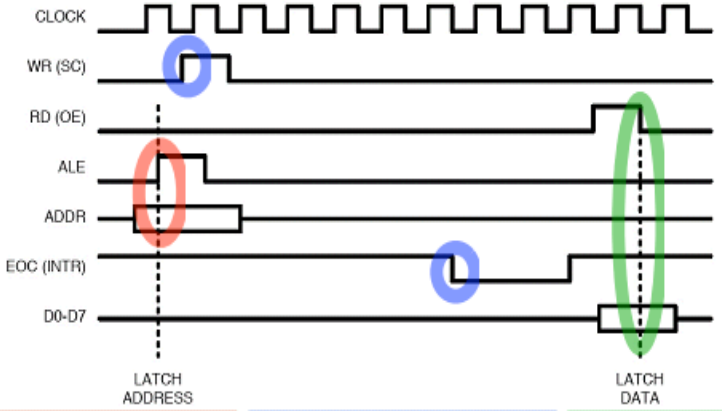
ADC0808/0809: Multi-(Analog)-Channel

- 8 analog input lines
  - Selected by 3-bit, internally share 1 ADC
  - Conceptually, analog multiplexor on input
  - ALE latches the address
- 8-bit output port
  - Similar to the single-channel ADC

Pin interface and timing diagram

- IN0..IN7: analog input channels
- SC, EOC: (=WR, INTR) start conv, end-of-conv
- OE: (=RD) output enable
- C B A : 3-bit channel select
- ALE: clock for latching CBA
- $V_{ref}(+), V_{ref}(-)$: max and "gnd"

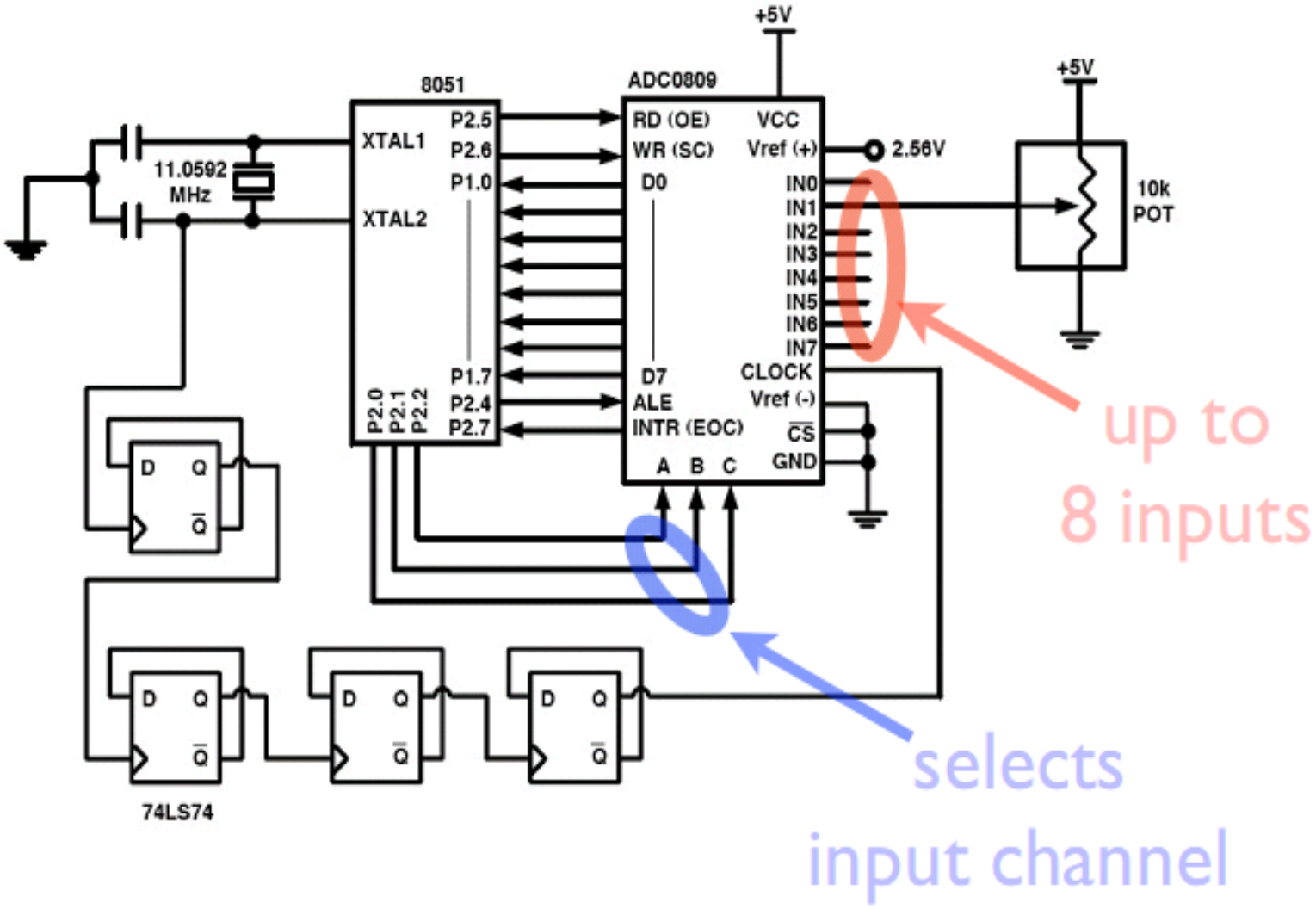




1. set ADDR, pulse ALE
2. pulse SC, wait for EOC
3. read data during OE

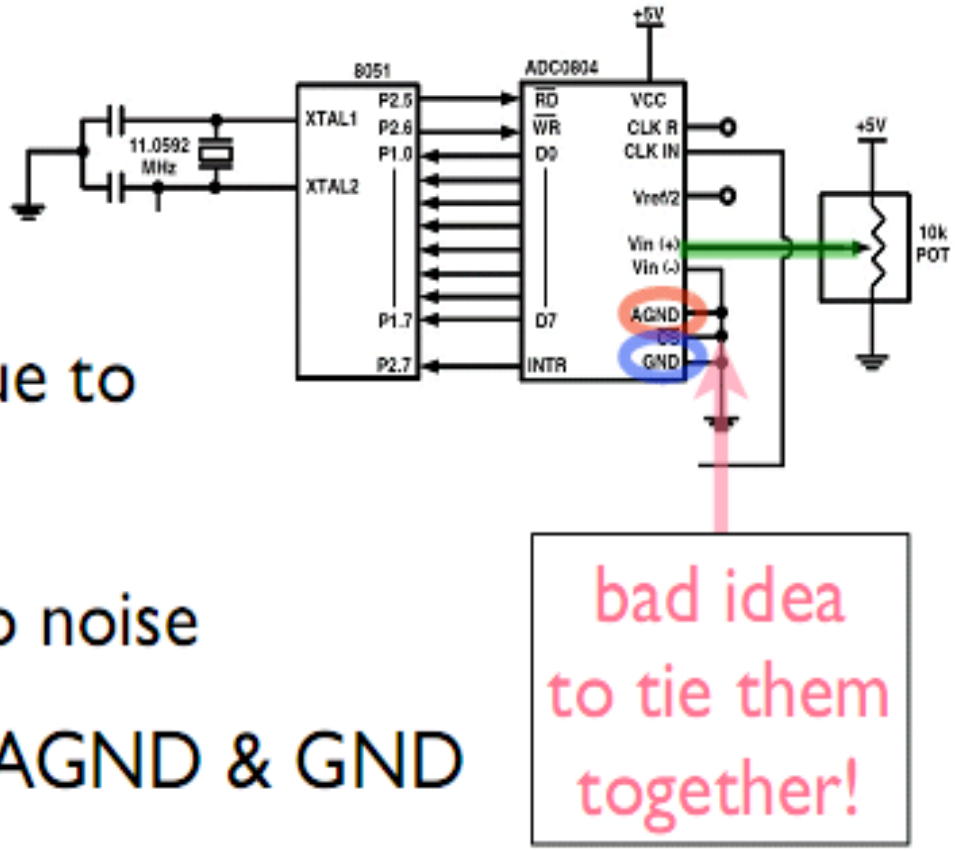
ADDR is formed by C B A

Schematic for ADC0809



Digital vs Analog Ground

- AGND: analog
- GND: digital
- Digital => noisy due to frequent switching
- Analog: sensitive to noise
- Solution: separate AGND & GND
- Keep analog signal lines short



PID Motor Control Using ADC0809

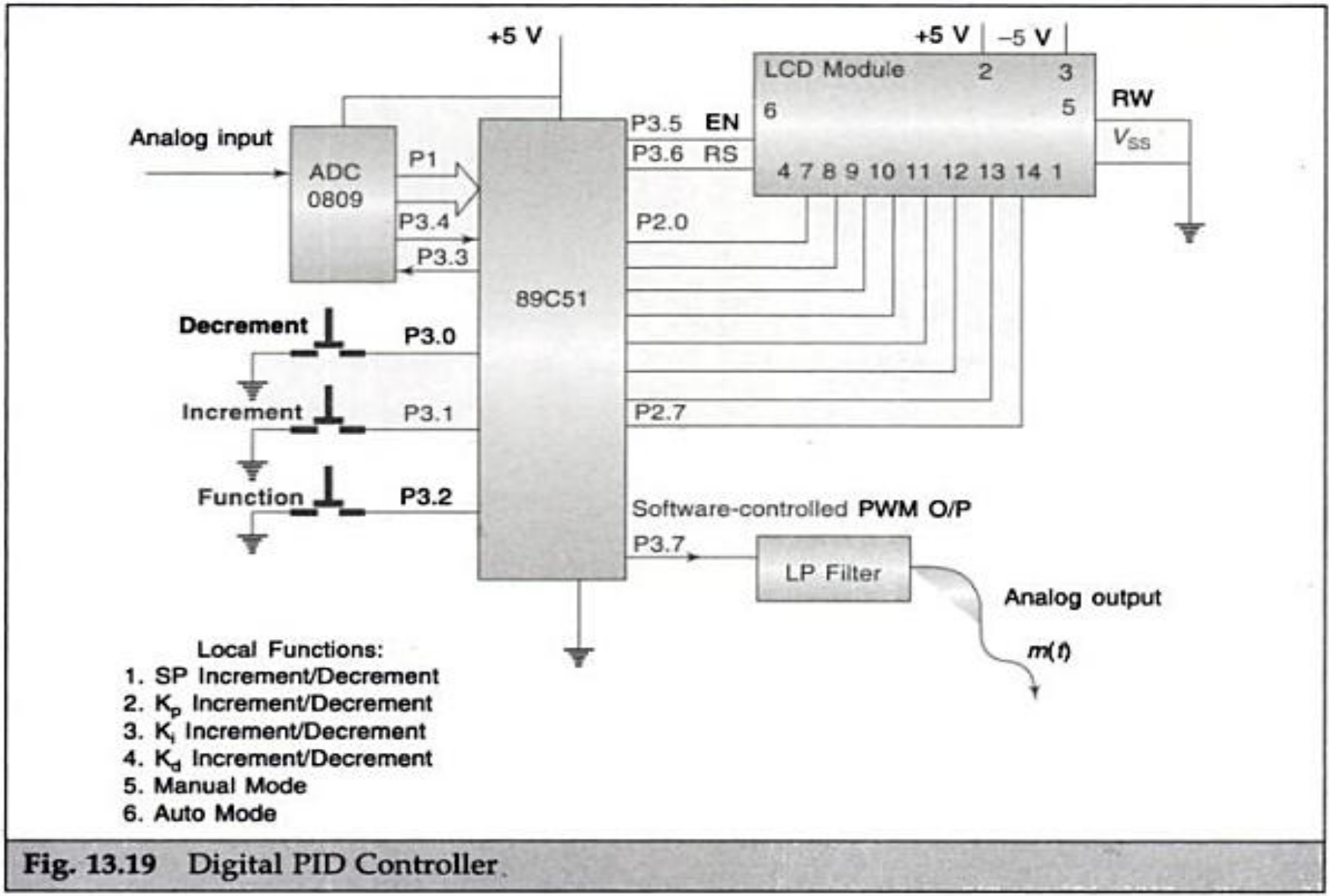


Fig. 13.19 Digital PID Controller