Combinational Circuit design and Simulation Using Gate

Objectives

Topics introduced in this chapter:

- **Draw a timing diagram for a combinational circuit with gate delays.**
- **Define static 0-and 1-hazards and dynamic hazard. Given a combinational circuit, find all of the static 0-and 1-hazards. For each hazard,specify the order in which the gate outputs must switch in order for the hazard to actually produce a false output.**
- **Given switching function, realize it using a two-level circuit which is free of static and dynamic hazards (for single input variable changes).**
- **Design a multiple-output NAND or NOR circuit using gates with limited fan-in.**
- **Explain the operation of a logic simulator that uses four-valued logic.**
- **Test and debug a logic circuit design using a simulator.**

8.2 Design of Circuits with Limited Gate Fan-in

Example: Realize $f(a,b,c,d) = \sum m(0,3,4,5,8,9,10,14,15)$ using 3-input NOR gate

map of f:

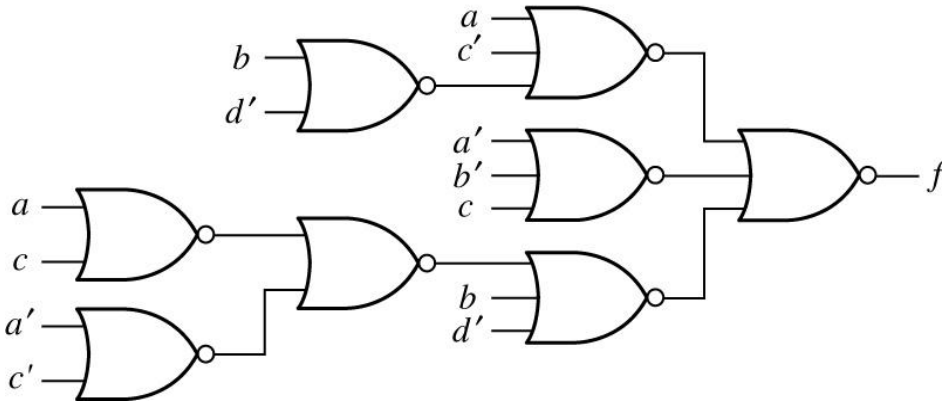
cd \ ab	00	01	11	10
00	1	1	0	1
01	0	1	0	1
11	1	0	1	0
10	0	0	1	1

$$f' = a'b'c'd + ab'cd + abc' + a'bc + a'cd'$$

8.2 Design of Circuits with Limited Gate Fan-in

$$f' = b'd(a'c') + a'c(b + d') + abc'$$

$$f = [b + d' + (a + c)(a' + c')][a + c' + b'd][a' + b' + c']$$



8.2 Design of Circuits with Limited Gate Fan-in

Example: Realize the functions given in Figure 8-2,
using only 2-input NAND gates and inverters.

If we minimize each function separately,the result is

$$f_1 = b'c' + ab' + a'b$$
$$f_2 = b'c' + bc + a'b$$
$$f_3 = a'b'c + ab + bc'$$

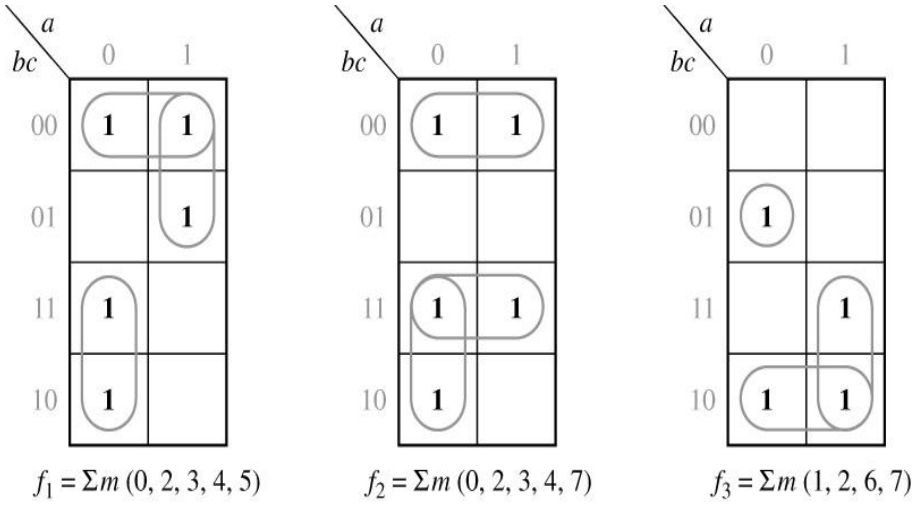


Figure 8-2

8.2 Design of Circuits with Limited Gate Fan-in

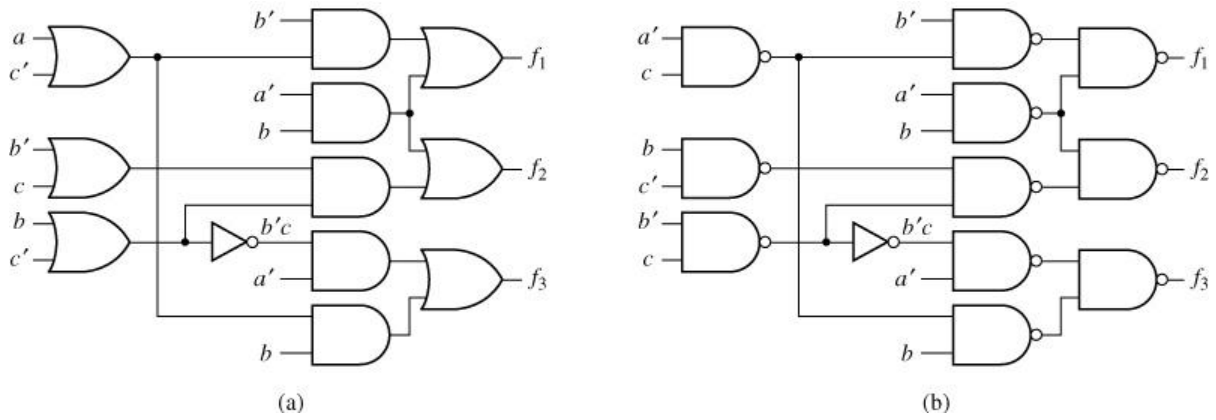


Figure 8-3: Realization of Figure 8-2

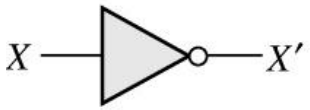
$$f_1 = b'(a'+c') + a'b$$
$$f_2 = b(a'+c) + b'c'$$
$$f_3 = a'b'c + b(a+c')$$

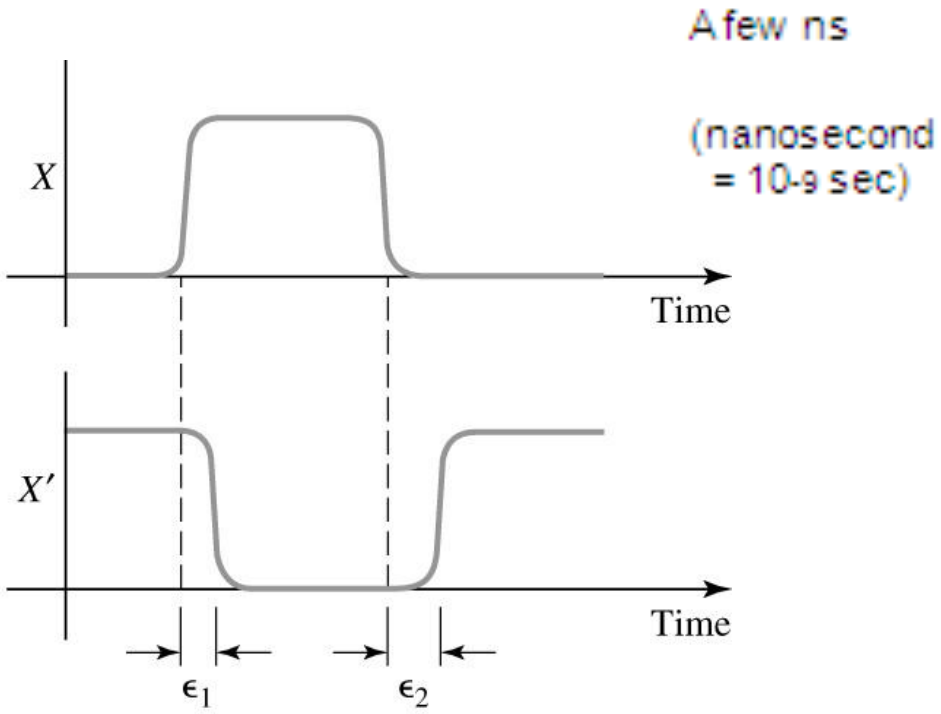
$$f_2 = (b'+c)(b+c') + a'b$$

$$a'b'c = a'(b'c) = a'(b+c')'$$

8.3 Gate Delays and Timing Diagrams

Propagation Delay in an Inverter

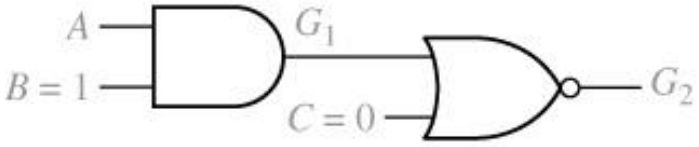


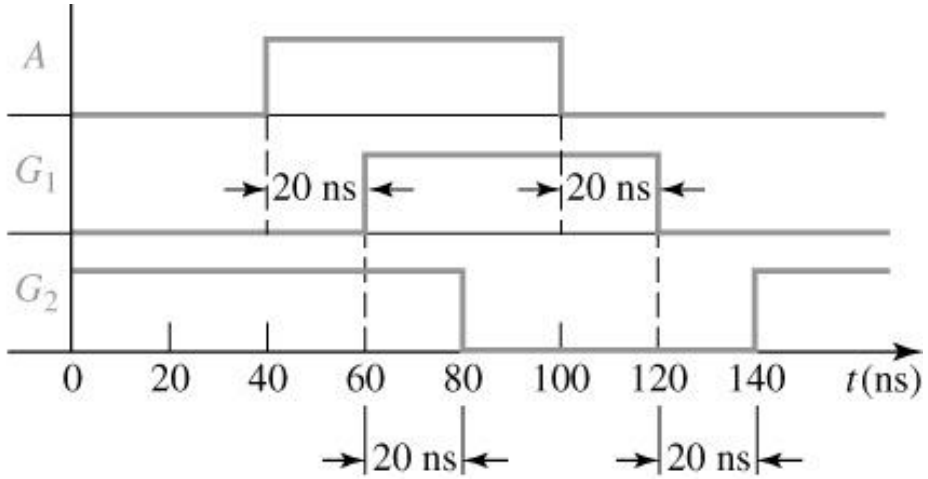


- Output of logic gates take some time to change value (propagation delay)
- The propagation delay may be different for input 0 → 1, and 1 → 0

8.3 Gate Delays and Timing Diagrams

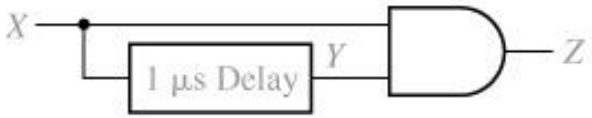
Ex: Timing Diagram for AND-NOR Circuit

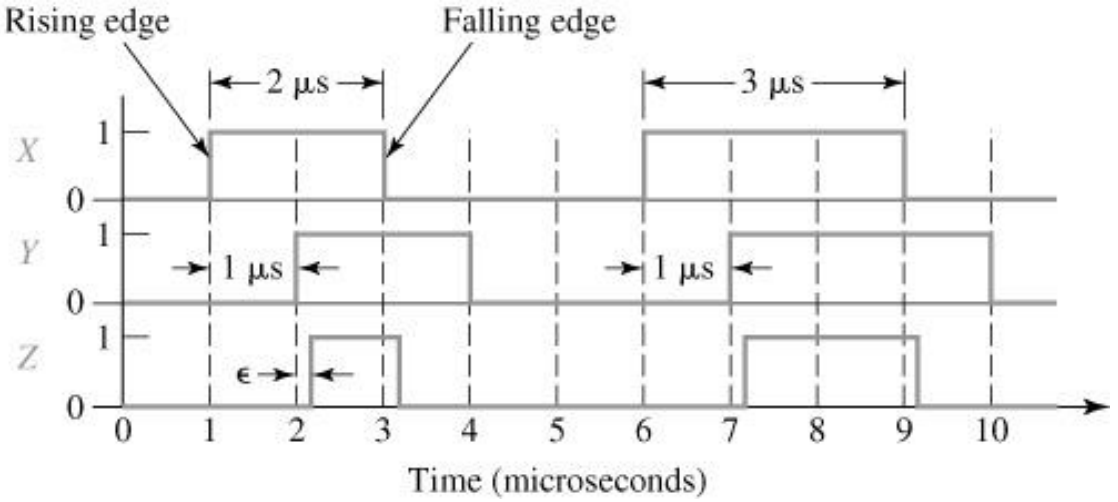




8.3 Gate Delays and Timing Diagrams

Timing Diagram for Circuit with Delay





④ The input X consists of two pulses:

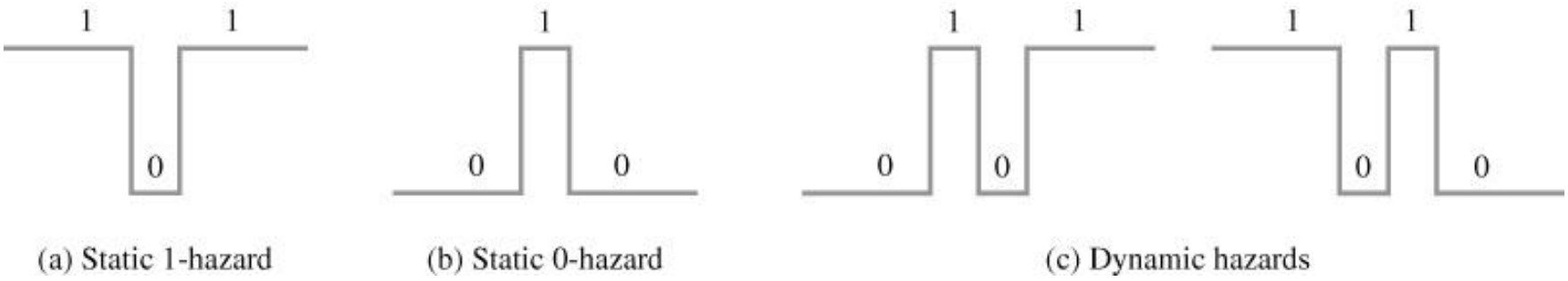
④ The first of which is 2 microseconds (2×10^{-6} second) wide and the second is 3 microseconds wide.

8.4 Hazards in Combinational Logic

④ Static 1-hazard: a circuit output may momentarily go to 0 when it should remain a constant 1.

④ Static 0-hazard: a circuit output may momentarily go to 1 when it should remain a constant 0.

④ Dynamic hazard: output change 3 or more time s when the output changes from 0 to 1 (1to 0)

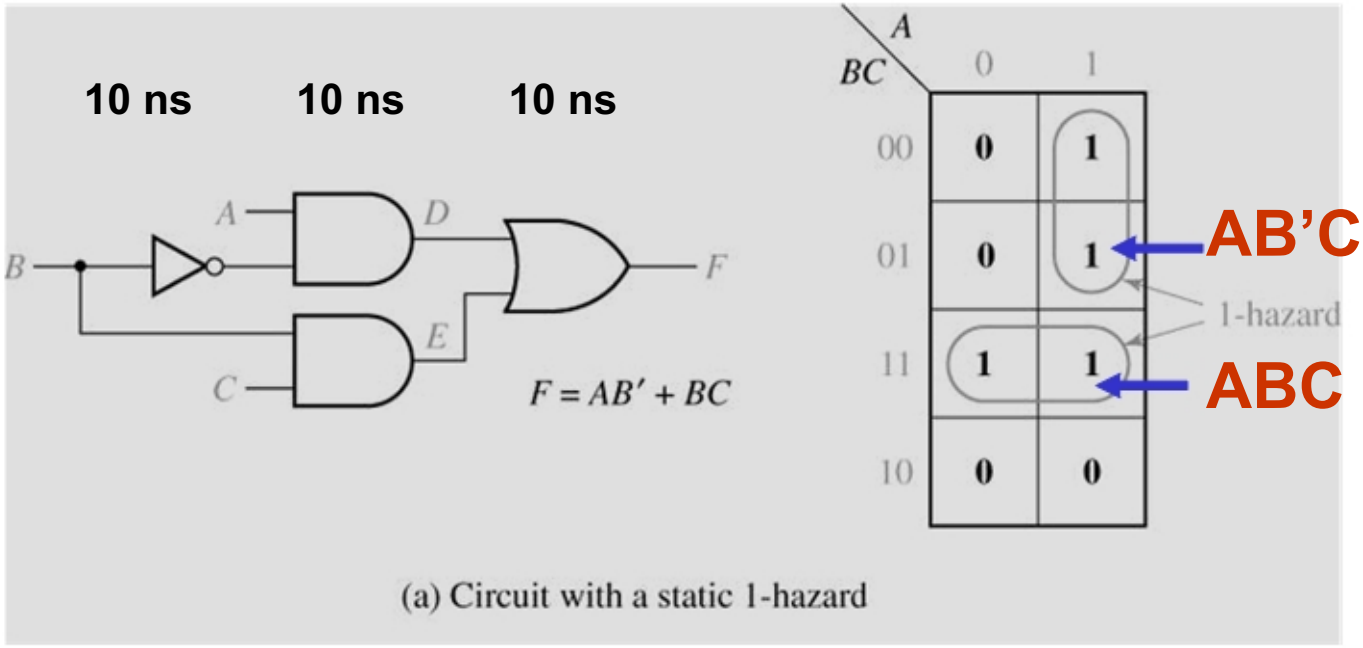


Types of Hazards

Example (1/2)

④ Example of 1-hazard: (Fig. 8-8)

1. A = C =1
2. After B changes to 0, both B and B' are 0 until the propagation delay is elapsed.

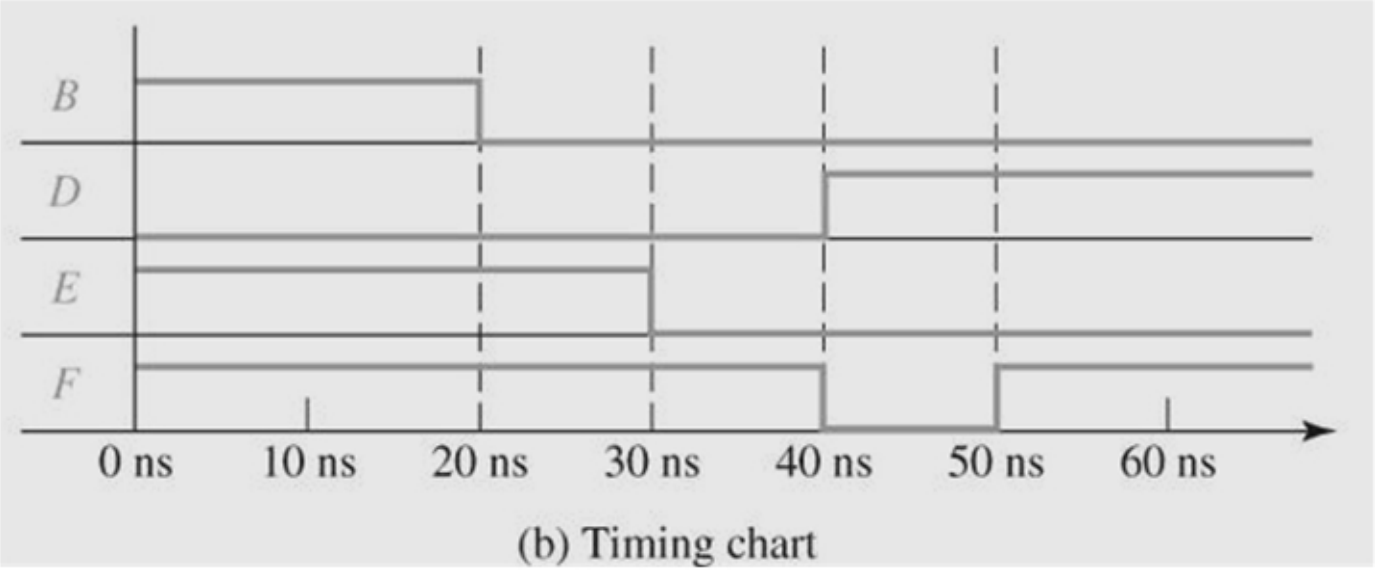


(a) Circuit with a static 1-hazard

Example (2/2)

④ Check hazard from K-map: No loops cover b oth minterms ABC and AB'C.

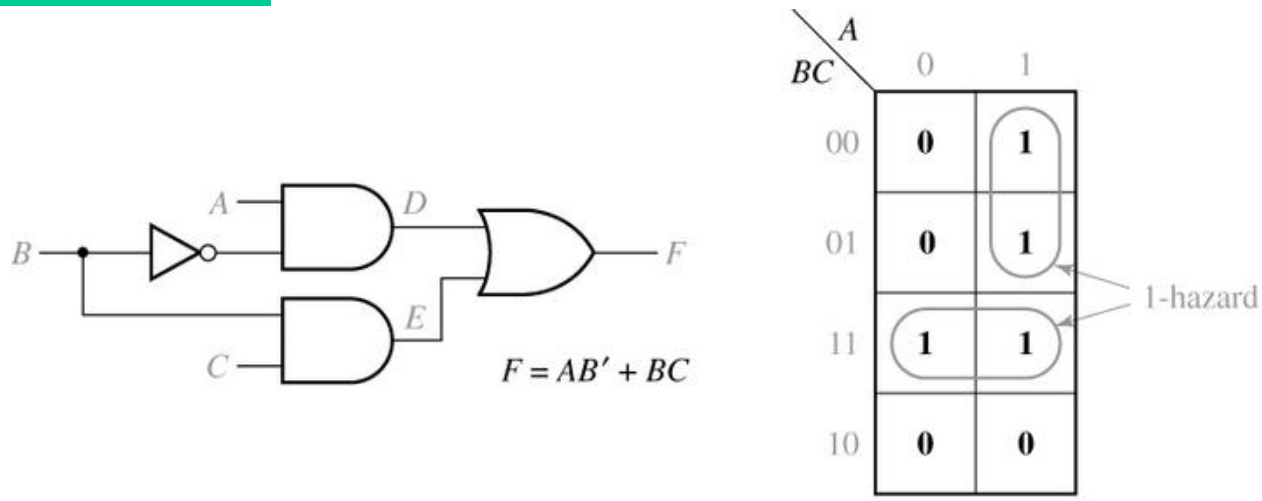
↱ When A = C = 1, B changes => Both term s go momentarily to 0 ↱ Glitch in F.



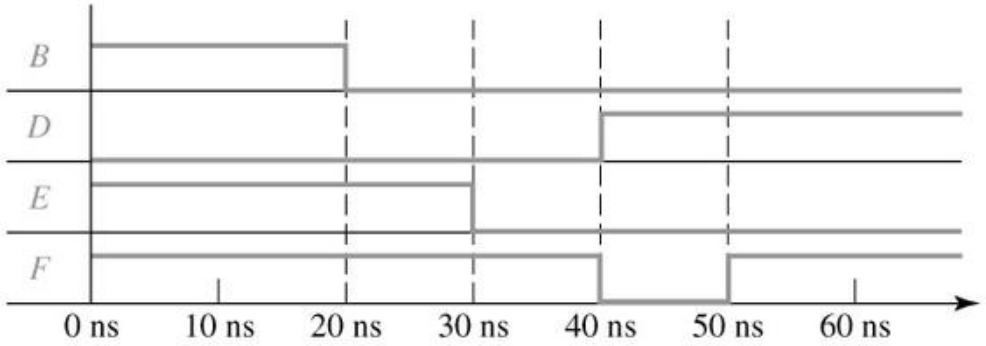
(b) Timing chart

8.4 Hazards in Combinational Logic

Detection of a 1–Hazard



(a) Circuit with a static 1-hazard

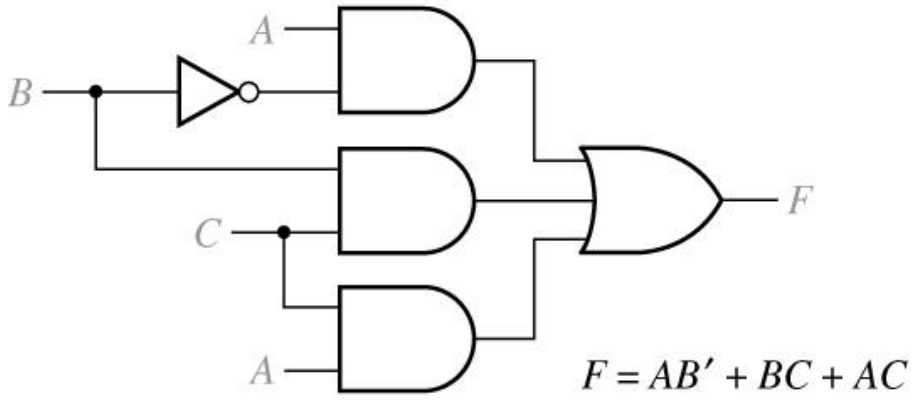


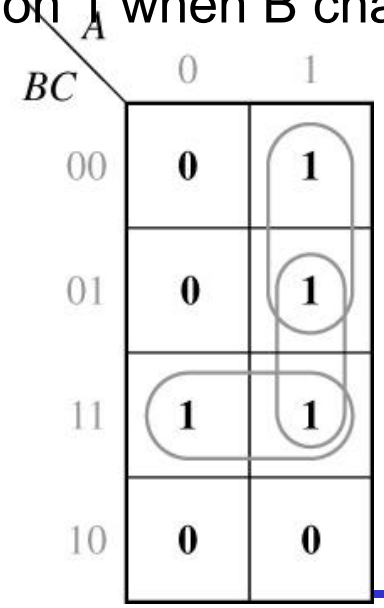
(b) Timing chart

Hazard in 2-level AND-OR network

1. Write down SOP form.
2. Plot each term on map and loop it.
3. If any two adjacent 1's are not covered by the same loop, a 1-hazard exists. For an n-variable map, this transition occurs when one variable changes an d the other (n-1) variables are held constant.
4. Solution: Insensitive to change of B: AC keeps on 1 when B changes.

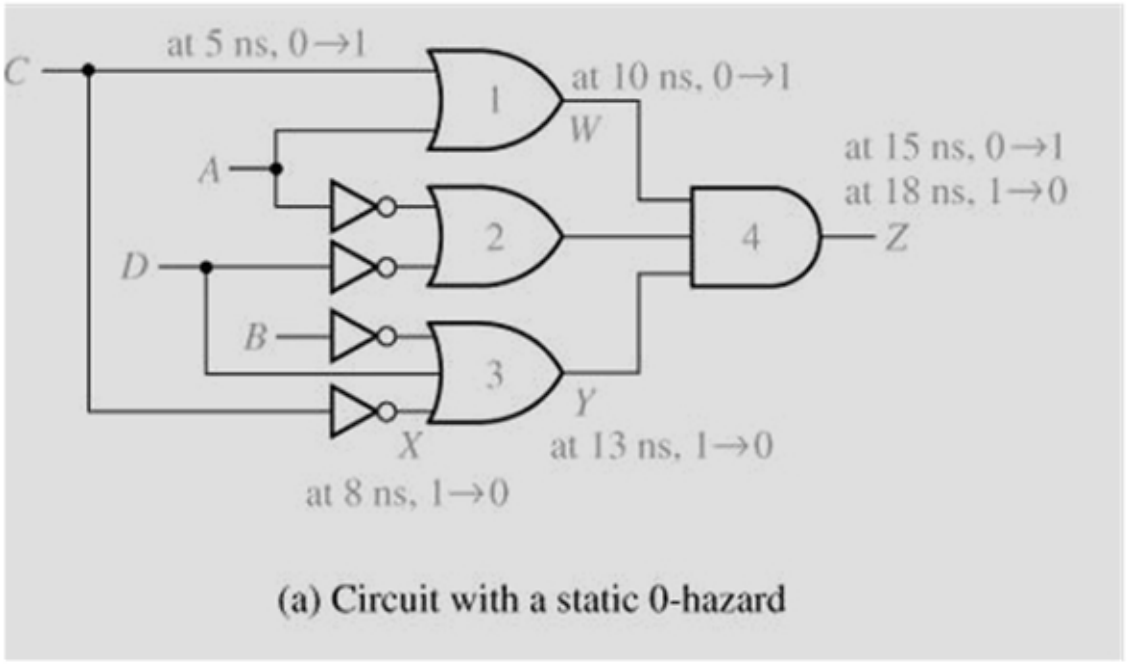
Circuit with Hazard Removed



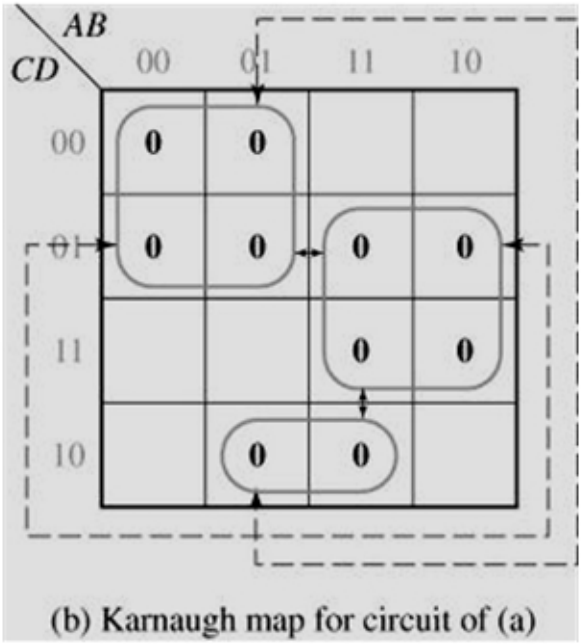


Example (1/3)

1. **A = 0, B = 1, D = 0, C from 0 to 1**
   ⇒ 0-hazard
2. Delay: Invert: 3ns AND/OR: 5ns

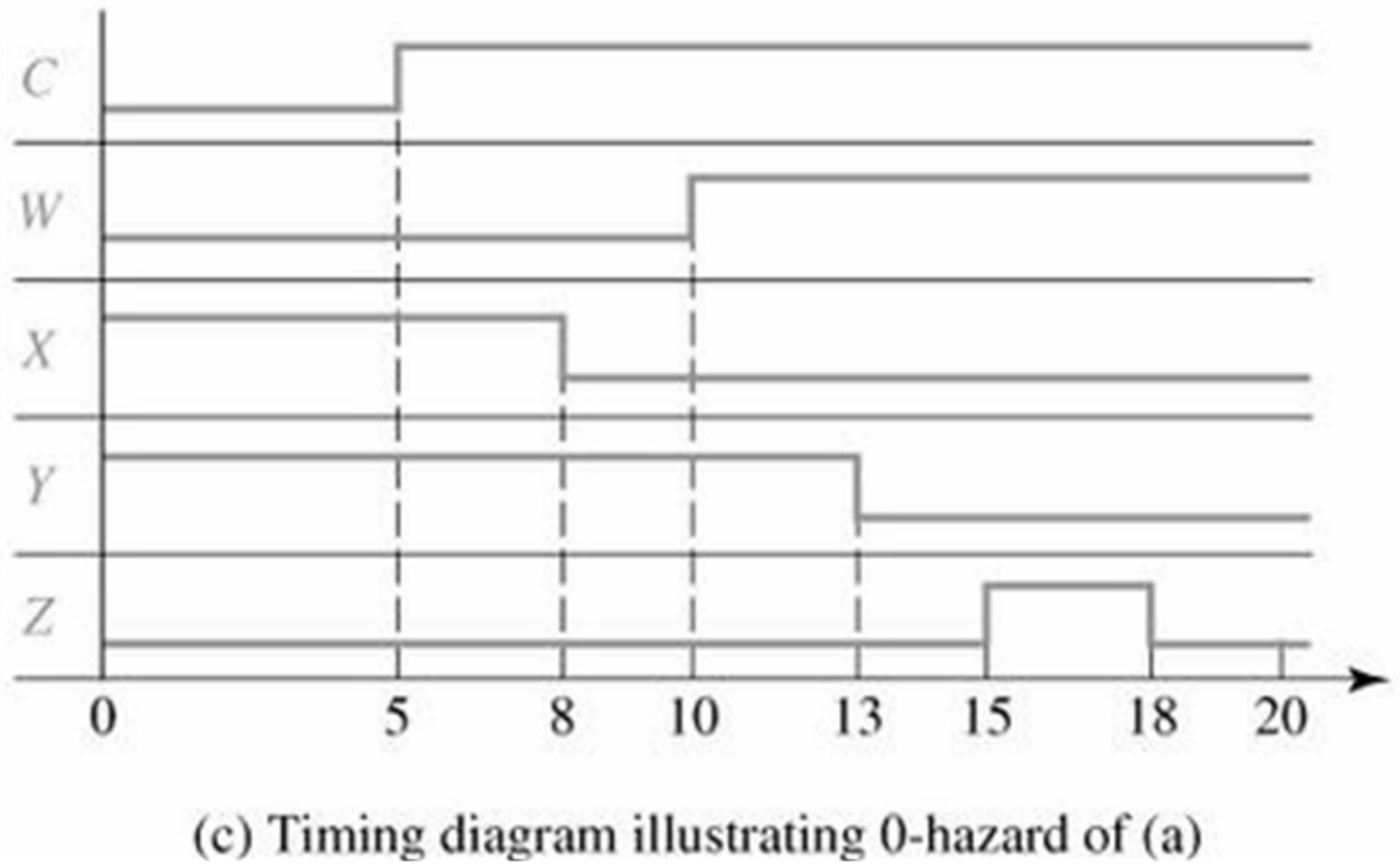


(a) Circuit with a static 0-hazard



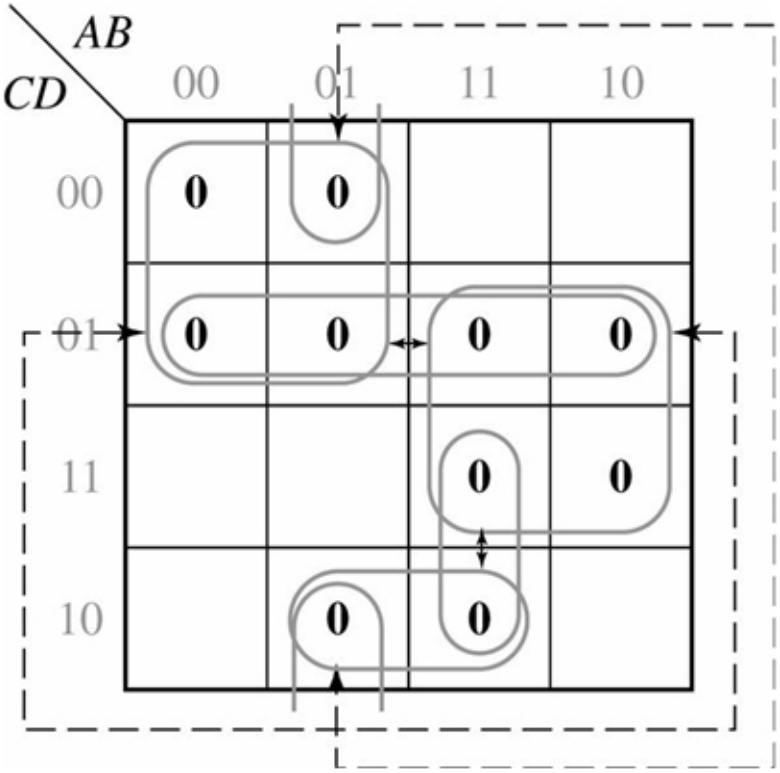
(b) Karnaugh map for circuit of (a)

Example (2/3)



(c) Timing diagram illustrating 0-hazard of (a)

Example (3/3)



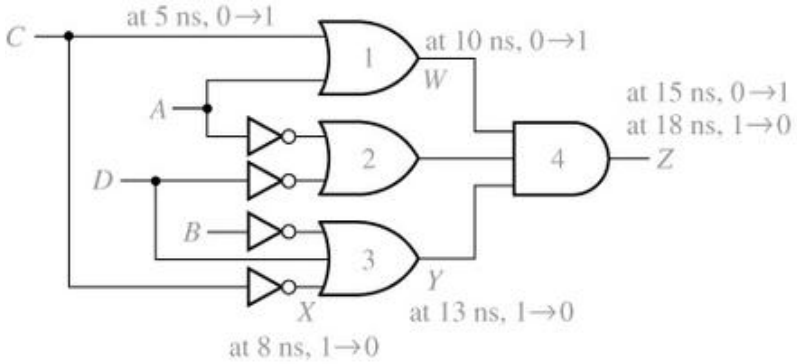
♍ Add 3 addition loops

♎ F = (A + C)(A' + D')(B' + C' + D) (C + D')(A + B' + D)(A' + B' + C')

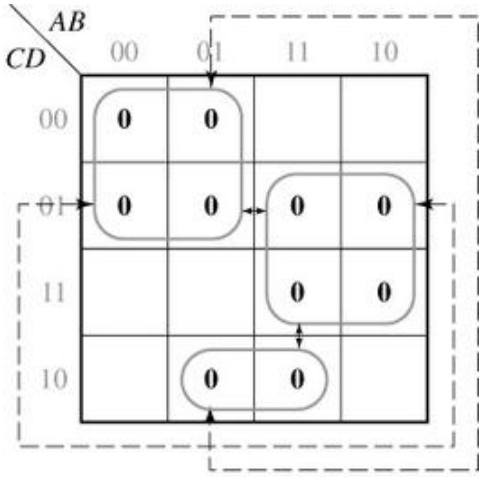
8.4 Hazards in Combinational Logic

Detection of a Static 0-Hazard

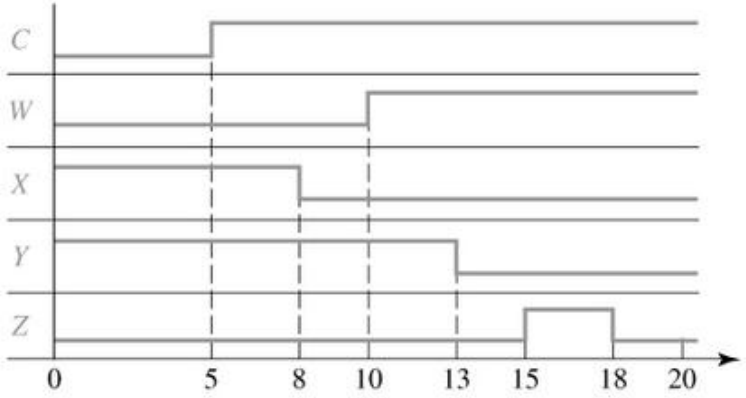
$$F = (A + C)(A' + D')(B' + C' + D)$$



(a) Circuit with a static 0-hazard



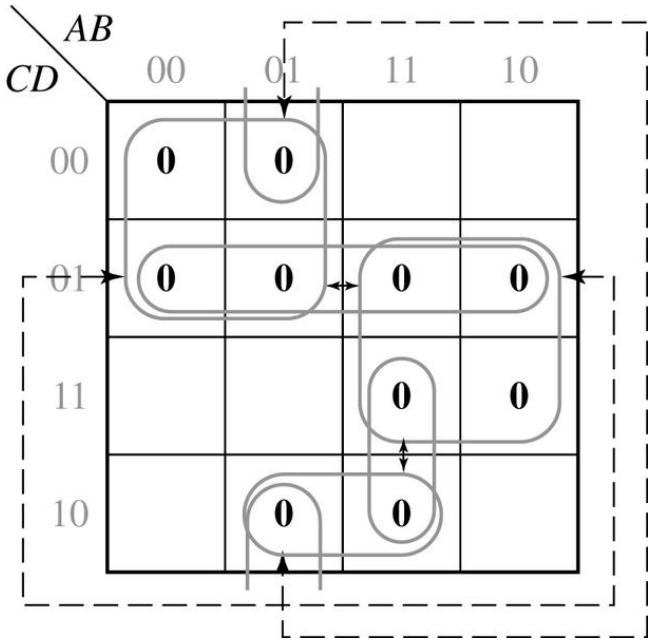
(b) Karnaugh map for circuit of (a)



(c) Timing diagram illustrating 0-hazard of (a)

8.4 Hazards in Combinational Logic

Karnaugh Map Removing Hazards



$$F = (A + C)(A' + D')(B' + C' + D)(C + D')(A + B' + D)(A' + B' + C')$$

Simulation of Logic Gates

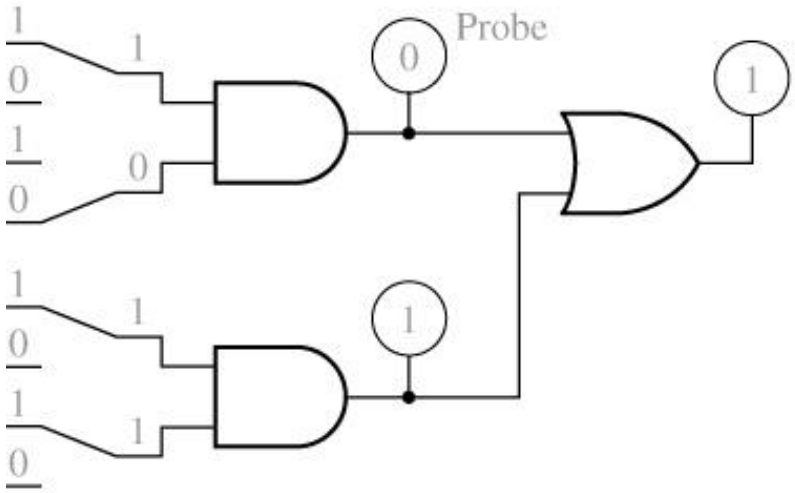
④ **Logic circuits are verified by**

- Actually build them
- Computer simulation

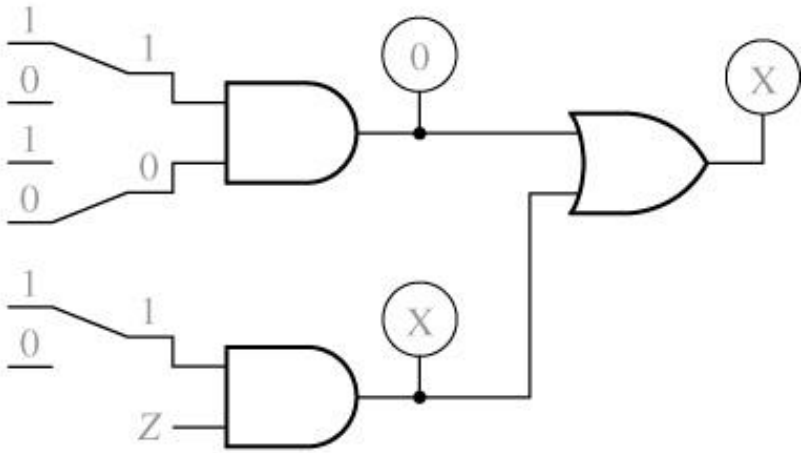
1) Computations are performed stage-by-stage (From input)

2) Evaluations are performed every time inputs change.
   - X: value of gate input is unknown Z: open circuit or high-impedance (hi-Z)

8.5 Simulation and Testing of Logic Circuit



(a) Simulation screen showing switches



(b) Simulation screen with missing gate input

Four-valued logic values:

0,1,X(unknow), Z(hi-Z)

8.5 Simulation and Testing of Logic Circuit

And and OR Functions for Four-Valued Simulation

x	0	1	X	Z
0	0	0	0	0
1	0	1	X	X
X	0	X	X	X
Z	0	X	X	X

AND Gate

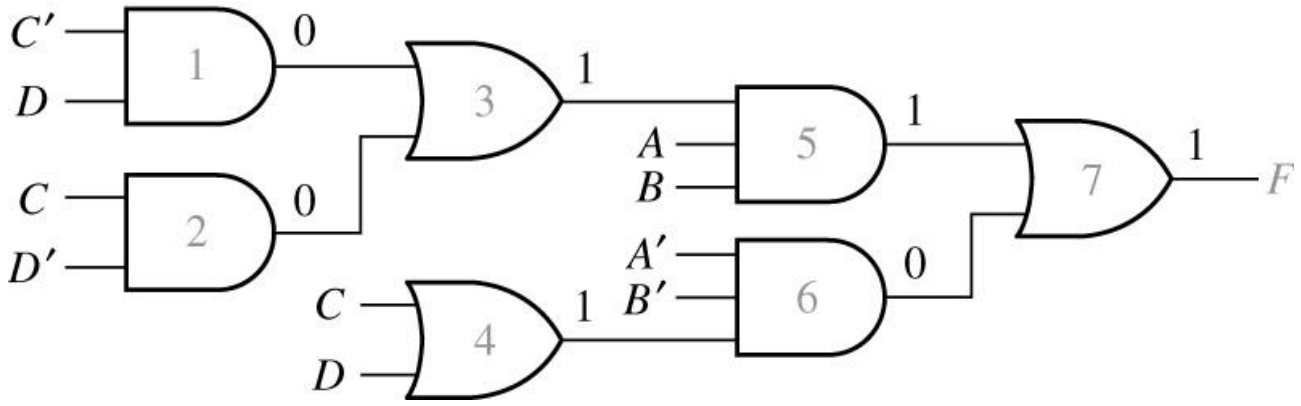
+	0	1	X	Z
0	0	1	1	1
1	1	1	1	1
X	X	1	X	X
Z	X	1	X	X

OR Gate

8.5 Simulation and Testing of Logic Circuit

Logic Circuit with Incorrect Output

Example: $F = AB(CD'+CD') + A'B'(C + D)$



Possible Errors in Your Designs

- In simulations:
  - Incorrect design
  - Gates connected wrong
  - Wrong input signals to the circuits
- In actual circuits
  - Defective gates
  - Defective connecting wires