## 2025 Digital IC Design Homework 5

Simulation Result  Functional simulation  Pass Pattern 7: area = 0f37c  [FASS] Pattern 8: area = 01066  [FASS] Pattern 8: area = 01066  [FASS] Pattern 9: area = 1567a  All 10 patterns passed!  Cycle: 3372  "Note: Ofinish : D:/intelFFGA/DIC/BMS/Destfixture.sv(82)  "Note: Ofinish : D:/intelFFGA/DIC/BMS/Dic/BMS/Destfixture.sv(82)  "Note: Ofinish : D:/intelFFGA/DIC/BMS/Dic/BMS/Destfixture.sv(82)  Time: 33725 ns Iteration: 0 Instance: /testfixture  Synthesis Result  Total logic elements  2,499 / 55,856 ( 4 % )  Total registers  513	2025 Digital IC Design Homework 5						
Simulation Result  Functional simulation  Pass   Pre-Layout simulation   Pass   Pass	NAME 陳冠言						
Functional simulation  Pass   Pre-Layout simulation   Pass   Simulation   Pass   Pre-Layout simulation   Pass   Pass   Pasteen 7: area = 0.026   Pass   Pasteen 7: area = 0.026   Pass   Pasteen 8: area = 0.026   Pass   Pasteen 8: area = 0.026   Pass   Pass   Pasteen 9: area = 1.026   Pass   Pasteen 9: area = 1.026   Pasteen 9: ar	Student ID P76134082						
simulation    Cass   Pass   Simulation   Pass   Pa	Simulation Result						
[PASS]   Pattern 8: area = 01066	Pass				•	Pass	
Total logic elements  2,499 / 55,856 ( 4 % )  Total memory bits  0 / 2,396,160 ( 0 % )  Total registers  513  Embedded multiplier 9-bit elements  6 / 308 ( 2 % )  Clock period (ns)  24 ns  Total Cycle used  3373  Flow Summary  ← <filter>&gt; Flow Status Quartus Prime Version Revision Name  MCH Top-level Entity Name MCH Top-level Entity Name MCH Top-level Entity Name MCH Total logic elements  7 (2,499 / 55,856 ( 4 % )  Total logic elements  2,499 / 55,856 ( 4 % )  Total registers  513  Total logic elements  2,499 / 55,856 ( 4 % )  Total registers  513  Total pins  36 / 325 (11 % )  Total wirtual pins  0 / 2,396,160 (0 % )  Embedded Multiplier 9-bit elements  6 / 308 ( 2 % )  7 ( 4 ( 0 % )</filter>	## PASS Pattern 8: area = 01066  ## [PASS] Pattern 8: area = 01066  ## [PASS] Pattern 9: area = 15e7a  ## [PASS] Pattern 9: area = 15e7a  ## All 10 patterns passed!  ## Cycle: 3372  ## Note: Sfinish : D:/intelFPGA/DIC/HW5/testfixture.sv(82)						
Total memory bits  Total registers  513  Embedded multiplier 9-bit elements  6 / 308 ( 2 % )  Clock period (ns)  24 ns  Total Cycle used  3373  Flow summary	Synthesis Result						
Total registers  Embedded multiplier 9-bit elements  6 / 308 ( 2 % )  Clock period (ns)  24 ns  Total Cycle used  3373	Total logic elements			2,499 / 55,856 ( 4 % )			
Embedded multiplier 9-bit elements 6 / 308 ( 2 % )  Clock period (ns) 24 ns  Total Cycle used 3373  Flow Summary  Concept Cycle Service Servic	Total memory bits			0 / 2,396,160 ( 0 % )			
Clock period (ns)  Total Cycle used  3373  Flow Summary	Total registers			513			
Total Cycle used    Sara   Sara	Embedded multiplier 9-bit elements			6/308(2%)			
Total Cycle used   3373	Clock period (ns)			24 ns			
Flow Summary  C <filter>&gt; Flow Status  Quartus Prime Version  Revision Name  MCH  Top-level Entity Name  MCH  Family  Cyclone IV E  Device  EP4CE55F23A7  Timing Models  Total logic elements  2,499 / 55,856 (4 % )  Total pins  36 / 325 (11 % )  Total wirtual pins  Total memory bits  D/ 2,396,160 (0 % )  Embedded Multiplier 9-bit elements  6 / 308 (2 % )  Total PLLs  Successful - Sat Jun 07 02:50:37 2025  Successful - Sat Jun 07 02:50:37 2025  Lite Edition  MCH  Cyclone IV E  By Cyclone IV E  By Cyclone IV E  By Cyclone IV E  Device  EP4CE55F23A7  Timing Models  Final  Total registers  513  Total pins  36 / 325 (11 % )  Total wirtual pins  0  Total Multiplier 9-bit elements  6 / 308 (2 % )  Total PLLs  0 / 4 (0 % )</filter>	Total Cycle used			3373			
Flow Status   Successful - Sat Jun 07 02:50:37 2025     Quartus Prime Version   20.1.1 Build 720 11/11/2020 SJ Lite Edition     Revision Name   MCH     Top-level Entity Name   MCH     Family   Cyclone IV E     Device   EP4CE55F23A7     Timing Models   Final     Total logic elements   2,499 / 55,856 (4 %)     Total registers   513     Total pins   36 / 325 (11 %)     Total virtual pins   0     Total memory bits   0 / 2,396,160 (0 %)     Embedded Multiplier 9-bit elements   0 / 4 (0 %)							
Description of your design	Flow Status   Successful - Sat Jun 07 02:50:37 2025     Quartus Prime Version   20.1.1 Build 720 11/11/2020 SJ Lite Edition     Revision Name   MCH     Top-level Entity Name   MCH     Family   Cyclone IV E     Device   EP4CE55F23A7     Timing Models   Final     Total logic elements   2,499 / 55,856 ( 4 % )     Total registers   513     Total pins   36 / 325 ( 11 % )     Total virtual pins   0     Total memory bits   0 / 2,396,160 ( 0 % )     Embedded Multiplier 9-bit elements   6 / 308 ( 2 % )						
			Descript	ion o	of your design		

整體電路設計為一個同步時序的有限狀態機 (Finite State Machine, FSM),依序執行以下主要階段:載入座標點、對座標點進行極座標排序、建構凸包頂點序列,以及計算最終面積。

狀態機運作流程 本設計的核心為一有限狀態機,包含以下五個狀態:

- 1. LOAD (載入狀態): 在此狀態下,模組會依序接收 20 組 (X, Y) 座標。每接收一組座標,便將其存入內部的 px 和 py 陣列暫存器。同時,會找出所有輸入點中 Y 座標最小的點作為「基準點」(anchor point)。若有多個點 Y 座標相同,則選擇其中 X 座標最小的點作為基準點。當 20 個點全部載入完成後 (load counter == 19),狀態機進入 SORT 狀態。
- 2. SORT (排序狀態): 此狀態的目標是將除了基準點以外的所有點,相對於 基準點進行極座標角度的逆時針排序。透過 swapped\_anchor 旗標控制, 花費兩個時脈週期將先前找到的基準點與 px, py 的內容交換,使基準點 固定在索引 0 的位置,以簡化後續排序操作。
- 3. LOWER: 此狀態實作格雷厄姆掃描法的核心步驟:利用堆疊 (stack) 建構 凸包。初始化時,將排序後的前兩個點 (索引 0 和 1,即基準點和角度最 小的點) 壓入堆疊 stack, top 指標指向堆疊頂部。接著,從排序後的第三 個點開始 (scan\_idx 從 2 開始),依序檢查每個點。
- 4. AREA (面積計算狀態): 此狀態使用鞋帶公式計算由 LOWER 狀態得到的 凸包面積。 area\_idx 用於遍歷堆疊 stack 中的凸包頂點。j 變數始終指 向 area\_idx 的下一個頂點。在每個時脈週期,根據公式  $\sum (xiyj-xjyi) \sum (xiyj-xjyi)$  更新累加值 sum。此 sum 的最終值會是凸包實際面積的兩倍。 當所有凸包頂點都參與計算後 (area\_idx == top 1),狀態機進入 DONE 狀態。
- 5. DONE (完成狀態): 將 Done 輸出訊號設為高電位,通知外部系統計算已完成。 計算 sum 的絕對值,並將其低 17 位元賦值給 area 輸出埠。 重置模組內部各個計數器、索引和旗標,為處理下一組 20 個座標點做準備。 狀態機轉換回 LOAD 狀態。