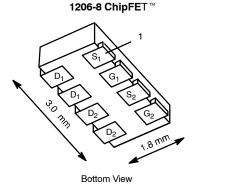
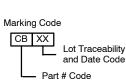


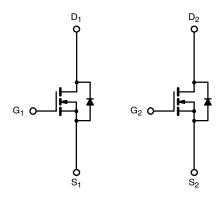
Dual N-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$r_{DS(on)}(\Omega)$	I _D (A)		
20	0.075 @ V _{GS} = 4.5 V	±4.2		
	0.134 @ V _{GS} = 2.5 V	±3.1		









N-Channel MOSFET N-Channel MOSFET

Ordering Information: Si5904DC-T1

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter		Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage		V_{DS}	20		٧	
Gate-Source Voltage		V_{GS}	±12			
	T _A = 25°C	- I _D	±4.2	±3.1		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 85°C		±3.0	±2.2		
Pulsed Drain Current		I _{DM}	±10		Α	
Continuous Source Current (Diode Conduction) ^a		I _S	1.8	0.9		
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.1	1.1	W	
	T _A = 85°C		1.1	0.6		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		00	
Soldering Recommendations (Peak Temperature)b, c				260	°C	

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
	t ≤ 5 sec	R _{thJA}	50	60	°C/W		
Maximum Junction-to-Ambient ^a	Steady State		90	110			
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	30	40			

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

Si5904DC

Vishay Siliconix

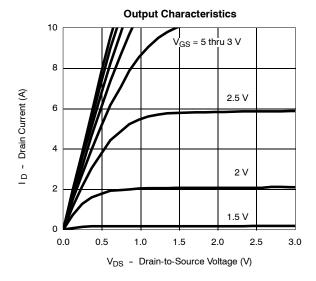


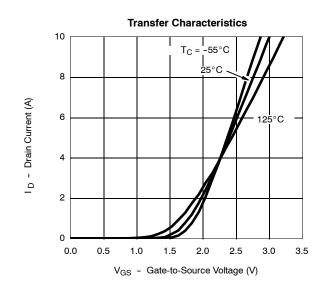
Parameter	Symbol	Test Condition	Min	Тур	Max	Unit		
Static	•		•	•				
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.6			V		
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA		
7. 0.1 1/1 0.10		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			1	1 .		
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^{\circ}\text{C}$			5	μΑ		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	10			Α		
Drain-Source On-State Resistance ^a	r _{DS(on)}	$V_{GS} = 4.5 \ V, I_D = 3.1 A$		0.065	0.075	Ω		
Dialif-Source Off-State Resistance-		$V_{GS} = 2.5 \text{ V}, I_D = 2.3 \text{ A}$		0.115	0.143	52		
Forward Transconductancea	9fs	$V_{DS} = 10 \text{ V}, I_D = 3.1 \text{ A}$		8		S		
Diode Forward Voltage ^a	V _{SD}	I _S = 0.9 A, V _{GS} = 0 V		0.8	1.2	V		
Dynamic ^b								
Total Gate Charge	Qg			4	6	nC		
Gate-Source Charge	Q _{gs}	V_{DS} = 10 V, $\ V_{GS}$ = 4.5 V, I_D = 3.1 A		0.6				
Gate-Drain Charge	Q _{gd}			1.3				
Turn-On Delay Time	t _{d(on)}			12	18	ns		
Rise Time	t _r	V_{DD} = 10 V, R_L = 10 Ω		35	55			
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 1 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_G = 6 \Omega$		19	30			
Fall Time	t _f			9	15			
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 0.9 A, di/dt = 100 A/μs		40	80	1		

Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)









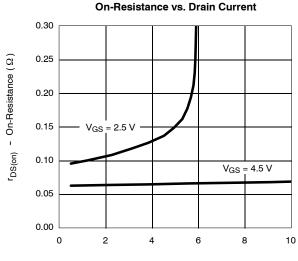
5

V_{GS} - Gate-to-Source Voltage (V)

- Source Current (A)

Vishay Siliconix

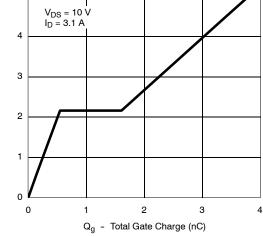
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



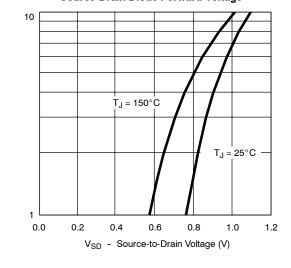




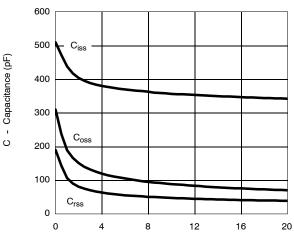
Gate Charge



Source-Drain Diode Forward Voltage

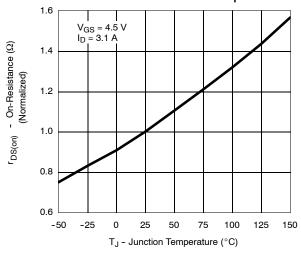


Capacitance

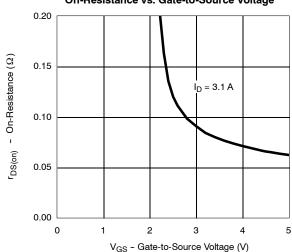


V_{DS} - Drain-to-Source Voltage (V)

On-Resistance vs. Junction Temperature



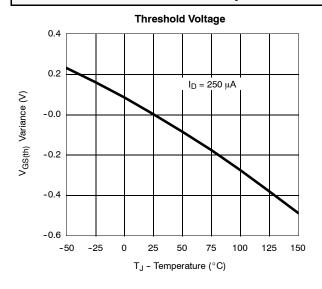
On-Resistance vs. Gate-to-Source Voltage

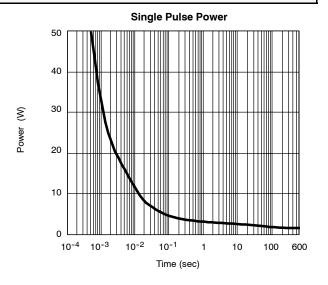


Vishay Siliconix

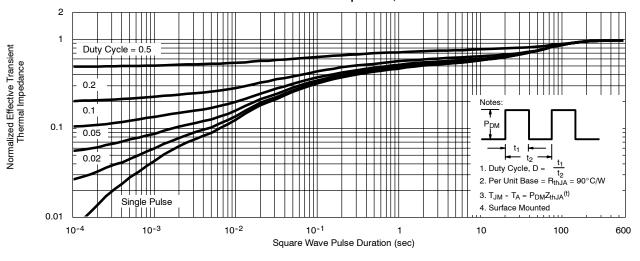


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





Normalized Thermal Transient Impedance, Junction-to-Ambient



1000

Normalized Thermal Transient Impedance, Junction-to-Foot

