

CS 343, Spring 2022

MIDTERM Lab Project

Instructor: Professor Izidor Gertner

Start Date March 23, 2022 Time 12:00 -1:40 PM, 2:00-3:40PM

Due Date March 23, 2022

What to submit: Report with screenshots and explanations, archived project files for verification, README file with details instructions on how to verify your design, short video based on your report.

This is individual test project.

Please hand write and sign statements affirming that you will not cheat:

"I will neither give nor receive unauthorized assistance on this exam.

I will use only one computing device to perform this test"

Please **hand write and sign** here:

• **Assignment 1 based on Tutorial**

“Laboratory Exercise Tutorial Memory blocks using VHDL array and LPM modules.”
DESIGN MEMORY AS A VHDL ARRAY AS SHOWN IN PART III, and using LPM SRAM modules.

- **Design 32 bit word Data Memory** module based on LPM tutorial attached.
Data memory size 16 words.
- **Design 32 bit word INSTRUCTION Memory** module based on LPM tutorial attached. Instruction memory size 32 words.
- **Design 32 bit register DUAL PORTED REGISTER FILE** module based on 2-port RAM LPM tutorial attached. EACH register is 32 bits.
- **What to submit:**
- **1 Report should include VHDL code, waveform in simulation, as you did in self check labs, please include explanation on how did you get the screenshots.**
- **2. Verification using ModelSim , (waveforms),**

CS 343, Spring 2022

MIDTERM Lab Project

Instructor: Professor Izidor Gertner

Start Date March 23, 2022 Time 12:00 -1:40 PM, 2:00-3:40PM

Due Date March 23, 2022

What to submit: Report with screenshots and explanations, archived project files for verification, README file with details instructions on how to verify your design, short video based on your report.

- *You have to enter 5 32 bit words to data memory USING MIF FILE and demonstrated this using waveforms.*
- *You have to enter 5 32 bit MIPS instructions(you can take instructions from MIPS using MARS) to instruction memory and demonstrated this using waveforms. You have to enter 3 32 bit words to register file. YOU HAVE TO DEMONSTRATE HOW DO YOU READ 2 WORDS and WRITE 1 word to REGISTER FILE in SIMULATION.*
- *3.. Archived Project files with readme*
- **Assignment 2 based on Intel AP note**

“USING LIBRARY MODULES IN VHDL DESIGNS”

Design 32 bit ADD/SUB unit as described in the second attached tutorial.

You have to create two versions:

- From scratch and
- Another one using LPM modules.
- You have to load data to ADD/SUB unit from DATA memory (just copy NOT TO USE LOAD INSTRUCTION) USE MIF file to load data to memory.
- You have to design circuit to output N – negative flag, Z- zero flag, O -overflow flag.
- Demonstrate operation using waveforms.
- Demonstration of ACCUMULATOR unit for ADD and for SUB.