

CS342/CS343  
Instructor: Professor Izidor Gertner  
Spring 2022  
Lab 1, Azwad Shameem, 2/13/2022

<b>Table of Contents</b>	<b>Page</b>
<b>Objective</b>	2
<b>Code</b>	
Part A	2-7
Part B	7-11
Part C	11-15
<b>Explanation</b>	16
<b>Conclusion</b>	16

## Objective:

Part A. Create the project for the digital circuit based on the tutorial.

Part B. Create a 2:1 multiplexer where each signal is one bit.

Part C. Create a 2:1 multiplexer where each of the signals are 32 bits, beside the selector signal which is only 1 bit.

## Code:

### (Part A)

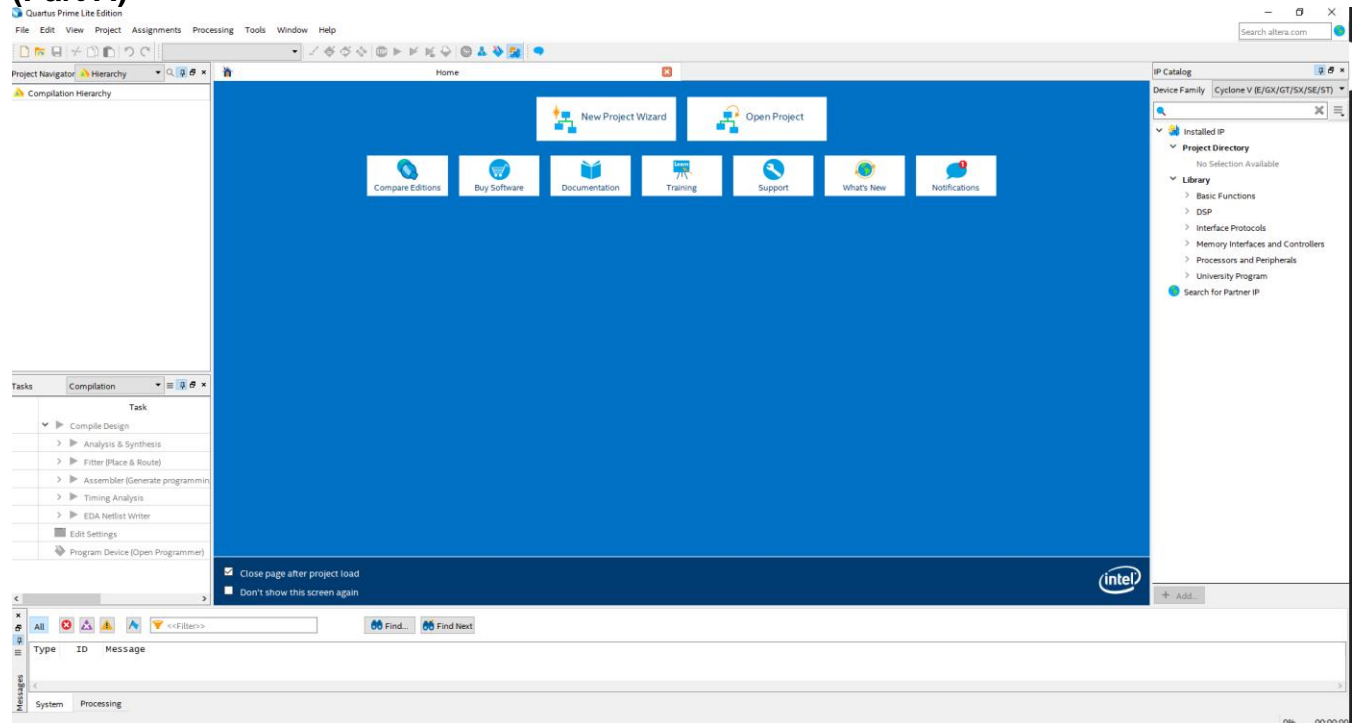


Figure 1: The Main Quartus Prime Display Screen

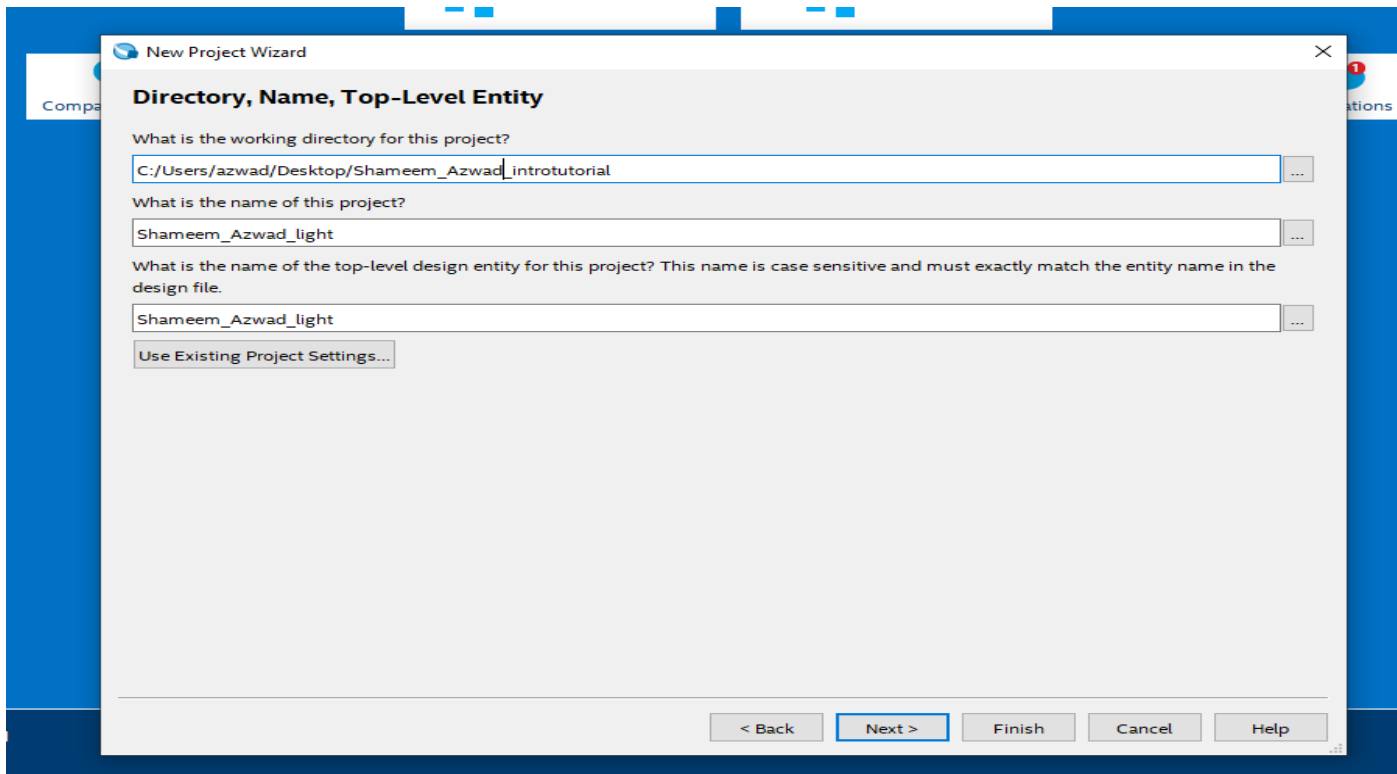


Figure 2: Creation of the project

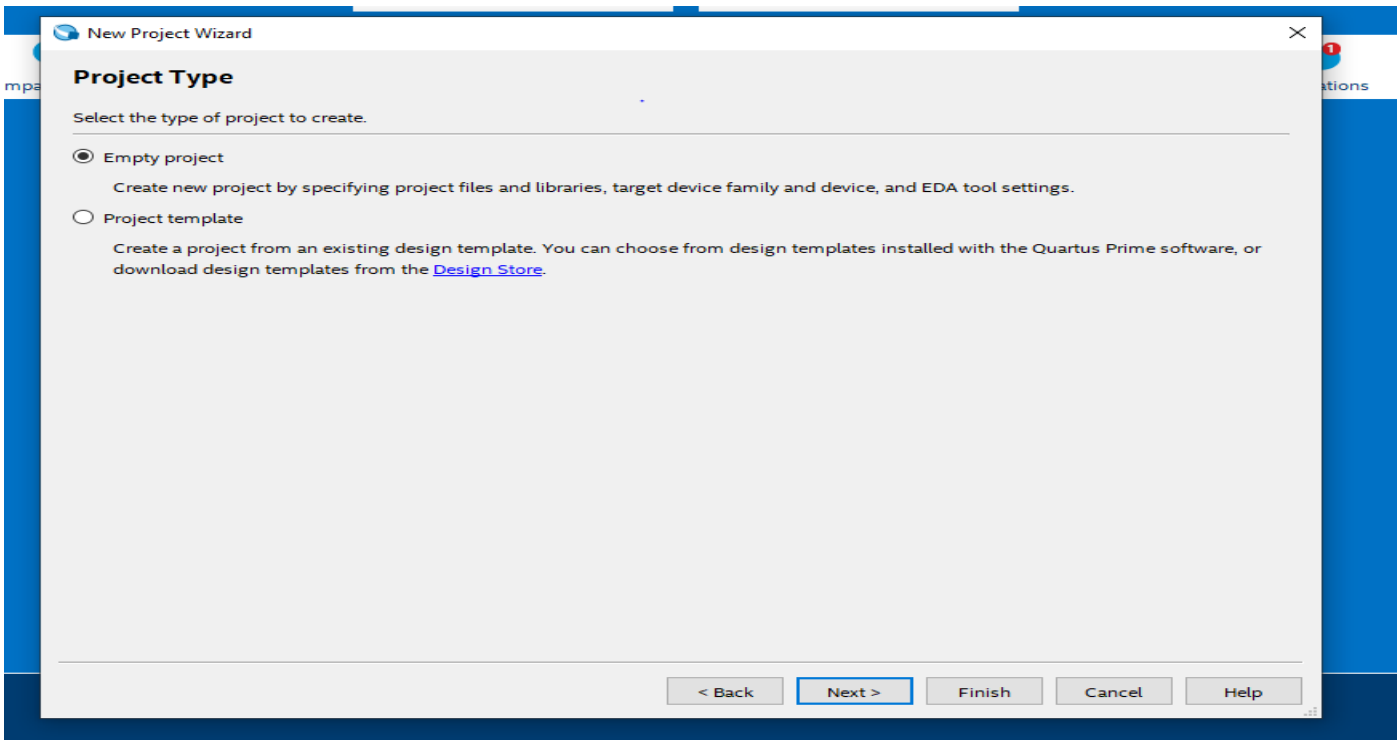


Figure 3: The Project created as an Empty project

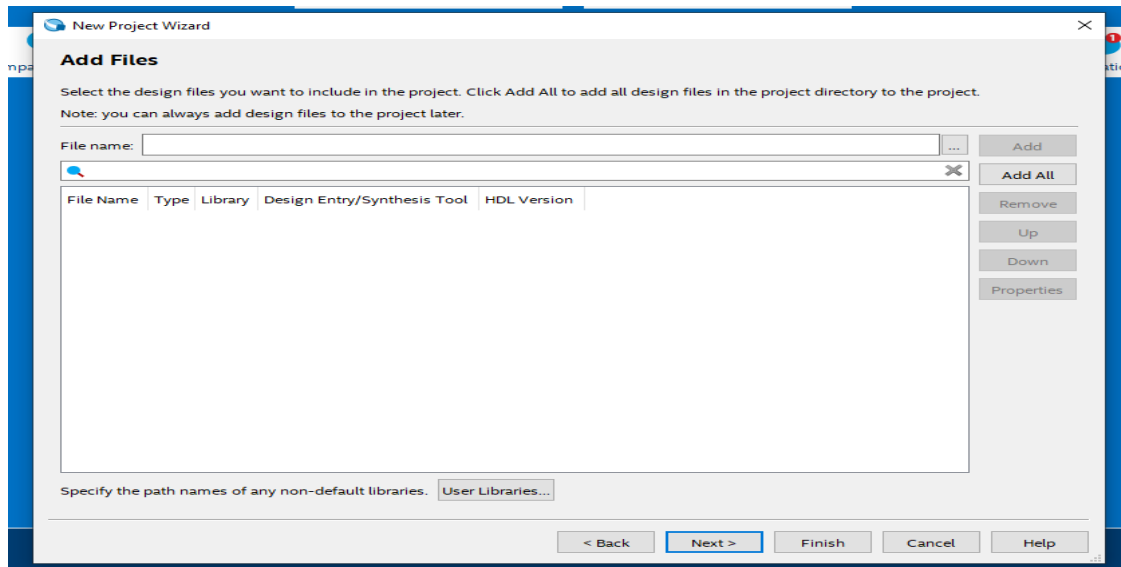


Figure 4: No extra files were added just like in the tutorial

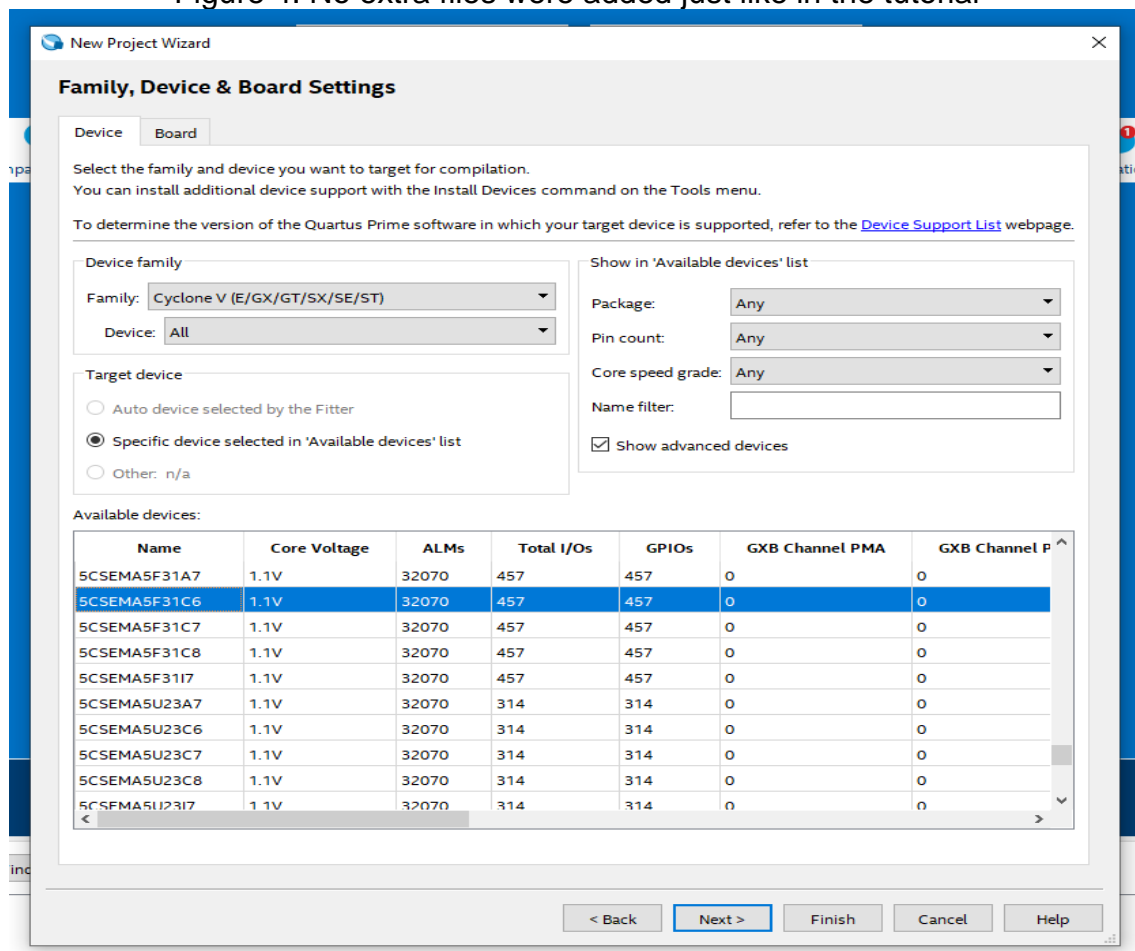


Figure 5: The same device used as in the tutorial

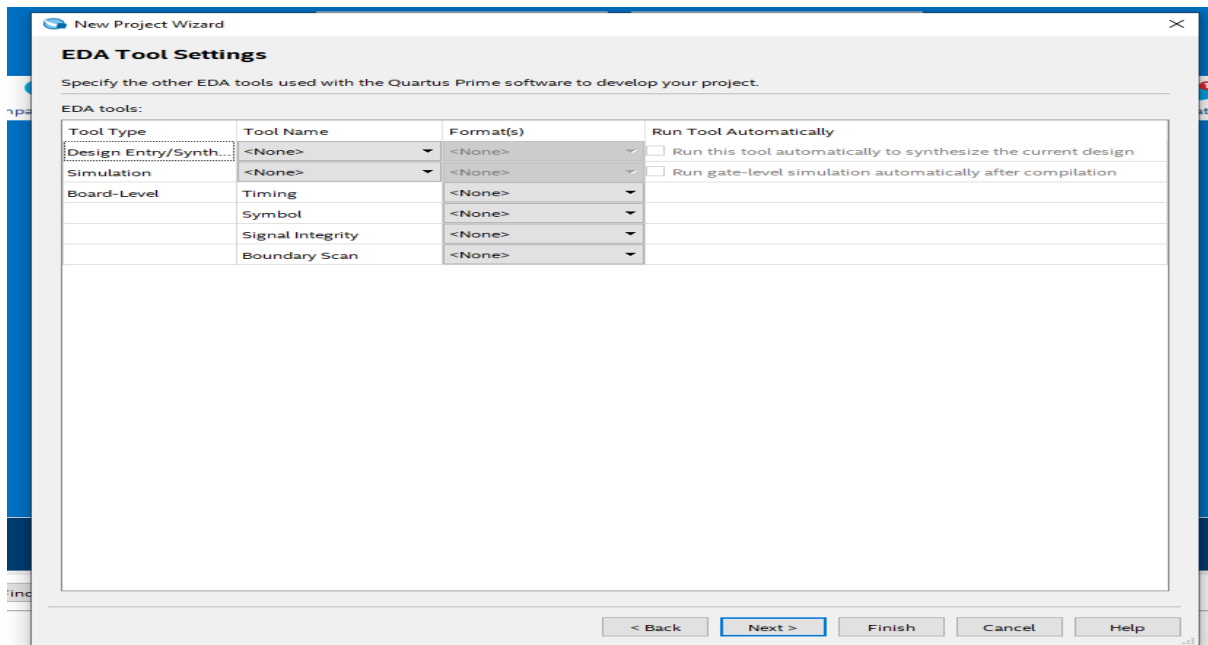


Figure 6: EDA Tools Settings

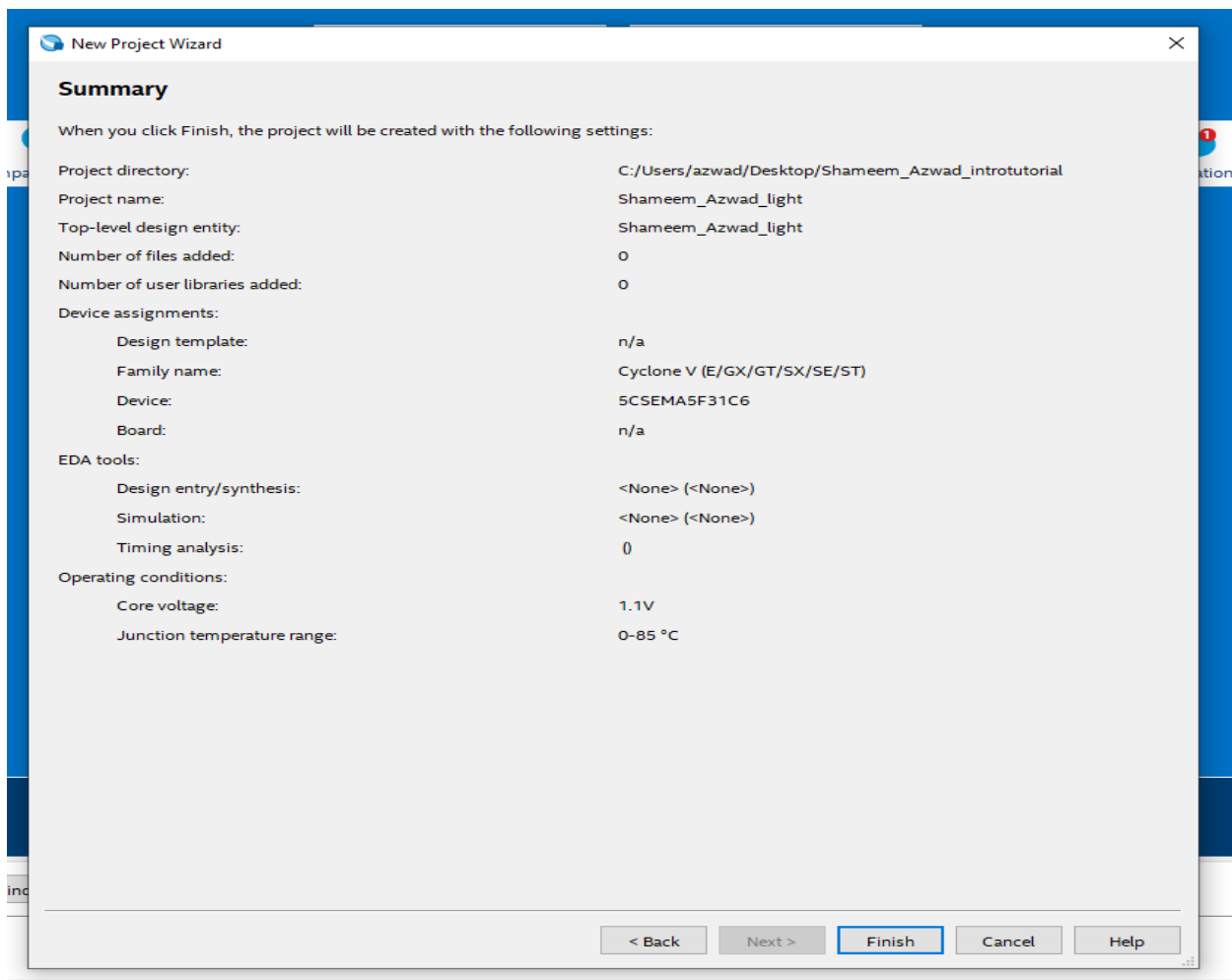


Figure 7: Project Summary

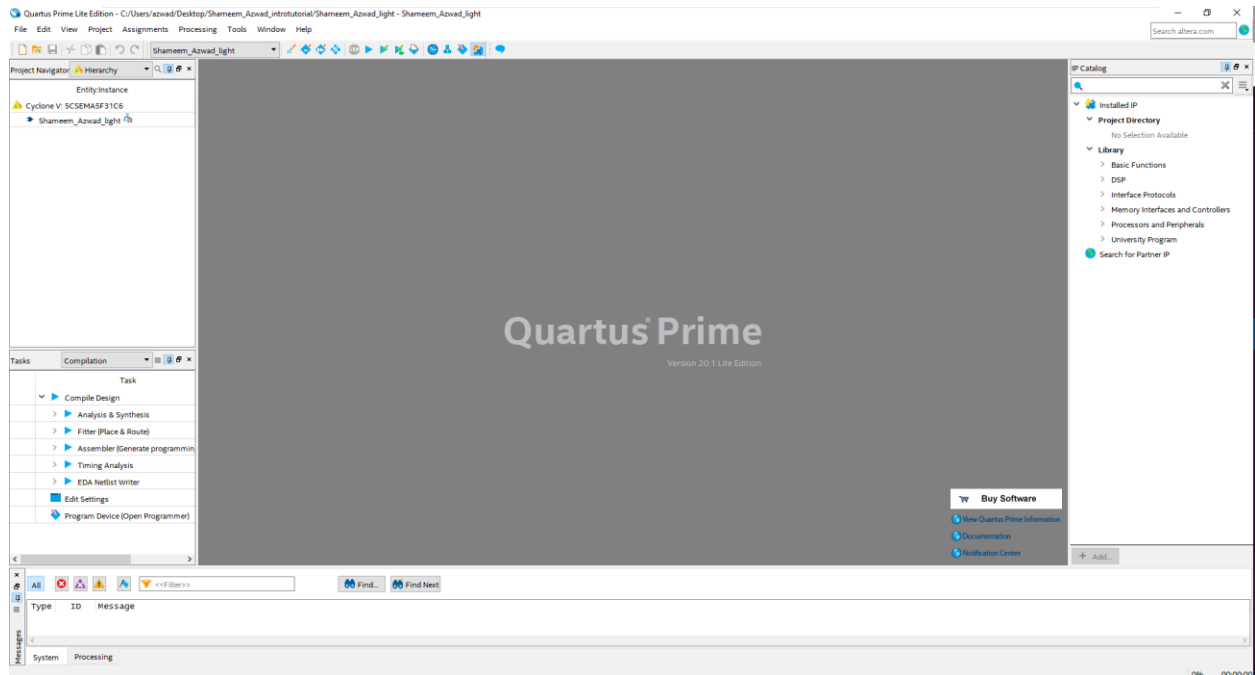


Figure 8: The Quartus Prime window for a created project

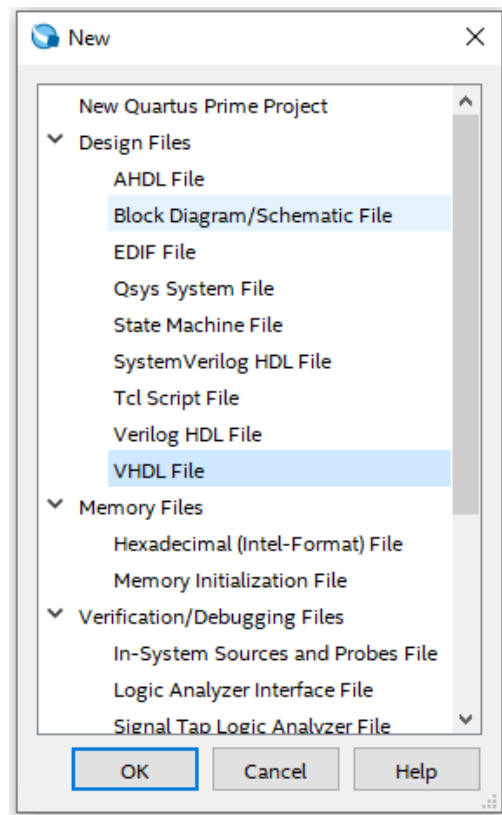


Figure 9: Create a VHDL File

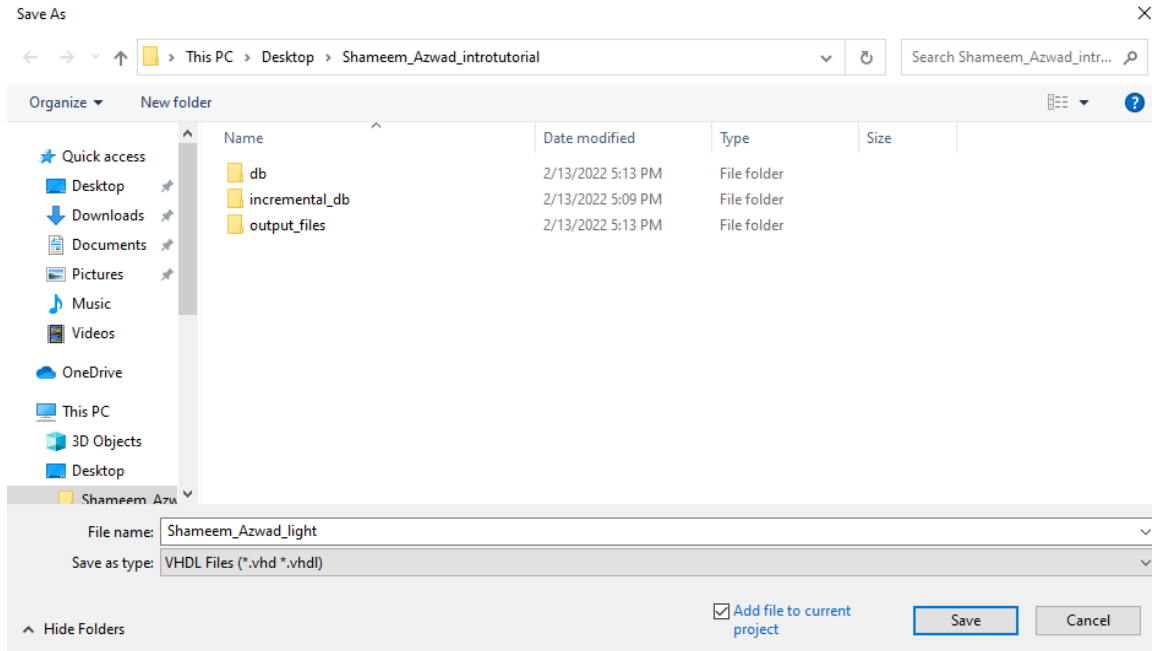


Figure 10: Name the File

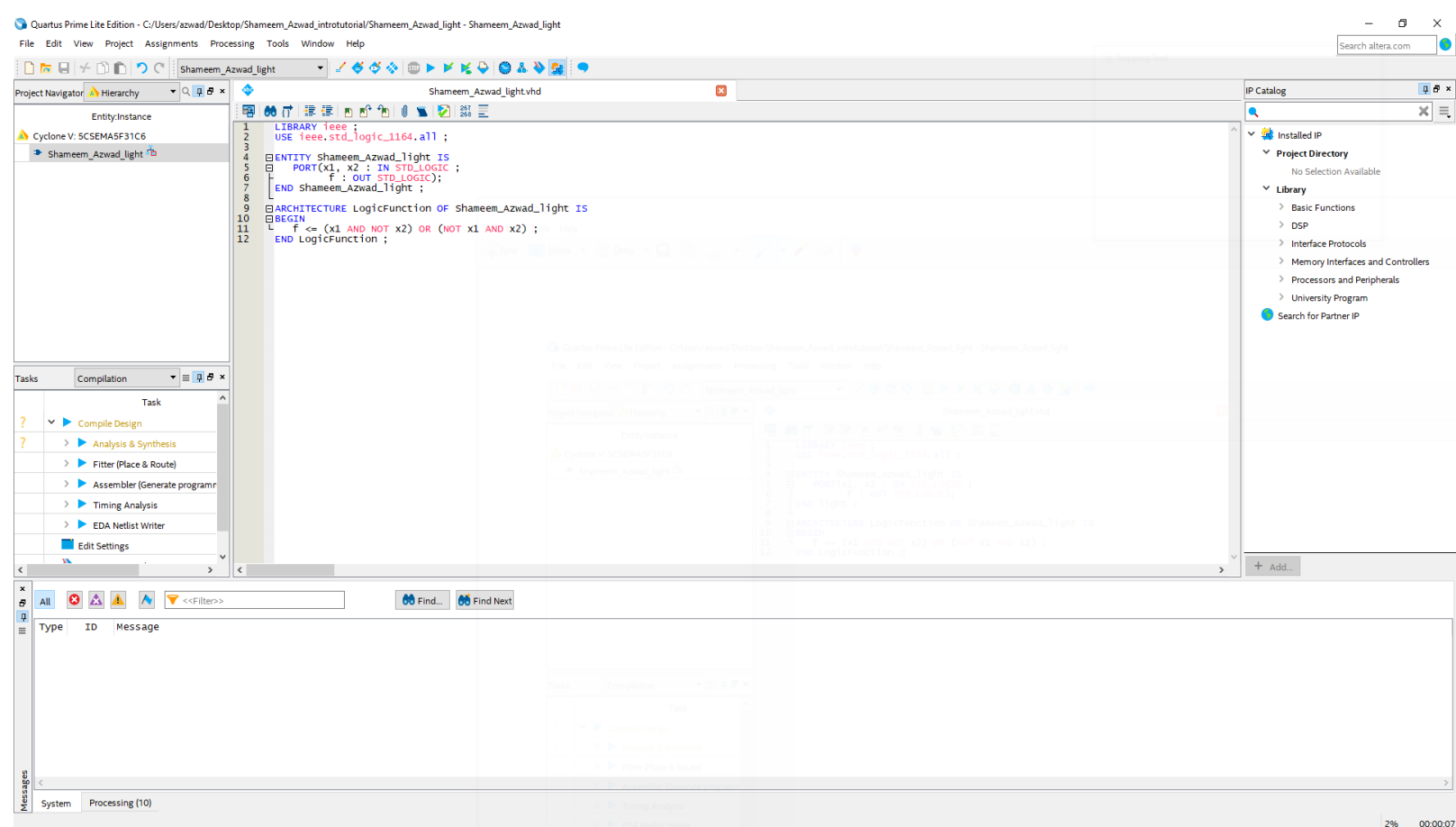


Figure 11: Text Editor Window

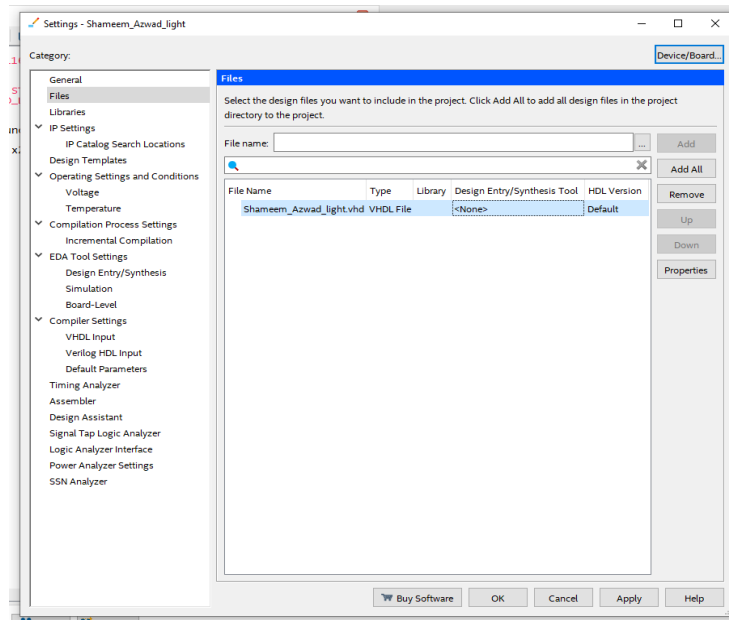


Figure 12: Adds the file to the project (Image on the left)

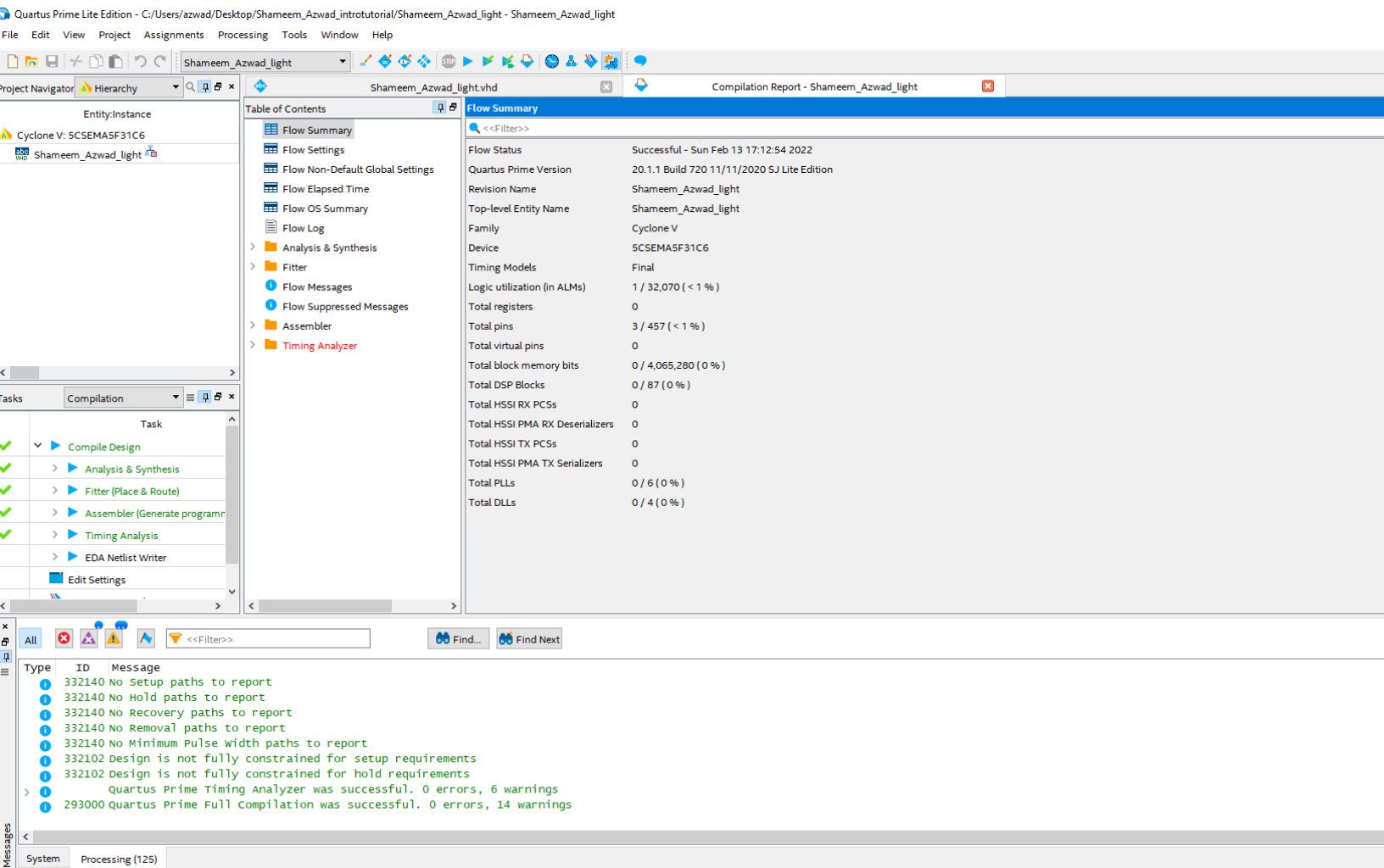
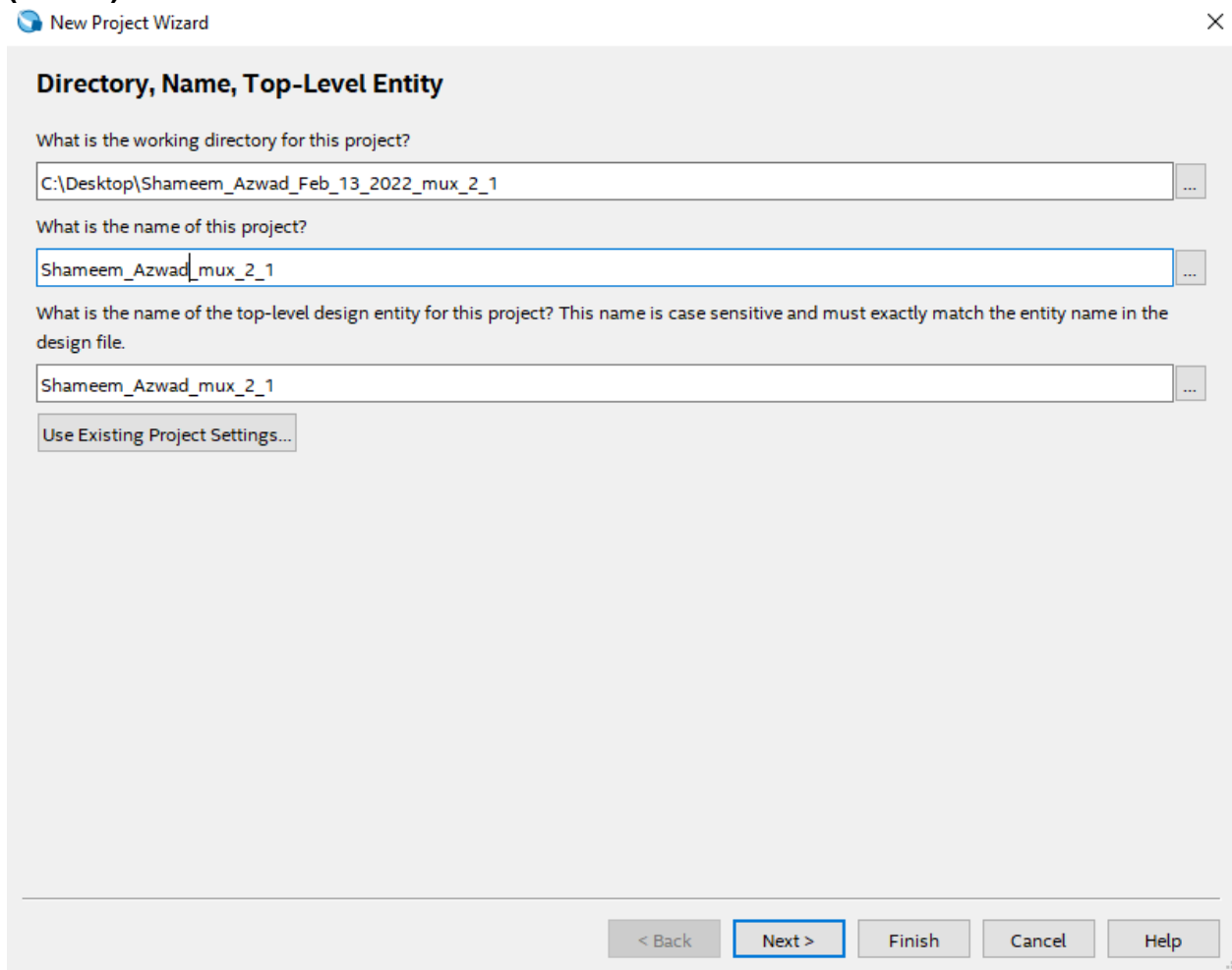


Figure 13: The project displayed after a successful compilation.



**(Part B)**

The image shows a 'New Project Wizard' dialog box with a title bar containing a blue icon, the text 'New Project Wizard', and a close button. The main area is titled 'Directory, Name, Top-Level Entity'. It contains three text input fields, each with a browse button ('...') to its right. The first field is labeled 'What is the working directory for this project?' and contains the path 'C:\Desktop\Shameem\_Azwad\_Feb\_13\_2022\_mux\_2\_1'. The second field is labeled 'What is the name of this project?' and contains 'Shameem\_Azwad\_mux\_2\_1'. The third field is labeled 'What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.' and contains 'Shameem\_Azwad\_mux\_2\_1'. Below these fields is a button labeled 'Use Existing Project Settings...'. At the bottom of the dialog is a row of five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Next >' button is highlighted with a blue border.

**Directory, Name, Top-Level Entity**

What is the working directory for this project?

C:\Desktop\Shameem\_Azwad\_Feb\_13\_2022\_mux\_2\_1

What is the name of this project?

Shameem\_Azwad\_mux\_2\_1

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

Shameem\_Azwad\_mux\_2\_1

Use Existing Project Settings...

< Back   Next >   Finish   Cancel   Help

Figure 14: The directory name and the name of the project plus the top-level design entity name.

New Project Wizard

### Family, Device & Board Settings

Device | Board

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)

Device: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Core speed grade: Any

Name filter:

☒ Show advanced devices

Available devices:

Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel PCS
5CSEMA4U23C7	1.1V	15880	314	314	0	0
5CSEMA4U23C8	1.1V	15880	314	314	0	0
5CSEMA4U23I7	1.1V	15880	314	314	0	0
5CSEMA5F31A7	1.1V	32070	457	457	0	0
5CSEMA5F31C6	1.1V	32070	457	457	0	0
5CSEMA5F31C7	1.1V	32070	457	457	0	0
5CSEMA5F31C8	1.1V	32070	457	457	0	0
5CSEMA5F31I7	1.1V	32070	457	457	0	0

< Back | Next > | Finish | Cancel | Help

Figure 15: The device picked for this project (Image on the left)

New Project Wizard

### Summary

When you click Finish, the project will be created with the following settings:

Project directory: C:\Desktop\Shameem\_Azwad\_Feb\_13\_2022\_mux\_2\_1

Project name: Shameem\_Azwad\_mux\_2\_1

Top-level design entity: Shameem\_Azwad\_mux\_2\_1

Number of files added: 0

Number of user libraries added: 0

Device assignments:

Design template: n/a

Family name: Cyclone V (E/GX/GT/SX/SE/ST)

Device: 5CGXFC7C7F23C8

Board: n/a

EDA tools:

Design entry/synthesis: <None> (<None>)

Simulation: <None> (<None>)

Timing analysis: {}

Operating conditions:

Core voltage: 1.1V

Junction temperature range: 0-85 °C

< Back | Next > | Finish | Cancel | Help

Figure 16: The Project summary (Image on the left)

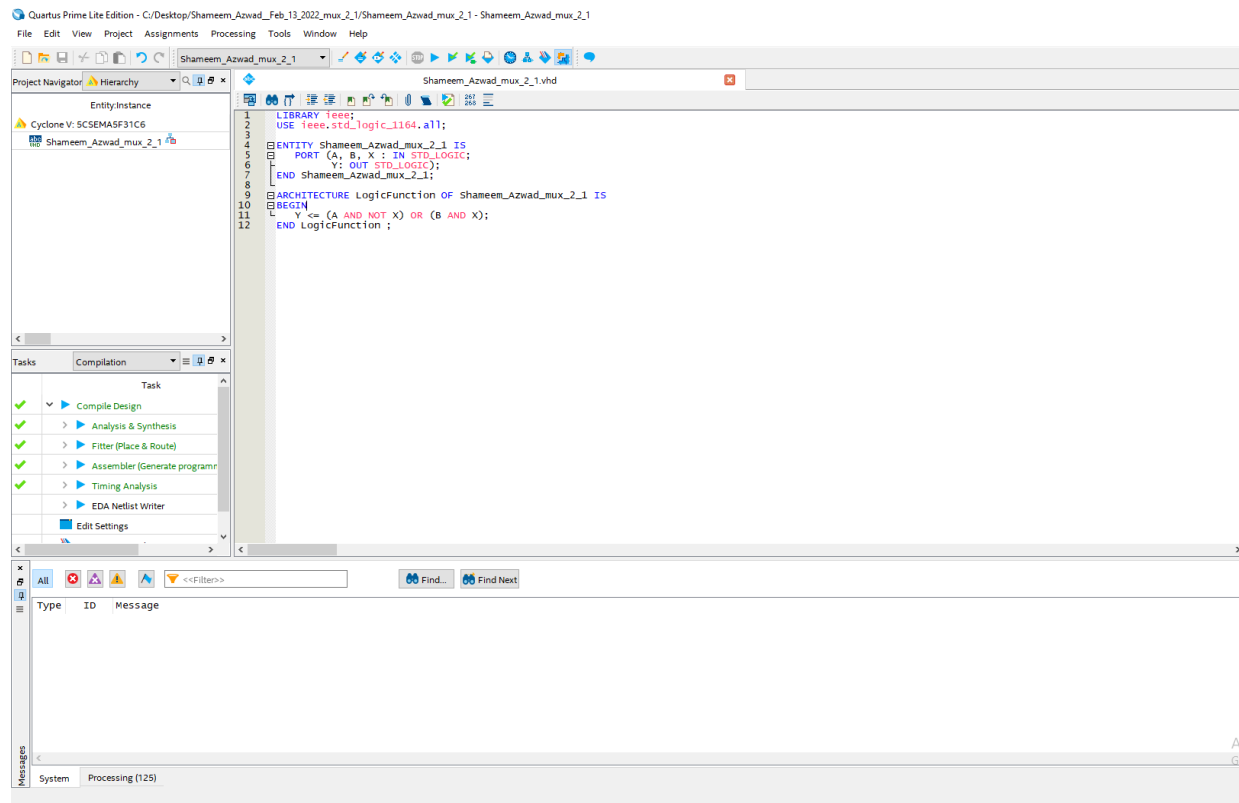


Figure 17:  
VHDL code  
for the  
mux 2:1

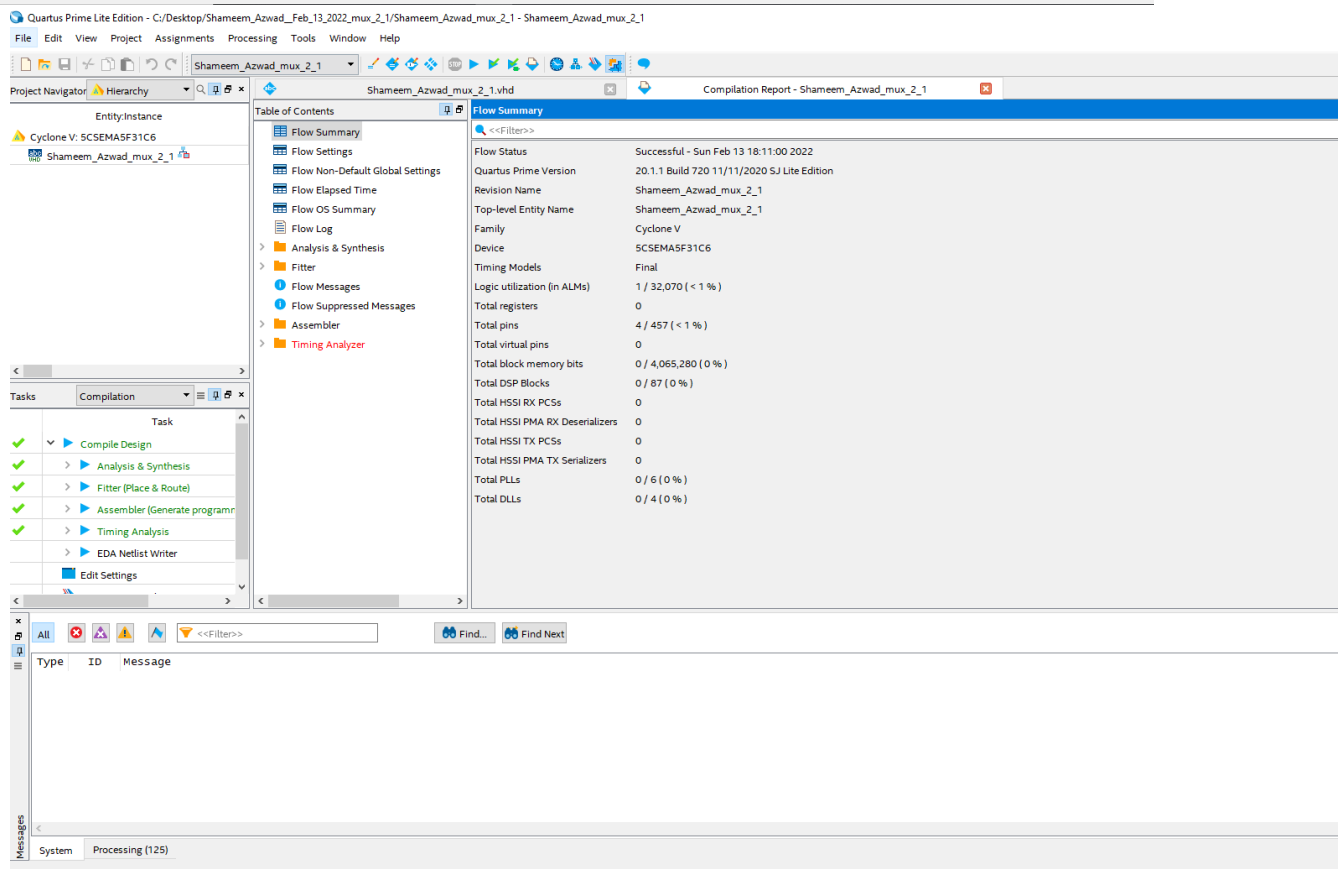


Figure 18: The project compiled successfully.

**(Part C)**

New Project Wizard

### Directory, Name, Top-Level Entity

What is the working directory for this project?

C:\Desktop\Shameem\_Azwad\_Feb\_13\_2022\_mux\_2\_1\_32bit

What is the name of this project?

Shameem\_Azwad\_mux\_2\_1\_32bit

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

Shameem\_Azwad\_mux\_2\_1\_32bit

Use Existing Project Settings...

< Back Next > Finish Cancel Help

Figure 19:  
The directory name and the project name plus the top-level design entity name is shown.

New Project Wizard

### Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)

Device: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Core speed grade: Any

Name filter:

☒ Show advanced devices

Available devices:

Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel P ^
5CSEMA4U23C7	1.1V	15880	314	314	0	0
5CSEMA4U23C8	1.1V	15880	314	314	0	0
5CSEMA4U23I7	1.1V	15880	314	314	0	0
5CSEMA5F31A7	1.1V	32070	457	457	0	0
5CSEMA5F31C6	1.1V	32070	457	457	0	0
5CSEMA5F31C7	1.1V	32070	457	457	0	0
5CSEMA5F31C8	1.1V	32070	457	457	0	0

< Back Next > Finish Cancel Help

Figure 20:  
Family, Device & Board settings displayed.

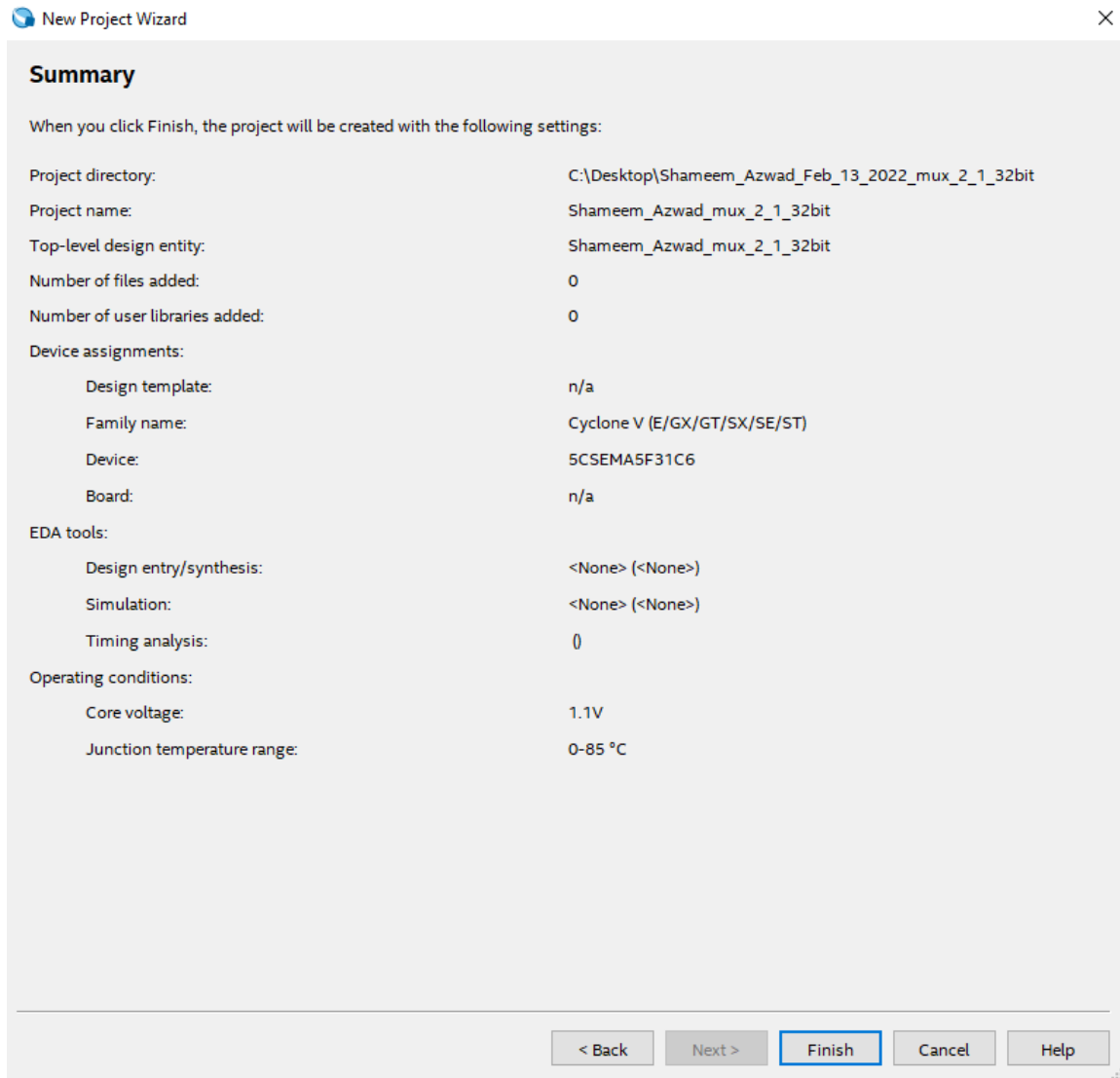


Figure 21: Project Summary displayed

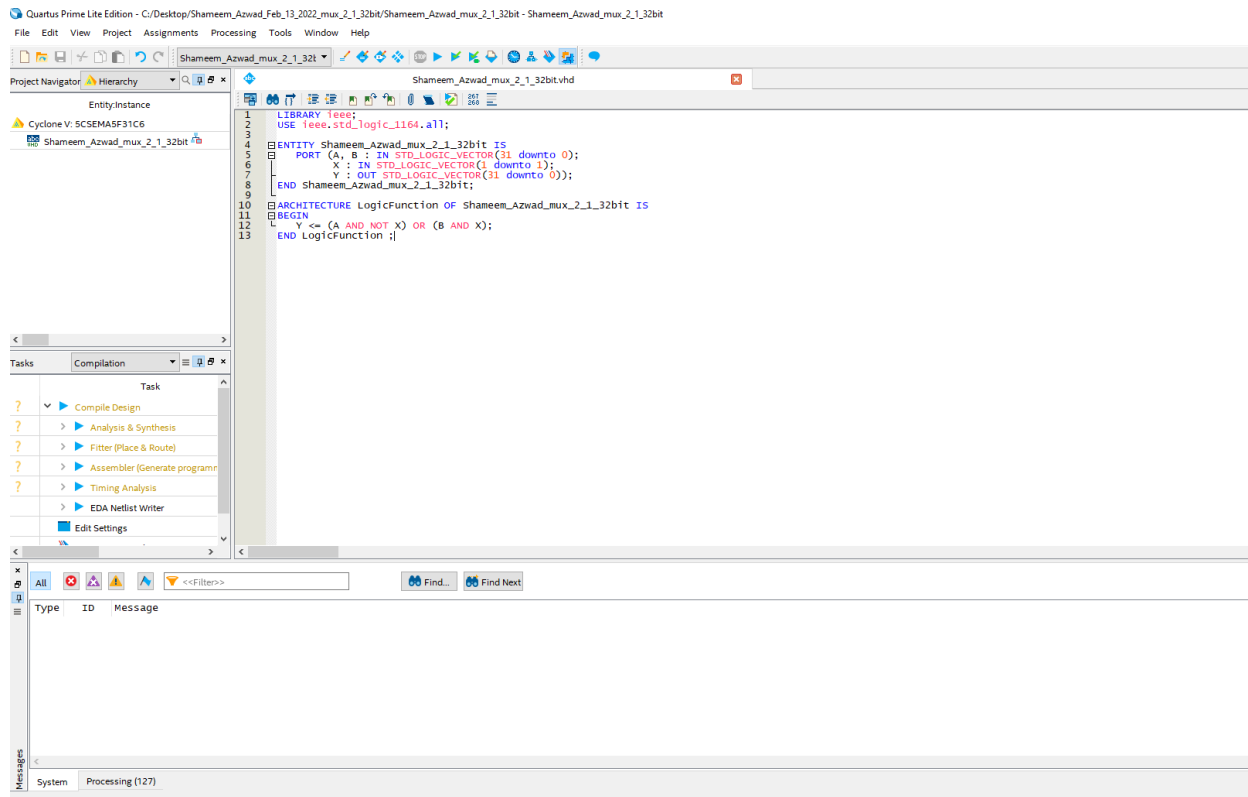


Figure 22: VHDL code used for mux 2:1 32-bit with a 1-bit signal selector

X is listed as a Vector because the circuit runs into errors with inputs as a bit.

Furthermore, we know X is the signal selector with a single bit, which means X needs to be a single bit. Therefore, in order to solve the issue we used a std\_logic\_vector(1 downto 1) which is basically a vector with only one bit.

Quartus Prime Lite Edition - C:/Desktop/Shameem\_Azwad\_Feb\_13\_2022\_mux\_2\_1\_32bit/Shameem\_Azwad\_mux\_2\_1\_32bit - Shameem\_Azwad\_mux\_2\_1\_32bit

File Edit View Project Assignments Processing Tools Window Help

Shameem\_Azwad\_mux\_2\_1\_32bit.vhd

Compilation Report - Shameem\_Azwad\_mux\_2\_1\_32bit

IP Catalog

Entity Instance

Cyclone V: 5CSEMA5F31C6

Shameem\_Azwad\_mux\_2\_1\_32bit

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Flow Messages
- Flow Suppressed Messages
- Assembler
- Timing Analyzer

Flow Summary

Flow Status: Successful - Sun Feb 13 19:34:38 2022

Quartus Prime Version: 20.1.1 Build 720 11/11/2020 SJ Lite Edition

Revision Name: Shameem\_Azwad\_mux\_2\_1\_32bit

Top-level Entity Name: Shameem\_Azwad\_mux\_2\_1\_32bit

Family: Cyclone V

Device: 5CSEMA5F31C6

Timing Models: Final

Logic utilization (in ALMs): 1 / 32,070 (< 1 %)

Total registers: 0

Total pins: 97 / 457 (21 %)

Total virtual pins: 0

Total block memory bits: 0 / 4,065,280 (0 %)

Total DSP Blocks: 0 / 87 (0 %)

Total HSSI RX PCSs: 0

Total HSSI PMA RX Deserializers: 0

Total HSSI TX PCSs: 0

Total HSSI PMA TX Serializers: 0

Total PLLs: 0 / 6 (0 %)

Total DLLs: 0 / 4 (0 %)

Tasks

Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Timing Analysis
- EDA Netlist Writer
- Edit Settings

Find...

Find Next

Messages

Type ID Message

- 332140 No Setup paths to report
- 332140 No Hold paths to report
- 332140 No Recovery paths to report
- 332140 No Removal paths to report
- 332140 No Minimum Pulse Width paths to report
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
- 293000 Quartus Prime Full Compilation was successful. 0 errors, 109 warnings

System Processing (127)

100% 00:01:23

Figure 23: Project compiled successfully

### **Explanation:**

#### **(Part A)**

The code and the pictures displaying the project follows the tutorial's instructions and shows the screenshots of the intro tutorial.

#### **(Part B)**

The images show the creation of the project following the same route shown in intro tutorial. The code contains A, B, X inputs as a single bit and Y as a single bit output as stated for this mux 2:1 circuit. In addition, the VHDL code uses the equation for the mux 2:1 circuit which is  $Y = (A * \bar{X}) + (B * X)$ , which follows in code as  $\rightarrow (A \text{ AND NOT } X) \text{ OR } (B \text{ AND } X)$ . This equation makes sure the results are right because it uses the equation which follows the truth table for the right results.

#### **(Part C)**

The images show the creation of the project following the same route shown in intro tutorial. The code contains A, B inputs as a 32-bit vector with X as a single bit and Y also as a 32-bit vector for this mux 2:1 circuit. In addition, the VHDL code uses the equation for the mux 2:1 circuit which is  $Y = (A * \bar{X}) + (B * X)$ , which follows in code as  $\rightarrow (A \text{ AND NOT } X) \text{ OR } (B \text{ AND } X)$ . This equation makes sure the results are right because it uses the equation which follows the truth table for the right results.

### **Conclusion:**

This lab was very useful to begin learning the usage of Quartus because it allows us to learn the creation and programming of VHDL code for a circuit by using Quartus. In fact, this lab also allowed us to learn the usage of inputs and outputs which are not only single bits but also several its. Lastly, this lab set up a starting understanding of the nuances of how Quartus Lite works and how to use it to code in VHDL.