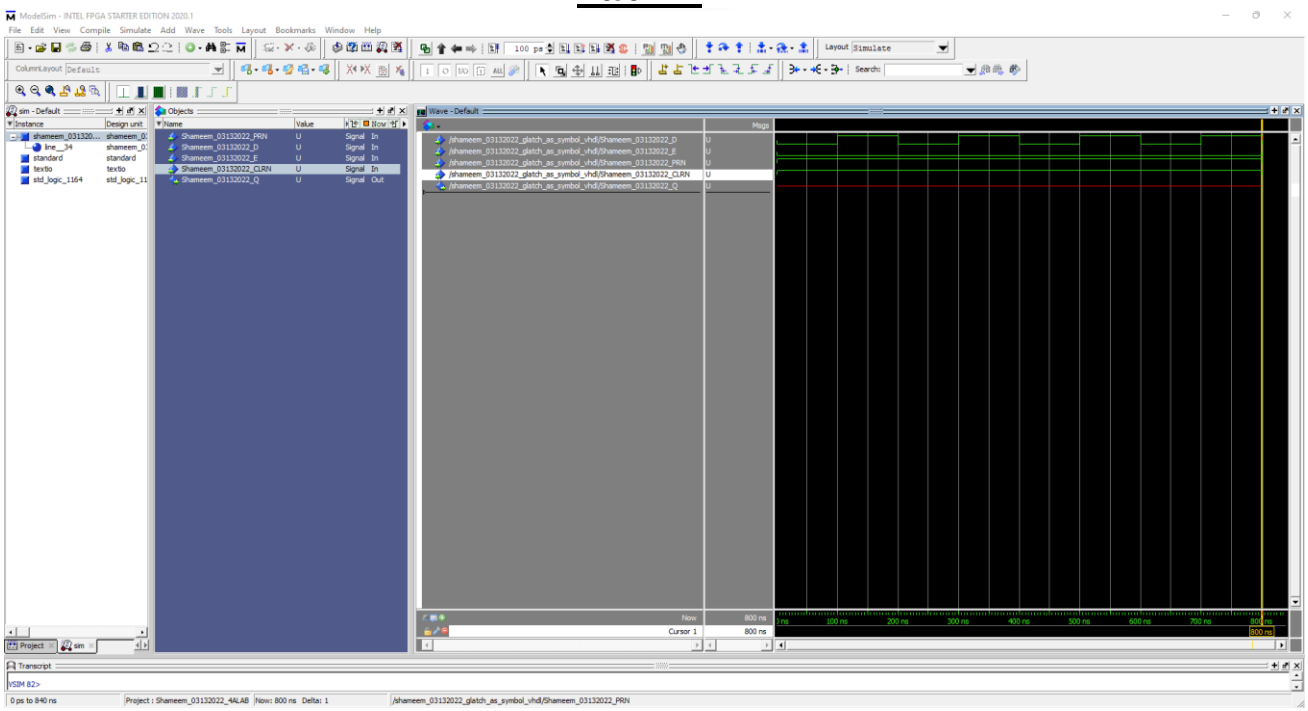
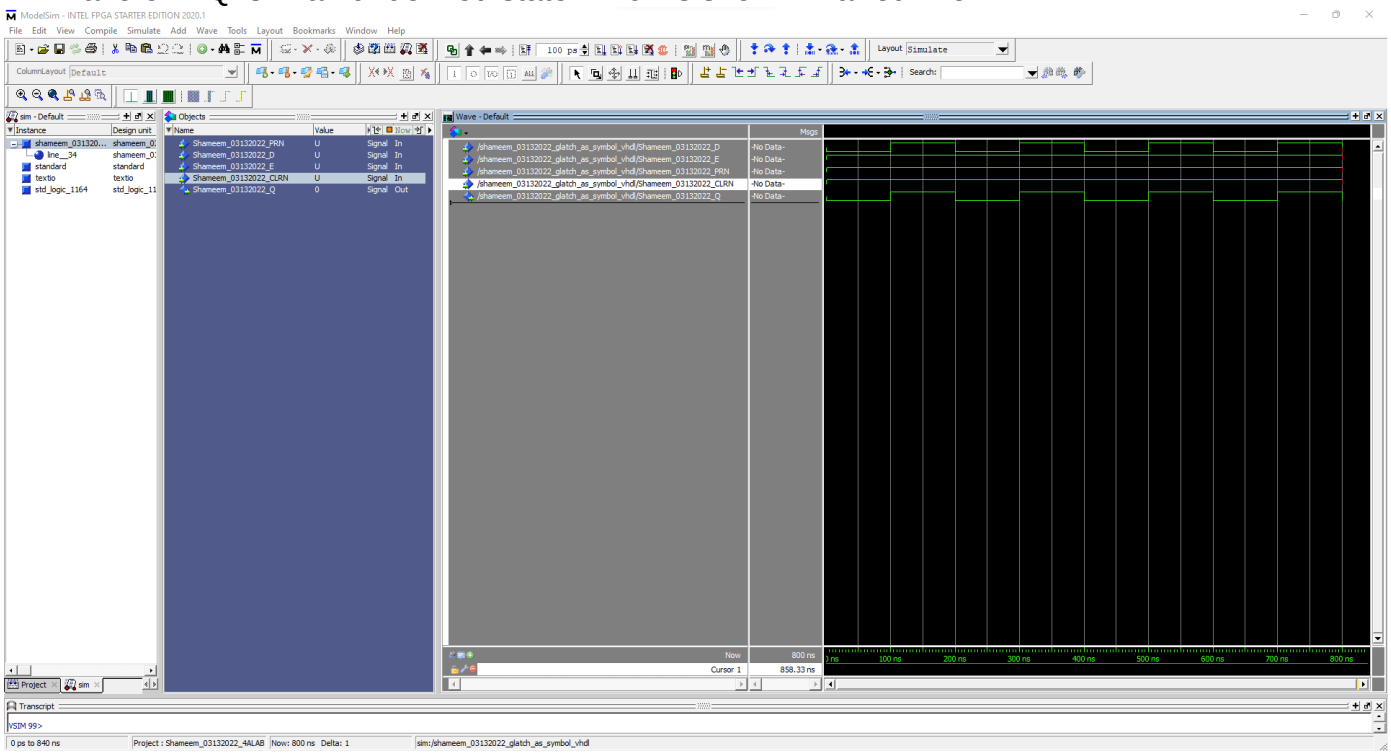
CS 342000 | CS343000
Instructor: Professor Izidor Gertner
Spring 2022
Azwad Shameem, 3/13/2022

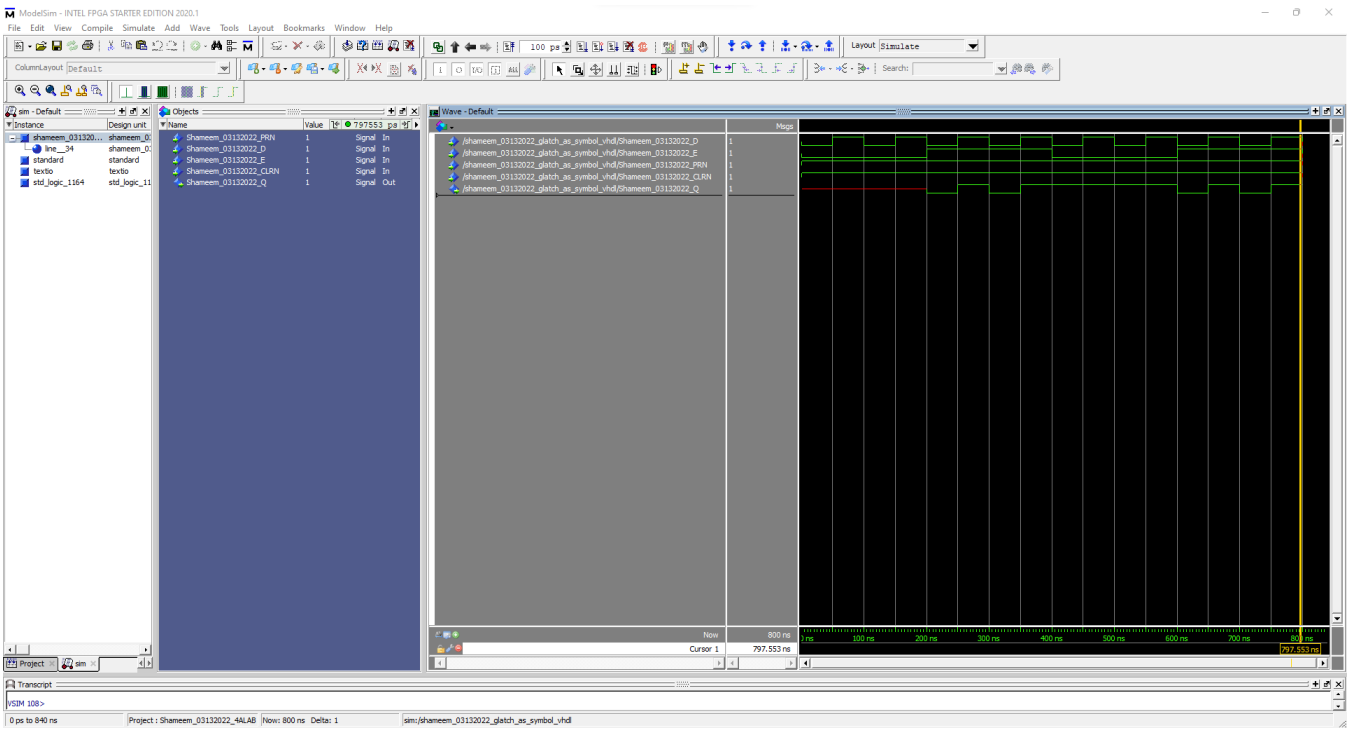
Lab 4A



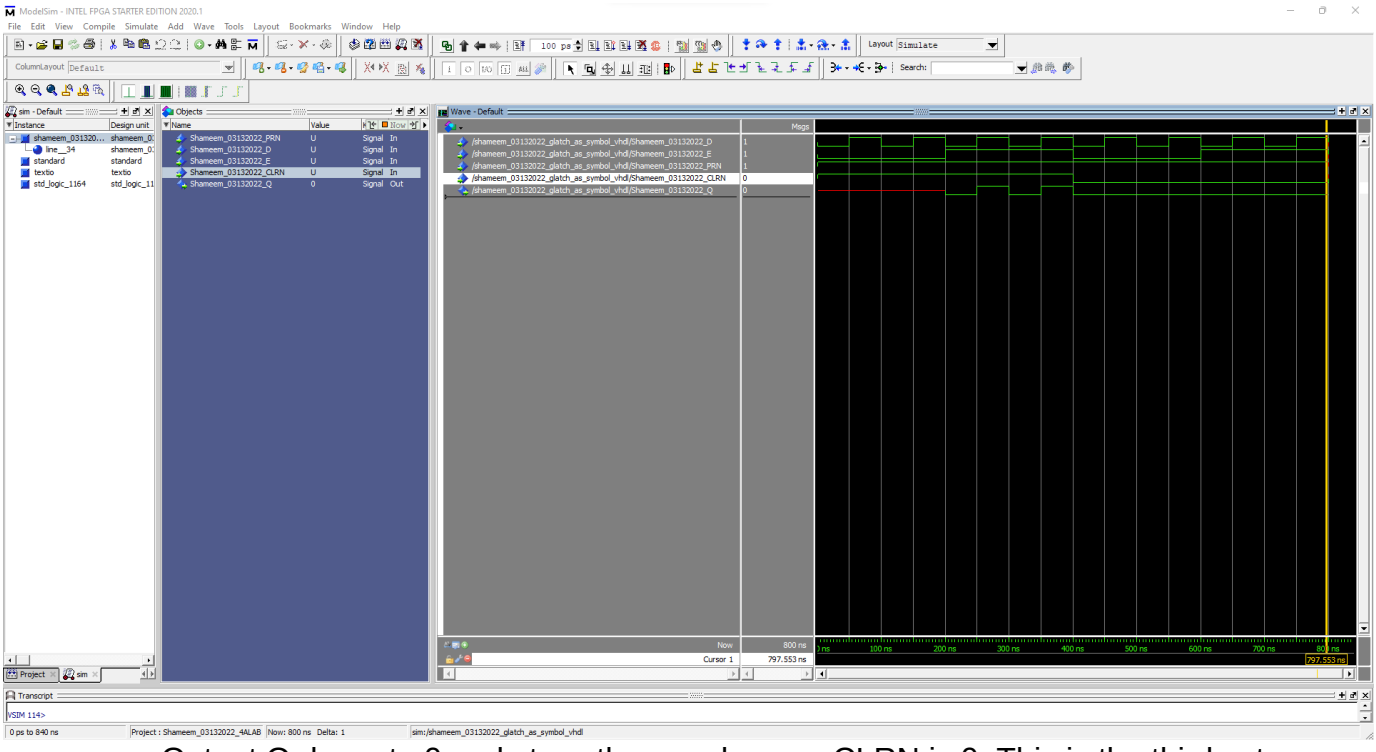
The screenshot above follows Lab 4A's waveform guides and shows that in this waveform Q is in an undefined state which is shown in a red line.



This time, input E is 1 always which makes output Q follows the value of input D, which is also shown in the simulation for Lab 4A.

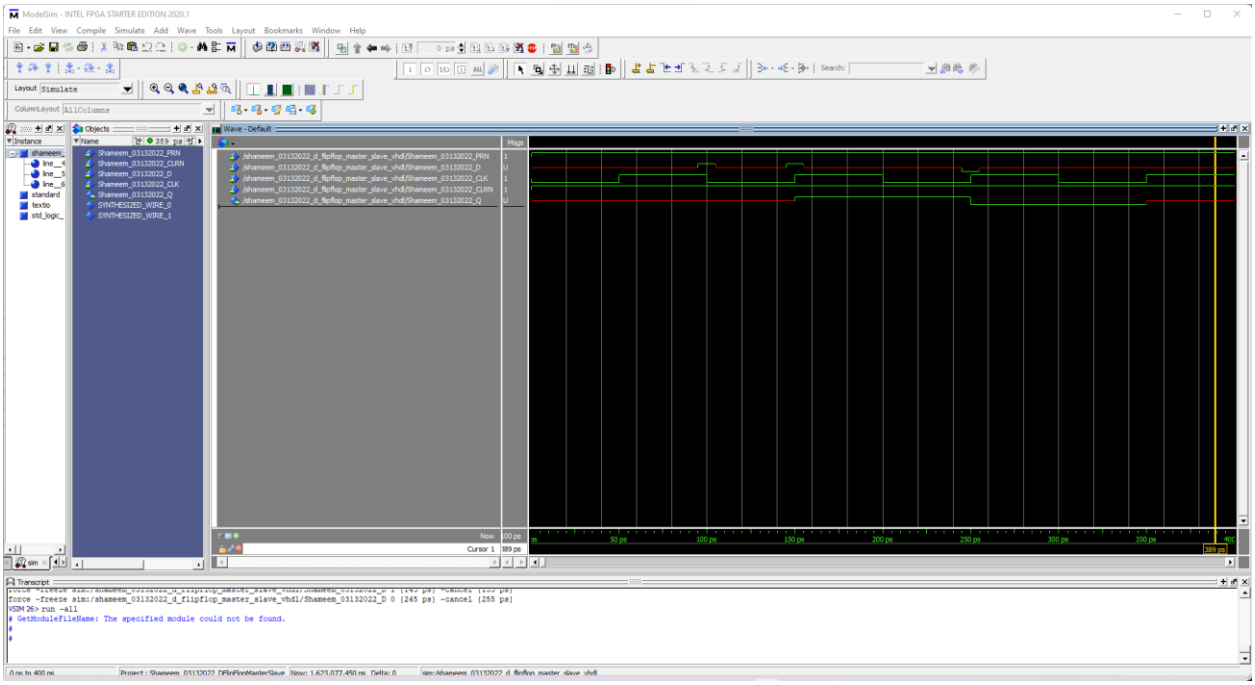


At the moment when input E first moves from 0 to 1, output Q leaves the undefined state and starts mirroring D. This is the same waveform as the third simulation in Lab 4A.



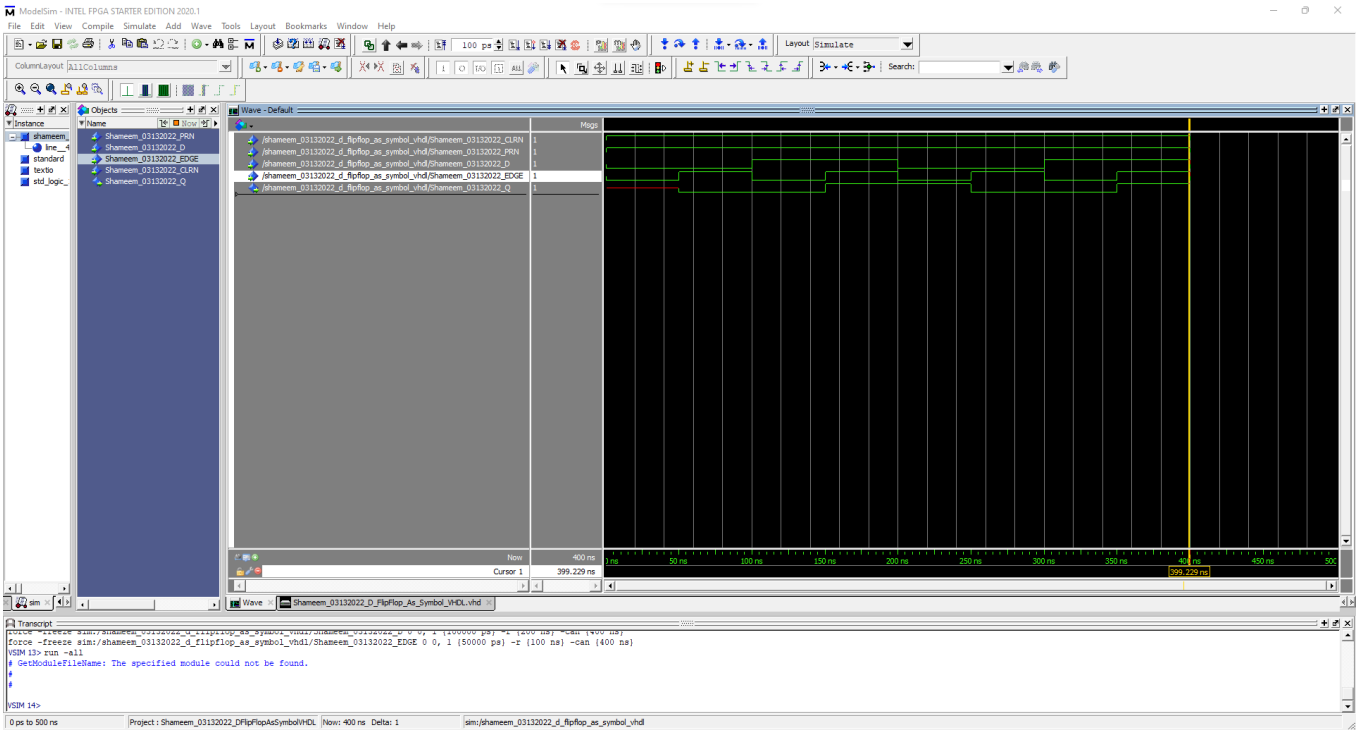
Output Q drops to 0 and stays there as long as CLRN is 0. This is the third setup in LAB 4A and it still follows the waveform showed.

Part 2



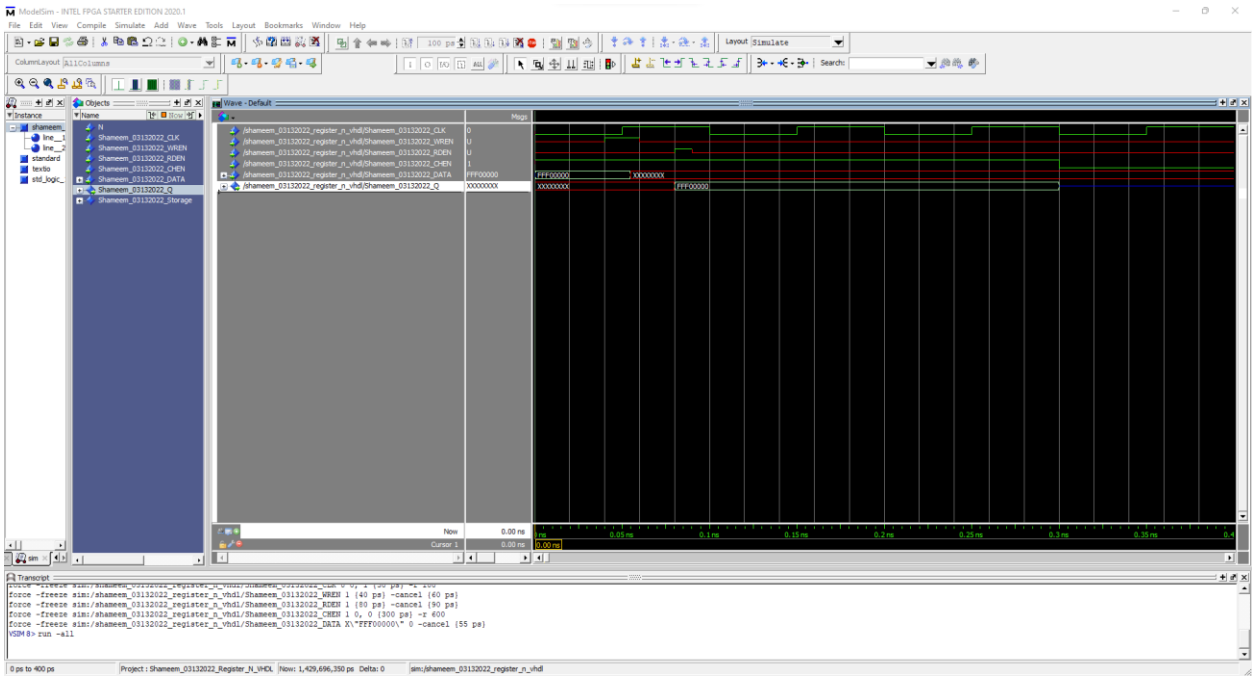
Simulation of the Master-Slave D-FlipFlop shows the same wave patterns as the simulation lab.

Part 3

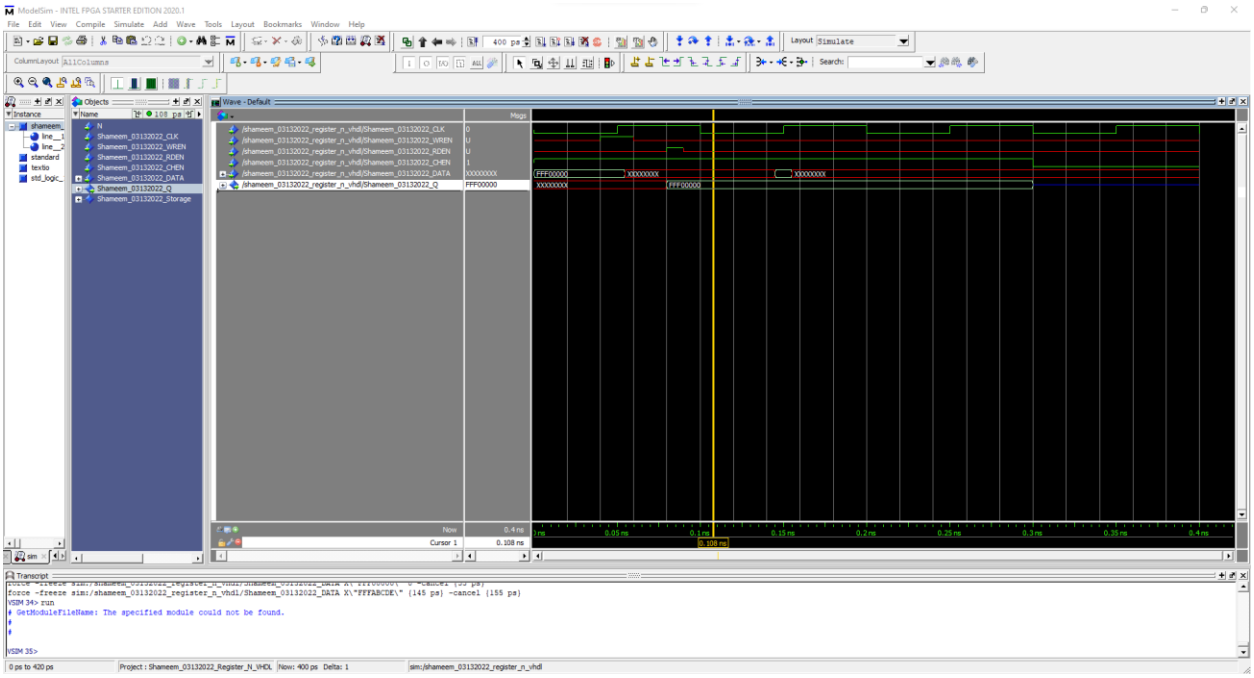


Forced CLRN and PRN to 1 and Edge as a clock oscillating twice the speed of D. This resulted in the same waveform as the lab simulation.

Lab 4B

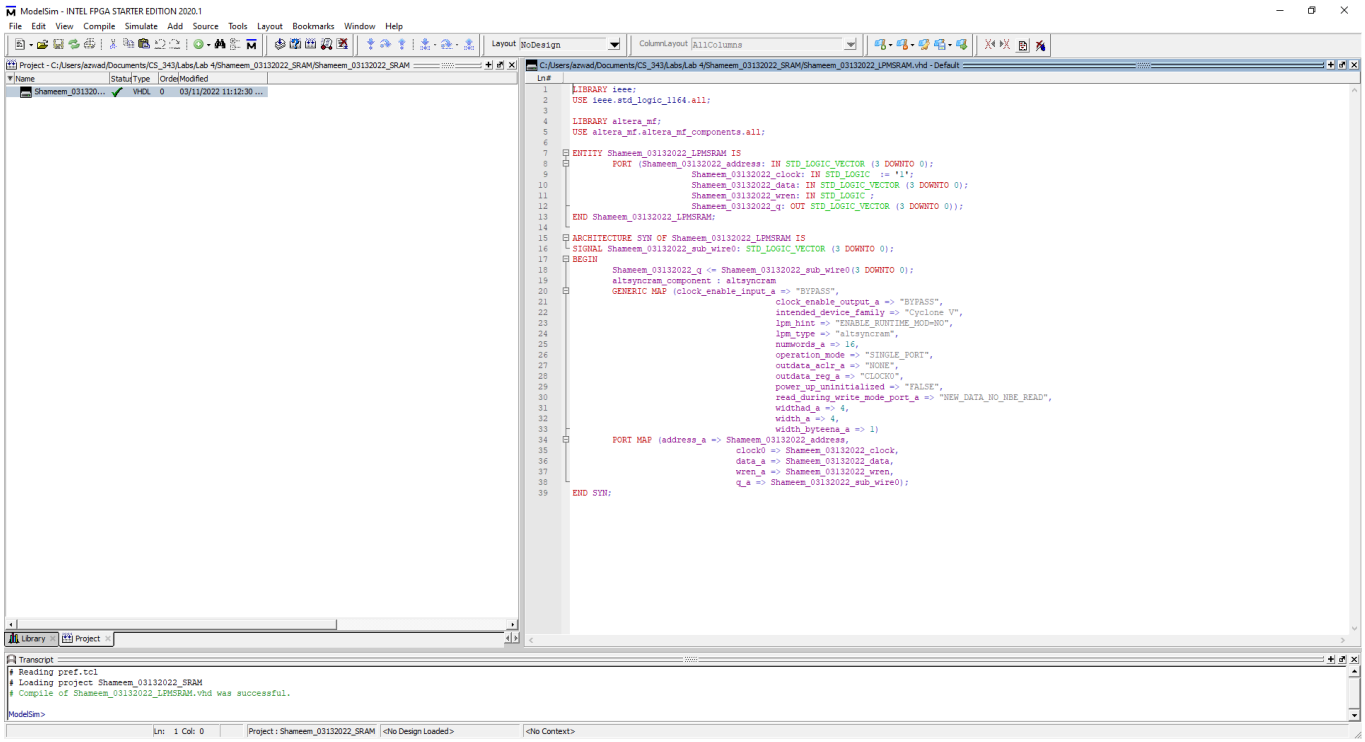


The waveform follows the instructions of the signals as shows the same waveform as the simulation.

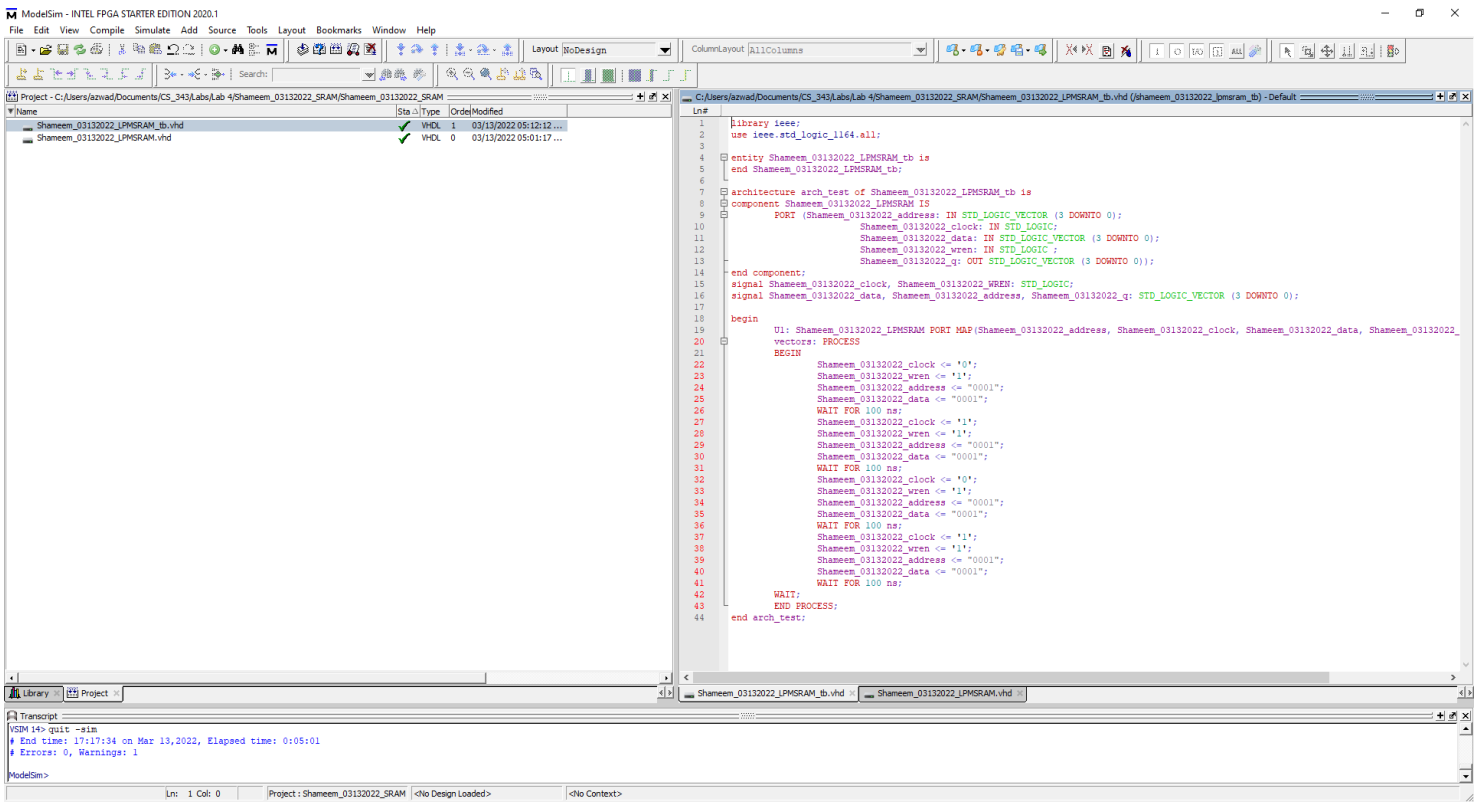


Waveform after adding after adding new data for 145 ps to 155 ps.

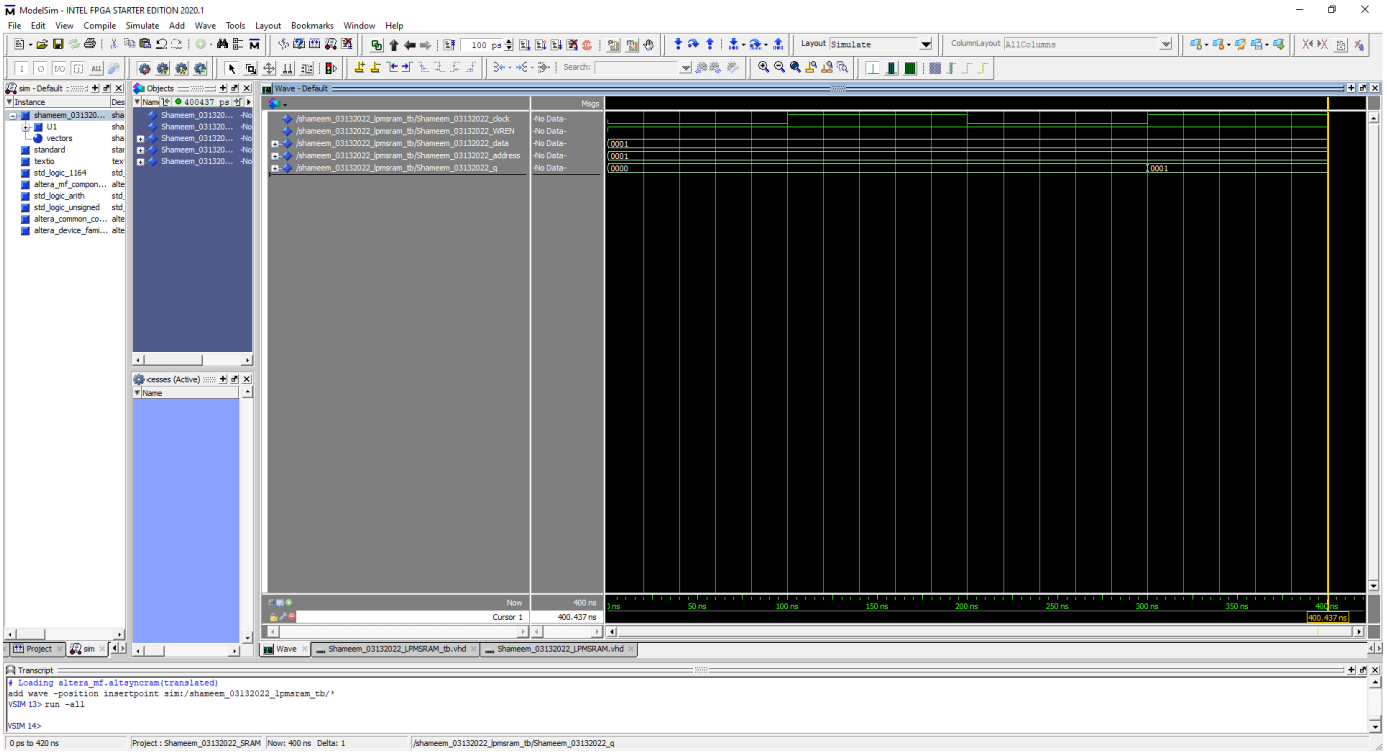
Memory Lab



LPM SRAM VHDL Code in ModelSim compiled successfully.



LPM SRAM testbench, used only 0001 to test if it works.



LPM SRAM Simulated with a testbench