

CS 342000 / CS343000
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The screenshot displays the Intel FPGA Starter Edition 2020.1 IDE interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Wave, Tools, Layout, Bookmarks, Window, and Help. The top toolbar contains icons for various simulation and design tasks. The top status bar shows the project name 'ColumnLayout_011000000' and the current layout 'Layout: Simulate'. The left pane shows a project tree with 'shameen_03_23' selected. The main area shows a waveform with signals like 'shameen_03_23_22_datamemory/shameen_03_23_22_address' and 'shameen_03_23_22_datamemory/shameen_03_23_22_data'. The bottom status bar indicates the simulation is at 0 ps to 3600 ps.

From 0 ps to 500 ps the Data memory is reading 5 integers from the .mif file from addresses 0 to 4. From 500 ps to 1000 ps the Data Memory is writing to SRAM memory by enabling wren=1 and using data as the input to write 5 different numbers to SRAM memory. From 1000 ps to 1600 ps the Data memory reads from the addresses 4 to 0 to make sure the 5 different numbers written to SRAM memory is written correctly.

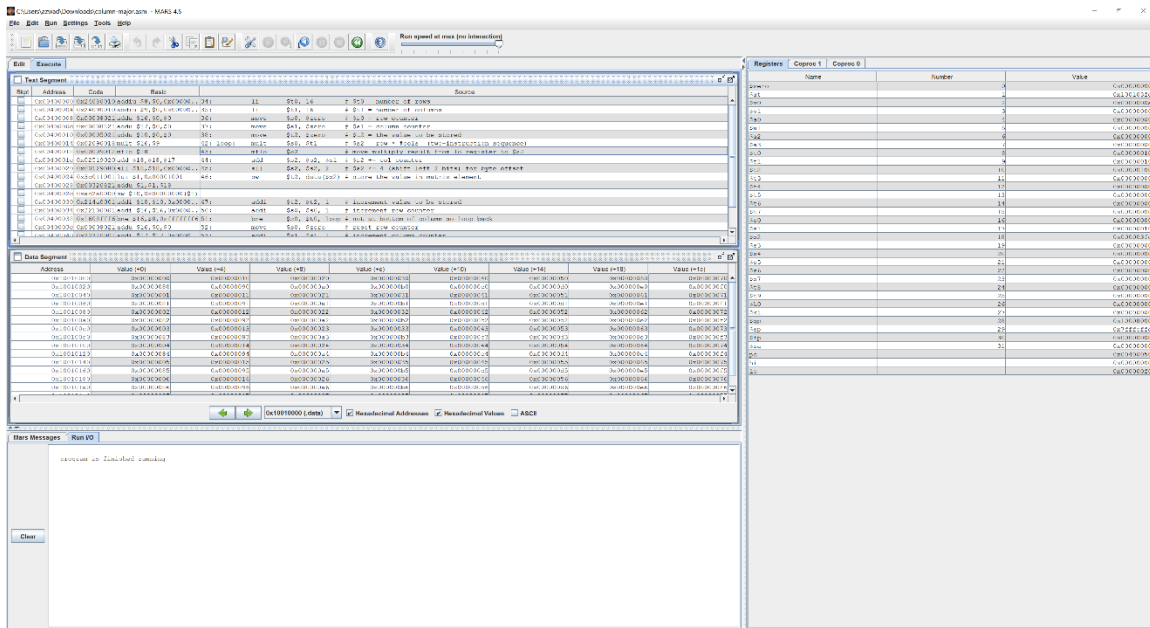
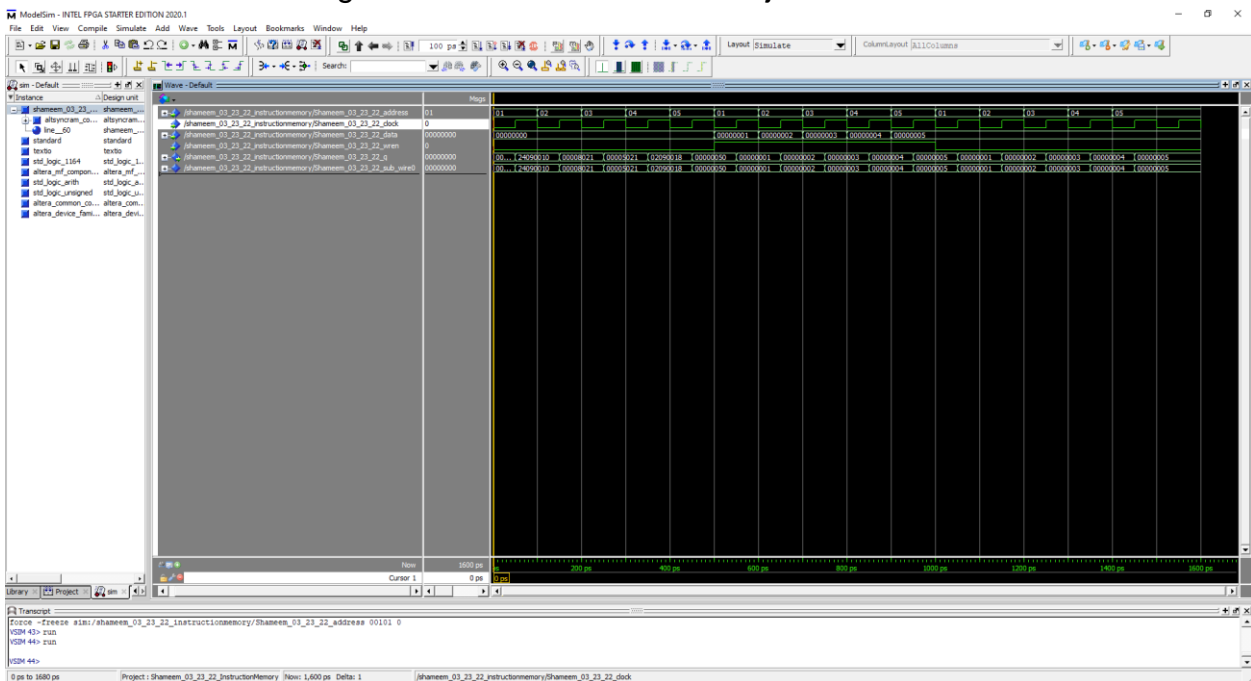


Figure 2: Mars – ran column-major.asm

Figure 3: Simulation of Instruction Memory NOTE: The radix is **Hexadecimal** in simulation.

From 0 ps to 500 ps the Instruction Memory is reading 5 integers from Mars instruction from addresses 1 to 5. From 500 ps to 1000 ps the Instruction Memory is writing to SRAM memory by enabling wren=1 and using data as the input to write 5 different numbers to SRAM memory. From 1000 ps to 1600 ps the Instruction Memory reads from the addresses 5 to 1 to make sure the 5 different numbers written to SRAM memory is written correctly.