Design of Gilbert Cell Multiplier using 28nm CMOS Technology

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***Abstract*— This document explores the design of a Gilbert cell using 28nm CMOS technology. A Gilbert cell is a mixer. It multiplies two input signals and produces their product as the output. It allows 4-quadrant multiplication. Hence, it is an integral component of integrated circuit balanced multipliers.**

Keywords— Gilbert cell, balanced multiplier, 28nm CMOS

I. RERENCE CIRCUIT DETAILS

The Gilbert cell is based on cascode structure. It is formed by stacking two differential pairs on top of a control differential pair. CMOS technology is better suited for digital circuits than bipolar technology due to its low processing cost and low power consumption. However, reaching the level of nonlinear error that bipolar multipliers can achieve is difficult in CMOS technology.[2]

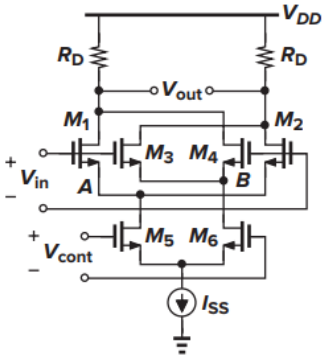

Figure 1: Gilbert cell [3]

II. REFERENCE CIRCUIT DESIGN

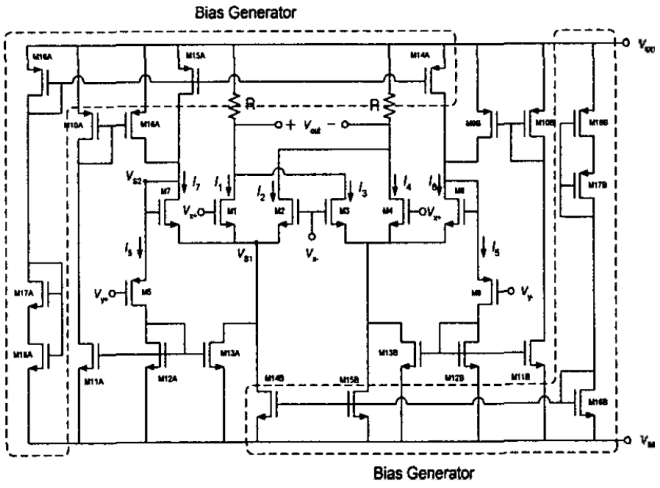

Figure 2: Circuit diagram of a CMOS multiplier using Gilbert cell [1]

III. REFERENCE WAVEFORMS AND AREA ESTIMATE

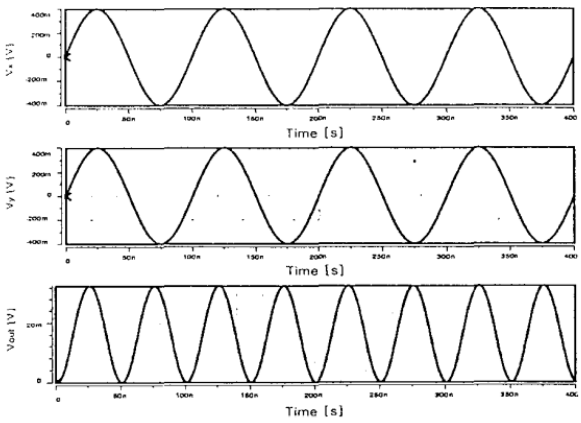

Figure 3: Multiplier of two sine waves of the same frequency [1]

Table 1: Performance parameters of reference circuit fabricated using 0.8µm CMOS technology [1]

Power supply voltage	2V
Bias currents (M14A~M18A, M14B~18B)	12 μA
Input range	±0.4V
Linearity error	< 1.3%
-3dB Frequency	288MHz
Power dissipation	255 μW
Active chip area	130×250 μm^2

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