

unit-1

→ Brief introduction to IC Technology;

Integrated circuit: It is a circuit where all components, such as passive and active elements are fabricated on single crystal chip is called integrated circuit.

→ The first IC consist of two transistors and other components.

→ As on increasing the no. of components (or) transistor per IC, the technologies was developed as follows.

| Name | Year | Transistor | logic-gates number |
|--------------------------------------|------|---------------------|--------------------|
| Small-scale Integration (SSI) | 1964 | 1 to 10 | 1 to 12 |
| medium-scale Integration (MSI) | 1968 | 10 to 500 | 13 to 99 |
| large-scale Integration (LSI) | 1971 | 500 to 20,000 | 100 to 9,999 |
| Very large-scale Integration (VLSI) | 1980 | 20,000 to 1,000,000 | 10,000 to 99,999 |
| Ultra large scale-Integration (ULSI) | 1984 | 1,000,000 to more | 100,000 and more |

→ classification of IC's

→ IC's are of two types namely

{ Linear IC's

2. Digital IC's

1. Linear IC: These are used when relationship

between input and output of a circuit

is linear.

Ex: op.Am, FET, Transistor, etc.

2. Digital IC: When the circuit is in on-state (or) off-state and not in two states, that circuit is called Digital IC.

A. Advantages of IC:

- low power consumption
- low weight
- low cost
- small in size
- reliability

Disadvantages

- operates at low voltage
- quite delicate.

I_{DS} vs. Relationships

→ Here I_{DS} = Drain to source current

V_{DS} = Drain to source voltage

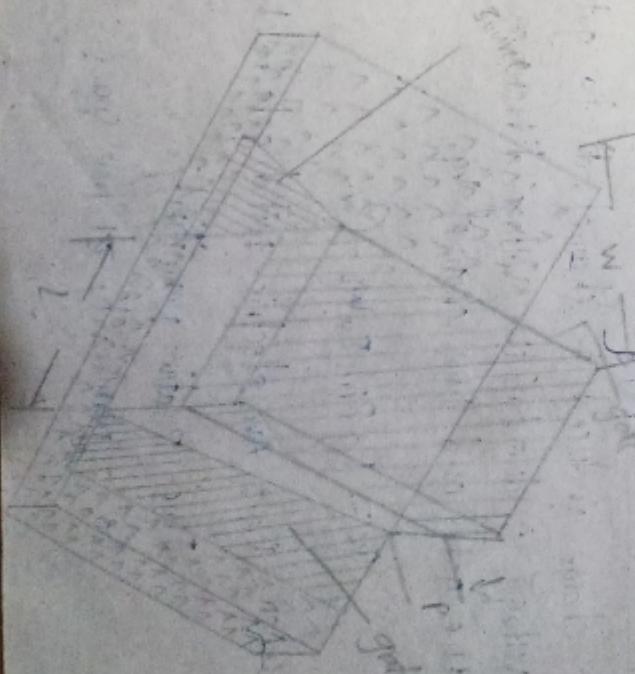
→ since the charge induced is dependent upon the gate to source voltage (V_{GS}), the I_{DS} depends upon both V_{GS} and V_{DS}

$$I_{DS} = -\bar{I}_{SD} = \frac{\text{charge induced in channel}(\sigma)}{\text{Electron transit time}(\tau)}$$

First transit time

$$\tau_{SD} = \frac{\text{length of channel}(l)}{\text{velocity}(v)}$$

(1)



-> Above figure show the NMOS transistor structure

$$\text{velocity } (V) = \mu E_{ds}$$

where μ : mobility

E = Electric field.

Now

$$E_{ds} = \frac{V_{ds}}{L}$$

$$V = \frac{\mu V_{ds}}{L}$$

$$T_{sd} = \frac{L^2}{\mu V_{ds}}$$

$$T_{sd} = \frac{L^2}{\mu V_{ds}} - \textcircled{2}$$

Non-Saturated Region

-> charge induced in channel due to gate

Voltage is due to the voltage difference b/w the gate and the channel V_{gs} .

$$Q_C = F_g \epsilon_{ins} \epsilon_0 W L - \textcircled{3}$$

where

F_g : Avg electric field gate to channel

ϵ_{ins} : Relative permittivity

ϵ_0 : permittivity of free space

Now consider,

$$F_g = \left[\frac{(V_{gs} - V_t)}{L} - \frac{V_{ds}}{2} \right]$$

Sub F_g value in eq(3)

$$Q_C = \left[\frac{(V_{gs} - V_t) - \frac{V_{ds}}{2}}{L} \right] \epsilon_0 \epsilon_{ins} W L - \textcircled{4}$$

$$\bar{I}_{ds} = \frac{Q_C}{2}$$

$$\bar{I}_{ds} = \frac{\left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right] \epsilon_0 \epsilon_{ins} W L}{L^2}$$

$$\bar{I}_{ds} = \left[\frac{\mu V_{ds}}{L^2} \left((V_{gs} - V_t) - \frac{V_{ds}}{2} \right) \right] \epsilon_0 \epsilon_{ins} W L$$

$$\bar{I}_{ds} = \epsilon_0 \epsilon_{ins} \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$\bar{I}_{ds} = \mu \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] - \textcircled{5}$$

$$\bar{I}_{ds} = \beta \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] - \textcircled{6}$$

$$\bar{I}_{ds} = \frac{C_m}{L^2} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad (7)$$

$$\bar{I}_{ds} = \frac{C_m w}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad (8)$$

Saturation Region: saturation begins when

$$V_{ds} = V_{gs} - V_t$$

$$\bar{I}_{ds} = k \frac{w}{L} \left[(V_{gs} - V_t) (V_{gs} - V_t) - \frac{(V_{gs} - V_t)^2}{2} \right]$$

$$= k \frac{w}{L} \left[(V_{gs} - V_t)^2 - \frac{(V_{gs} - V_t)^2}{2} \right]$$

$$\bar{I}_{ds} = k \frac{w}{L} \left[(V_{gs} - V_t)^2 \right] \quad (9)$$

Transconductance (G_m): It is the relation ship between output current \bar{I}_{ds} and input voltage V_{gs} is called transconductance.

$$G_m = \frac{\partial I_{ds}}{\partial V_{gs}} \quad V_{ds} = \text{constant}$$

O/p conductance (G_{os}):

$$\bar{I}_{ds} = \frac{G_m w}{L^2} \left[\frac{(V_{gs} - V_t)^2}{2} \right] \quad (10)$$

$$\bar{I}_{ds} = \frac{G_m w}{L} \left[\frac{(V_{gs} - V_t)^2}{2} \right] \quad (11)$$

Mos transistor threshold voltage : The minimum voltage required to switch on the mos transistor is called mos transistor threshold voltage.

Or

The voltage applied between gate and source of a mosfet to turn on device is called mos transistor threshold voltage.

\rightarrow output conductance (G_{os}) can be expressed as

$$G_{os} = \frac{\partial I_{ds}}{\partial V_{ds}}$$

Figure of merit :

-> It is a ~~quantity~~ quantity used to characterize the performance of a device by comparing with other devices of similar kind. It is called figure of merit.

-> defined as : $\omega_0 = g_m / c_g$

where, g_m = Transconductance

c_g = gate capacitance

-> From equation switching speed depends upon

1. carrier mobility

2. gate voltage.

3. Inversely on square of channel length.

The pass Transistor:

-> The main advantage of pass transistor used in circuit is we can avoid unnecessary transistors.

o

-> The No. of transistors are reduced in the circuit.

-> N-MOS Inverter circuit diagram shown in below figure.

-> Pass characteristics

| Device | Transmission of '1' | Transmission of '0' |
|--------|---------------------|---------------------|
| N | poor | good |
| P | good | poor. |

-> Truth table of two-input AND gate using pass transistor

| A | B | F = AB |
|---|---|--------|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

* NMOS Inverter

-> The word NMOS stands for "N channel metal oxide semiconductor".

-> NMOS Inverter is a versatile electronic component.

-> widely used as switch in various electronic applications.

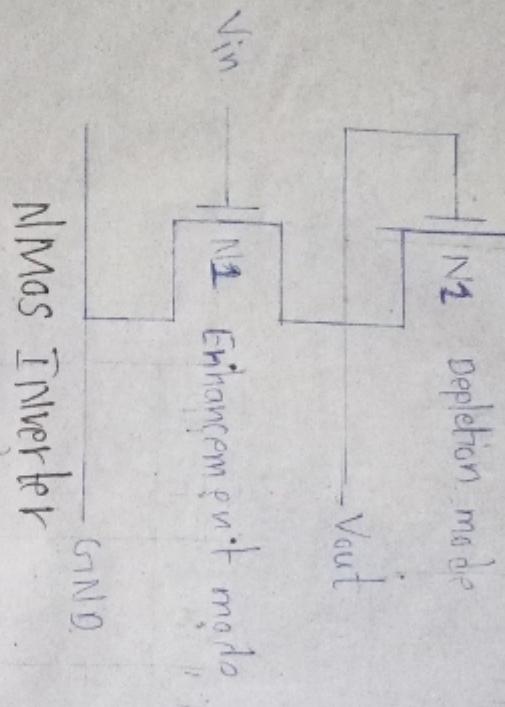
V_{DD}

$\rightarrow V_{in} = 0 \rightarrow N1 \rightarrow \text{open ckt.}$

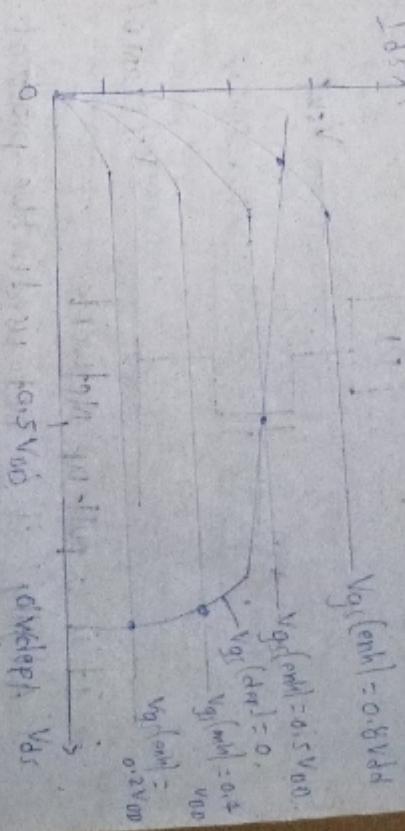
$\rightarrow V_{in} = 1 \rightarrow N2 \rightarrow \text{short ckt.}$

$\rightarrow V_{in} = \frac{V_{DD}}{2} \rightarrow N1N2 \rightarrow \text{saturation}$

\rightarrow output characteristics



- > The basic inverter circuit consists of two transistors with source connection, ground (GND), positive supply (V_{DD})
- > For depletion mode transistor, the gate is connected to source so it is always on.
- > In above circuit,
- > The depletion mode is called pull-down transistor
- > The enhancement mode is called pull-up transistor

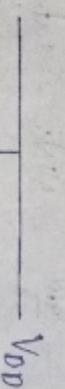


- > In above output characteristics graph.
- $V_{GS}(\text{enh})$ indicates Enhancement mode curves
- $V_{GS}(\text{dep})$ indicates depletion mode curves

* The various pull-ups

1. The Load Resistance R_L :

→ Actually:

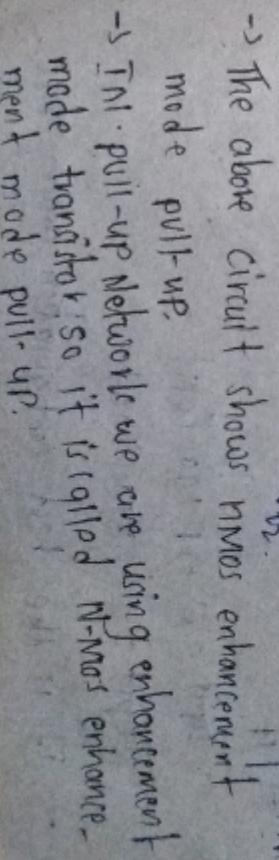
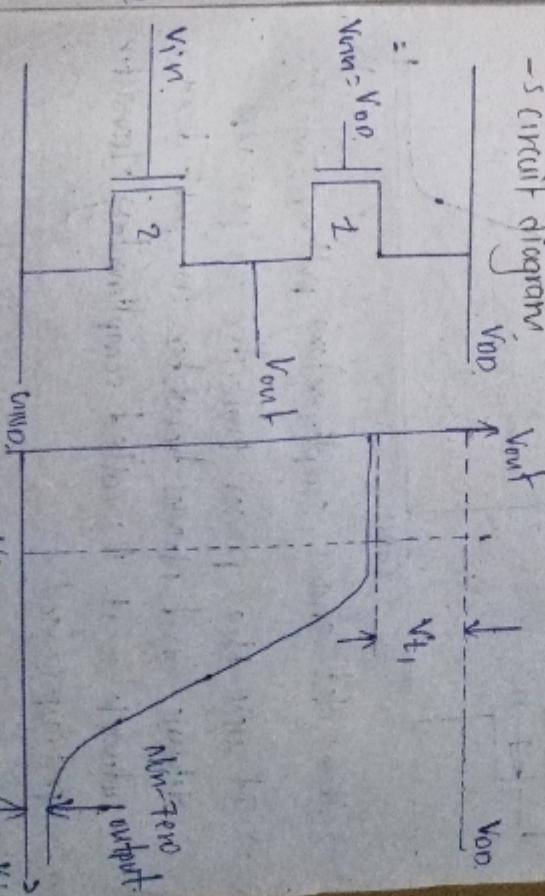


→ It is a pull-up network.

→ Actually it is not used in the practical use, because it occupies more resistors.

2. N-Mos depletion mode pull-up

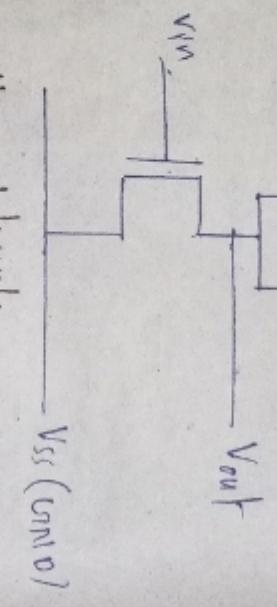
→ circuit diagram vout vs v_in



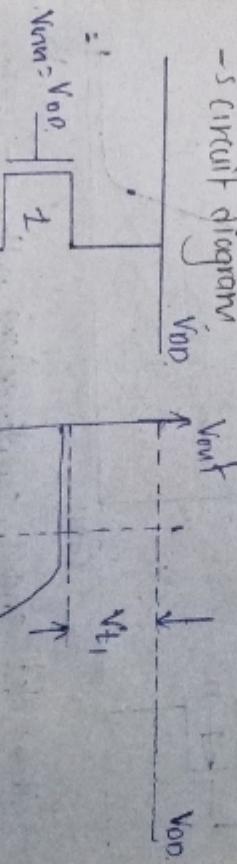
→ The above circuit shows NMOS depletion mode pull-up.

→ The above circuit shows NMOS enhancement mode pull-up.

→ The above circuit shows NMOS depletion mode pull-up.



→ circuit diagram vout vs v_in

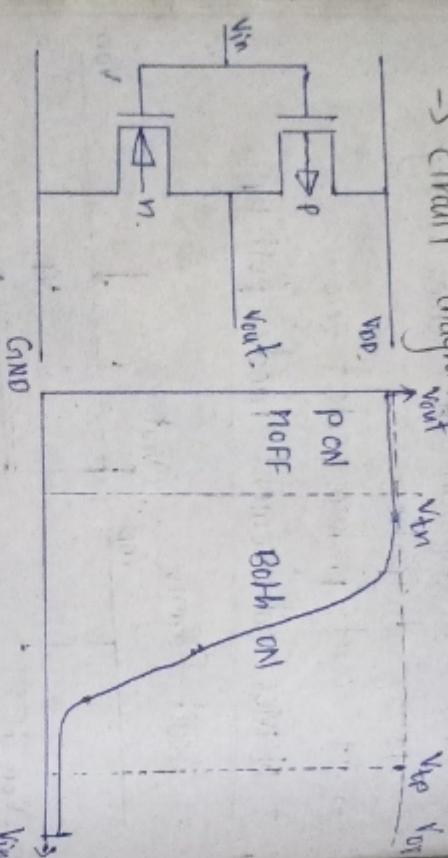


→ Above arrangement consumes a high power dissipation.

→ It can't produce perfect zero.

+ Complementary Transistor - pull-up (CMOS)

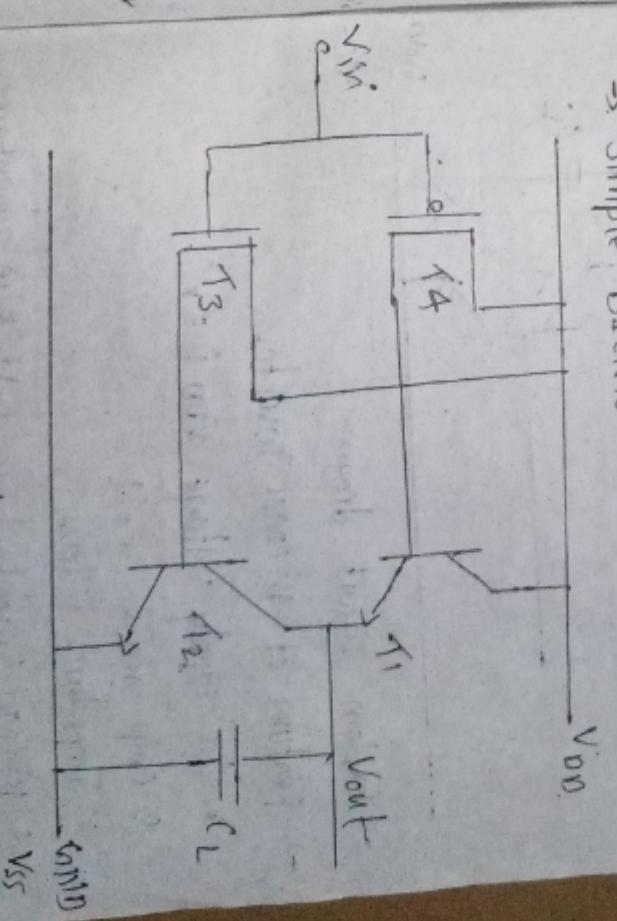
→ circuit diagram



→ Above circuit shows Complementary pull-up(CMOS).

→ It uses the PMOS transistor in pull-up Network and NMOS transistor in pull-down Network so it is called complementary Transistor pull-up (CMOS).

→ Explain circuit diagram.



→ Hence it is CMOS, we know that speed of BJT is very high.

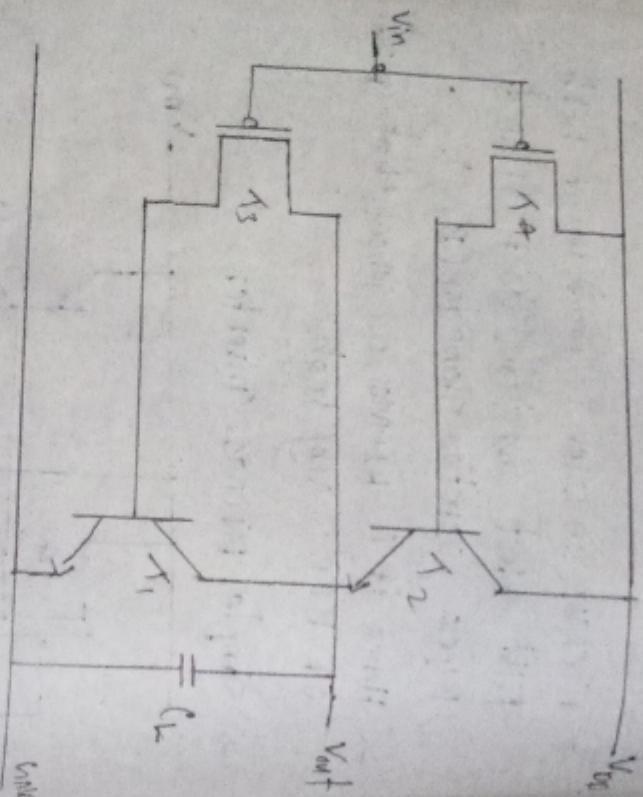
→ Simple CMOS Inverter

→ where BICMOS Inverter

→ BICMOS Inverter is made up of both Field effect transistor(MOSFET) and Bipolar Junction Transistor(BJT).

- If Input = 0 → PMOS (on)
- Input = 1 → NMOS (on)
- It is the best configuration among all

→ An alternative BiCMOS Inverter with no static current.



→ Explain circuit diagram.

→ Features of BiCMOS Inverter.

- The supply voltage V_{DD} is 5V.
- Chip area is small.

• Impedance is low.

• BiCMOS Inverter have both the advantage of RJT and CMOS.

- c. The Max o/p voltage $V_{DD} - 0.7V$.

- c. The min o/p voltage is $0.7V$.

* CMOS Inverter analysis and design

→ CMOS stands for Complementary metal-oxide semiconductor Inverter.

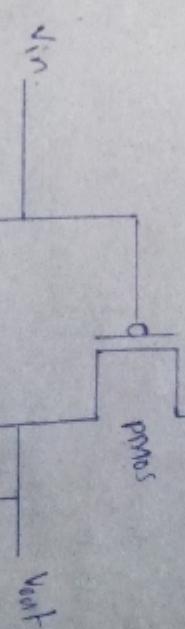
→ It is a type of silicon chip used in many devices.

→ For many electronic devices, CMOS serves as a brain.

→ Its size is small and significant.

→ Schematic design of CMOS Inverter.

V_{DD}



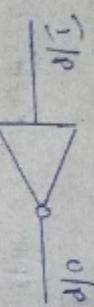
V_{DD}

GND

→ CMOS Inverter design consist of two transistors namely PMOS, NMOS connected in series.

→ Transistors connected b/w source and drain.

- Here input V_{in} is mutually connected to two transistors.



\rightarrow Types of CMOS Inverter.

o. Static CMOS Inverter.

o. Dynamic CMOS

o. Pseudo NMOS

o. Conventional CMOS

\rightarrow Components of CMOS Inverter.

o. NMOS Enhancement Transistor.

o. PMOS Transistor.

o. Substrate.

o. V_{DD} and V_{SS}

o. Gate Connection

\rightarrow Characteristics of CMOS Inverter.

| \bar{I}/ρ | I/ρ |
|----------------|----------|
| 0 | 1 |
| 1 | 0 |

o Advantages

→ Low power consumption
→ More Applications

Diseadvantages

→ High cost.
→ Finite propagation

* Difference b/w CMOS and Bipolar

CMOS

Bipolar

\rightarrow Low power dissipation.

\rightarrow Low g_m (g_m < v_{in})

\rightarrow High input impedance

\rightarrow High package density

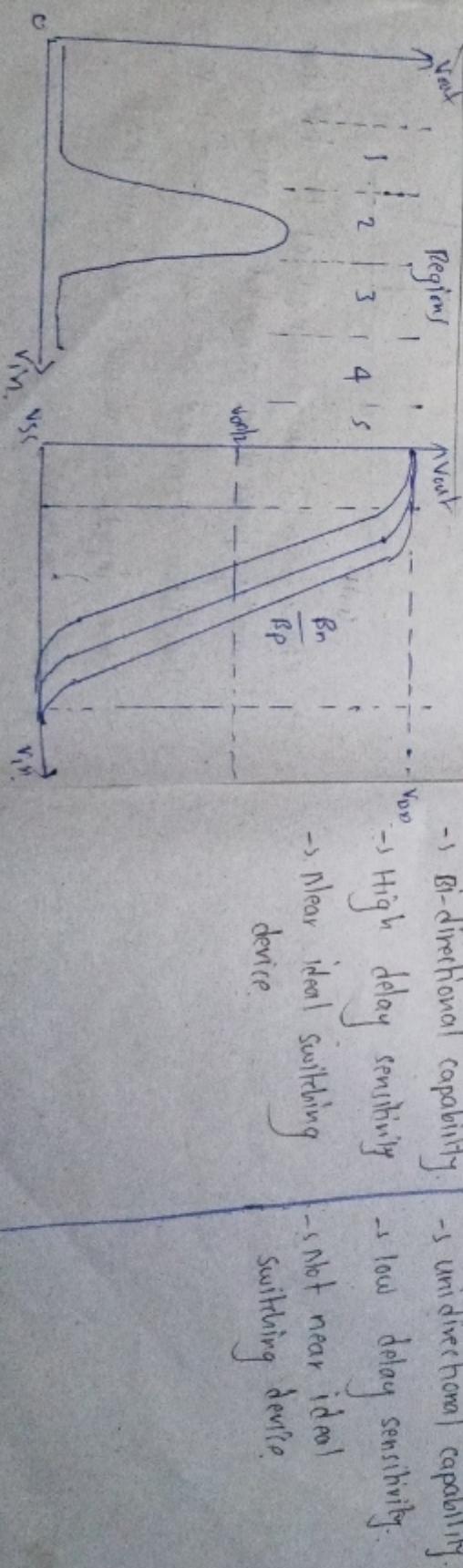
\rightarrow High noise margin

\rightarrow Low o/p drive current

\rightarrow Bi-directional capability

\rightarrow High delay sensitivity

\rightarrow Near ideal switching device



* BiCMOS Technology

→ BiCMOS is combination of ~~of~~ Bipolar and CMOS.

Advantages

- s used in analog Amplifiers.
- Low power dissipation.
- s High speed.
- s Low latch up problem.

Disadvantages

- Fabrication is complex
- s High cost.

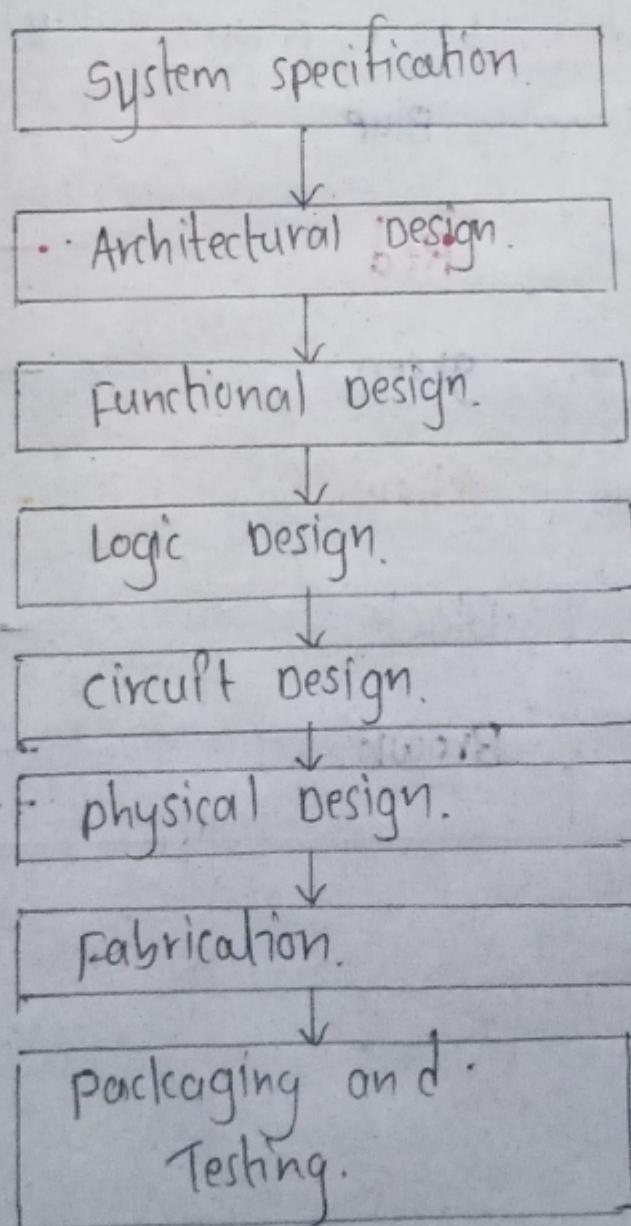
Applications

- In Microprocessor.
- s sample and hold circuit.
- s Adders, mixers, etc.

unit - 2

* VLSI Design flow

- > very large scale integration is the process of making integrated circuits (ICs) by combining no. of components like R,L,C, transistors on a single chip.
- > VLSI design flow is iterative cycle.



* Mos layers :

- Mos layer - metal oxide semiconductor layer.
- The four basic Mos layers.

- a H-diffusion
- b p-diffusion
- c polysilicon
- d Metal

| Layer Name | Layer colour | Representation |
|-----------------------------|--------------|----------------|
| 1. Metal | Blue | — |
| 2. polysilicon | Red | — |
| 3. N ⁺ diffusion | green | — |
| 4. P ⁺ diffusion | yellow | — |
| 5. Contact | black | — |
| 6. Demarcation Line | Brown | — |

| Transistors | Colour coding | Representation |
|--------------------|----------------|----------------|
| 7. NMOS transistor | red over green | — |

| | | |
|--------------------------------|--|---|
| 8. PMOS transistor | red over yellow | — |
| 9. NMOS which is in depletion. | red over green with yellow in X at center. | — |

* Stick diagram :

The stick diagrams are the rough representation for layout diagram.

→ Here the devices and conductors are represented by "sticks".

→ Stick diagram doesn't include size, length and width of devices.

→ Ex. NMOS layout.

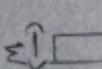
NMOS - stick diagram

n⁺ (green)

n⁺

poly-silicon.

poly-silicon
(red)



- stick and layout diagram are represented in colours.
- Layout diagram means representing a transistor, n+p+ in block representation, each layer having length and width.
- stick diagram, means representing a transistor, n+p+ in layers on sticks.

* Design Rules and layout:

- Design Rules provide an effective interface between the circuit and system and fabrication engineer
- Generally there are two types of design rules.

* Lambda-based design rules

- Lambda based design rules are based on a single parameter Lambda.

* Scaling of MOS circuits

Scaling: The process of reduction of feature size (L) and width (w) is called scaling.

→ Scaling improves performance and reduces the overall fabrication cost.

Impact of scaling

→ power dissipation.

→ production cost.

→ Max operational freq.

→ No. of gates on one chip.

Scaling methods

→ Three types of scaling methods used in VLSI.

○ combined voltage (V) & dimension (D) scaling model

→ Consider two scaling factors α, β .

→ $1/\beta$ is supply voltage.

→ $1/\alpha$ is linear dimension.

○ constant electric field model:

$$\rightarrow \alpha = \beta$$

○ constant voltage scaling model

$$\rightarrow \beta = 1$$

* Scaling Factors

1. gate Area (A_g) :

$$A_g = L \times W, \quad L: \text{channel length}$$

W : channel width

\rightarrow Both are scaled by $\frac{1}{\alpha}$

$$A_g = \frac{1}{\alpha} * \frac{1}{\alpha}$$

$$\boxed{A_g = \frac{1}{\alpha^2}}$$

2. Gate capacitance per unit area (C_0) :

$$C_0 = \frac{\epsilon_0 \gamma}{D}$$

$$C_0 = \frac{1}{(\frac{1}{\alpha})} = \beta$$

$$\boxed{C_0 = \beta}$$

③ gate capacitance (C_g) :

$$C_g = C_0 * L * W$$

$$C_g = \beta * \frac{1}{\alpha}$$

$$\boxed{C_g = \frac{\beta}{\alpha}}$$

④ parasitic capacitance (C_p)

$$C_p = \frac{A_p}{d} \Rightarrow C_p = \frac{1/\alpha^2}{1/\alpha} \Rightarrow \boxed{C_p = \frac{1}{\alpha}}$$

(3) carrier density (in channel) (Q_{ch}):

$$Q_{ch} = \epsilon_0 \gamma V_{gs}$$

$$Q_{ch} = \beta * \frac{1}{\beta}$$

$$\boxed{Q_{ch} = 1}$$

⑤ channel resistance (R_{ch})

$$R_{ch} = \frac{L}{W} * \frac{1}{Q_{ch} + M_C}$$

$$= \frac{1}{\alpha} * \frac{1}{1+1}$$

$$\boxed{R_{ch} = \frac{1}{2}}$$

⑥ gate delay (τ_d)

$$\tau_d = R_{ch} * \gamma$$

$$= 1 * \frac{\beta}{\alpha}$$

$$\boxed{\tau_d = \frac{\beta}{\alpha}}$$

⑦ current density (J)

$$J = \bar{J}_{dn} / \alpha$$

$$J = \frac{1/q}{1/\alpha} = \alpha$$

$$\boxed{J = \frac{\alpha}{q}}$$

⑧ power dissipation per unit area (W)

$$P_A = \frac{P_d}{A} = \frac{1/p^2}{1/\alpha^2}$$

$$\boxed{P_A = \frac{\alpha}{p^2}}$$

⑨ power speed product (R_s)

$$P_T = V_{gs} I_S V_D$$

$$= \frac{1}{\alpha} * \frac{\beta}{\alpha}$$

$$\boxed{P_T = \frac{1}{\alpha^2} * \frac{\beta}{\alpha}}$$

* Limitations of scaling

- > Substrate doping.
- > limit due to current density
- > limit due to subthreshold current.
- > limit of interconnect.
- > limit of contact resistance.
- > limit of miniaturization.
- > limit of logic levels.

1. Substrate doping

- > The effect of barrier potential is neglected
- > As the channel length reduced, depletion region width also reduced

$$\rightarrow \text{depletion width } d = \sqrt{\frac{2\epsilon_0 \epsilon_{Si} V}{q N_D}}$$

where N_D = doping level.

$$V_e = \text{effective voltage. } (V = V_a + V_b)$$

2. Limit of miniaturization

- > The minimum size of transistor is determined by both technology and physics of transistor.
- > Transistor size determined in terms of length L .

$$\rightarrow \text{Depletion width } D = \sqrt{2\epsilon_0 \epsilon_{Si} V/q N_D}$$

where

ϵ_{Si} = relative permittivity of silicon.

ϵ_0 = permittivity of free space.

V = Effective voltage.

$$V = V_a + V_b$$

3. Limit due to subthreshold currents

\rightarrow The subthreshold current I_{sub} is directly proportional to $e^{(V_{gs} - V_t)^2/2\tau}$

\rightarrow As voltages are reduced, the ratio of $(V_g - V_t)$ will reduce, so I_{sub} current increases

④ limits of interconnects and contact resistance

\rightarrow Since, width, thickness and spacing of interconnections are scaled by $1/\alpha$.

\rightarrow Cross-sectional Area scaled by $1/\alpha^2$, conductor length is also $1/\alpha$.

\rightarrow If interconnections are increased both resistance, capacitance of interconnects are increases.

⑤ limit due to depletion width

\rightarrow When N_D increased, the depletion width decreases and V_E increases, which is not desirable.

$$V_{diff} = \mu E, L = 2d$$

$$\text{Transit time } \tau = 1/V_{diff} = 2d/\mu E$$

* Design rules and layout :

-> The physical mask layout of any circuit to be manufactured using a particular process and must to follow set of rules called as Layout Design Rules.

-> These rules specify length of and width, minimum size of objects on chip such as transistor, metal, poly silicon etc

-> The design rules are usually described in two ways.

1. Micron Rules : The layout contains such

as size, length, width, are stated in micrometers are called micron rules.

2. Lambda Rules: The layout contains such as size, length, width, in term of single parameter (λ), it called Lambda Rules.

o Lambda based design rules for wires

minimum width.

n -diffuser.

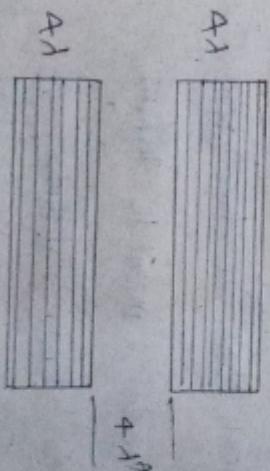
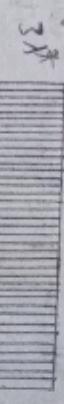
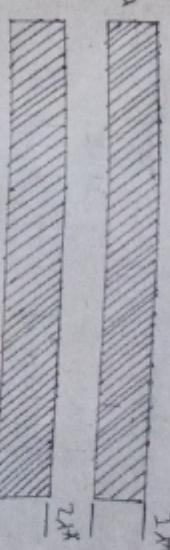
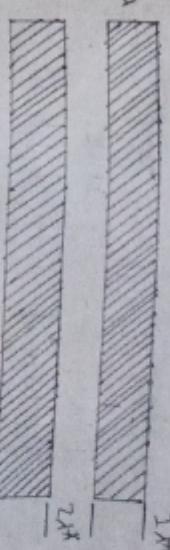
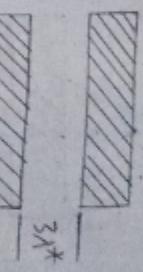
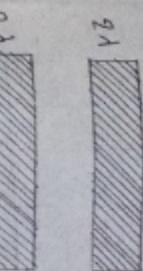
p -diffuser.

thinox.

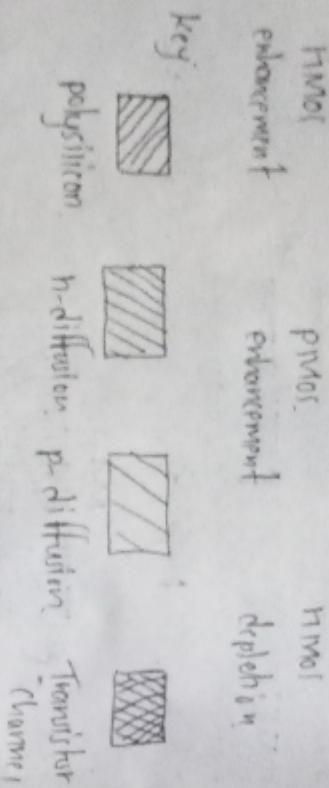
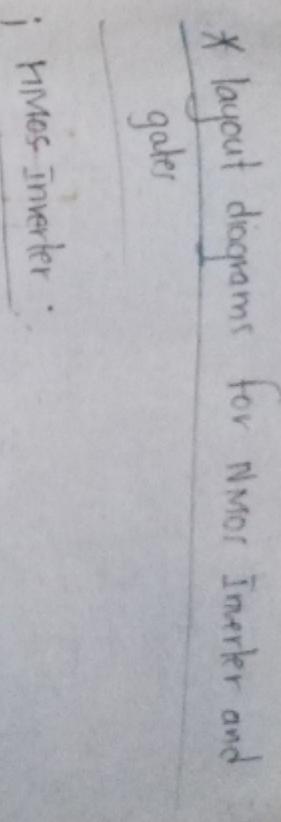
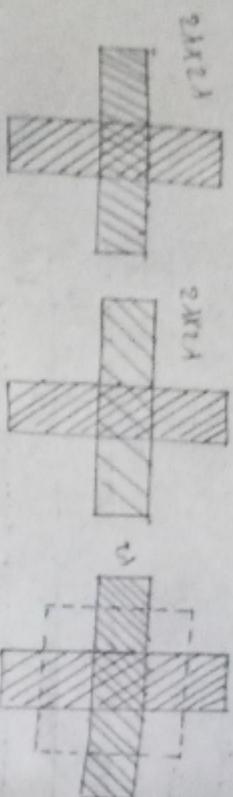
poly silicon.

Metal 1

Metal 2



* o Lambda based design rules for Transistor



o Lambda based design, rules for contacts

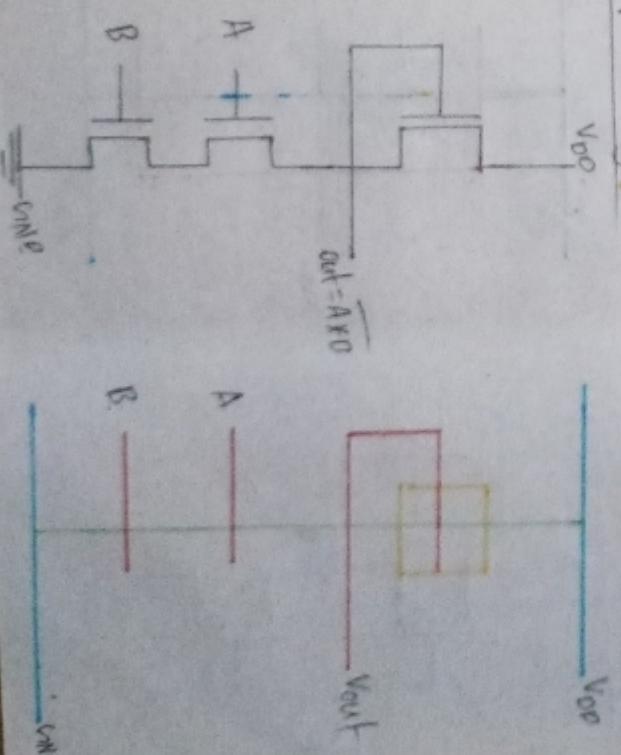
-> contact means, making connections below layer

-> when making connections below metal, polysilicon and diffusion there are three possible ways

1 poly to metal & metal to diffusion.

ii Buried contact (poly to diffusion)

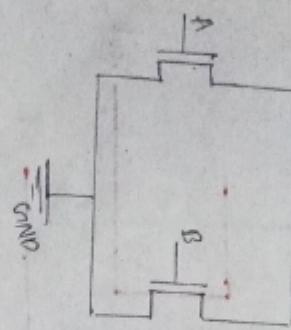
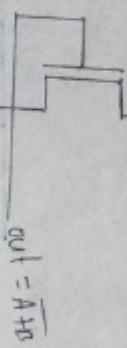
iii Butting contact (poly to diffusion through metal)



(3) Input Nor gate

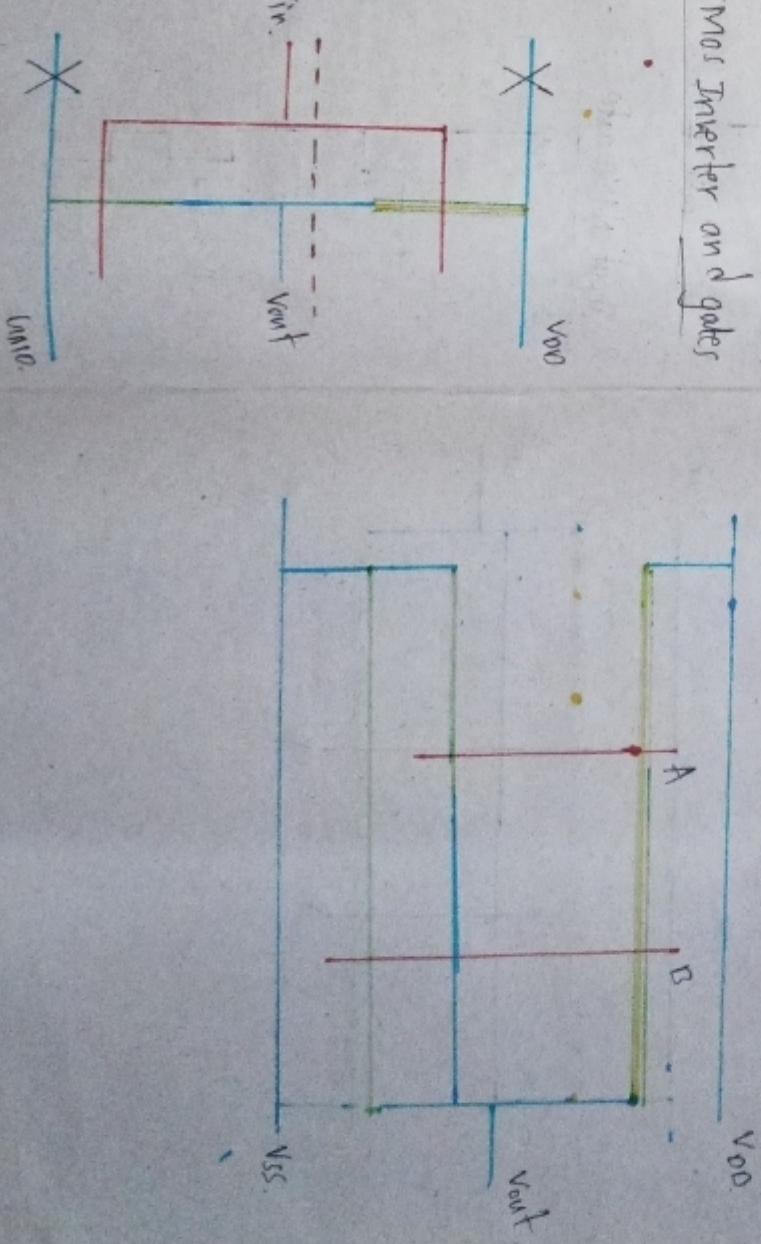
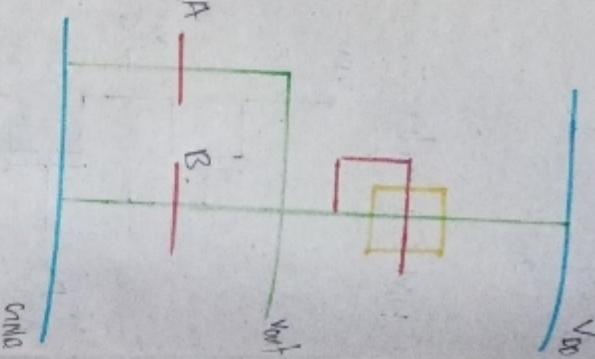
V_{DD}

V_{SS}



* Layout diagram for CMOS Inverter and gates

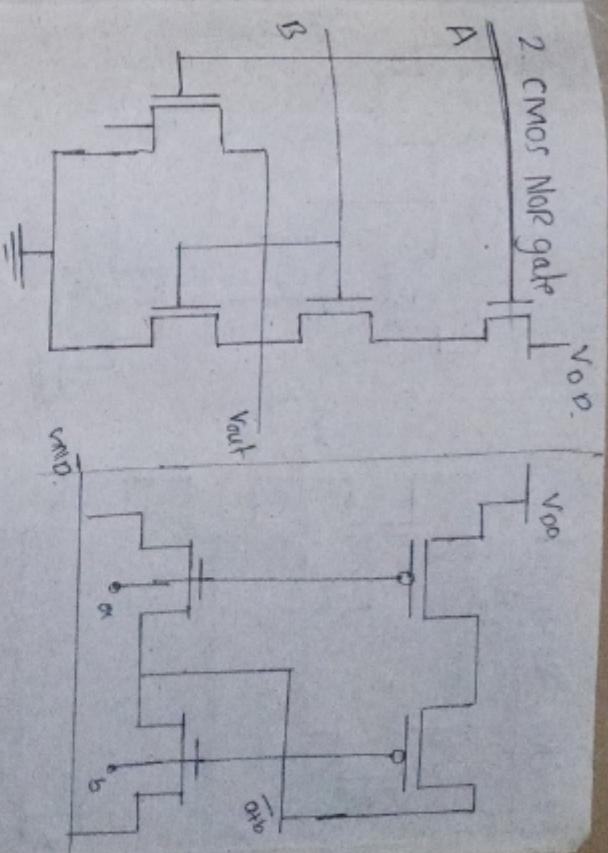
(i) CMOS Inverter



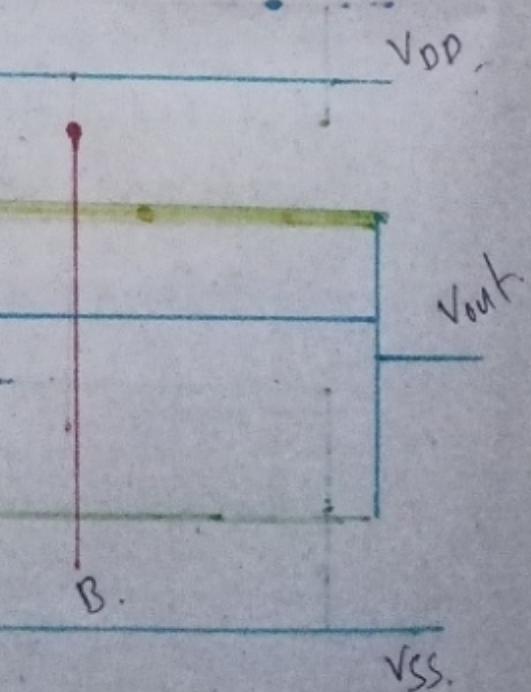
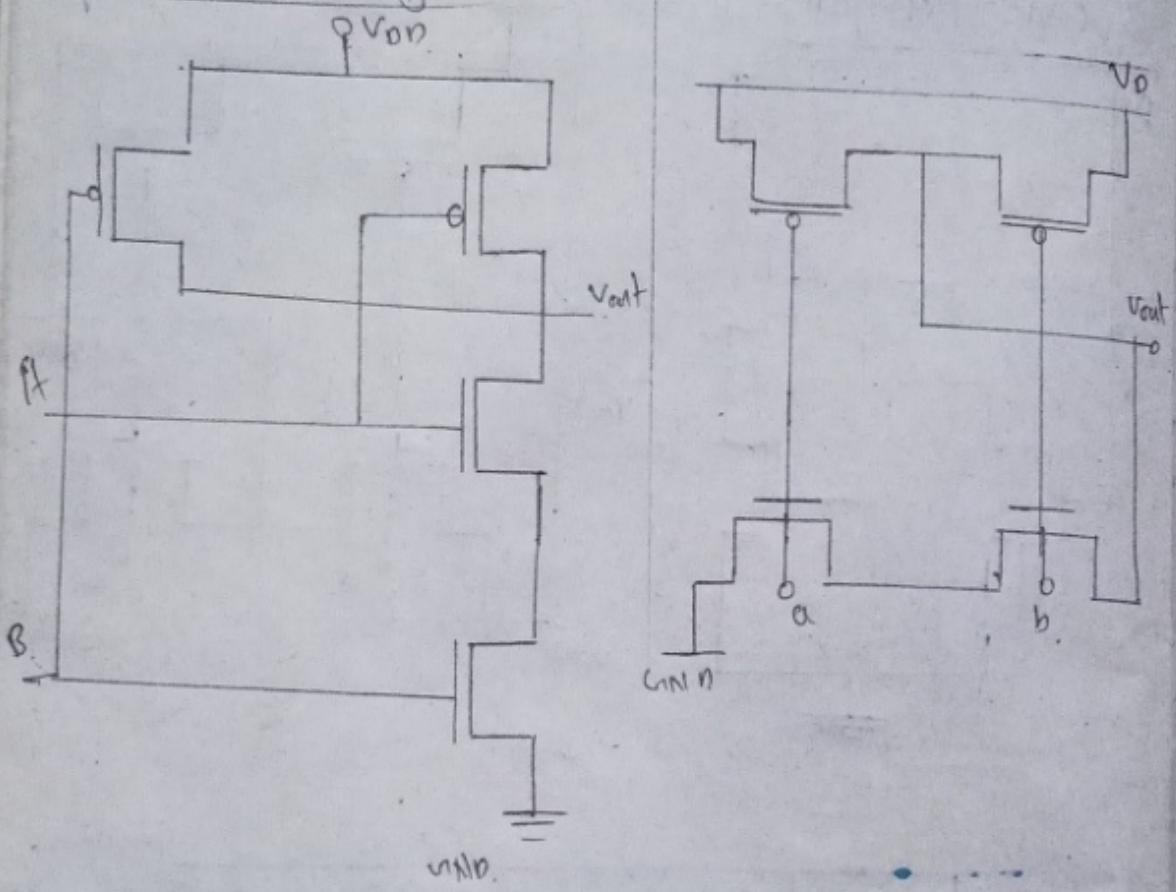
2. CMOS Nor gate

V_{DD}

V_{SS}



3. CMOS NAND gate



Unit - III

Gate level Design

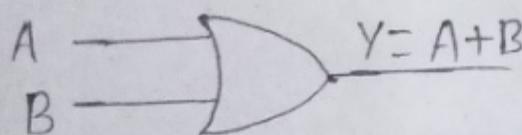
Logic gates

logic gates : The logic gates are devices that acts as a building blocks for digital circuits. is called logic gates.

-> Types of Logic gates

①. OR gate

-> symbol



-> The Boolean expression $y = A + B$,

-> Truth table for two inputs

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

2. AND gate

→ Symbol



→ The Boolean expression $Y = A \cdot B$.

→ Truth table for two inputs

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

3. NOT gate

→ Symbol



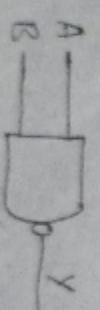
→ The Boolean expression $Y = \bar{A}$.

→ Truth table for one input

| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

4. NAND gate

→ Symbol



- It is combination of AND and NOT
- The Boolean expression $Y = \overline{A \cdot B}$
- Truth table for two inputs

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

5. NOR gate

→ Symbol



→ It is combination of OR and NOT

→ The Boolean expression $Y = \overline{A + B}$

→ Truth table for two inputs

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Q. Exclusive-or gate (XOR)

Complex gates

-> Symbol




- > The Boolean expression $y = A \oplus B$
- > Truth Table for two inputs

| A | B | y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

X-NOR gate

-> Symbol

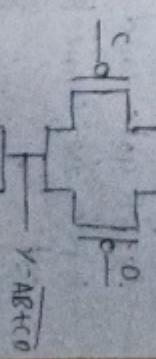
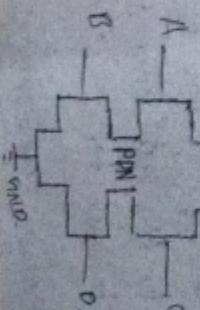
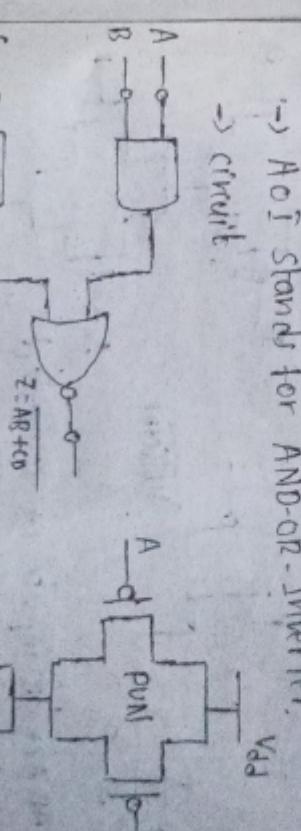
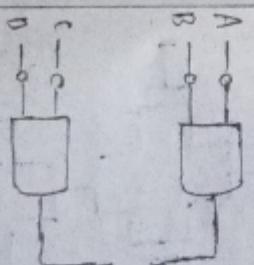



- > The Boolean expression $y = A \overline{B}$
- > Truth table for two inputs

| A | B | y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

AOI gate

- > AOI stands for AND-OR-Inverter.
- > circuit



Complex gate: we can represent boolean logic by creating circuit diagrams that consist of logic gates. It is called complex gate.

\rightarrow A and B inputs are connected to AND gate
and C and D inputs are connected to AND gate.

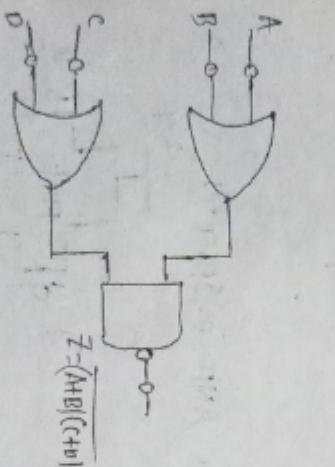
\rightarrow The o/p's of two AND gates connected to OR gate, and op gate o/p connected to Inverter

\rightarrow Boolean expression $Y = \overline{AB + CD}$

②. OA&I gate

\rightarrow OA&I stands for OR-AND-Inverter.

\rightarrow circuit



\rightarrow AB and B inputs are connected to OR gate and C and D inputs are connected to AND gate.

\rightarrow Inputs A and B are connected to OR gate and C and D are connected to AND gate.

\rightarrow The o/p's of two OR gates connected to AND gate, and op gate o/p connected to Inverter.

\rightarrow Boolean expression $Y = \overline{(AB)(CD)}$

Alternate gate circuits

\rightarrow Alternate gate circuits are classified into 4 types, namely

1. pseudo-NMOS logic

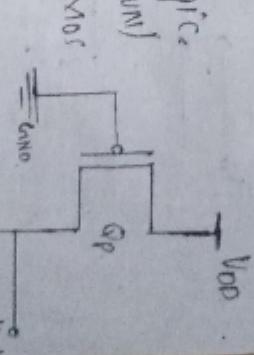
2. dynamic-CMOS

3. clocked CMOS logic

4. domino CMOS

①. pseudo NMOS logic

\rightarrow In pseudo NMOS logic, the pull-up network (PUN) is realized by single p-MOS transistor.



\rightarrow The gate terminal of p-MOS transistor is connected to ground.

\rightarrow It remains in ON state

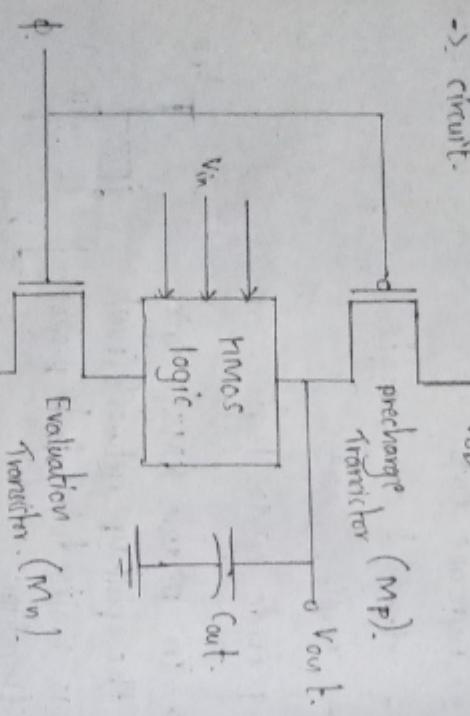
Advantages

- a. low power dissipation.
- b. layout problems
- c. Requires less transistor.

Diamond Inverter

2 Dynamic CMOS logic

- > In dynamic CMOS logic pull-up network can be realized by precharge transistor (M_P).
- > In dynamic CMOS logic pull-down network can be realized by Evaluation Transistor (M_h).
- > circuit.



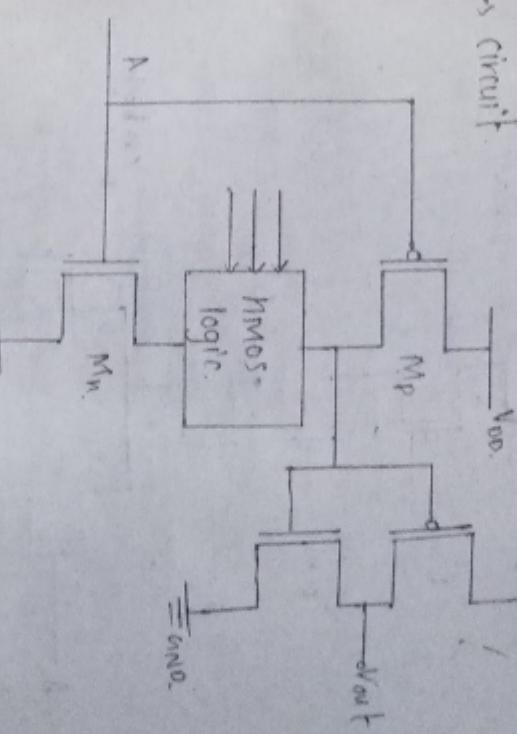
- > It uses capacitor for charge storing.
- > when clock $\phi = 0$, the circuit is in precharge phase.
- > when clock $\phi = 1$, the circuit is in evaluation phase.

Phase.

- > It uses less transistors.
- > Fast switching speed.
- > High performance.

3. CMOS Domino logic

- > CMOS domino logic is slightly advanced version of dynamic CMOS logic.
- > circuit.



- > Static inverter is connected at output.
- > High operating speed.
- > Pull-up Network - Precharge Transistor.
- > Pull-down Network - Evaluation Transistor.
- > Charge distribution is difficult.

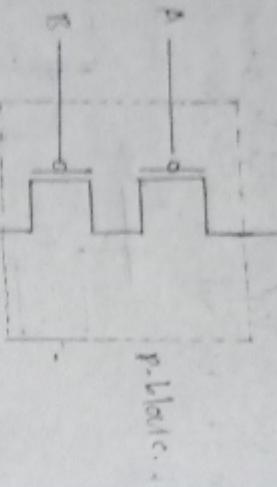
④. Clock CMOS logic

- > The logic is implemented in both pull-up and pull-down blocks.

\rightarrow ~~fan circuit~~

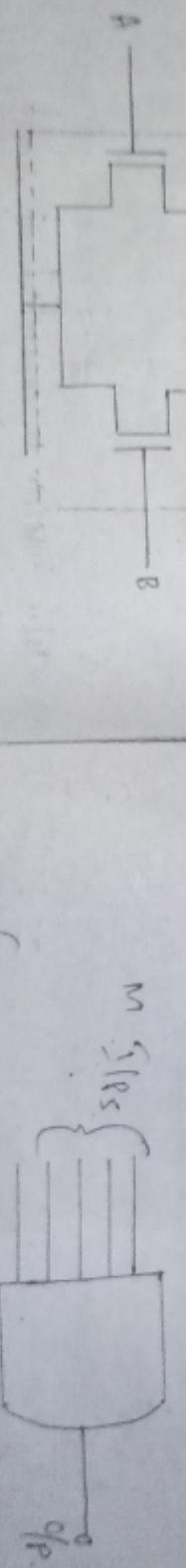
Fan-In-Fan-out

Fan-In



- Def: Fan-in defined as the max no. of input that a logic gate can accept.
- \rightarrow If the no. of inputs exceeds, the output will be incorrect.
 - \rightarrow It is specified by manufacturer.

\rightarrow Block diagram.



\rightarrow No. of inputs based on fan-in

Fan-out

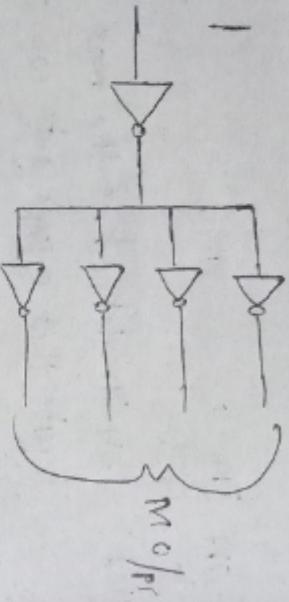
Def: Fan-out defined as the max no. of

input that can be connected to the o/p of gate, without exceeding.

\rightarrow It is specified by manufacturer.

- \rightarrow It consist of two blocks.
 - a. p-block
 - b. N-block.
- \rightarrow IN p-block transistors connected in series
 - \rightarrow IN N-block parallel.

→ Block diagram



$$\rightarrow \text{fan-out} (H) = \frac{I_{CH}}{I_{Th}}$$

$$\rightarrow \text{fan-out} (L) = \frac{I_{CL}}{I_{Th}}$$

Wiring capacitances

Capacitance: It is defined as, the ability of two conductors, separated by an insulating material, to store charge, is called capacitance.

→ wiring capacitance is classified into three types they are

1. Fringing field capacitance
2. Interlayer capacitance
3. Peripheral capacitance

①. Fringing field capacitance

→ Def: The capacitance which exists at the edge of only particular layer is called fringing field capacitance.

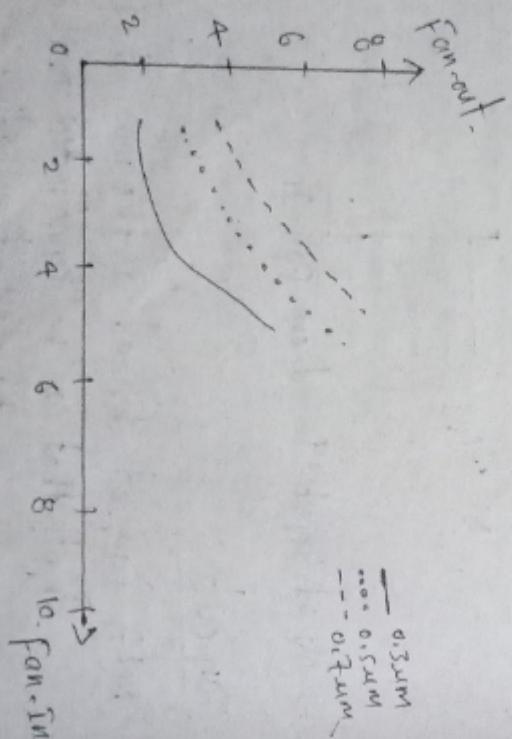
→ It is called as Edge capacitance.

→ Taking one mos layer

finding fringing field capacitance.

$$C_W = \frac{\epsilon A}{D}$$

$$\rightarrow C_W = \text{Const.}$$



-> The expression of FFC =

$$C_{FF} = \epsilon_{SiO_2} \epsilon_0 \frac{\pi}{l} \left[\ln \left(1 + \frac{2d}{l} \left(1 + \sqrt{1 + \frac{l}{d}} \right) \right) \right]^2$$

where l = length of width.

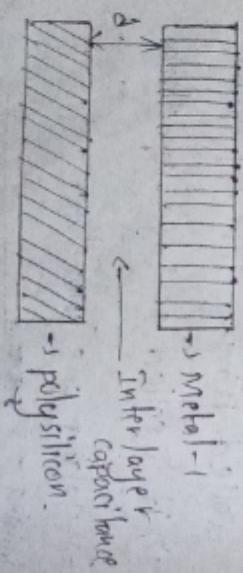
t = thickness

$$C_W = C_{area} + C_{FF}$$

(2) Interlayer capacitance :

Def : The capacitance which exists below two different layers is called interlayer capacitance.

-> Diagram.

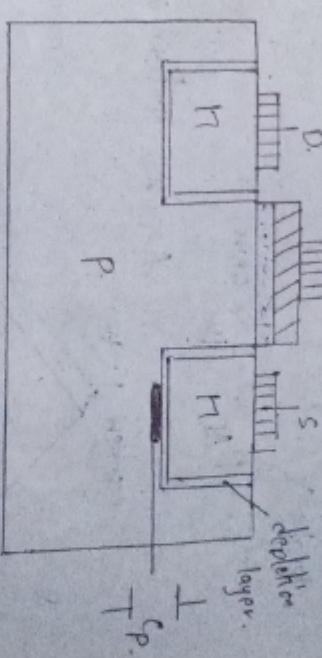


capacitance.

-> It is also called as diffusion capacitance.

(or) side wall capacitance.

-> It is measured in picofarads.



Basic circuit concepts

$$C_{total} = C_{area} + C_{peripheral}$$

Sheet Resistance : sheet resistance is the

resistance of a square piece of thin material with contact made to opposite sides of the square.

Square is called sheet resistance.

- > sheet resistance is used to characterize materials made by semiconductor doping

Ex: silicon, polysilicons

(3). peripheral capacitance

Def : The capacitance which exist below two peripherals is called peripheral semiconductor layers.

\rightarrow It is applicable to two dimensional systems

\rightarrow Typical sheet resistance value for mos layers

Ex:
Consider a uniform slab of conducting material of resistivity ρ , width w , thickness t , and length L

$$R_{AB} = \frac{\rho L}{tw} \text{ ohm}$$

A = Cross section area.

where $L = w$



(a) For n-mos transistor (or) standard size transistor

$$\begin{array}{c} L=2\lambda \\ w=2\lambda \\ \hline \end{array} \quad R = \rho_s \frac{L}{w} = \rho_s \frac{2\lambda}{2\lambda} \Rightarrow R = R_s$$

$$10^4 \Omega_m = 10^4 \Omega$$

n-transistor channel

p-transistor channel

| Mos layer | $R_s \cdot \Omega / sq$ |
|--------------|-------------------------|
| metal | 0.03 |
| diffusion | 10 to 50 |
| poly silicon | 15 to 100 |

(b) For p-mos transistor

$$\begin{array}{c} L=8\lambda \\ w=2\lambda \\ \hline \end{array} \quad R = R_s \frac{L}{w} = R_s \frac{8\lambda}{2\lambda} = 4R_s$$

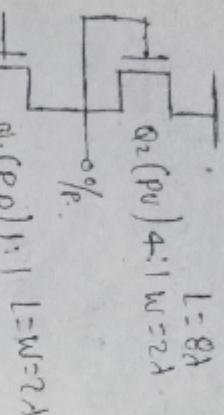
$$= 4(2.5 \times 10^4) = 100 \Omega$$

R_s : sheet resistance

$$\text{Thus: } R_s = \frac{\rho}{t} \text{ ohm per square}$$

C. NMOS Inverter

Driving large capacitive loads



$L = 8\lambda$

$W = 2\lambda$

$\rightarrow \frac{1}{L} = 0\%$

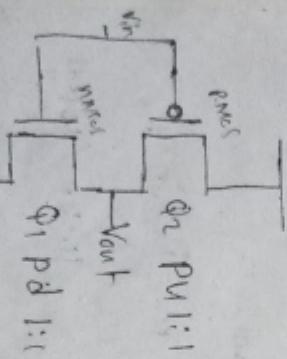
$1 = W = 2\lambda$

$$R_{pd} = R_s \cdot \frac{2\lambda}{2\lambda} = R_s = 10^4 \Omega = 10k\Omega$$

$$R_{pu} = R_s \frac{8\lambda}{2\lambda} = R_s(4) = 10^4(4) = 40k\Omega$$

$$R_{pd} + R_{pu} = 10k\Omega + 40k\Omega = 50k\Omega$$

D. CMOS Inverter



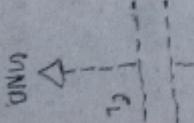
$$R_{pd} = R_s \frac{L}{W} = R_s \frac{8\lambda}{2\lambda} = 10^4 \Omega = 10k\Omega$$

$$R_{pu} = R_s \frac{L}{W} = R_s \frac{8\lambda}{2\lambda} = 2.5 \times 10^4 \Omega = 25k\Omega$$

$$R_{pd} + R_{pu} = 10k\Omega + 25k\Omega = 35k\Omega$$

$$\rightarrow k = cd/cg$$

$$\rightarrow f_{opt} = e^{(k+f_{opt})}/f_{opt}$$



\rightarrow large capacitive load arises when signals must be propagated from the chip to off chip destinations.

\rightarrow long buses.

$\rightarrow C_L \geq 10^4$

\rightarrow Must be driven through low resistances

\rightarrow Three solutions:

a. Cascading inverters as buffers

b. Super buffers

c. BiCMOS drivers

C cascading Inverters as buffers

where

- C_d = drain capacitance

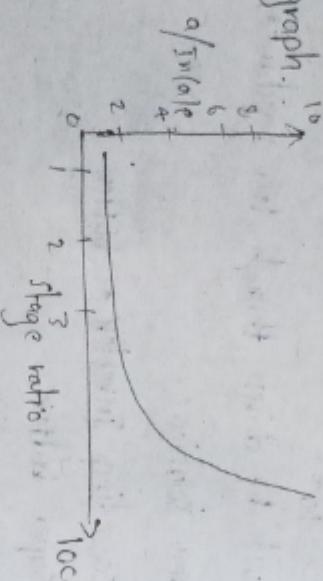
- $C_g = \text{gate}$ "

- $k = \frac{C_d}{C_g}$ varies acc. to technology.

$$k = \frac{C_d}{C_g} = 0.0043 / 0.12 = 0.215$$

$$f_{opt} = 2.93 \text{ (approx } = 3\text{)}$$

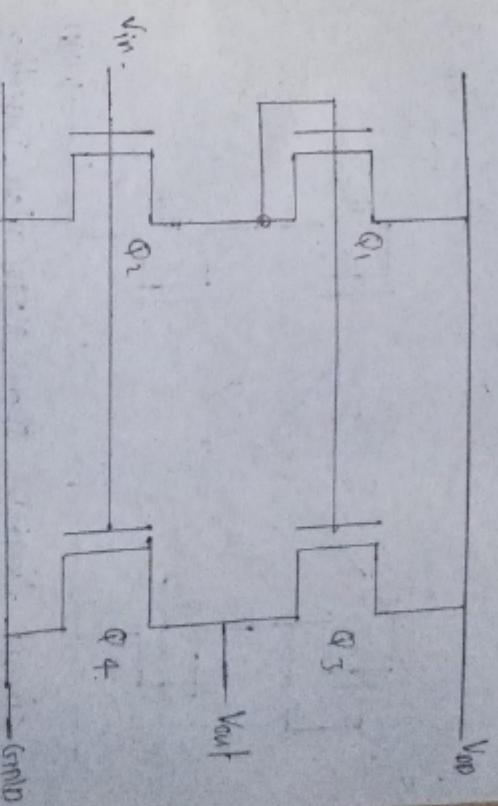
→ graph.



② Super Buffer

- A super buffer has 4 internal transistors whose V_t/V_i ratios and connections give better characteristics of charging/discharging.
- Super buffers are of two types.
 - o Inverting buffer.
 - o Non-inverting buffer.

① Inverting Super buffer



→ circuit diagram shows NMOS inverting super buffer.

- circuit consist of four transistors, V_{dd} and V_{ss}
- case i $V_{in} = 1$.
 - Transistor Q_1 and Q_2 ON.
 - Transistor Q_3 is OFF.
 - Transistor Q_4 is ON.
- case ii $V_{in} = 0$.
 - Transistor Q_1 is OFF.
 - Transistor Q_4 is OFF.
 - Transistor Q_3 is ON due to V_{in} connection to V_{dd} connection.
 - Hence Q_2 is pulled down due to V_{in} hence charge load quickly.

o Non-Inverting Super buffer

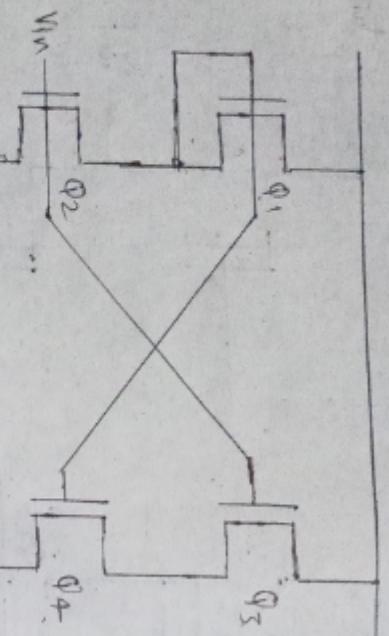
→ Circuit consist of resistance, load capacitance,
 V_{in} , V_{DD} , GND etc.

→ Two main components of BiCMOS.

$$T_{in} = \text{initial time}$$

$$\text{BiMOS} = 2\text{ns}$$

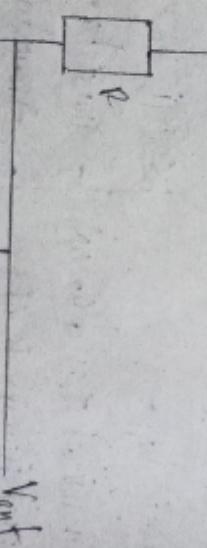
$$\text{CMOS} = 1\text{ns}$$



GND

→ circuit diagram shows NMOS Non-Inverting Super buffer.

(3) BiCMOS Drivers



Vin

Vout

GND

* Inverter delays

→ The inverter delay for inverters ~~del-~~ having 4:1 ratio is $5T$.

→ This is used for measuring delay of two inverters

→ consider an H-Mos inverter delay with respect to ratio - 4:1. Then $\frac{R_{pu}}{R_{pd}} = \frac{4}{1}$

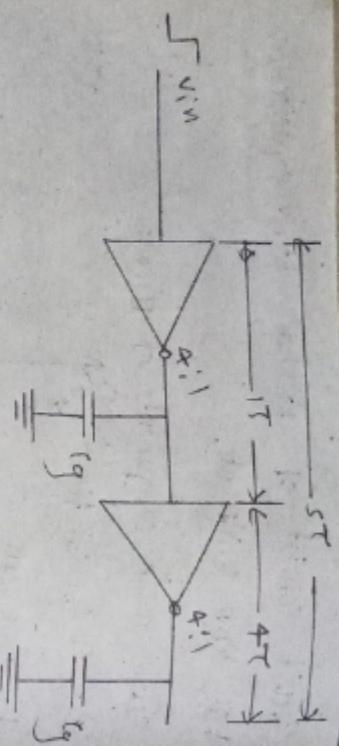
R_{pd}

o H-Mos Inverter pair delay

→ consider a pair of cascade of nmos inverters.

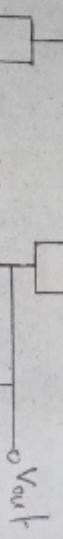
→ BiCMOS is the combination of Bipolar and CMOS Technology.

o CMOS Inverter pair delay

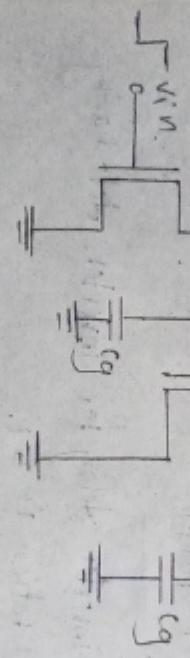
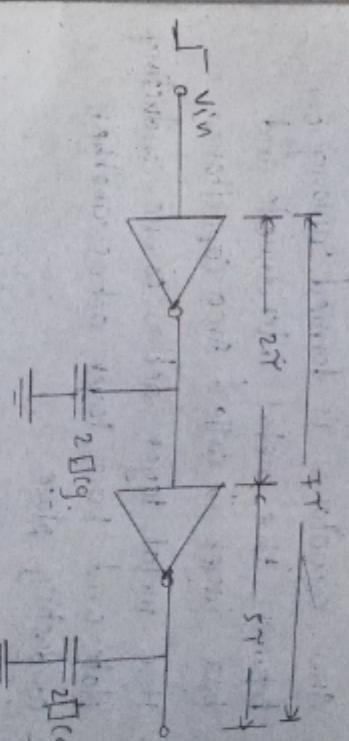


→ Above circuit shows NMOS Inverter pair delay.

→ Equivalent circuit.



→ Above circuit shows CMOS Inverter pair delay.
→ Equivalent circuit.



→ Consider input $V_{in} = V_{DD}$

$$\tau_i = R_{pd} \times Dcg \quad \text{--- (1)} \Rightarrow \tau_i = R_s \times Dcg \quad \text{--- (1)}$$

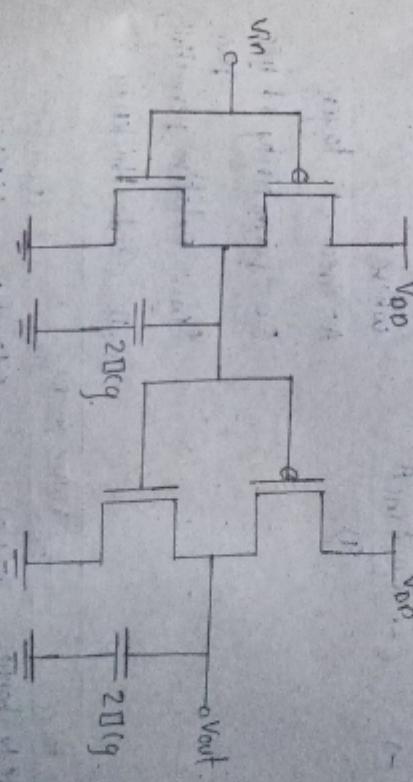
$$\tau_d = R_{pd} \times Dcg \quad \text{--- (2)} \quad \tau_d = 4R_s \times Dcg \quad \text{--- (2)}$$

$$\gamma_d = \gamma_i + \gamma_o$$

$$= R_s \times Dcg + 4R_s \times Dcg$$

$$= 5R_s \times Dcg$$

$$\tau_d = ST$$



→ Consider input $V_{in} = V_{DD}$

$$\tau_i = R_s \times 2Dcg \Rightarrow \tau_i = R_s \times 2Dcg \quad \text{--- (1)}$$

$$\tau_o = R_p \times 2Dcg \Rightarrow \tau_o = R_s \times 2.5 \times R_s \times 2Dcg \quad \text{--- (1)}$$

$$\gamma_d = \gamma_i + \gamma_o$$

$$= R_s \times 2Dcg + 2.5 \times R_s \times 2Dcg$$

$$= 2.5Dcg (R_s + 2.5R_s)$$

$$\tau_d = \frac{\tau_i}{\tau_o}$$

Area capacitances

- Area capacitance is formed among (or) between the metal interconnect and base layer is called Area capacitance.
- Here metal layer acts as one conducting plate and base layer acts another conducting plate.
- Thus, in between these two layers some capacitance is formed i.e. area capacitance
- $C = \frac{\epsilon_0 \epsilon_{\text{ins}} A}{D}$ where,
- A = Area of layer
- ϵ_0 = permittivity of free space
- ϵ_{ins} = relative permittivity
- D = oxide thickness.

| Capacitance | Value in $\text{pF}/\mu\text{m}$ | Value in $\text{pF}/\mu\text{m}$ |
|-----------------------------|----------------------------------|----------------------------------|
| 1. metal to channel | 4(1.0) | 8(1.0) |
| 2. diffusion | 1(0.25) | 1.75(0.21) |
| 3. polystyrene to substrate | 0.4(0.1) | 0.6(0.05) |
| 4. metal-1 to substrate | 0.3(0.075) | 0.33(0.04) |
| 5. metal-2 to substrate | 0.2(0.05) | 0.17(0.02) |

6. metal-2 to metal-1

0.4(0.01) 0.5(0.06) 0.5(0.03)

7. metal-2 to polystyrene

0.3(0.075) 0.3(0.038) 0.3(0.018)

→ Standard units of Area capacitance

$\square \text{Cg} = \text{channel capacitance}$

w = width
l = length

For sum technology

Area/square = $2\mu\text{m} \times 2\mu\text{m}$

$$= 25\mu\text{m}^2$$

Capacitance = $4 \times 10^{-4} \text{ pF}/\mu\text{m}^2$

$$\square \text{Cg} = 25\mu\text{m}^2 \times 4 \times 10^{-4} \text{ pF}/\mu\text{m}^2$$

$$= 10^{-2} \text{ pF} = 0.01 \text{ pF}$$

For 2 μm technology

Area/square = $2\mu\text{m} \times 2\mu\text{m}$

$$= 4\mu\text{m}^2$$

Capacitance = $8 \times 10^{-4} \text{ pF}/\mu\text{m}^2$

$$\square \text{Cg} = 4\mu\text{m}^2 \times 8 \times 10^{-4} \text{ pF}/\mu\text{m}^2$$

$$= 32 \times 10^{-4} \text{ pF}$$

$$= 0.0032 \text{ pF}$$

$$= 0.0023 \text{ pF}$$

For 1.2 μm technology

Area/square = $1.2 \times 1.2 \mu\text{m}$

$$= 1.44\mu\text{m}^2$$

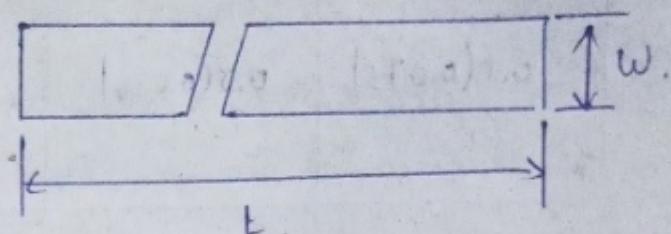
Capacitance = $16 \times 10^{-4} \text{ pF}/\mu\text{m}^2$

$$\square \text{Cg} = 1.44\mu\text{m}^2 \times 16 \times 10^{-4} \text{ pF}/\mu\text{m}^2$$

$$= 0.0023 \text{ pF}$$

* Some Area capacitance calculations

1.



$$L = 20\lambda$$

$$w = 3\lambda$$

→ consider Area in metal - 1

$$\text{Relative Area} = \frac{20\lambda \times 3\lambda}{2\lambda \times 2\lambda} = \frac{60\lambda^2}{8\lambda^2} = 15$$

$$\text{Capacitance to substrate} = 15 \times 0.075 \text{ fF} = 1.125 \text{ fF}$$

2. consider same Area in polysilicon

$$\begin{aligned}\text{Capacitance to substrate} &= 15 \times 0.1 \text{ fF} \\ &= 1.5 \text{ fF}\end{aligned}$$

VLSI Design styles

① Full custom Design

→ Full custom is a design methodology.

→ In full-custom design, the designers do not use predesigned standard cell library.

→ Each and every part designed in this approach.

→ The chips are highly optimized for area, power, speed.

→ Full-custom design is the superior for all other designs.

→ In this design cycle time is higher compared to other designs.

→ used for high performance and volume products.

→ Each circuit element is carefully handcrafted.

→ Huge design effort.

→ High cost.

→ Advantages

- good performance
- small size.
- low power.

→ Disadvantages

- High cost.
- Time taking

② Standard cell design

- standard cell is a design methodology
- The standard cell is also known as poly cell.
- It requires a full - custom mask set.
- A library may contain a few hundred cells

Ex: Inverters, NAND, NOR, AND, OR, latches and flip-flops.

→ The inverter gate can have different sizes

designer can select proper size to

high clk speed.

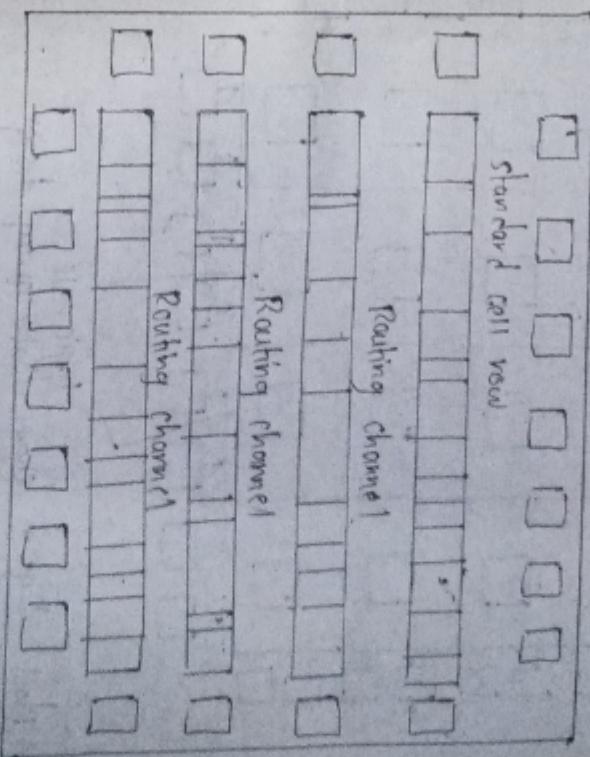
→ Each cell is characterized as follows

◦ circuit simulation model

◦ timing simulation model

◦ Fault simulation model

→ Block diagram.



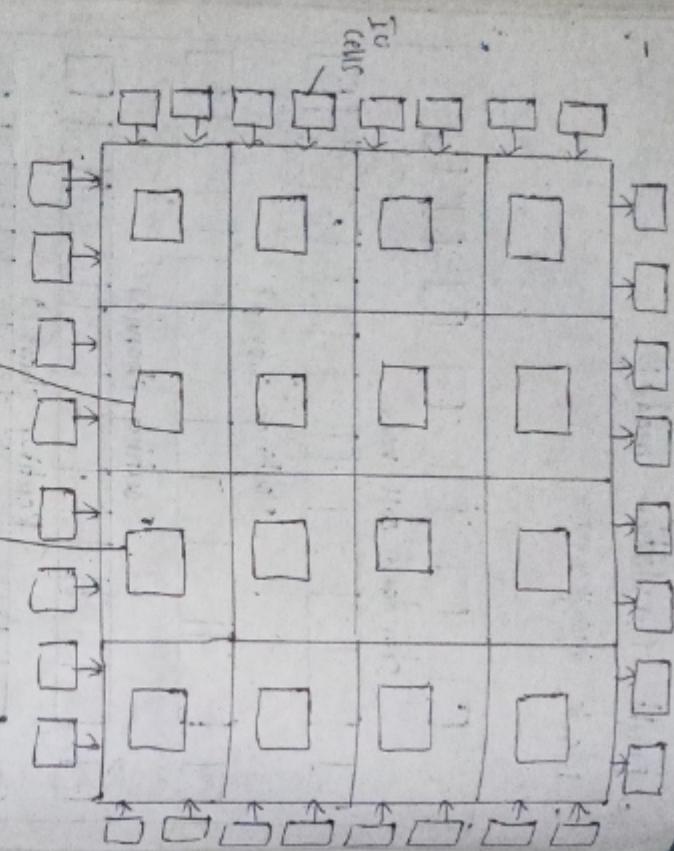
③ Gate array design :

Def: In gate array design, the transistor level masks are fully defined and designer can not change them.

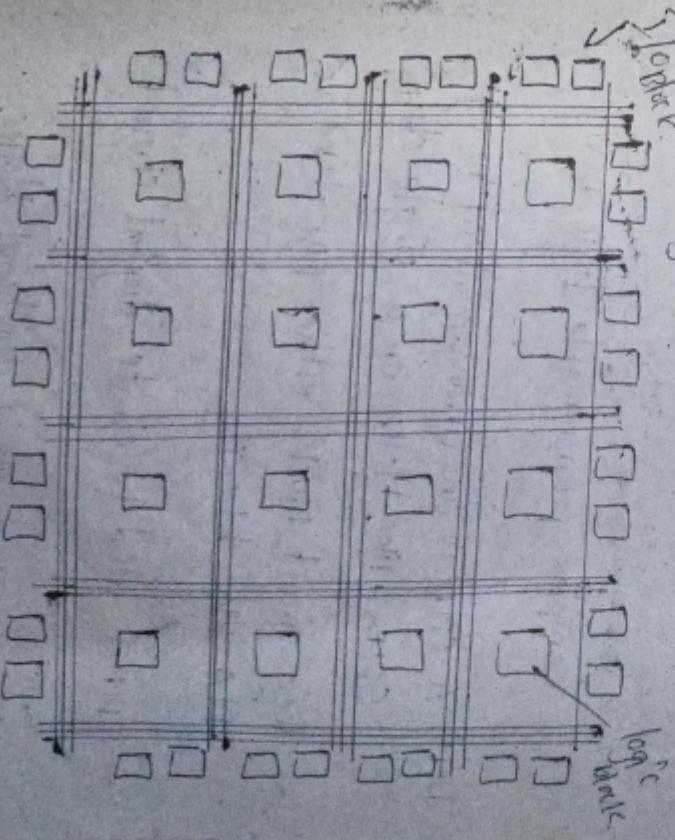
→ gate array is a type of semiconductor device.

→ gate array generally consist of several basic components, such as logic gates, programmable I/O, op-amp.

④. FPGAs



- > FPGAs - stands for field programmable gate array.
- > FPGAs is advanced version of gate array.
- > FPGAs contains more than million logic gates with programmable Interconnection.
- > programmable interconnections are available for users and designers.
- > A typical model FPGAs chip shown in below figure.



-> Block diagram shows gate array design.

Advantages

- o low cost
- o Less time to market.

Disadvantages

- o size is fixed
- o Transistor are fixed
- o Low efficiency

→ Vertical channels are called programmable multiplexers

→ Horizontal channels are called dCBLS

Advantages

→ Requires less time

→ No physical manufacturing

Disadvantages

→ It is costly.

CPLD

→ CPLD stands for -

Complex programmable logic Device

Def: A CPLD is an arrangement of many SPLS-like blocks on a single chip.

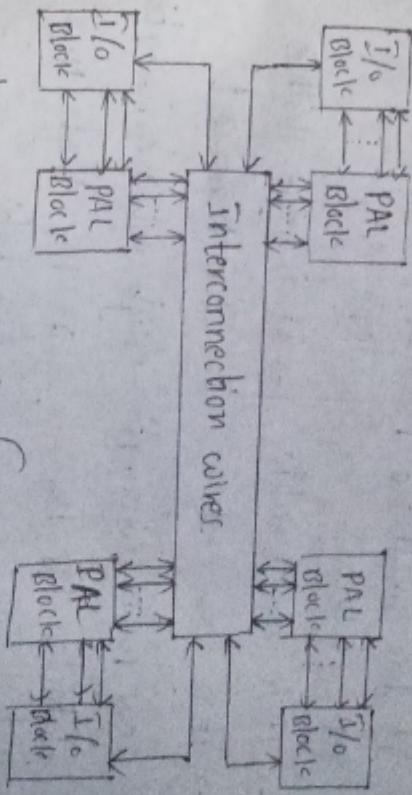
→ These circuit blocks either PAL-like or PLA-like blocks.

→ CPLD is used to create digital circuit

→ CPLD is made up of functional blocks.

→ The I/O of functional blocks is connected through global interconnection matrix [unit].

Block diagram of CPLD



→ Block diagram consists of

• PAL [programmable array logic]

functional block.

o. Interconnection matrix.

o. I/O Block.

Advantages

Disadvantages

→ It is easy to design

→ It is low cost.

→ It is more reliable.

| CPLD | FPGA | Full custom design | Semi custom design |
|--|--|---|---|
| <ul style="list-style-type: none"> -> CPLD stands for Complex programmable logic devices. -> It has small no. of logic cells. -> It is less flexible -> It is low cost -> low power consumption -> It has less flip-flop ratio -> It has less reconfigurability. -> Density - low to medium. | <ul style="list-style-type: none"> -> FPGA - field programmable logic devices. -> It has large no. of logic cells. -> It is more flexible -> It is high cost -> High power consumption -> It has high flip-flop ratio -> It has more reconfigurability. -> Density - medium to high. | <ul style="list-style-type: none"> -> complete design, layout, geometry and placement of transistor is done by designer. -> It is high cost. -> High circuit performance. -> High speed. -> High design time. -> complex circuit layout. -> used for mass production. -> test | <ul style="list-style-type: none"> -> Some design, layout, geometry and placement of transistor is interfaced with given demand -> It is low cost. -> low circuit performance. -> low speed. -> low design time. -> simple circuit layout. -> can't used for mass production. |

Shifters

Def: A shifter is a circuit that can multiply a number by 2, 4 (or) 8 by shifting the number right. Similarly shifter can divide a number by 2, 4 or 8 by shifting number left.

→ Types of shifters.

1. logical shifter.
2. Arithmetic shifter.
3. Barrel shifter.

①. Logical shifter: A logical shifter is a digital circuit that performs logical shift operations on binary numbers.

→ In logical shift operation binary number shift to left or right.

→ Few two operations:
o. shift right operation
e. shift left operation.

→ Ex: shift Right. Ex: shift left

$$\begin{array}{r}
 & 1 & 0 & 1 & 1 & 0 & 1 & 0 \\
 & \swarrow & \searrow & \swarrow & \searrow & \swarrow & \searrow & \swarrow \\
 1 & 1 & 1 & 0 & 0 & 1 & 0 & 1 & 1
 \end{array}
 \quad
 \begin{array}{r}
 1 & 0 & 1 & 1 & 0 \\
 \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\
 0 & 1 & 0 & 1 & 0
 \end{array}$$

②. AirHmetic shifter: An arithmetic shift is a shift operator, sometimes termed as signed shift.

→ In Arithmetic shift operations binary numbers shifts to left or right.

→ Two basic operations

- a. AirHmetic shift left.
- b. AirHmetic shift right.

→ Ex: Arithmetic shift right operation.

| LSB | | | | | | | |
|-----|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

(3) Barrel shifter: A barrel shifter is a

logic circuit for shifting a data word by a specified no. of bits.

→ In barrel shift operation binary numbers

shift toward left and right.

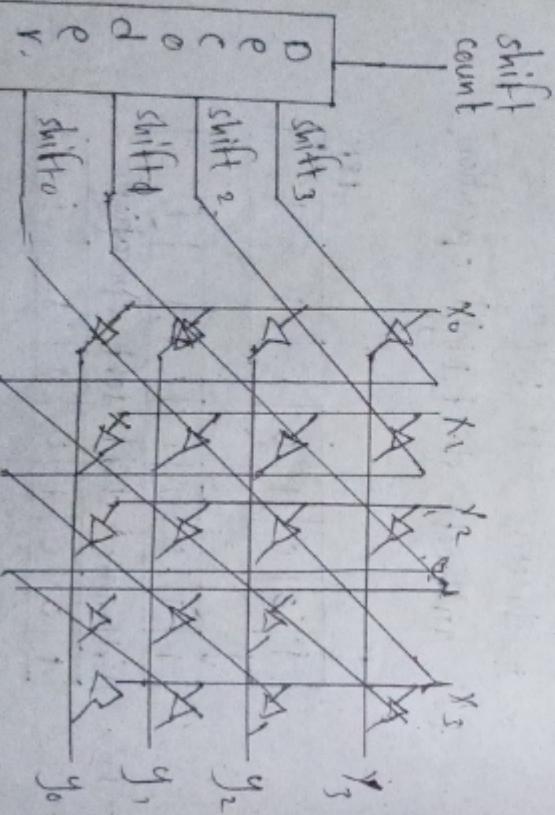
→ Barrel shifter operation is also called as

rotation operation.

→ Two basic operations

- rotate right
- rotate left

→ Block diagram:



parity generators

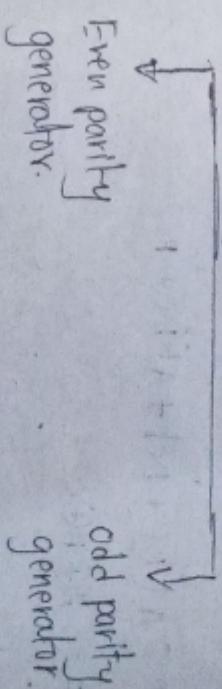
parity generator: The parity generator is a

combination circuit at the transmitter, it takes the original signal message as input and generates parity bit for that message and transmitter in this generator messages along with parity bit is called

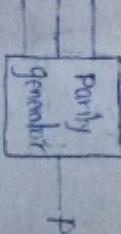
parity generator

→ classification of parity generators

parity generator



Even parity generator



→ Even parity generator maintains the

binary data in even number of '1's.

→ For example, given data is odd number of '1's, this even parity generator maintains

the data as even number of 1's by adding the '1' to odd number of 1's

\rightarrow Truth Table.

| $A \oplus B \oplus C$ | Even parity |
|-----------------------|-------------|
| 000 | 0 |
| 001 | 1 |
| 010 | 0 |
| 011 | 1 |
| 100 | 0 |
| 101 | 1 |
| 110 | 0 |
| 111 | 1 |

$$P = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC.$$

| $A \oplus B \oplus C$ | Odd parity |
|-----------------------|------------|
| 000 | 1 |
| 001 | 0 |
| 010 | 0 |
| 011 | 1 |
| 100 | 1 |
| 101 | 0 |
| 110 | 0 |
| 111 | 1 |

\rightarrow odd parity generator maintains the binary data in odd number of 1's

\rightarrow For example given data is even number of 1's this odd parity generator, main data is odd number of 1's by adding 1 to even no. of 1's

\rightarrow Truth Table

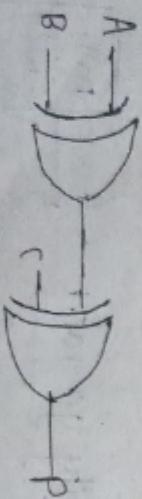
| $A \oplus B \oplus C$ | Odd parity |
|-----------------------|------------|
| 000 | 1 |
| 001 | 0 |
| 010 | 0 |
| 011 | 1 |
| 100 | 1 |
| 101 | 0 |
| 110 | 0 |
| 111 | 1 |

$$P = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$P = \bar{A}(\bar{B}\bar{C} + BC) + A(\bar{B}\bar{C} + B\bar{C})$$

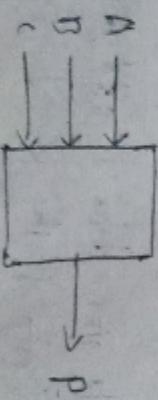
Here odd parity is compliment of even parity

$$P = \overline{A \oplus B \oplus C}$$



2. Odd parity generator

\rightarrow



Adder:

Def: Adder are digital circuits which can perform addition of digital data in microprocessor arithmetic operation.

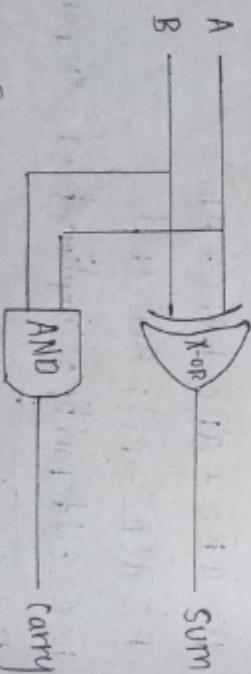
→ Types of adder.

1. Half adder - addition of 2-bit

2. Full adder - addition of 3-bit

①. Half-adder : Half adder is a combinational logic circuit which is designed by connecting one Ex-or gate and one AND gate.

→ Half adder circuit.



→ Half adder ckt has two input A and B

→ logical expression.

$$\text{Sum} = A \text{XOR } B$$

$$\text{carry} = A \text{ AND } B$$

Truth Table

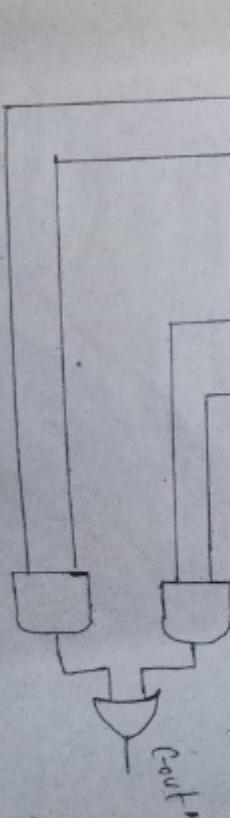
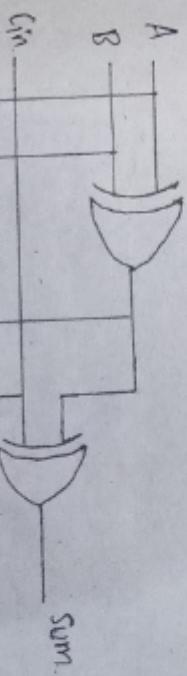
| Input | | Output | |
|-------|---|--------|-------|
| A | B | Sum | Carry |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Combinational logic

②. Full adder : A full adder is a circuit

that which is designed by connecting two X-or gates, two AND gates and one OR gate.

→ Full adder circuit.



→ Full adder ckt has three inputs A, B and Cin

→ Truth Table

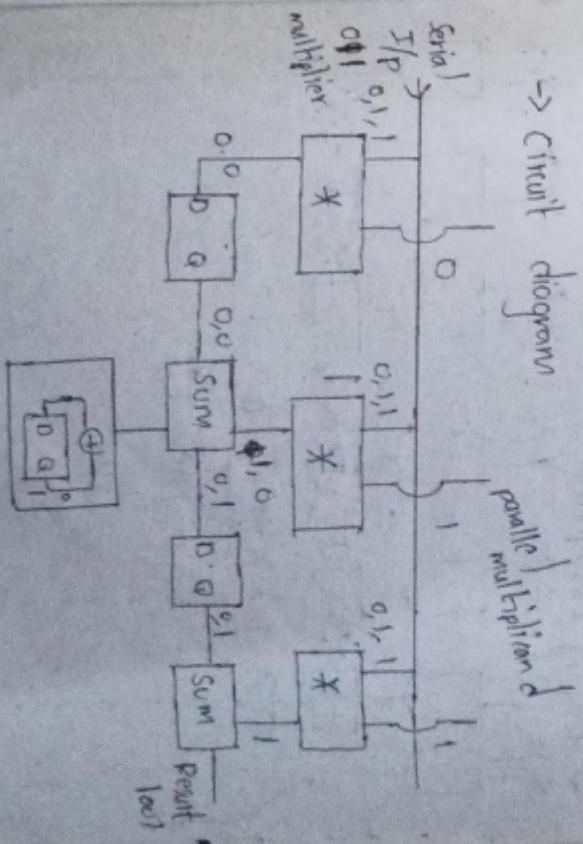
| Input | | Output | |
|-------|---|--------|-----|
| A | B | Cin | Sum |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

multiplier

- multiplier is a circuit based on add and shift algorithm.
- multiplier is a essential part of low power VLSI design.
- used to multiply two binary numbers
- multiplication is of two types they are-
 1. Serial - parallel multiplication
 2. Array multiplication

①. serial-parallel multiplication

→ Circuit diagram

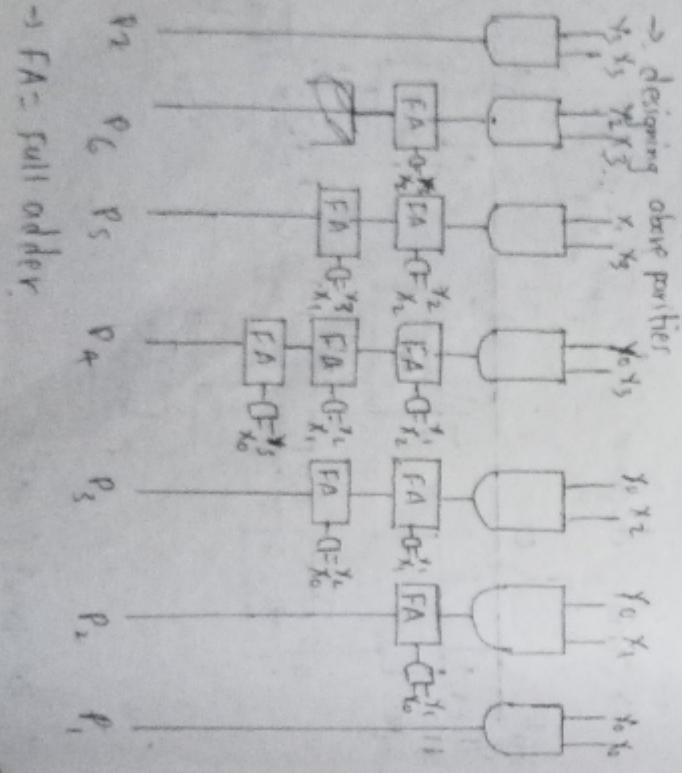


→ Here Result is 1001

→ Explain circuit.

② Array multiplication

| X ₃ | X ₂ | X ₁ | X ₀ multiplier |
|-------------------------------|-------------------------------|-------------------------------|---|
| X ₃ Y ₃ | X ₂ Y ₂ | X ₁ Y ₁ | Y ₀ multiplier |
| Y ₃ Y ₃ | Y ₂ Y ₂ | Y ₁ Y ₁ | Y ₀ Y ₀ |
| Y ₃ Y ₂ | Y ₂ Y ₁ | Y ₁ Y ₀ | |
| Y ₃ Y ₁ | Y ₂ Y ₀ | | |
| P ₇ | P ₆ | P ₅ | P ₄ P ₃ P ₂ P ₁ |



ALU

ALU - Arithmetic logic unit

→ ALU stands for Arithmetic logic unit.

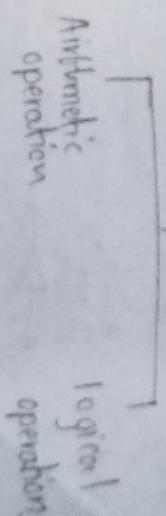
→ It is a main function used in computer

CPU.

→ It is also used in microprocessor

→ ALU is used to do arithmetic and logic operations.

→ ALU performs



Arithmetic operations

* Addition

* Subtraction

* Multiplication

* Division

→ Binary data 4-bit

$$A = 0100, B = 0010$$

→ FA = Full adder

→ Acc to op code, Arithmetic operations

perform in ALU i.e.

op code operand

ADD A,B

SUB A,B

MUL A,B

DIV A,B

Logical operations

→ The logical operations are:

NOT, AND, OR, NAND, NOR, XOR, XNOR

→ logic operations

A AND B $\frac{A}{B} = \square - \text{AND}$

A OR B $\frac{A}{B} = \square - \text{OR}$

NOT A $A - \square - \bar{A}$

NOT B $B - \square - \bar{B}$

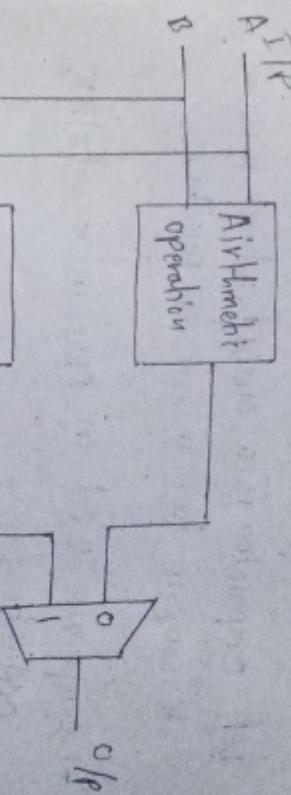
ANAND B $\frac{A}{B} = \square - \text{ANAND}$

A NOR B $\frac{A}{B} = \square - \text{NOR}$

A XOR B $\Rightarrow D - \text{XOR}$

A XNOR B $\Rightarrow D - \text{XNOR}$

→ circuit diagram of ALU



| A | B | Cin | Sum | Carry |
|---|---|-----|-----|-------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

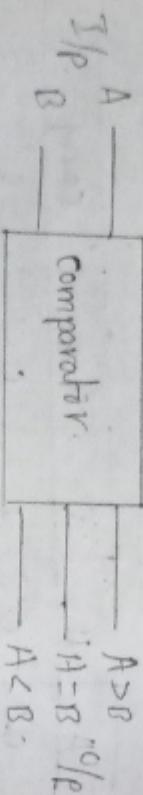
Comparators

Def: Comparator is a circuit, which is used to compare two magnitude numbers.

->

Comparator used in CPUs, microcontroller, applications.

-> Block diagram of 2-bit comparator.



-> Comparator have two inputs, and three output.

-> Output

$$A > B$$

$$A = B$$

$$A < B$$

Output format
various
 $a_1 a_0$

$a_1 a_0$ $a_1 a_0$ $a_1 a_0$ $a_1 a_0$ $a_1 a_0$

00 00 00 10 00

00 01 00 11 00

00 10 00 00 00

01 00 10 00 00

01 01 11 00 00

10 00 00 00 00

10 01 10 00 00

11 00 11 00 00

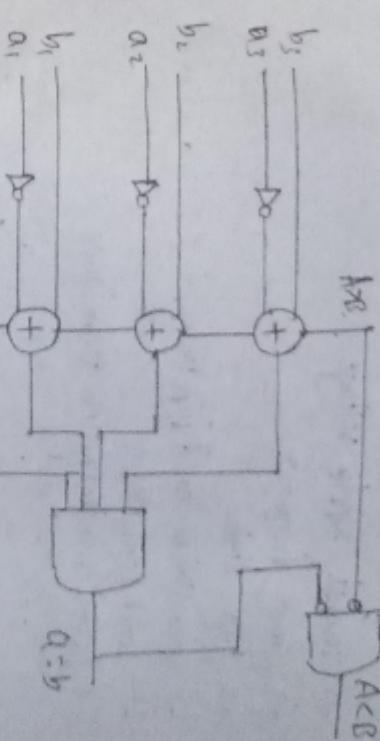
11 01 10 00 00

11 10 11 00 00

11 11 11 00 00

-> output = 1,
-> 4-bit comparator have two AND gates,
4 summers, 4 NOT gates

-> Explain circ.



-> Block diagram of 4-bit comparator.

* parameters influencing low power design

- lowest supply voltage.
- small frequency
- logic style.
- parallelism and pipelining.
- load capacitance.
- power minimization techniques.

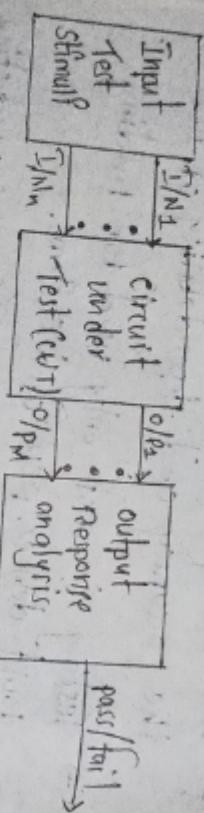
Unit-5

Need for testing:

- VLSI testing methods are essential for the accuracy and dependability of IC's.
- Testing is not only used for finding fault-devices, PCB's and systems.
- Testing is also used for improve production yeild by analyzing the defects (or) faults.
- VLSI testing is important to designers, test engineers, product engineers and end users, etc.
- A small defect can easily result a faulty transistor.
- Due to this whole IC can become fault.
- ⇒ Therefore testing is required to guarantee fault free devices.
- If testing is not done, then we don't know whether the transistor is fault-free.
- we make an IC without testing; after it doesn't work, then our money and time got wasted.
- so testing is required thing in VLSI.

→ Testing during the VLSI life cycle

→ The Block diagram of circuit under test (CUT) is shown in below figure



circuit under Test

→ Explain block diagram

Design for Testability:

→ Design for testability (DFT) is essential in VLSI design because:

- By designing IC with testability in mind, it becomes easier to identify and fault.
- After finding fault in IC, make IC fault free before shipped to the customer.

→ DFT is used to improve quality

→ DFT is used to increase productivity

→ Basic Principles of DFT

- controllability
- observability.

Design for Testability Techniques

→ Design for Testability Techniques are classified into two types they are:

1. Ad hoc DFT Technique
2. Built in self-test (BIST) Technique.

1. Ad hoc DFT Technique

→ Ad hoc testing contains a collection of tricks and techniques, that can be used to increase the observability and controllability of a design.

- It is a temporary technique.
- multiplexing and demultiplexing of test points.
- partitioning of registers and large combined circuit.

→ provides test points for controllability and observability.

- provide easier initialization.

→ Bypass clock clkt.

→ bypass asynchronous logic.

ii Built-in Self Test (BIST).

Basics

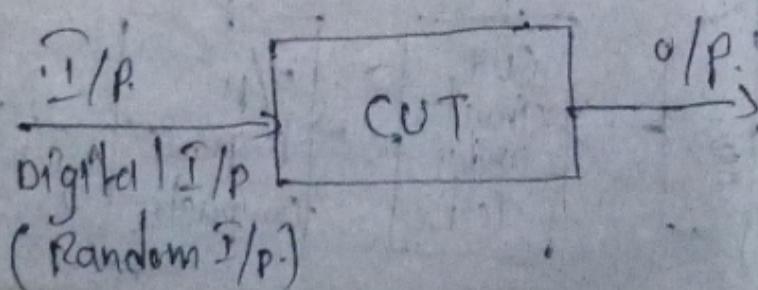
- BIST - Built In self Test.
- BIST is a DFT technique used in VLSI design to test the functionality of integrated circuits.
- It is a technique to design additional hardware and software into IC's to perform self testing.
- Aim of BIST is to reduce cost on testing.

⇒ Types of BIST

- BIST is classified into two types namely
 - i Logic BIST (LBIST)
 - ii Memory BIST [MBIST]

① Logic BIST

- It is designed for testing random logic.



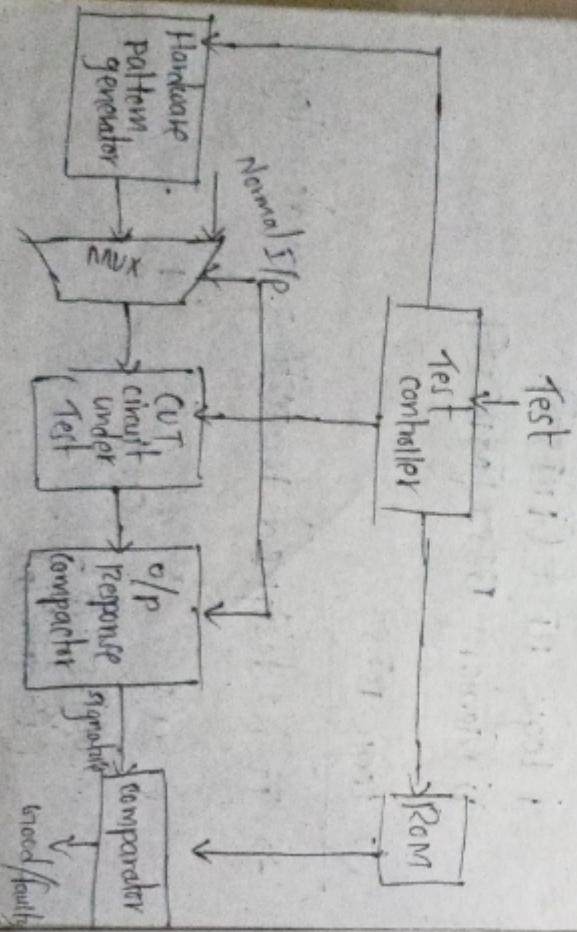
→ Here we use pseudo random pattern generator to generate random I/O patterns.

→ Here input is MISR [multiple I/O signature register] and MISR indicates defects in the device.

② Memory BIST (MBIST):

- It is used for testing memories.
- It has a circuit that apply read-and compare test patterns.
- MBIST will operate in two modes:
 1. Test mode.
 2. Normal mode.

Basic Architecture of BIST:



→ Explain diagram.

→ Explain diagram.

→ Explain diagram.

→ Advantages:

- o Low cost for testing.

- o Test time is short.

- o Better fault coverage.

o speed testing.

→ Disadvantages:

- o In IC additional 1 pin required for testing.
- o In IC " " circuit " "

* Design for Testability

- > design for testability (DFT) makes it possible to:
 - o The detection of all faults in a circuit
 - o It reduces the time and cost
 - o It reduces the execution time of performing
- > There are two very concept for Testability.
 1. controllability.
 2. observability.

1. controllability : controllability of a digital

circuit is defined as the difficulty of setting a particular logic signal. often it is called controllability.

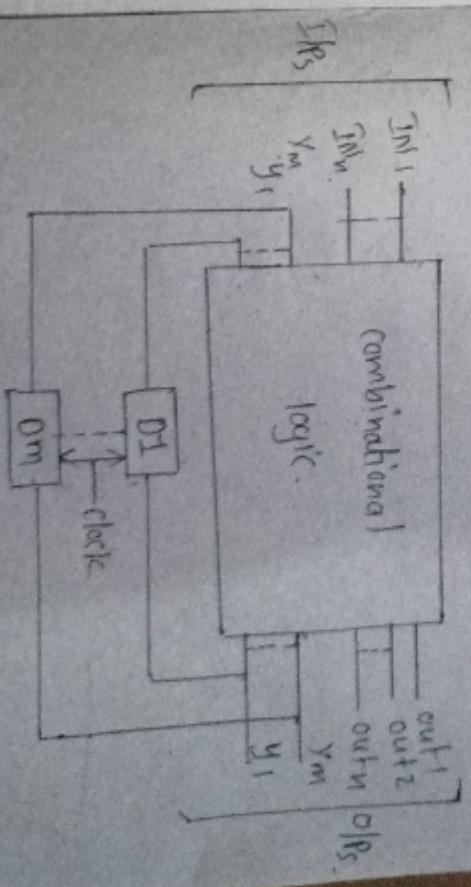
2. observability : observability of a digital circuit is defined as the difficulty of observing the state of logic signal. often it is called observability.

-> The degree of controllability and observability of a circuit can be measured with whether the test vectors are generated deterministically (or) randomly.

* Testing Combinational Logic

- > The solution to the problem of testing combinational logic is to generate a set of patterns which will detect all possible fault conditions.
- > The first approach for testing an N - input circuit is to generate 2^N input signals (controllability) and observe the output (observability).

* Testing sequential logic



- > Above circuit diagram shows testing sequential logic.
- > Sequential circuits are represented as finite machines, may be modified as combinational logic.
- > D_m = delay flip flop (or) register.
- > clock is placed b/w D_1 and D_m .
- > Testing sequential logic consist of ~~n~~ of N no. of inputs and outputs.