

NOVA Microhypervisor Interface Specification

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Preliminary

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Part I

Introduction

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1 System Architecture

The NOVA OS Virtualization Architecture facilitates the coexistence of multiple legacy guest operating systems and a multi-server user environment on a single platform. The core system leverages virtualization technology provided by recent x86 platforms and comprises the hypervisor and a virtual-machine monitor.

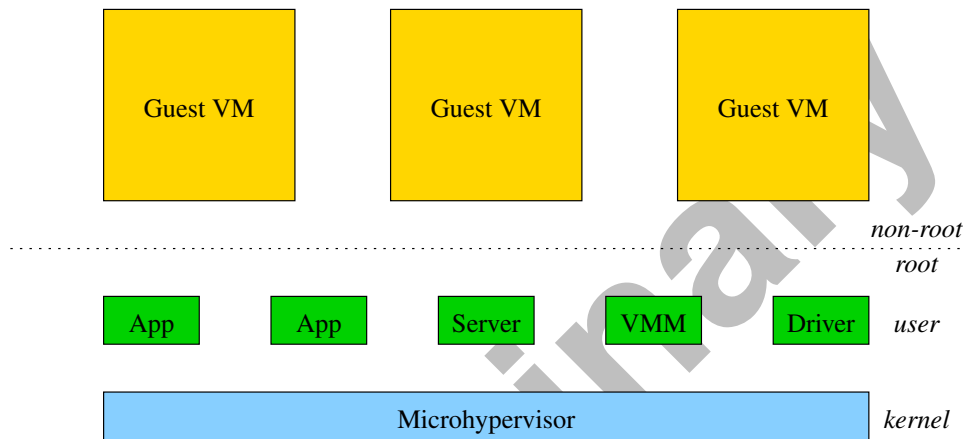


Figure 1.1: System Architecture

Figure 1.1 shows the structure of the system. The hypervisor is the only component running in privileged root/kernel mode. It isolates the user-level servers, including the virtual-machine monitor, from one another by placing them in different address spaces in unprivileged root/user mode. Each legacy guest operating system runs in its own virtual-machine environment in non-root mode and is therefore isolated from the other components. On platforms that do not provide hardware support for virtualization, legacy operating systems can be supported through use of address spaces and paravirtualization.

Besides isolation, the hypervisor also provides mechanisms for partitioning and delegation of platform resources, such as CPU time, physical memory, I/O ports and hardware interrupts and for establishing communication paths between different protection domains.

The virtual-machine monitor handles virtualization faults and implements virtual devices that enable legacy guest operating systems to function in the same manner as they would on bare hardware. Providing this functionality outside the hypervisor in the VMM considerably reduces the size of the trusted computing base for the multi-server user environment and for applications that do not require virtualization support.

The architecture and interfaces of the VMM and the multi-server user environment are not described in this document.

Part II

Basic Abstractions

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2 Kernel Objects

2.1 Protection Domain

1. The protection domain (PD) is a unit of protection and isolation.
2. A protection domain is referenced by a protection domain capability CAP_{PD} (4.1).
3. A protection domain is composed of a set of spaces that hold capabilities to platform resources or kernel objects that can be accessed by execution contexts within the protection domain. These spaces are:
 - Memory Space
 - I/O Space
 - Object Space
4. The memory space of a protection domain holds capabilities to page frames.
5. The I/O space of a protection domain holds capabilities to I/O ports.
6. The object space of a protection domain holds capabilities to the following kernel objects:
 - Protection Domain
 - Execution Context
 - Scheduling Context
 - Portal
 - Semaphore

2.2 Execution Context

1. The execution context (EC) is an abstraction for an activity within a protection domain.
2. An execution context is referenced by an execution context capability CAP_{EC} (4.1).
3. The protection domain in which an execution context was created holds in its object space an EC capability referencing that execution context.
4. An execution context is permanently bound to the protection domain in which it was created.
5. An execution context optionally has a scheduling context bound to it.
6. There exist two flavors of execution context:
 - Kernel thread
 - Virtual CPU
7. An execution context comprises the following information:
 - Reference to protection domain (2.1)

- Scheduling context (2.3)
- UTCB (4.6)
- CPU registers (architecture dependent)
- FPU registers (architecture dependent)
- Reply capability register (4.1)

2.3 Scheduling Context

1. The scheduling context (SC) is a unit of dispatching and prioritization.
2. A scheduling context is referenced by a scheduling context capability CAP_{SC} (4.1).
3. The protection domain in which a scheduling context was created holds in its object space an SC capability referencing that scheduling context.
4. At any point in time, a scheduling context is bound to exactly one execution context.
5. Donation of a scheduling context to another execution context binds the scheduling context to that other execution context.
6. A scheduling context is permanently bound to exactly one CPU.
7. A scheduling context comprises the following information:
 - Reference to execution context (2.2)
 - Time quantum
 - Priority

2.4 Portal

1. A portal (PT) represents a dedicated entry point into the protection domain in which the portal was created.
2. A portal is referenced by a portal capability CAP_{PT} (4.1).
3. The protection domain in which a portal was created holds in its object space a portal capability referencing that portal.
4. A portal is permanently bound to exactly one execution context.
5. A portal comprises the following information:
 - Reference to execution context (2.2)
 - Message transfer descriptor (4.4)
 - Entry instruction pointer
 - Portal identifier

2.5 Semaphore

1. A semaphore (SM) provides a means to synchronize execution and interrupt delivery by selectively blocking and unblocking execution contexts.
2. A semaphore is referenced by a semaphore capability CAP_{SM} (4.1).
3. The protection domain in which a semaphore was created holds in its object space a semaphore capability referencing that semaphore.

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3 Mechanisms

3.1 Scheduling

The microhypervisor implements a round-robin scheduler with multiple priority levels. Whenever an execution context is ready to execute, the runqueue contains the highest-priority scheduling context bound to that execution context. When an execution context blocks, the hypervisor removes the corresponding scheduling context from the runqueue.

When the hypervisor needs to make a scheduling decision, it selects the highest-priority scheduling context from the runqueue and dispatches the execution context bound to that scheduling context.

The parameters of a scheduling context influence the scheduling behavior of the system as follows:

- The priority defines the importance of a scheduling context. A higher-priority scheduling context always has precedence and immediately preempts a lower-priority scheduling context.
- The time quantum defines the number of microseconds that the execution context bound to the scheduling context can utilize the CPU when it is dispatched. A dispatched execution context consumes the time quantum of its scheduling context until the quantum reaches zero; at that point the execution context is descheduled until the time quantum has been replenished.

3.2 Communication

Message passing between protection domains is governed by portals. Each portal represents a dedicated entry point into the protection domain where the portal was created. An execution context in a protection domain can traverse any portal for which the protection domain holds a capability. Portal capabilities can be delegated to establish cross-domain communication channels.

To initiate a message-passing operation from one protection domain to another, the caller execution context presents a capability selector for a capability referencing the destination portal and a message transfer descriptor of the data to be transmitted to the hypervisor. The hypervisor looks up the portal in the object space of the source protection domain, determines the destination protection domain and loads the entry instruction pointer for that domain from the portal.

An arbitrary number of portals can be bound to a callee execution context in a protection domain. The callee provides the stack for handling one incoming request on any of these portals. If the callee is busy handling another request at the time of portal traversal, the caller blocks until the callee becomes available, unless the nonblocking flag has been specified.

Once the callee is available to handle a request and a caller exists for any portal bound to the callee, the hypervisor arranges a rendezvous and transfers the specified message from the caller to the callee.

If the request established a reply capability for the callee, the callee may subsequently respond directly to the caller through a reply operation without risking to block, because the caller is already waiting for the response.

The following subsections describe the currently supported forms of message passing.

Send

During the send operation the caller execution context traverses the destination portal, rendezvouses with a callee execution context and transfers a message to it. Unlike call, the send operation does not establish a reply capability in the callee protection domain so that the callee cannot respond directly. Furthermore, the caller remains ready and does not donate the current scheduling context to the callee.

Nondonating Call

The nondonating call (ncall) operation differs from send in that the hypervisor establishes a reply capability in the callee protection domain. Similar to send, the caller does not donate the current scheduling context to the callee. The caller blocks on the instruction following the hypercall. The callee may later invoke the reply capability to send a response directly to the blocked caller. Upon receiving the response the caller becomes unblocked.

Donating Call

The donating call (dcall) operation differs from ncall in that the caller donates the current scheduling context to the callee. The donation mechanism implements time quantum and priority inheritance from the caller to the callee. The caller blocks on the instruction following the hypercall and the callee starts executing immediately. The hypervisor also establishes a reply capability in the callee protection domain. When the callee later invokes that reply capability to send a response, the hypervisor returns the previously donated scheduling context from the callee back to the caller. Upon receiving the response the caller becomes unblocked.

Reply and Wait

The reply-and-wait operation sends a message back to the caller identified by the reply capability and revokes that capability. If the reply capability was established by a dcall operation, the hypervisor returns the previously donated scheduling context back to the caller. The callee blocks until the next request.

3.3 Exceptions and Intercepts

When an execution context triggers a hardware exception or VM intercept, the hypervisor translates the exception number or intercept reason to a capability selector in the object space of the protection domain. If the capability selector refers to a portal capability CAP_{PT} , the hypervisor arranges an implicit *dcall* hypercall for the execution context through the corresponding portal; otherwise the execution context is shut down.

The entire handling of the exception or intercept is performed using the current scheduling context of the execution context that triggered the event. Furthermore, that execution context remains blocked until the handler has replied with a message to resolve the exception or intercept.

The number of capability selectors reserved for exception and intercept handling is conveyed in the hypervisor information page (6.2). The translation of hardware exception numbers and intercept reasons to capability selectors is described in the processor-specific ABI (IV).

3.4 Interrupts

The hypervisor provides a semaphore per global system interrupt (GSI). An execution context waits for an interrupt by performing a *semctl(down)* hypercall to block on the corresponding semaphore. When the interrupt occurs, the hypervisor issues a *semctl(up)* operation for the semaphore.

Initially the object space of the root protection domain holds a semaphore capability CAP_{SM} for each interrupt. The root protection domain can delegate capabilities for these semaphores to other protection domains.

3.5 Capability Delegation

Delegation of capabilities from one protection domain to another is performed during inter-domain communication. The execution context that sends a message specifies in its message transfer descriptor which range of capabilities from the sender's protection domain it offers to the receiver. The receiver specifies which range of capabilities it is willing to accept and where they should be installed in the receiver's protection domain.

The hypervisor computes the intersection of the sender and receiver ranges and delegates only those capabilities that are covered by both ranges. If the capabilities have access permissions associated with them, the sender may optionally reduce the permissions so that the receiver obtains less privileged capabilities.

If the capability ranges of the sender and receiver differ in size, the capability hotspot, specified by the sender, is used for disambiguation as illustrated in Figure 3.1.

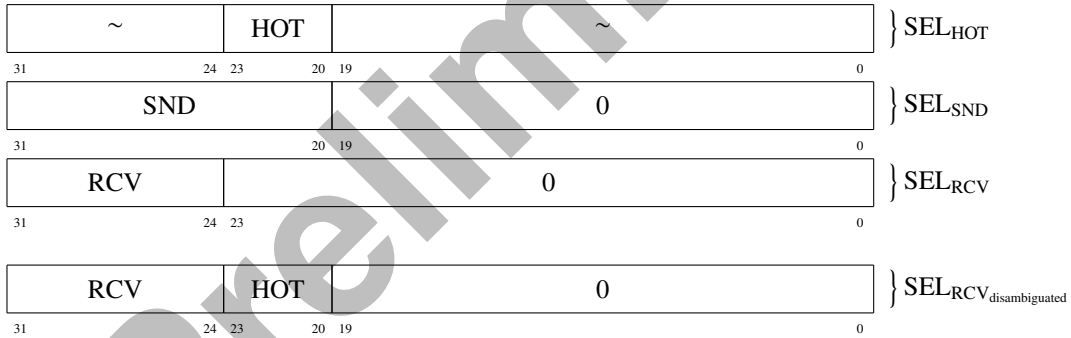


Figure 3.1: Capability Range Disambiguation

In this example, the sender has specified a capability range of order 20, starting at SEL_{SND} , whereas the receiver has specified a capability range of order 24, starting at SEL_{RCV} . There exist 2^4 possible locations in the receiver range, where the sender range could be delegated. Whenever two capability ranges differ in size, the hypervisor truncates the larger range by taking the ambiguous bits from the capability hotspot.

3.6 Capability Revocation

Accepting a capability delegation constitutes an implicit agreement that the capabilities may be revoked again at any time without the receiver's consent. Revoking a range of capabilities from a protection domain additionally revokes that range from all protection domains that directly or indirectly inherited it from that protection domain.

Part III

Application Programming Interface

4 Data Types

4.1 Capability

A capability (CAP) is a reference to a kernel object plus associated auxiliary data, such as access permissions. Capabilities are opaque and immutable to the user – they cannot be inspected, modified or addressed directly; instead user programs access a capability via a capability selector (4.2). The following types of capabilities exist:

Protection Domain Capability

A protection domain capability CAP_{PD} references a protection domain (2.1). It is stored in the object space of a protection domain and can be neither delegated nor revoked.

Execution Context Capability

An execution context capability CAP_{EC} references an execution context (2.2). It is stored in the object space of a protection domain and can be neither delegated nor revoked.

Scheduling Context Capability

A scheduling context capability CAP_{SC} references a scheduling context (2.3). It is stored in the object space of a protection domain and can be neither delegated nor revoked.

Portal Capability

A portal capability CAP_{PT} references a portal (2.4). It is stored in the object space of a protection domain and can be delegated and revoked as described in Section 3.5.

Semaphore Capability

A semaphore capability CAP_{SM} references a semaphore (2.5). It is stored in the object space of a protection domain and can be delegated and revoked as described in Section 3.5.

Reply Capability

A reply capability CAP_{RP} references a caller execution context and the scheduling context donated by that caller, if any. It is stored in the reply register of an execution context during inter-domain communication and automatically destroyed when invoked.

Memory Capability

A memory capability CAP_{MEM} references a 4KB page frame and defines read, write and execute permissions for that page frame. It is stored in the memory space of a protection domain and can be delegated and revoked as described in Section 3.5.

I/O Capability

An I/O capability $CAP_{I/O}$ references an I/O port. It is stored in the I/O space of a protection domain and can be delegated and revoked as described in Section 3.5.

Null Capability

A null capability CAP_0 does not reference any kernel object.

4.2 Capability Selector

A capability selector (SEL) is a user-visible abstract key for accessing a capability. The capability selector serves as integer index for the memory space, I/O space or object space of a protection domain. All capability selectors that do not refer to capabilities of another type refer to a null capability. For example, in Figure 4.1 capability selector 2 refers to a capability for an execution context.

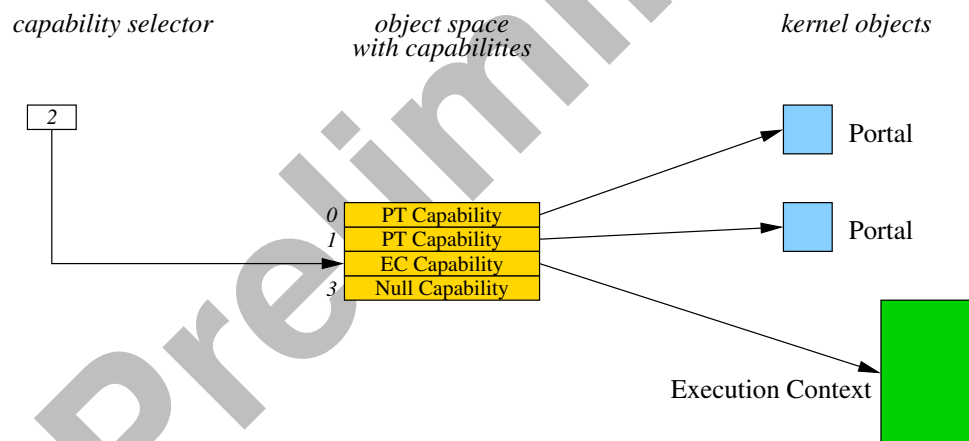


Figure 4.1: Capability Selector

4.3 Capability Range Descriptor

A capability range descriptor (CRD) covers all capabilities of a particular type in the selector range $\text{Base} \dots \text{Base} + 2^{\text{Order}} - 1$. It must be naturally aligned such that $\text{Base} \equiv 0 \pmod{2^{\text{Order}}}$. A capability range descriptor with all bits cleared prohibits delegation of capabilities.

Memory Capability Range Descriptor

A memory capability range descriptor CRD_{MEM} covers the memory capabilities located within the specified range of the memory space. Each memory capability covers 2^{12} bytes of memory. The permissions bits are defined as follows:

- r** read permissions are revoked (0) or remain unchanged (1)
- w** write permissions are revoked (0) or remain unchanged (1)
- x** execute permissions are revoked (0) or remain unchanged (1)

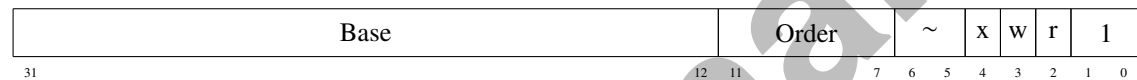


Figure 4.2: Capability Range Descriptor: Memory

I/O Capability Range Descriptor

An I/O capability range descriptor $\text{CRD}_{\text{I/O}}$ covers the I/O capabilities located within the specified range of the I/O space.

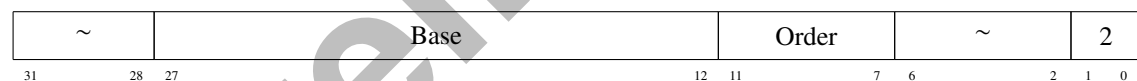


Figure 4.3: Capability Range Descriptor: I/O

Object Capability Range Descriptor

An object capability range descriptor CRD_{OBJ} covers all delegatable capabilities located within the specified range of the object space.

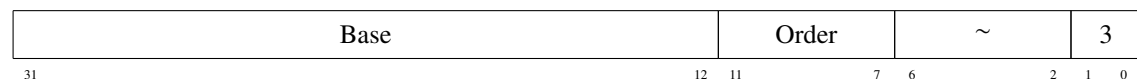


Figure 4.4: Capability Range Descriptor: Kernel Objects

4.4 Message Transfer Descriptor

The message transfer descriptor (MTD) specifies the contents of a message to be transferred from the sender to the receiver. For inter-domain communication the MTD is provided by the sender execution context. For exceptions and intercepts the MTD is provided by the portal associated with the event.

The hypervisor conveys the contents of a message in the message transfer result field in the UTCB (4.6) of the receiver.

The following subsections describe the layout of the MTD for the different message types in detail.

Inter-Domain Communication

The message transfer descriptor for inter-domain communication comprises the following two fields:

Message Words:

Number of message words transferred from the sender UTCB to the receiver UTCB, starting at w_0 .

Transfer Items:

Number of transfer items immediately following the message words.



Figure 4.5: Message Transfer Descriptor: Inter-Domain Communication

Exceptions, Intercepts

The message transfer descriptor for exceptions and interrupts comprises the following two fields:

Architectural State:

Architecture-specific bitfield. For each bit set to 1, the hypervisor transfers the processor state controlled by that bit to or from the respective fields of the UTCB data area. The layout of the bitfield and the fields in the UTCB data area are described in the processor-specific ABI (IV).

Transfer Items:

Number of transfer items immediately following the architectural state.



Figure 4.6: Message Transfer Descriptor: Exceptions, Intercepts

4.5 Quantum Priority Descriptor

The quantum priority descriptor (QPD) specifies the priority of a scheduling context and its time quantum in microseconds. It has the following format:



Figure 4.7: Quantum Priority Descriptor

4.6 User Thread Control Block

Each execution context that acts as a kernel thread has an associated user thread control block (UTCB), which comprises a header area and a data area as illustrated in Figure 4.8.

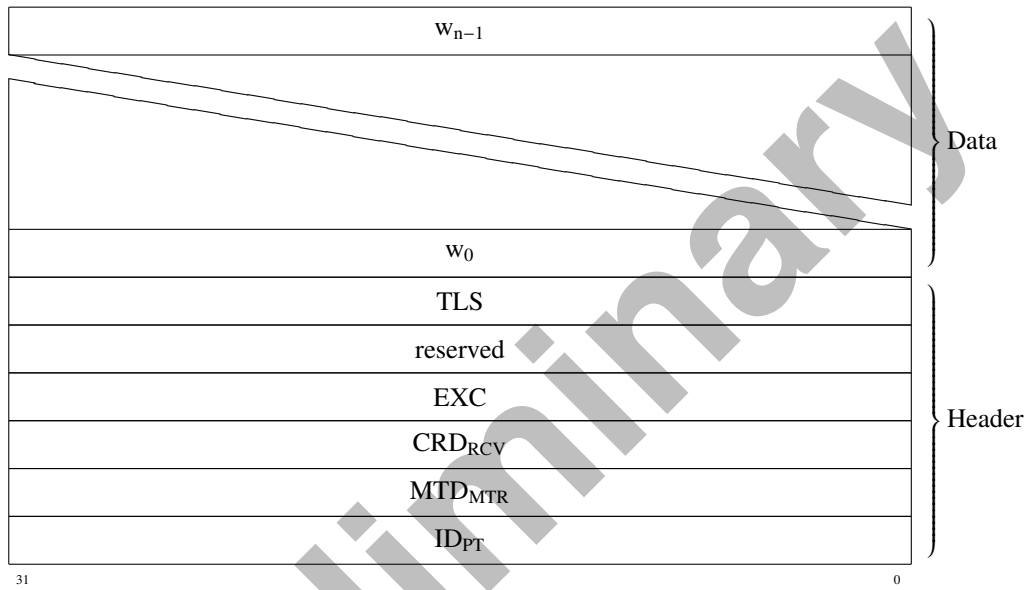


Figure 4.8: User Thread Control Block: General Layout

Header Area

The UTCB header fields are defined as follows:

ID_{PT}

Portal identifier of the last portal traversed to enter the protection domain.

MTD_{MTR}

Message transfer result (4.4) of the last message received into the UTCB. The transfer result denotes which UTCB fields contain valid data.

CRD_{RCV}

Receive capability range descriptor (4.3). Denotes what type of capabilities the execution context is willing to accept, if any.

EXC

Exception capability selector base.

TLS

This field is never written by the hypervisor and can be used to store thread-local data.

Data Area

The size of the data area is defined by the size of the UTCB minus the size of the header area. An execution context uses its UTCB data area to send or receive message words. The data area is also used to provide transfer items for capability delegation. The message transfer descriptor (4.4) defines the number of message words and transfer items.

Message Word

The hypervisor transfers message words from the beginning of the UTCB data area. For example, a transfer of x message words copies words $w_0 \dots w_{x-1}$ from the sender to words $w_0 \dots w_{x-1}$ in the UTCB data area of the receiver. The hypervisor does not interpret the contents of the message words.

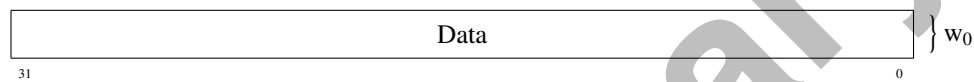


Figure 4.9: User Thread Control Block: Message Word

Transfer Item

The transfer items immediately follow the message words in the UTCB data area. Each transfer item occupies two words as illustrated in Figure 4.10. For example, when y transfer items have been specified in the MTD, the hypervisor interprets words $w_x \dots w_{x+2y-1}$ of the sender's UTCB data area.

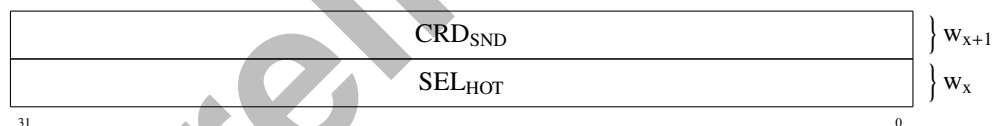


Figure 4.10: User Thread Control Block: Transfer Item

For each transfer item, the hypervisor compares the sender's capability range descriptor CRD_{SND} with the capability range descriptor CRD_{RCV} in the receiver's UTCB header area. If the types match, the hypervisor computes the range of capabilities to delegate from the sender to the receiver, using the hotspot SEL_{HOT} for range disambiguation, as described in Section 3.5.

5 Hypercalls

5.1 Definitions

Hypercall Numbers

Each hypercall is identified by a unique number. Figure 5.1 lists the currently defined hypercalls.

Number	Hypercall	Section
0	CALL	5.2.1
1	REPLY	5.2.2
2	CREATE_PD	5.3.1
3	CREATE_EC	5.3.2
4	CREATE_SC	5.3.3
5	CREATE_PT	5.3.4
6	CREATE_SM	5.3.5
7	REVOKE	5.3.6
8	RECALL	5.4.1
9	SEMCTL	5.4.2

Figure 5.1: Hypercall Numbers

Status Codes

Figure 5.2 shows the status codes returned to indicate success or failure of a hypercall.

Number	Status Code
0	SUCCESS
1	TIMEOUT
2	BAD_SYS
3	BAD_CAP
4	BAD_MEM
5	BAD_FTR

Figure 5.2: Status Codes

5.2 Inter-Domain Communication

5.2.1 Call

Synopsis:

status = call (SEL_{PT}, MTD)

Parameters:

SEL_{PT} Capability Selector: Target Portal

MTD Message Transfer Descriptor

Flags:

0	DR	DD	DB
7	3	2	1 0

DB Disable Blocking (0=blocking, 1=nonblocking)

DD Disable Donation (0=dcall, 1=ncall)

DR Disable Replycap (0=dcall/ncall, 1=send)

Description:

1. If the execution context (2.2), to which the destination portal referenced by SEL_{PT} is bound, is busy, the hypervisor considers the 'disable blocking' flag. If the flag is set, the hypercall returns with a timeout. Otherwise the caller blocks until the callee execution context becomes available.
2. The hypervisor transfers a message, whose contents is determined by the message transfer descriptor, from the caller to the callee.
3. If the 'disable replycap' flag is clear, the hypervisor establishes a reply capability (4.1) in the reply register of the callee. The caller blocks until the callee invokes the reply capability. If the 'disable donation' flag is clear, the current scheduling context, previously bound to the caller, is donated and thereby bound to the callee.
4. The callee becomes ready.
5. The scheduler determines the current scheduling context and current execution context.

Status:

SUCCESS Hypercall completed successfully.

TIMEOUT A rendezvous could not be arranged immediately.

BAD_CAP SEL_{PT} did not refer to a PT capability.

5.2.2 Reply

Synopsis:

status = reply (MTD)

Parameters:

MTD Message Transfer Descriptor

Description:

1. If the reply register contains a reply capability, the hypervisor transfers a message, whose contents is determined by the message transfer descriptor, to the caller execution context referenced by the reply capability.
2. If the caller had donated its scheduling context to the callee, the hypervisor binds that scheduling context back to the caller, thereby terminating the donation.
3. The hypervisor revokes the reply capability by replacing it with a null capability CAP_0 .
4. The callee blocks until a subsequent request arrives.
5. The caller becomes ready.
6. The scheduler determines the current scheduling context and current execution context.

Status:

SUCCESS Hypercall completed successfully.

5.3 Capability Management

5.3.1 Create Protection Domain

Synopsis:

```
status = create_pd (SELPD, UTCB, QPD, CRDOBJ)
```

Parameters:

SEL_{PD} Capability Selector: Created PD

UTCB Virtual Address: UTCB Pointer

QPD Quantum Priority Descriptor (4.5)

CRD_{OBJ} Object Capability Range Descriptor (4.3)

Flags:

0	VM
7	1 0

VM VM capable (0=only threads, 1=threads and virtual CPUs)

Description:

Creates a new protection domain and a bootstrap execution context in that protection domain. Prior to the hypercall SEL_{PD} must refer to a null capability. The creator PD obtains in place of SEL_{PD} a protection domain capability that references the created PD. The created PD obtains two capability selectors: PRE+0¹ refers to an execution context capability for the bootstrap EC and PRE+1 refers to a scheduling context capability for the bootstrap SC. The hypervisor configures the bootstrap SC with the parameters specified by QPD. Furthermore, the hypervisor delegates the capability range specified by CRD_{PT} from the creator PD to the created PD. When the bootstrap EC starts executing, it generates an architecture-specific exception and vectors through the corresponding portal.

Status:

SUCCESS Hypercall completed successfully.

BAD_CAP SEL_{PD} did not refer to a null capability.

BAD_MEM UTCB address is unaligned or beyond the user address space.

BAD_FTR Virtualization features are not supported.

¹PRE denotes the number of predefined capabilities as described in Section 6.2.

5.3.2 Create Execution Context

Synopsis:

```
status = create_ec (SELEC, UTCB, SP)
```

Parameters:

SEL_{EC} Capability Selector: Created EC

UTCB Virtual Address: UTCB Pointer

SP Virtual Address: Stack Pointer

Description:

Creates a new execution context in the creator protection domain. Prior to the hypercall SEL_{EC} must refer to a null capability. The creator PD obtains in place of SEL_{EC} an execution context capability that references the created EC.

Status:

SUCCESS Hypercall completed successfully.

BAD_CAP SEL_{PD} did not refer to a null capability.

BAD_MEM UTCB address is unaligned, not free or beyond the user address space.

5.3.3 Create Scheduling Context

Synopsis:

```
status = create_sc (SELSC, SELEC, QPD)
```

Parameters:

SEL_{SC} Capability Selector: Created SC

SEL_{EC} Capability Selector: Target EC

QPD Quantum Priority Descriptor (4.5)

Description:

Creates a new scheduling context in the creator protection domain and binds it to the execution context referred to by SEL_{EC}. Prior to the hypercall SEL_{SC} must refer to a null capability. The hypervisor configures the SC with the parameters specified by QPD. The creator PD obtains in place of SEL_{SC} a scheduling context capability that references the created SC.

Status:

SUCCESS Hypercall completed successfully.

BAD_CAP SEL_{SC} did not refer to a null capability or SEL_{EC} did not refer to an EC capability.

5.3.4 Create Portal

Synopsis:

```
status = create_pt (SELPT, SELEC, MTDPT, IP)
```

Parameters:

SEL_{PT} Capability Selector: Created PT

SEL_{EC} Capability Selector: Callee EC

MTD_{PT} Message Transfer Descriptor (4.4)

IP Virtual Address: Instruction Pointer

Description:

Creates a new portal and binds it to the callee execution context referred to by SEL_{EC}. Prior to the hypercall SEL_{PT} must refer to a null capability. The creator PD obtains in place of SEL_{PT} a portal capability that references the created portal.

Status:

SUCCESS Hypercall completed successfully.

BAD_CAP SEL_{PT} did not refer to a null capability or SEL_{EC} did not refer to an EC capability.

5.3.5 Create Semaphore

Synopsis:

```
status = create_sm (SELSM, CNT)
```

Parameters:

SEL_{SM} Capability Selector: Created Semaphore

CNT Unsigned: Initial Counter Value

Description:

Creates a new semaphore. Prior to the hypercall SEL_{SM} must refer to a null capability. The creator PD obtains in place of SEL_{SM} a semaphore capability that references the created semaphore.

Status:

SUCCESS Hypercall completed successfully.

BAD_CAP SEL_{SM} did not refer to a null capability.

5.3.6 Revoke Capability Range

Synopsis:

```
status = revoke (CRD)
```

Parameters:

CRD Capability Range Descriptor (4.3)

Flags:

0	SR
7	1 0

SR Self Revoke (0=only children, 1=including self)

Description:

Revokes the capabilities within the range specified by the capability range descriptor from all protection domains that directly or indirectly obtained these capabilities through delegation from the calling protection domain. If the self revoke bit is set, the capabilities will also be revoked from the calling protection domain itself. Once all capabilities to a kernel object have been revoked and no references to the kernel object exist anymore, the kernel object will be destroyed. This operation never fails but can take a long time to complete if there are many capabilities to revoke.

Status:

SUCCESS Hypercall completed successfully.

5.4 Execution Control

5.4.1 Recall Execution Context

Synopsis:

```
status = recall (SELEC)
```

Parameters:

SEL_{EC} Capability Selector: Execution Context

Description:

Pends a recall event for the specified execution context, which causes it to generate an architecture-specific exception before its next return from the hypervisor.

Status:

SUCCESS Hypercall completed successfully.

BAD_CAP SEL_{EC} did not refer to an execution context capability.

5.4.2 Semaphore Control

Synopsis:

```
status = semctl (SELSM)
```

Parameters:

SEL_{SM} Capability Selector: Semaphore

Flags:

0							OP
7					1		0

OP Operation (0=up, 1=down)

Description:

The *down* operation blocks the calling execution context if the semaphore counter is zero, otherwise it decrements the counter. The *up* operation releases an execution context blocked on the semaphore if one exists, otherwise it increments the counter.

Status:

SUCCESS Hypercall completed successfully.

BAD_CAP SEL_{SM} did not refer to a semaphore capability.

Preliminary

6 Booting

6.1 Root Protection Domain

When the hypervisor has finished booting it creates and starts the root protection domain, which is configured as follows:

Memory Space

Program Segments

The hypervisor loads the program segments of the roottask into the memory space as specified by the ELF program headers of the roottask image.

Hypervisor Information Page

The hypervisor information page is mapped into the memory space at a specific address that is passed to the roottask during startup.

Bootstrap UTCB

The UTCB of the bootstrap EC is mapped into the memory space just below the HIP.

The other regions of the memory space are initially empty.

Memory capability range descriptors that delegate from the root protection domain to the root protection domain do not refer to capabilities in the memory space; instead they refer directly to physical memory.

I/O Space

The I/O space is initially empty.

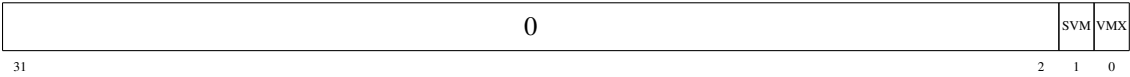
I/O capability range descriptors that delegate from the root protection domain to the root protection domain do not refer to capabilities in the I/O space; instead they refer directly to physical I/O ports.

Object Space

Capability selectors in the range $PRE \dots PRE + GSI - 1$ hold capabilities to interrupt semaphores. All other capability selectors refer to null capabilities.

6.2 Hypervisor Information Page

The hypervisor information page conveys information about the platform and configuration to the root protection domain. The processor register that contains the virtual address of the hypervisor information page during booting is ABI-specific (IV). Figure 6.1 shows the layout of the hypervisor information page. All fields are unsigned values unless stated otherwise.



VMX: Intel Virtual Machine Extensions
 SVM: AMD Secure Virtual Machine

API Version:

API version number.

SEL:

Number of available capability selectors in each object space. Specifying a capability selector beyond the maximum number supported wraps around to the beginning of the object space.

PRE:

Number of predefined capability selectors in each object space. Capability selectors in the range 0 ... PRE – 1 are used for exception and intercept handling (3.3).

GSI:

Number of global system interrupts (3.4).

PAGE Sizes:

If bit n is set, the implementation supports memory pages of size 2ⁿ bytes.

UTCB Sizes:

If bit n is set, the implementation supports user thread control blocks of size 2ⁿ bytes.

TSC Freq:

Time Stamp Counter Frequency in kHz.

BUS Freq:

Interconnect Frequency in kHz.

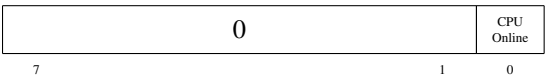
CPU Descriptor

Package, Core, Thread:

CPU multiprocessor topology information.

Flags:

CPU status flags.



MEM Descriptor

Address:

Physical base address of memory region.

Size:

Size of memory region in bytes.

Type:

Type of memory region. Note that the allocated ranges overlap the available ranges.

Type	Description	
-2	Multiboot Module	Allocated ranges
-1	Microhypervisor	
1	Available Memory	Available ranges
2	Reserved Memory	
3	ACPI Reclaim Memory	
4	ACPI NVS Memory	

Auxiliary:

Physical address of command line if type is 'Multiboot Module', reserved otherwise.

Preliminary

Part IV

Application Binary Interface

7 ABI x86-32

7.1 Initial State

Figure 7.1 details the state of the CPU registers when the hypervisor has finished booting and transfers control to the root protection domain.

Register	Description
CS	Selector=~, Base=0, Limit=0xFFFFFFFF, Code Segment, ro
SS,DS,ES,FS,GS	Selector=~, Base=0, Limit=0xFFFFFFFF, Data Segment, rw
EIP	Address of entry point from ELF header
ESP	Address of hypervisor information page
EAX,ECX,EDX,EBX,EBP,ESI,EDI	~
EFLAGS	0x202

Figure 7.1: Initial State

7.2 Predefined Capability Selectors

For the delivery of exception and intercept messages, the hypervisor performs a portal traversal using the capability selector corresponding to the event.

Exceptions

Selector	Exception	Selector	Exception	Selector	Exception	Selector	Exception
0x0	#DE	0x8	#DF ¹	0x10	#MF	0x18	reserved
0x1	#DB	0x9	#RC	0x11	#AC	0x19	reserved
0x2	reserved	0xa	#TS ¹	0x12	#MC ¹	0x1a	reserved
0x3	#BP	0xb	#NP	0x13	#XM	0x1b	reserved
0x4	#OF	0xc	#SS	0x14	reserved	0x1c	reserved
0x5	#BR	0xd	#GP	0x15	reserved	0x1d	reserved
0x6	#UD	0xe	#PF	0x16	reserved	0x1e	reserved
0x7	#NM ¹	0xf	reserved	0x17	reserved	0x1f	#SX

VMX Intercepts

Selector	Intercept	Selector	Intercept	Selector	Intercept
0x20	Exception or NMI ¹	0x35	VMPTRLD	0x4a	reserved
0x21	INTR ¹	0x36	VMPTRST	0x4b	TPR Below Threshold
0x22	Triple Fault ²	0x37	VMREAD	0x4c	APIC Access
0x23	INIT ²	0x38	VMRESUME	0x4d	reserved
0x24	SIPI ²	0x39	VMWRITE	0x4e	GDTR/IDTR Access
0x25	I/O SMI	0x3a	VMXOFF	0x4f	LDTR/TR Access
0x26	Other SMI	0x3b	VMXON	0x50	EPT Violation ²
0x27	Interrupt Window	0x3c	CR Access ¹	0x51	EPT Misconfiguration ¹
0x28	NMI Window	0x3d	DR Access	0x52	INVEPT
0x29	Task Switch ²	0x3e	I/O Access ²	0x53	RDTSCP
0x2a	CPUID ²	0x3f	RDMSR ²	0x54	VMX Preemption Timer
0x2b	GETSEC ²	0x40	WRMSR ²	0x55	INVVPID
0x2c	HLT ²	0x41	Invalid Guest State ²	0x56	WBINVD
0x2d	INVD ²	0x42	MSR Load Failure	0x57	XSETBV
0x2e	INVLPG ¹	0x43	reserved	0x58	reserved
0x2f	RDPMSR	0x44	MWAIT	0x59	reserved
0x30	RDTSC	0x45	MTF	0x5a	reserved
0x31	RSM	0x46	reserved	0x5b	reserved
0x32	VMCALL	0x47	MONITOR	0x5c	reserved
0x33	VMCLEAR	0x48	PAUSE	0x5d	reserved
0x34	VMLAUNCH	0x49	Machine Check	0x5e–0xff	reserved

SVM Intercepts

Selector	Intercept	Selector	Intercept	Selector	Intercept
0x20–0x2f	CR Read	0x8e	RDTSC	0xa1	VMMCALL
0x30–0x3f	CR Write	0x8f	RDPMSR	0xa2	VMLOAD ²
0x40–0x4f	DR Read	0x90	PUSHF	0xa3	VMSAVE ²
0x50–0x5f	DR Write	0x91	POPF	0xa4	STGI
0x60–0x7f	Exception ¹	0x92	CPUID	0xa5	CLGI ²
0x80	INTR ¹	0x93	RSM	0xa6	SKINIT ²
0x81	NMI ¹	0x94	IRET	0xa7	RDTSCP
0x82	SMI	0x95	INT	0xa8	ICEBP
0x83	INIT ²	0x96	INVD ²	0xa9	WBINVD
0x84	Interrupt Window	0x97	PAUSE	0xaa	MONITOR
0x85	CR0 Selective Write	0x98	HLT ²	0xab	MWAIT
0x86	IDTR Read	0x99	INVLPG	0xac	MWAIT (cond.)
0x87	GDTR Read	0x9a	INVLPGA	0xad	reserved
0x88	LDTR Read	0x9b	I/O Access ²	0xae	reserved
0x89	TR Read	0x9c	MSR Access ²	0xaf	reserved
0x8a	IDTR Write	0x9d	Task Switch	0xb0	reserved
0x8b	GDTR Write	0x9e	FERR Freeze	0xb1–0xfd	reserved
0x8c	LDTR Write	0x9f	Triple Fault ²	0xfe	NPT Fault ²
0x8d	TR Write	0xa0	VMRUN	0xff	Invalid Guest State ²

¹These events do not currently cause a portal traversal, because the microhypervisor handles them internally.

²These events are currently force-enabled by the microhypervisor or by hardware.

7.3 Message Transfer Descriptor

Figure 7.2 illustrates the format of the architectural bitfield of the message transfer descriptor for exceptions and intercepts, as described in Section 4.4.

0			TSC	STA	INJ	CTRL	QUAL	SYS	DR	CR	IDTR	GDTR	LDTR	TR	CS SS	FS GS	DS ES	EFL	EIP	ESP	BSD	ACDB
22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 7.2: Message Transfer Descriptor: Architectural Bitfield

The individual bits transfer the following processor state to/from their respective UTCB fields (7.4).

ACDB General-Purpose Registers EAX, ECX, EDX, EBX

BSD General-Purpose Registers EBP, ESI, EDI

ESP Stack Pointer ESP

EIP Instruction Pointer EIP, Instruction Length

EFL Flags Register EFLAGS

DS ES Segment Registers DS and ES (Selector, Base, Limit, Access Rights)

FS GS Segment Registers FS and GS (Selector, Base, Limit, Access Rights)

CS SS Segment Registers CS and SS (Selector, Base, Limit, Access Rights)

TR Task Register (Selector, Base, Limit, Access Rights)

LDTR Local Descriptor Table Register (Selector, Base, Limit, Access Rights)

GDTR Global Descriptor Table Register (Base, Limit)

IDTR Interrupt Descriptor Table Register (Base, Limit)

CR Control Registers CR0, CR2, CR3, CR4

DR Debug Register DR7

SYS SYSENTER MSRs for CS, ESP, EIP

QUAL Exit Qualification

CTRL Execution Controls

INJ Injection Info, Injection Error Code

STA Interruptibility State, Activity State

TSC TSC Offset

7.4 UTCB Data Layout

SYSENTER EIP	SYSENTER ESP	SYSENTER CS	Instruction Length		+0x110
TSC Offset		Secondary Exit Ctrl	Primary Exit Ctrl		+0x100
reserved	Secondary Exit Qual	reserved	Primary Exit Qual		+0xf0
Activity State	Interruptibility State	Injection Error	Injection Info		+0xe0
reserved	IDTR Base	IDTR Limit	reserved		+0xd0
reserved	GDTR Base	GDTR Limit	reserved		+0xc0
reserved	TR Base	TR Limit	TR AR	TR Sel	+0xb0
reserved	LDTR Base	LDTR Limit	LDTR AR	LDTR Sel	+0xa0
reserved	GS Base	GS Limit	GS AR	GS Sel	+0x90
reserved	FS Base	FS Limit	FS AR	FS Sel	+0x80
reserved	DS Base	DS Limit	DS AR	DS Sel	+0x70
reserved	SS Base	SS Limit	SS AR	SS Sel	+0x60
reserved	CS Base	CS Limit	CS AR	CS Sel	+0x50
reserved	ES Base	ES Limit	ES AR	ES Sel	+0x40
DR7	reserved	CR4	CR3		+0x30
CR2	CR0	EIP	EFLAGS		+0x20
EDI	ESI	EBP	ESP		+0x10
EBX	EDX	ECX	EAX		

7.5 Calling Convention

The following pages describes the calling convention for each hypercall. An execution context calls into the hypervisor by loading the hypercall identifier and other parameters into the specified processor registers and then executes the *sysenter* instruction.

The hypercall identifier consists of the hypercall number and hypercall-specific flags, as illustrated in Figure 7.3.

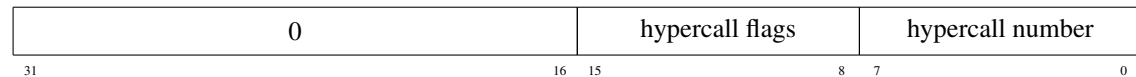


Figure 7.3: Hypercall Identifier

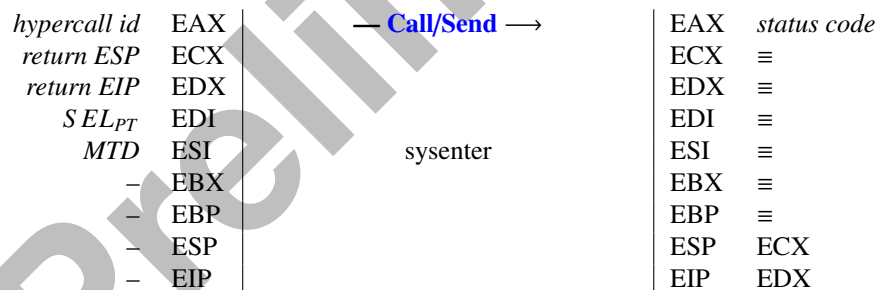
The status code returned from a hypercall has the format shown in Figure 7.4.



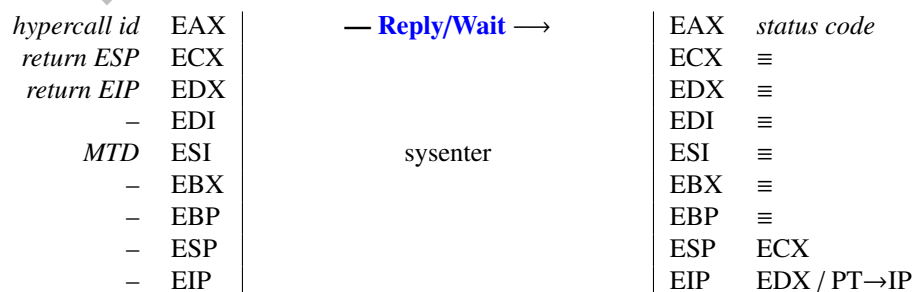
Figure 7.4: Status Code

The assignment of hypercall parameters to general-purpose registers is shown on the left side; the contents of the registers after the hypercall is shown on the right side.

Call/Send



Reply/Wait



Create Protection Domain

<i>hypercall id</i>	EAX	— Create PD →	EAX	<i>status code</i>
<i>return ESP</i>	ECX		ECX	≡
<i>return EIP</i>	EDX		EDX	≡
<i>SEL_{PD}</i>	EDI		EDI	≡
<i>UTCB</i>	ESI	sysenter	ESI	≡
<i>QPD</i>	EBX		EBX	≡
<i>CRD_{PT}</i>	EBP		EBP	≡
–	ESP		ESP	ECX
–	EIP		EIP	EDX

Create Execution Context

<i>hypercall id</i>	EAX	— Create EC →	EAX	<i>status code</i>
<i>return ESP</i>	ECX		ECX	≡
<i>return EIP</i>	EDX		EDX	≡
<i>SEL_{EC}</i>	EDI		EDI	≡
<i>UTCB</i>	ESI	sysenter	ESI	≡
<i>SP</i>	EBX		EBX	≡
–	EBP		EBP	≡
–	ESP		ESP	ECX
–	EIP		EIP	EDX

Create Scheduling Context

<i>hypercall id</i>	EAX	— Create SC →	EAX	<i>status code</i>
<i>return ESP</i>	ECX		ECX	≡
<i>return EIP</i>	EDX		EDX	≡
<i>SEL_{SC}</i>	EDI		EDI	≡
<i>SEL_{EC}</i>	ESI	sysenter	ESI	≡
<i>QPD</i>	EBX		EBX	≡
–	EBP		EBP	≡
–	ESP		ESP	ECX
–	EIP		EIP	EDX

Create Portal

<i>hypercall id</i>	EAX	— Create PT →	EAX	<i>status code</i>
<i>return ESP</i>	ECX		ECX	≡
<i>return EIP</i>	EDX		EDX	≡
<i>SEL_{PT}</i>	EDI		EDI	≡
<i>SEL_{EC}</i>	ESI	sysenter	ESI	≡
<i>MTD_{PT}</i>	EBX		EBX	≡
<i>IP</i>	EBP		EBP	≡
–	ESP		ESP	ECX
–	EIP		EIP	EDX

Create Semaphore

<i>hypercall id</i>	EAX	— Create SM →	EAX	<i>status code</i>
<i>return ESP</i>	ECX		ECX	≡
<i>return EIP</i>	EDX		EDX	≡
<i>SEL_{SM}</i>	EDI		EDI	≡
<i>CNT</i>	ESI	sysenter	ESI	≡
—	EBX		EBX	≡
—	EBP		EBP	≡
—	ESP		ESP	ECX
—	EIP		EIP	EDX

Revoke Capability Range

<i>hypercall id</i>	EAX	— Revoke →	EAX	<i>status code</i>
<i>return ESP</i>	ECX		ECX	≡
<i>return EIP</i>	EDX		EDX	≡
<i>CRD</i>	EDI		EDI	≡
—	ESI	sysenter	ESI	≡
—	EBX		EBX	≡
—	EBP		EBP	≡
—	ESP		ESP	ECX
—	EIP		EIP	EDX

Recall Execution Context

<i>hypercall id</i>	EAX	— Recall →	EAX	<i>status code</i>
<i>return ESP</i>	ECX		ECX	≡
<i>return EIP</i>	EDX		EDX	≡
<i>SEL_{EC}</i>	EDI		EDI	≡
—	ESI	sysenter	ESI	≡
—	EBX		EBX	≡
—	EBP		EBP	≡
—	ESP		ESP	ECX
—	EIP		EIP	EDX

Semaphore Control

<i>hypercall id</i>	EAX	— Semctl →	EAX	<i>status code</i>
<i>return ESP</i>	ECX		ECX	≡
<i>return EIP</i>	EDX		EDX	≡
<i>SEL_{SM}</i>	EDI		EDI	≡
—	ESI	sysenter	ESI	≡
—	EBX		EBX	≡
—	EBP		EBP	≡
—	ESP		ESP	ECX
—	EIP		EIP	EDX

8 ABI x86-64

8.1 Initial State

To be done.

8.2 Predefined Capability Selectors

See Section [7.2](#).

8.3 Message Transfer Descriptor

To be done.

8.4 UTCB Data Layout

SYSENTER RIP		SYSENTER RSP		+0x1a0
SYSENTER CS		Instruction Length		+0x190
TSC Offset		Secondary Exit Ctrl	Primary Exit Ctrl	+0x180
Secondary Exit Qual		Primary Exit Qual		+0x170
Activity State	Interruptibility State	Injection Error	Injection Info	+0x160
IDTR Base		IDTR Limit	reserved	+0x150
GDTR Base		GDTR Limit	reserved	+0x140
TR Base		TR Limit	TR AR TR Sel	+0x130
LDTR Base		LDTR Limit	LDTR AR LDTR Sel	+0x120
GS Base		GS Limit	GS AR GS Sel	+0x110
FS Base		FS Limit	FS AR FS Sel	+0x100
DS Base		DS Limit	DS AR DS Sel	+0xf0
SS Base		SS Limit	SS AR SS Sel	+0xe0
CS Base		CS Limit	CS AR CS Sel	+0xd0
ES Base		ES Limit	ES AR ES Sel	+0xc0
DR7		CR8		+0xb0
CR4		CR3		+0xa0
CR2		CR0		+0x90
RIP		RFLAGS		+0x80
R15		R14		+0x70
R13		R12		+0x60
R11		R10		+0x50
R9		R8		+0x40
RDI		RSI		+0x30
RBP		RSP		+0x20
RBX		RDX		+0x10
RCX		RAX		

8.5 Calling Convention

To be done.

Preliminary

Part V

Experimental Features

Preliminary

9 Experimental Hypercalls

The following functionality is experimental and may be removed or altered in future versions of the specification and/or implementation.

9.1 Capability Management

9.1.1 Lookup Capability ID

Synopsis:

```
status = lookup (SELPT)
```

Parameters:

SEL_{PT} Capability Selector: Portal

Description:

If the caller's protection domain owns the root capability for the specified portal capability selector, the hypercall returns the root capability selector. Otherwise the hypercall returns with an error.

Status:

SUCCESS Hypercall completed successfully.

BAD.CAP SEL_{PT} did not refer to a portal capability or the portal capability is not the root capability.

Lookup

255	EAX	— Lookup →	EAX	<i>status code</i>
<i>return ESP</i>	ECX		ECX	≡
<i>return EIP</i>	EDX	sysenter	EDX	≡
<i>SEL_{PT}</i>	EDI		EDI	<i>ID_{PT}</i>
—	ESI		ESI	≡
—	EBX		EBX	≡
—	EBP		EBP	≡
—	ESP		ESP	ECX
—	EIP		EIP	EDX