RENA-3™ IC (Readout Electronics for Nuclear Applications Integrated Circuit): 36-channel signal processor offering charge-sensitive amplification, peak detection and readout control

RENA-3™ IC User Specifications

Rev 1.1b, 2007 June 7

*Preliminary Version**

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1. Main Features

- 36 signal-processing channels
- Continuous feedback, channel is DC coupled to detector input, reset not required
- Input referred noise ≈ 150 e rms
- Signal linearity (input charge size to voltage output), +/-10%
- Two optimizations for detector capacitance (2pF and 9pF)
- Two input amplifier gain selections (9fC and 54fC maximum signal sizes)
- Two input amplifier feedback resistance selections (200MOhm and 1.2GOhm)
- Pole-Zero Cancellation with enable/disable control
- Selectable signal polarity on a channel-by-channel basis
- Selection of shaping time constants (16 selections between 0.29 and 38μs)
- Power down enable/disable per channel
- Test signal input bussed to all channels, individual enable switch at each channel to connect test signal bus to input of channel via a small capacitor (75 fF)
- Selectable gain adjustment, 1.6x, 1.8x, 2.3x, and 5x per channel
- Two signal paths, one with a fast shaper filter for timing and one with a slow shaper filter for energy mesurements
- Two adjustable 8-bit threshold DACs, one for each path in each channel
- Peak detector/follower circuit for slow path
- Timestamp circuit for fast path
- Two fully functional end channels that have internal nodes wired out as test pads to observe internal circuits functionality in more detail
- Capability to monitor in continuous (follower) mode the peak detector output of any given channel (for diagnostic use)
- Low-EMI signaling on all digital interfaces which must switch during signal acquisition, e.g., trigger, readout-initiate, reset
- Ability to wire several chips with simple scheme connected to a single controller
- Generalization of the "neighbor" readout mode using high-speed hit/read register to send hit pattern to and receive read pattern from external controller (FPGA). Sparse mode to work by default if no manipulation of the hit/read register is made during readout
- Differential analog output to allow direct connection between one or more RENA-3 ASICs and AD92xx or similar type A/D converters with only passive filter network
- Front-end saturation detection comparator senses large overload signals. A window comparator has been included and this circuit will respond when the input amplifier is saturated either high or low
- Power consumption, ≈ 6mW/channel nominal

- Signal linearity (input charge to voltage output), +/-10%
- Simulated operational temperature range, -20C to +90C (assuming protection against dew formation at lower temperatures)
- Die size: ≈ 6.905 x 6.380 mm^2

2. Description

2.1. Background

The RENA-3 application specific integrated circuit (ASIC) is an improved version of the precursor RENA-2 chip[1] which in turn was designed to supersede the original RENA, a 32-channel, mixed signal, low-noise, monolithic ASIC. The old RENA was developed as the front-end electronics chip for a Single Photon Emission Computed Tomography system and as such was designed mainly for silicon strip and CdZnTe pad detectors[2]. Significant effort was spent to make the RENA a versatile, low-noise chip, but user experience suggested new features and enhancements. The new RENA-2/RENA-3 design incorporates several of these improvements as discussed below.

2.2. Overview

A simplified block diagram for one channel of the RENA-3 ASIC is given in Figure 1 and the key design features for the chip are listed in Table I.The basic features of the RENA-3 include low-noise performance, self-trigger capability, and versatility in offering different peaking times and readout modes. Innovative features have also been added to the RENA-3 design, notably low-noise continuous feedback, user-selectable signal ranges, fast trigger output for coincident event detection, and the ability to provide channel-by-channel time difference information. The polarity, signal range, and peaking time are selectable on a channel-by-channel basis, instead of uniformly for the whole chip as in the old RENA. Further, the comparator thresholds are individually adjustable through an 8 bit DAC on each channel. This allows accurate and uniform threshold setting. The peaking time selection has been broadened to cover the ≈ 0.1 to 40 microsecond range, thus making the RENA-3 suitable for several types of detectors (see next section). The input amplifier has been designed to be tolerant of DC leakage current so that detectors may be DC coupled to the chip. Four extra channels have been added to the standard 32 to allow connection of the detector cathode side to the same ASIC. A pole-zero cancellation circuit has been included to handle higher count rates without significant pileup errors. Heeding two important requirements for space deployment, the chip power consumption has been made adjustable by limiting the current flow to the input transistor and a sound level of radiation hardness will be ensured by use of a submicron CMOS process to fabricate the ASIC. The functionality of the RENA-3 is also significantly enhanced with an interface made simpler by a

[1] T.O. Tümer, V.B. Cajipe, M. Clajus, F. Duttweiler, S. Hayakawa, J.L. Matteson, A. Shirley and O. Yossifor, "Test results of a CdZnTe pixel detector read out by RENA-2 IC", 2004 IEEE Nuclear Science Symposium Conference Record.
[2] Kravis, S. D., et al. , Nucl. Instrum. Methods A422 352 (1999).

reduced pin count. Last, while three readout modes (sparse, neighbor, and global) are provided in the original RENA chip, the readout pattern in the RENA-3 can be arbitrarily related to the hit pattern, under the control of external logic. Sparse readout (channels are read if and only if they are hit) is the default mode.

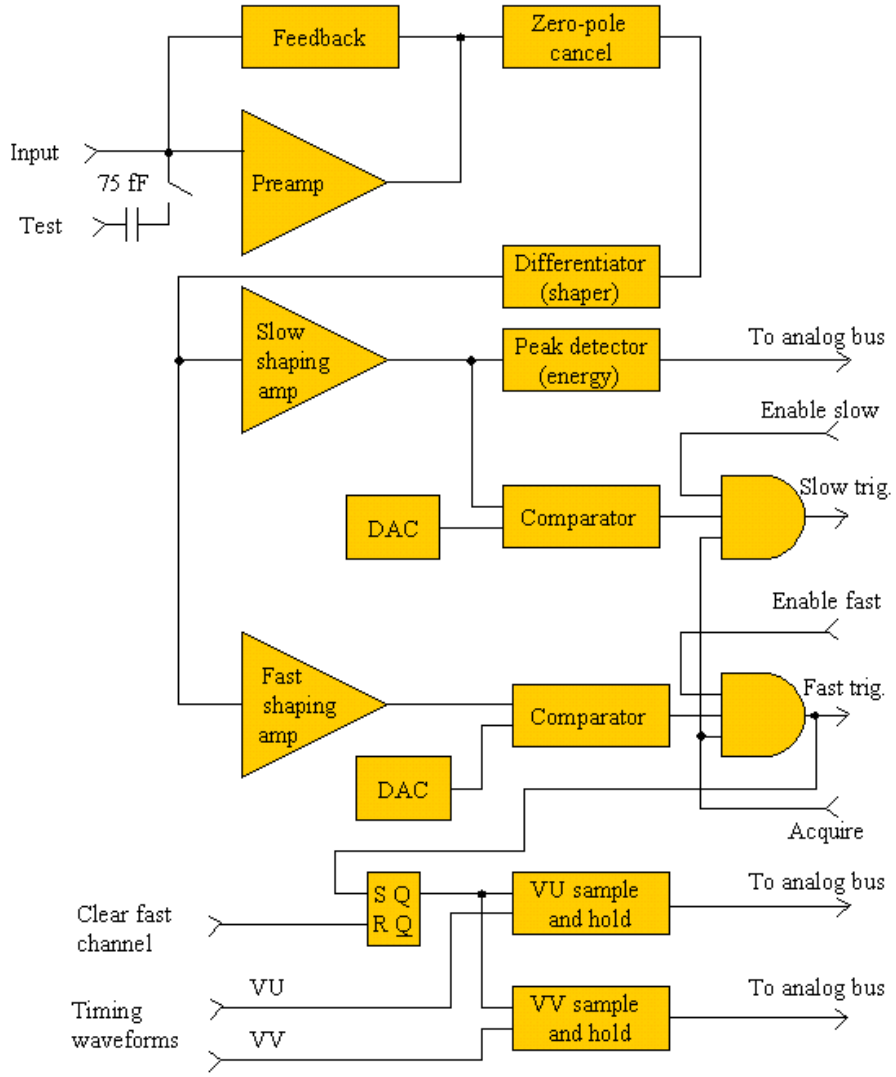


Figure 1: Simplified RENA-3 channel block diagram[3].

[3] Adapted from J. Matteson, R. Skelton, M. Pelling, S. Suchy, V. Cajipe, M. Clajus, S. Hayakawa, and T. Tümer, "Three-Dimensional Readout of CZT Detectors with the RENA-3 ASIC," presented at the 15th International Workshop on Room-Temperature Semiconductor X- and Gamma-Ray Detectors / IEEE Nuclear Science Symposium, San Diego, California, October 2006.

Table I. Key design features of the RENA-3 ASIC.

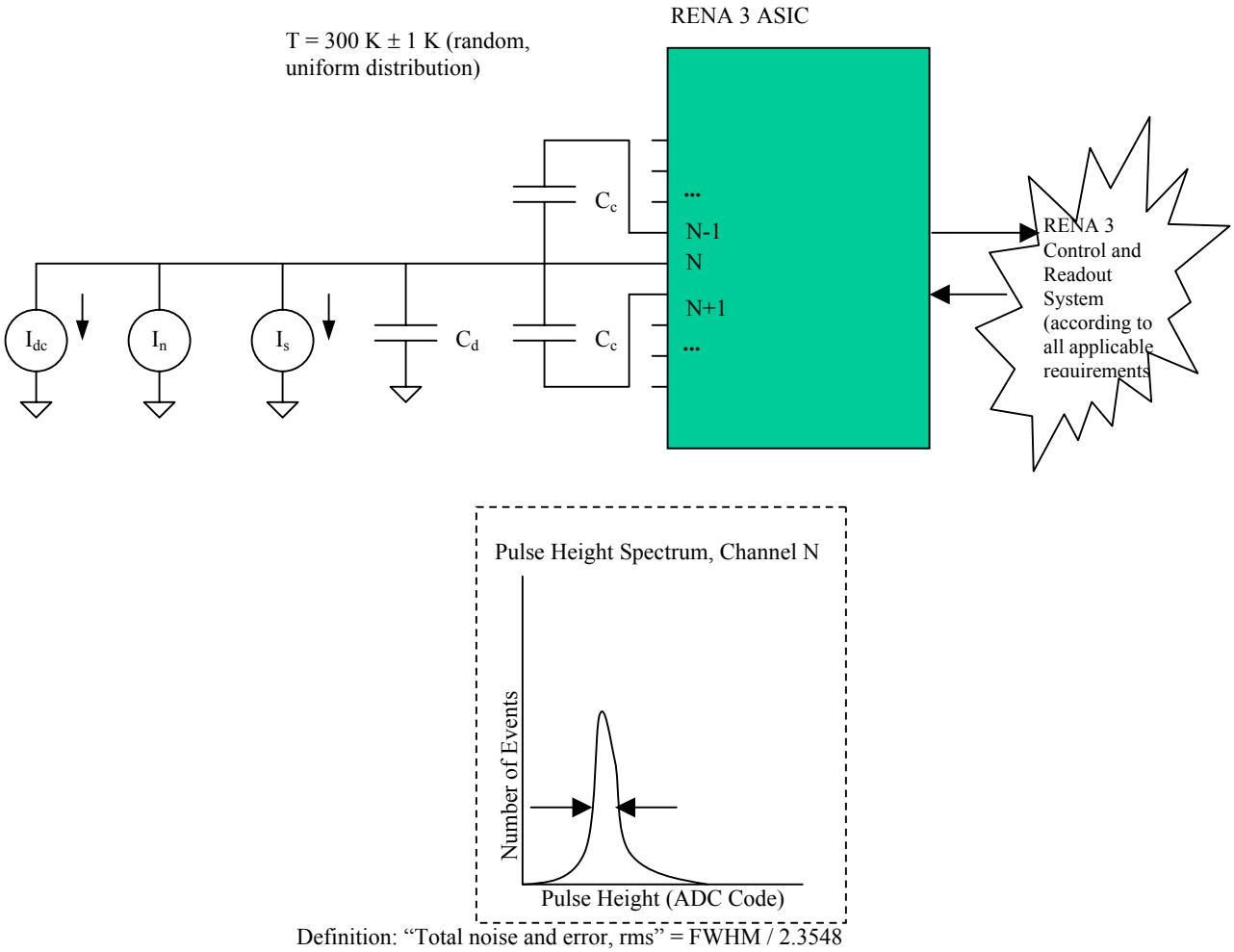
Signal range	Two full-scale ranges; 56 and 338 ke, externally selectable for each channel,(9fC and 54fC),(256keV and 1.5Mev)
Input polarity	Positive or negative, selectable channel-by-channel
Number of channels	36 (2 with test points for characterization)
Noise	</= 150 e RMS and </= 280 e RMS for low and high signal ranges
Noise optimization	Preamp optimized for 2 pF and 9 pF detector capacitance, externally selectable
DC leakage current	Tolerant to </= 5nA per channel
Power consumption	</= 6mW per channel with all features (reduction possible by powering down certain features)
Fast timing output	</= 10ns (for timing/coincidence measurements)
Channel-to-channel time difference	Implemented to enable determination of time difference between >/= 2 coincident pulses
Bias current	Adjustable through power supply current into input transistor
Trigger comparator thresholds	Individually adjustable by internal 8 Bit DACs for each channel
Peaking (shaping) times	0.29us to 38us in 16 steps
High count rates	Using pole zero cancellation, capable of over >200,000 counts per second per chip with digital readout system (external ADC will determine actual rate)
Detector structure	Heterogeneous or homogeneous
Key gamma signals	14 keV, 60 keV, 141 keV, 511 keV, 662 keV, up to 1.33 MeV
System components	Pipeline A/D converter, FPGA state machine controller, data FIFO
Interface	Minimum pin count and support component count. Up to 8 chips can be daisy-chained.
Readout mode	Maximum flexibility through programmable hit register
Deadtime per event	<5us for digital interface

2.3. Target Applications

Table II displays a summary of the detector and signal characteristics for applications that the RENA-3 design intends to address. The expected count rate in most cases is of the order of 5-10kCounts/sec. For application #10, the count rates would be higher, typically 200- 500kC/sec. Figure 2 presents an overview of signal detection as it occurs using the RENA-3.

Table II. Detector and Signal Characteristics in Specific Applications for the RENA-3

#	Application	Full-scale signal	Allowable electronics noise, rms	Capac-itance	Leakage	Charge collection time
1	CZT strip detector for astrophysics	1.33 MeV (47.4 fC)	2 keV (71.2 aC)	13 pF	5 nA	50 ns, 550 ns
2	CZT pixel detector for astrophysics (anodes)	1.33 MeV (47.4 fC)	1 keV (35.6 aC)	0.5 pF	1 nA	50 ns
3	CZT pixel detector for astrophysics (cathodes)	1.33 MeV (47.4 fC)	4 keV (142 aC)	12 pF	30 nA (AC coupled)	50 ns, 1 μs
4	CZT or CdTe pad detector for gamma camera	200 keV (7.12 fC)	800 eV (28.4 aC)	4 pF	2 nA	50 ns, 550 ns
5	CZT small pixel detector for astrophysics	1.33 MeV (47.4 fC)	1 keV (35.6 aC)	0.5 pF	250 pA	50 ns
6	Ge detector for astrophysics	1 MeV (54.1 fC)	680 eV (36.8 aC)	10 pF	50 pA	20 ns
7	Si detector for astrophysics	1.2 MeV (53.1 fC)	1 keV (44.3 aC)	10 pF	1 nA	20 ns
8	HgI2 detector for nuclear materials monitor	1.33 MeV (50.7 fC)	1.7 keV (64.8 aC)	5 pF	3 nA (AC coupled)	1 us, 25us (need 40us peaking time)
9	Silicon detector for electrons	300 keV (13.3 fC)	6 keV (266 aC)	40 pF	20 nA (AC coupled)	≈ 1 ns
10	Silicon detector for light ions	1.5 MeV (66.4 fC)	6 keV (266 aC)	20 pF	20 nA (AC coupled)	700 ps
11	Large active volume CZT detector	1.33 MeV (47.4 fC)	1.25 keV (44.5 aC)	3 pF	5 nA	50 ns
12	CZT detector for astrophysics	1.33 MeV (47.4 fC)	1.3 keV (46.2 aC)	8 pF	5 nA	50 ns, 550 ns



Definition: "Total noise and error, rms" = FWHM / 2.3548

I_{dc}	DC detector leakage current (noiseless)
I_n	White current noise 20 fA/√Hz (shot noise of 1.25nA)
I_s	Signal current: rectangular pulses, 50 ns width, rate 5 kHz
C_g	Detector capacitance to ground
C_c	Detector capacitance to neighbor channel (each of two)
C_d	Total input loading capacitance, = C_g+2C_c

Figure 2: Input signal characteristics and detection overview

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3. RENA-3 Design Specifications

A more detailed block diagram of the RENA-3 channel is displayed in Figure 3. Each major block is described below.

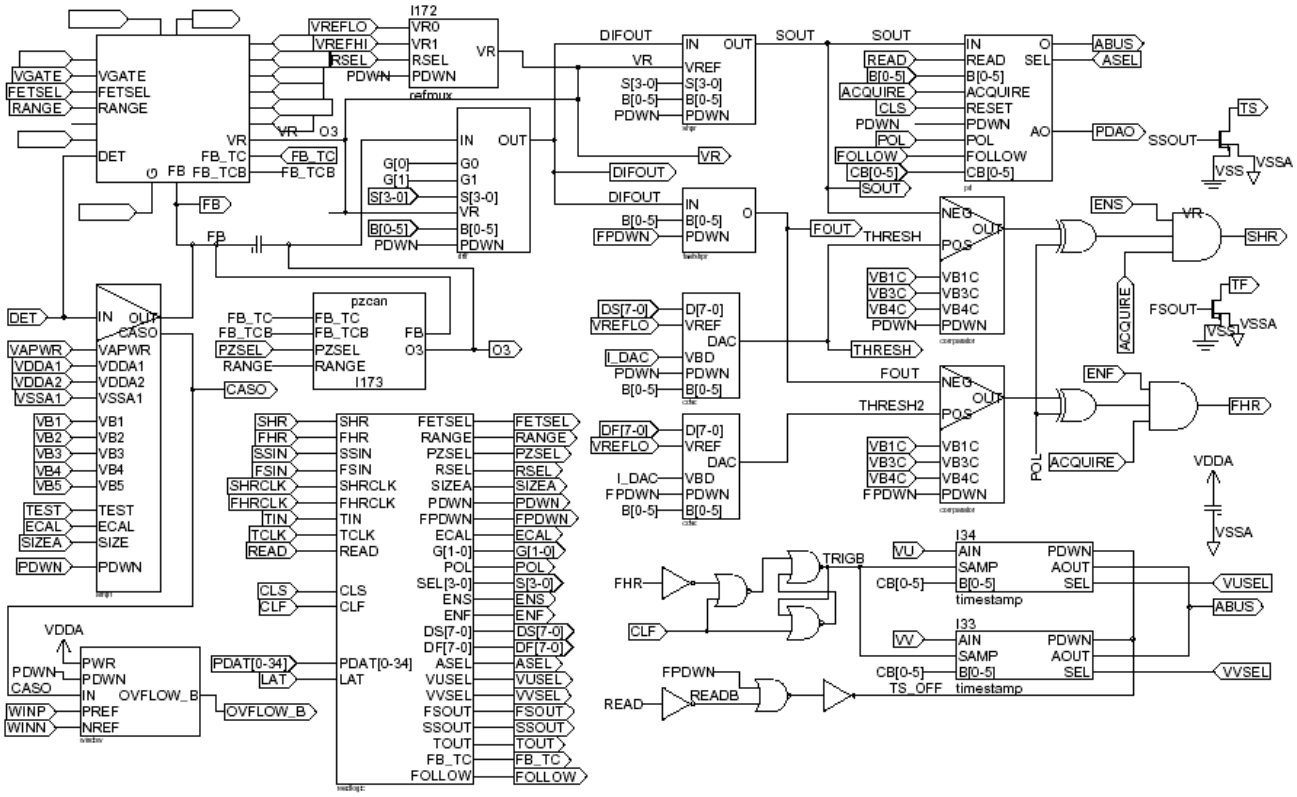

Figure 3: Block diagram of RENA-3 channel.

3.1. Input Amplifier

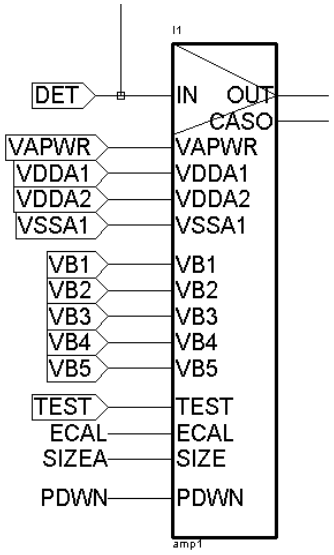

Figure 4: Input Amplifier

3.1.1. Features

- Two input FET size selections controlled by SIZE signal
- Power down control
- Test input and test input on/off control
- Low power operation
- Separate low noise power supply lines
- Two outputs, buffered (OUT) and unbuffered (CASO)

3.1.2. Electrical Specifications

Item	Specification
Output signal level	1.4V – 3.6V (must allow for 1V offset due to detector leakage)
VAPWR voltage level	2V
Test capacitor value	75fF
Input capacitive load	Approximately equal to detector capacitance optimization value
Power dissipation	2.2mW typ., 1.6mW min., adjustable to optimize power vs. noise

3.2. Feedback Circuit

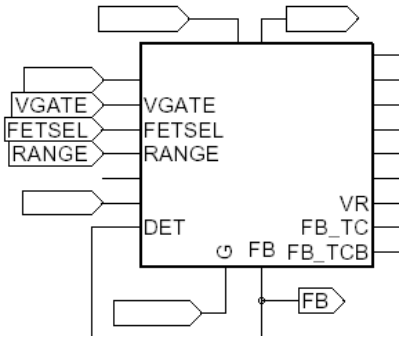

Figure 5: Feedback circuit

3.2.1. Description

The signal input is FB, which is compared to the reference level VR and the output DET is produced. The other inputs to this block consist of power, bias levels, and digital control signals.

3.2.2. Features

- Two feedback capacitor values (High gain for RANGE=0)
- Two feedback resistance values (200e6 Ohms for FB_TC=0, 1200e6 Ohms for FB_TC=1)
- Pole-zero feed forward control (enabled for PZSEL=1 with certain values set by RANGE & FB_TC)
- Simple FET feedback enable and control (FETSEL & VGATE)

3.3. Differentiator and Gain Circuit

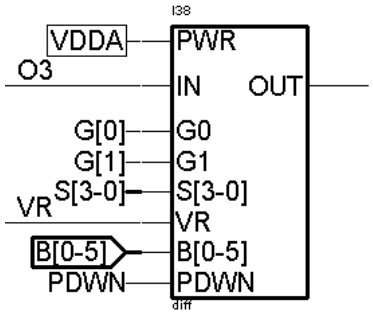

Figure 6: Differentiator and gain stage

3.3.1. Description

The differentiator circuit pulls the O3 signal to the VR voltage level through a selectable resistance. That resistance is selected with the use of the S[3-0] lines. There is also a gain stage in this block that provides gain based on the G[1-0] lines.

3.3.2. Features

- 16 Selectable resistance values between O3 and VR.
- Selectable gain values
- Power down control

3.3.3. Electrical Specifications

Item	Specification
VR reference range	1.5 – 3.5
Input signal range	1.0 – 4.0
Output signal range	1.0 – 4.0
Gain selections G[1-0] = 00 01 10 11	1.6, 1.8, 2.3, 5
Differentiation resistance values, S[3-0]	0000=2.9k 0001=3.1k 0010=3.2k 0011=3.4k 0100=3.6k 0101=3.7k 0110=4.0k 0111=4.2k 1000=9.9k 1001=11k 1010=14k 1011=17k 1100=24k 1101=34k 1110=68k 1111=800k
Frequency response	
Input impedance	
Output impedance	
Power dissipation	0.17mW typ.

3.4. Shaper

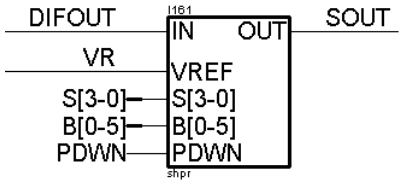

Figure 7: Shaper

3.4.1. Features

- 16 Selectable cutoff frequencies
- Power down control

3.4.2. Electrical Specifications

Item		Specification	
Input signal range		1.0 – 4.0	
Output signal range		1.0 – 4.0	
Reference level range		1.5 – 3.5	
Power dissipation		0.33mW, typ.	
Input impedance			
DC Gain		2.25	
		Peaking time (1 – 100% rise time)	10 – 90% rise time
Shaper settings, S[3-0]	0000	0.29us	0.18us
	0001	0.31us	0.18us
	0010	0.31us	0.19us
	0011	0.32us	0.20us
	0100	0.35us	0.22us
	0101	0.37us	0.23us
	0110	0.39us	0.24us
	0111	0.40us	0.25us
	1000	0.71us	0.43us
	1001	0.81us	0.49us
	1010	0.89us	0.54us
	1011	1.1us	0.64us
	1100	1.9us	1.12us
	1101	2.8us	1.69us
	1110	4.5us	2.73us
	1111	38us	23us

3.5. Fast Shaper

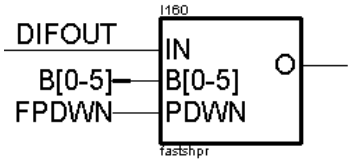

Figure 8: Fast shaper

3.5.1. Features

- Power down control

3.5.2. Electrical Specifications

Item	Specification
Input signal range	1.0 – 4.0
Output signal range	1.0 – 4.0
Power dissipation	0.17mW
Input impedance	Gate capacitance
Output impedance	
Rise Time (10-90%)	0.1 to 0.2us, depending on slow shaper setting
DC Gain	1

3.6. Threshold DAC

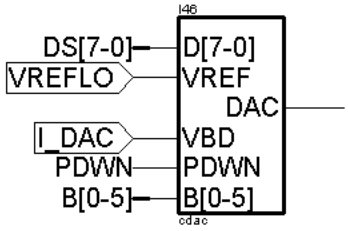

Figure 9: DAC

3.6.1. Features

- 8 Bit
- Power down control

- Adjustable upper and lower output level (VREF & VBD)
- Lowest value starts below VREF

3.6.2. Electrical Specifications

Item	Specification
VREF Range	1.5 – 3.5
Upper Limit of Range	VREFLO+13/16*DACREF*1.5
Lower Limit of Range	VREFLO – 3/16*DACREF*1.5
Power dissipation	0.17mW, typ. For output = VREFLO 0.55mW, typ. For output = max
DAC DNL	1 bit
Output impedance	Large, capacitive load only

3.7. Peak Detector

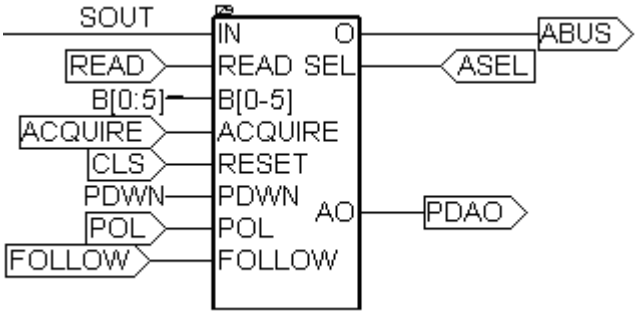

Figure 10: Peak detector

3.7.1. Description

The peak detector has several modes of operation: positive peak detect, negative peak detect, follower mode. These modes are controlled by POL, ACQUIRE, RESET, READ, SEL, and FOLLOW.

3.7.2. Features

- Dual polarity peak detection capable (POL)
- Output buffer power down control (READ)
- Power down control
- Follower mode capable (FOLLOW)

3.7.3. Functional Description

Standard peak detection sequence

1. Set POL=1 for positive peaks, POL=0 for negative peaks
2. Clear the fast path by pulsing CLF high
3. Clear the slow path by raising CLS (this resets the peak detector)
4. Assert ACQUIRE to enable the peak detector input
5. De-assert the CLS signal after 1us to arm the peak detector
6. Wait for an incoming event by observing the TS and TF signals
7. When an event has occurred, De-assert the ACQUIRE signal to capture any detected peaks. This can be delayed to account for slower detection of the events in adjacent channels.
8. Perform a readout (see below)
9. Repeat at step 1.

Follower mode

ACQUIRE=1, RESET(CLS)=0, FOLLOW=1, READ=1, SEL=1

3.7.4. Electrical Specifications

Item	Specification
Input signal range	1.0 – 4.0
Output signal range	1.0 – 4.0
Input impedance	Gate capacitance
Output impedance	
Output settling time with ABUS load of 5pF	300nsec after CLS goes low
Minimum CLS pulse width	900nsec
Minimum pulse size	40mV
Accuracy	
Power dissipation	0.85mW typ. Quiescent, +0.4mW during FOLLOW or RESET

3.8. Comparator Circuits

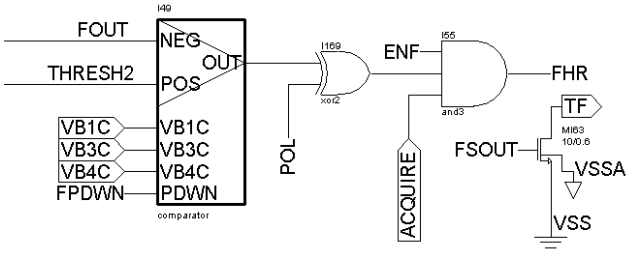

Figure 11: Comparator circuits

3.8.1. Electrical Specifications

Item	Specification
Input signal range	1.0 – 4.0
Threshold range	1.0 – 4.0
Input impedance	Gate capacitance
Trigger Response time for signal step starting at -10mV and going to +10mV	97nsec typ. 54nsec to 205nsec over process, temp., and polarity
Trigger Response time for signal step starting at -100mV and going to +100mV	46nsec typ. 25nsec to 64nsec over process, temp., and polarity
Output impedance	
Power dissipation	0.19mW, typ.

Note: Trigger output must be simulated with token logic because SHR & FHR goes back to logic block before returning to SSOUT & FSOUT and TS & TF.

3.9. Timestamp Circuits

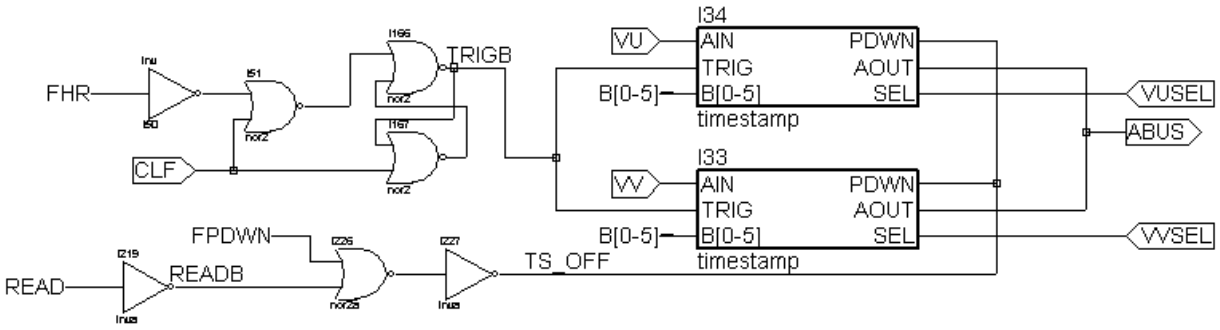

Figure 12: Timestamp circuits

3.9.1. Description

The timestamp circuit enables a triggering event to record an analog time value. That value is partitioned into two values, VU and VV which are 90 degree out of phase sine waves. When a fast trigger event occurs, the sample and hold circuit located in the timestamp block opens to capture the analog value currently present on those two input lines. When the result is read out, the relative time of the event to other events may be determined since VU and VV go to all channels in the array.

3.9.2. Electrical Specifications

Item	Specification
VU, VV voltage range	1.0 – 4.0
Output signal range	1.0 – 4.0
Power dissipation	0.5mW
Output impedance	
Input impedance	Sample and hold capacitance

3.10. Window Comparator

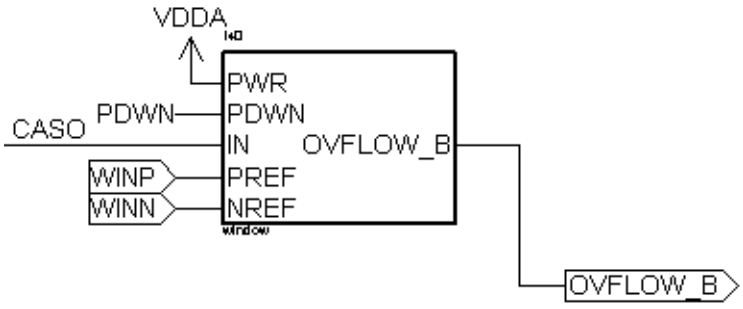

Figure 13: Window comparator

3.10.1. Electrical Specifications

Item	Specification
High trigger voltage	3.8V, typ.
Low trigger voltage	1.1V, typ.
Response time	
Power dissipation	0.1mW

3.11. Reference Multiplexer

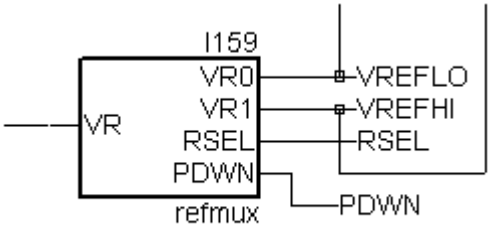

Figure 14: Reference mux

3.11.1. Electrical Specifications

Item	Specification
On resistance	<323 ohms
Valid signal range	1.5 – 3.5

3.12. Configuration and Token Logic

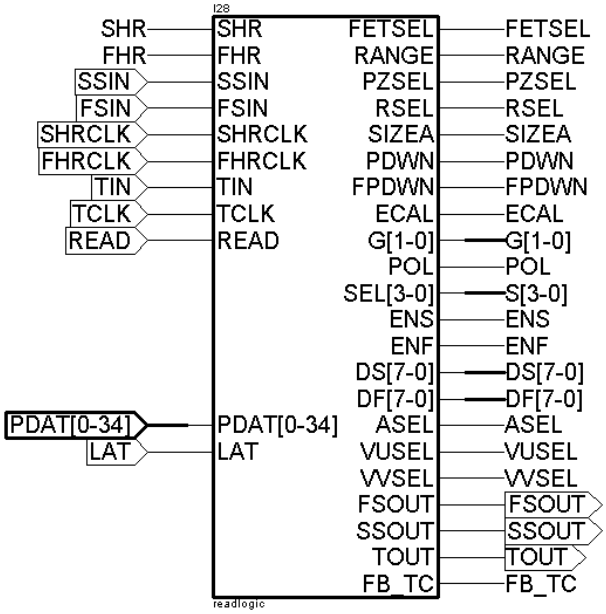

Figure 15: Logic

3.12.1. Description

The configuration logic consists of simple flip-flop cells that store the digital state of all of the configuration bits. The function of these configuration bits has been described in all the other sections covering the internal channel blocks. The token logic allows the user to gather the collected analog information off the chip with flexibility.

3.12.2. Token readout scheme

The signals SIN, SOUT, FIN, FOUT, TIN, TOUT, SHRCLK, FHRCLK, TCLK, CLS, READ, AOUTP, AOUTN are used to control readout. When an event has occurred, the analog data can be read by using the provided signals. This sequence is typically performed in conjunction with the peak detector operation. See the previous section on the peak detector to determine how this sequence fits into the complete operation.

- Analyze the token data
- Shift in the desired channels to observe
- Clock through the tokens while sampling AOUTP and AOUTN

Step 1 and Step 2; Analyzing token data and shift in the desired channels to observe.
Using SHRCLK and FHRCLK, tokens captured in an event can be observed on the SOUT and FOUT signals. The bits are shifted on the rising edges of these clocks and token bits for channel 35 are present before the first rising edge occurs. When these bits are observed, they should be loaded back into the channels by using the SIN and FIN signals. The bit pattern can be changed as desired in order to read out adjacent channels or any general pattern. The last bit to be shifted in is for channel 0 located at the top of the array. Both fast and slow token chains can be controlled independently.
Step 3: TIN should now be raised high for the first chip in the series. If there are multiple chips then TOUT of the first chip should be connected to TIN of the second chip, etc. Raise the READ signal to enable the analog output drivers. And then wait for the analog bus to settle due to the amplifiers powering up (~1us). Now, the first channel analog driver should be driven onto the AOUT lines and can be sampled by external circuits. This occurs automatically without clocking the TCLK for the first active channel only.

If TOUT immediately goes high after raising TIN then there were no tokens in the token chain. Otherwise, clocking the TCLK signal will progress the token from the current channel to the next stage that has a TOKEN.

Note that within a channel there are a possibility of 3 tokens, 1 for the slow path and 2 for the fast path (VU & VV). If both bits for a given channel are enabled it will take 3 TCLK rising edges to get all the channel data.

The clock period for TCLK can be as small as 333ns so that the output can settle to within 12 bit accuracy.

Step 4: The Token register now needs to be cleared. This can be accomplished (differently than in the RENA II) chip by pulsing CLS high for 20ns. This pulsing of CLS is also consistent with resetting the peak detector circuits.

3.13. Output Buffer

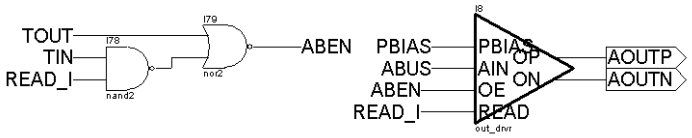

Figure 16: Output buffer circuits

3.13.1. Electrical Specifications

Item	Specification
Input voltage range	1.0 – 4.0
Output voltage range P	1.25V to 3.75V
Output voltage range N	1.25V to 3.75V
Output settling time, 12 bit	333ns
Expected receiving A/D	AD92XX
Output load	4 RENA-3 chips plus ADC and board trace (40pF total)
Power dissipation	2mW
Condition for output	READ=1 & Token is present in chip & Token not output

3.14. Differential Trigger Output Circuit

3.14.1. Electrical Specifications

Item	Specification
Output current level	
Response time	
Power dissipation	1mW

3.15. LVDS differential input circuit

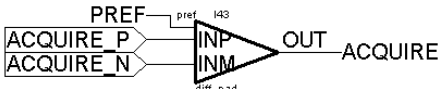

Figure 17: LVDS receiver

3.15.1. Electrical Specifications

Item	Specification
Response time 100mV step driving ACQUIRE parasitics	20ns
Power dissipation	0.5mW

3.16. Other Specifications

Item	Specification
Overall gain for 14keV signal	14keV signal produces 100% full scale at chip output for max gain settings.
Minimum operating trigger threshold requirement (applies to all channels simultaneously)	
High gain range	100 aC This is equivalent to 624 electrons
Low gain range	580 aC This is equivalent to 3620 electrons
Total dose (γ) tolerance <50% failure	20 kRad(Si) The radiation specs are goals to be attempted on a best effort basis with standard CMOS technology, no special process.
Timing jitter	10 ns (or better) Note that this is for input pulses of fixed amplitude - it excludes time walk due to amplitude variation.
Dead time per event	Event with n channels to read; HIT/READ register is read and written Goal is 5 μs + n∗(333 ns)

4. Pad List, Description, and Locations

Pad Name	Description
VRI	2V, Very low noise power supply
VDDA	5V, Analog power supply
VDDA1	5V, Low noise analog power supply #1
VDDA2	5V, Low noise analog power supply #2
VDD	5V, Digital power supply
VSS	0V, Digital ground
VSSA1	0V, Low noise analog ground
VSSA	0V, Analog ground
TEST	+/-720mV step input to simulate signal. This signal is for testing channels.
VGATE	0V or ~1.5V for simple gate feedback operation. Must enable with FETSEL bit in channel to use this.
DACREF	2 to 3V, DAC reference level. Sets the MAX DAC output voltage to VREFLO + 1.5*13/16*DACREF
VU	2 – 3V sine wave, U timing signal for sampling by fast trigger
VV	2 – 3V sine wave, V timing signal for sampling by fast trigger
ISET	6.98Kohm to VDDA, Sets input FET bias current
PBIAS	33.2Kohm to ground. Sets bias current for most amplifiers
FB_PBIAS	47.5Kohm to ground, Sets feedback circuit bias current
R_BIAS	93.1Kohm to ground, Sets feedback R bias current
VREFHI	3.5V, High reference for negative going signals
VREFLO	1.5V, Low reference for positive going signals and reference for low rail of DAC
IN[0-35]	Detector inputs pins
AOUTP	?, Positive differential output
AOUTN	?, Negative differential output
CSHIFT	Shift one bit (from Cin) into the shift register on the rising edge
CIN	Data input. Must be valid on the rising edge of CShift
CS	Chip Select. After shifting 41 bits, pulse this signal high to load the shifted data in the proper registers
TS_N	Differential out, Slow trigger output, Negative output
TS_P	Differential out, Slow trigger output, positive output
TF_N	Differential out, Fast trigger output, Negative Output
TF_P	Differential out, Fast trigger output, positive output
FOUT	Fast token output for fast token register
SOUT	Slow token output for slow token register
TOUT	Token output from token chain. Goes high when chip is finished to pass

Pad Name	Description
	token to next chip.
READ	Enables output of analog signals within a channel. Turns on the analog driver for a channel when token is present. Also enables output buffer.
TIN	Token input, Always set a 1 for first channel, or receives TOUT from previous chip.
SIN	Slow token input. Use with SHRCLK to load bits into slow token chain.
FIN	Fast token input. Use with FHRCLK to load bits into slow token chain.
SHRCLK	Slow hit register clock. Loads SIN bits on rising edge
FHRCLK	Fast hit register clock. Loads FIN bits on rising edge
ACQUIRE_P	Positive differential input, Peak detector is active when this signal is asserted (high).
ACQUIRE_N	Negative differential input, Peak detector is active when this signal is asserted (low).
CLS_P	Positive differential input, Peak detector reset signal. Resets the peak detector when asserted (high). Also clears the token register.
CLS_N	Negative differential input, Peak detector reset signal. Resets the peak detector when asserted (low). Also clears the token register.
CLF	This signal clears the fast latch (VU and VV sample circuit) when asserted, (high).
TCLK	This signal shifts the token from one channel to the next on the rising edge
TST[3-22]	Pull to VDD with 44Kohm resistor. Test signal outputs. AKA T[3-22]

NOVA R&D, Inc. 1525 Third St., Suite C, Riverside, CA 92507 (951) 781-7332 novarad@novarad.com

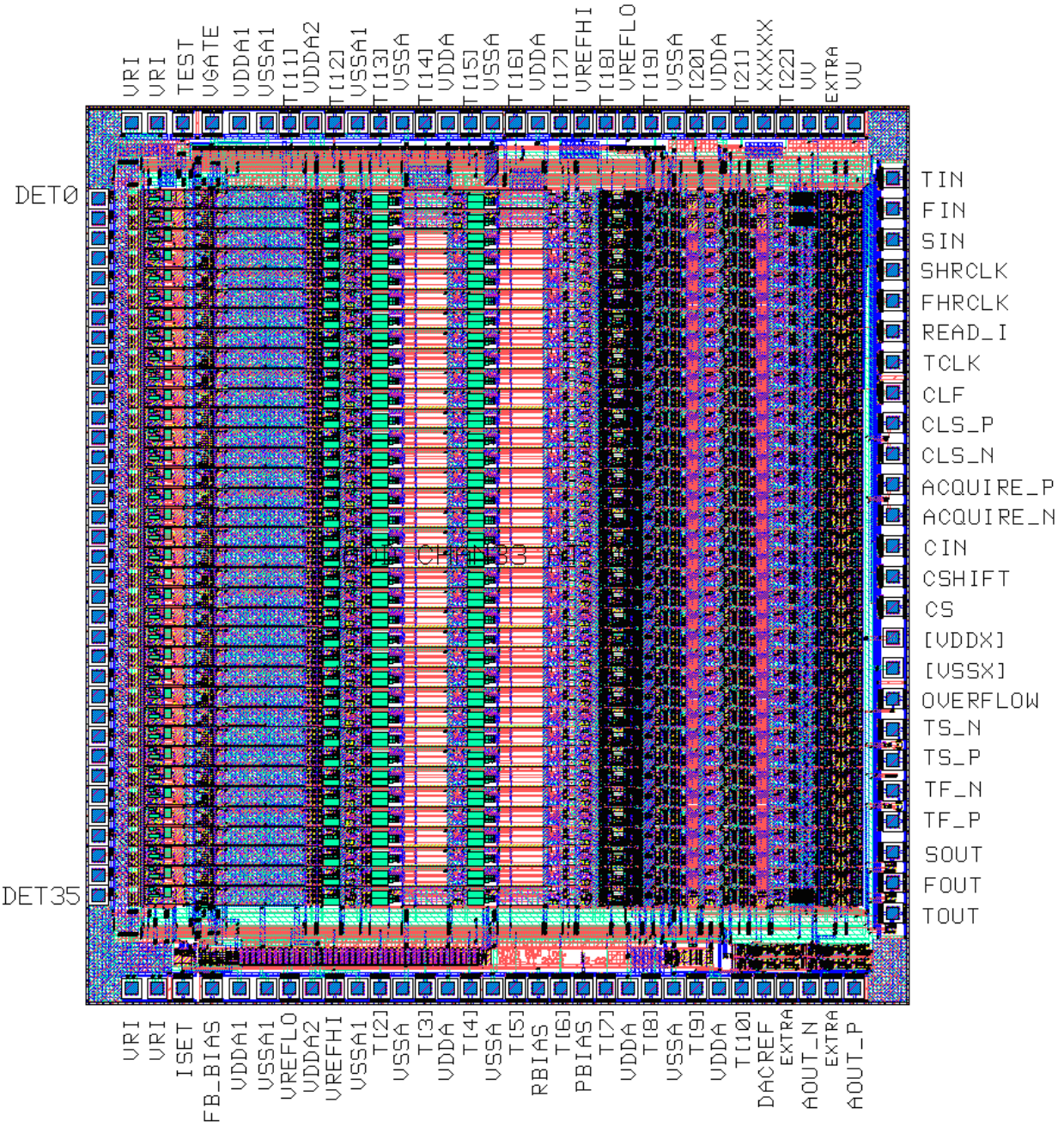

Figure 18: Chip plot and pin locations

4.1. Pad Spacing

Location	Pitch
Detector input pads	130 μm
Top and bottom pads	180um
Right side pads	200um

5. Channel Configuration, Bits and Description

The configuration of the RENA-3 is done with the use of three signals – CS, CShift, Cin, and a 41 bit shift register whose bits are designated for certain functions. The configuration of the RENA-3 will always be performed by loading in a 41-bit word of data into the serial shift register. These words are divided into address and channel configuration data. D[40] goes into shift register first and D[0] goes in last.

Bit #	Description
D[40-35]	6-bit control register address (MSB goes in first) Address 0 is at the top of the chip; Address 35 is at the bottom. This address points to the channel. Use CS to load the following 35 bits into the channel selected.
D[34]	FB_TC, Feedback time constant selection. Selects the size of the feedback resistor for the input stage. 1 Selects 1.2Gohm feedback resistance, 0 Selection 200Mohm.
D[33]	ECAL, Enable channel calibration. Set to 1 to enable TEST signal input to channel.
D[32]	FPDWN, Set to a 1 to power down fast path circuits. This includes the fast shaper, a DAC, and the comparator for the fast path.
D[31]	FETSEL, Set to a 1 to use the simple FET feedback instead of the resistive multiplier circuit.
D[30-29]	G[1-0], Gain selection. The gain selection following the differentiation stage has 4 selections for gain. [00] = 1.6, [01] = 1.8 [10] = 2.3 [11] = 5.0
D[28]	PDWN, Set to a 1 to power down most of the circuits in the channel. FPDWN must still be used to power down the fast components.
D[27]	PZSEL, Pole Zero cancellation selection. Set this bit to a 1 to enable the pole zero cancellation circuit.
D[26]	RANGE, Sets the feedback capacitor size. Set to a 1 for 60fF feedback. Set to a 0 for 15fF feedback.
D[25]	RSEL, Reference selection for the channel. Set to a 1 to select VREFHI (for negative going signals)
D[24-21]	SEL[3-0], Time constant selection. All 0's is the shortest time constant. All 1's is the longest time constant. Selections are, from shortest to longest (us):

Bit #	Description
	0.29, 0.31, 0.31, 0.32, 0.35, 0.37, 0.39, 0.40, 0.71, 0.81, 0.89, 1.1, 1.9, 2.8, 4.5, 38. SEL[0] is the LSB and this goes into the shift register after SEL[3-1].
D[20]	SIZEA, Selects the size of the input FET for noise optimization. Set to a 1 for a FET of size 1000um. Set to a 0 for a size of 450um.
D[19-12]	DF[7-0], Fast DAC value. All 0's gives the lowest output voltage (VREFLO - 3/16*1.5*DACREF). All 1's are largest output voltage (VREFLO + 13/16*1.5*DACREF). DF[0] is the LSB and goes into the shift register last.
D[11]	POL, Polarity selection for comparators. Select a 1 for positive going signals.
D[10-3]	DS[7-0], Slow DAC value. All 0's are smallest output voltage (VREFLO – 13/16*1.5*DACREF). All 1's are largest output voltage (VREFLO + 13/16*1.5*DACREF). DS[0] is the LSB and goes into the shift register last.
D[2]	ENF, Set to a 1 to enable FAST trigger.
D[1]	ENS, Set to a 1 to enable the SLOW trigger.
D[0]	FM, Follower mode. Set to a one to enable peak detector to work in follower mode. It only makes sense to have a single one of these bits set at a time for all channels.

Configuration shift register timing (see **Error! Reference source not found.**)
(typical)

T_{srh}	CShift high	10	ns
T_{srl}	CShift low	10	ns
T_{sds}	CIN setup time	9	ns
T_{sdh}	CIN hold time	9	ns
T_{chcs}	CShift to CS delay	20	ns
T_{sh}	CS high	20	ns
T_{csch}	CS to Cshift	20	ns

6. Timing Diagram

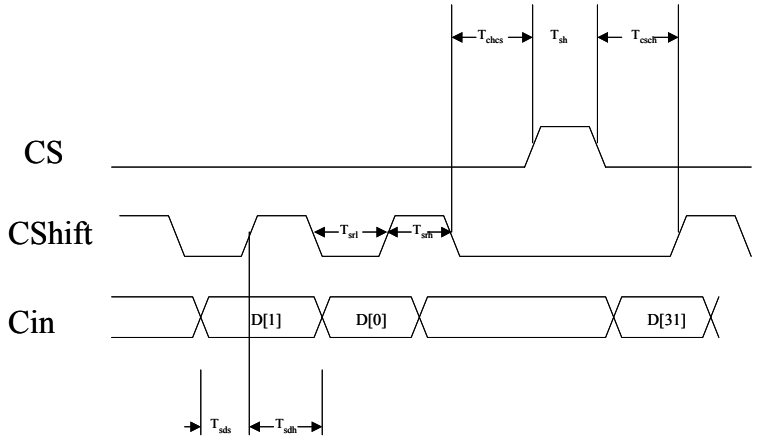

Figure 19: Configuration shift register timing.

7. Test and Calibration

7.1. Test Signal Outputs

TST[2-22] These signals are connected to the top and bottom channels and can be used to help diagnose any potential problems with the design. To activate these signals, connect a 40Kohm resistor from these signals to VDD (or up to 6.5V in order to get the entire operating range possible in the chip). The following schematics show how and where the connections are made inside the chip. Note that TST[0] and TST[1] are not wired out to pads because of changes to the chip near the time of chip submission.

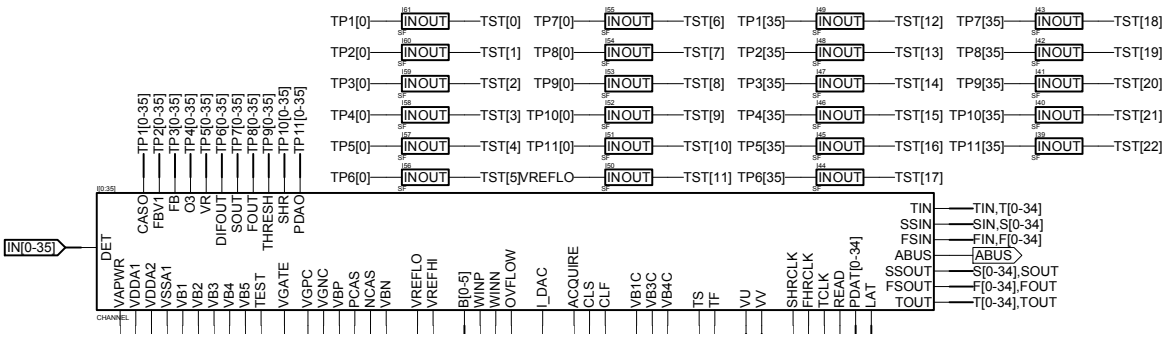

Figure 20: Test points for array

The above figure shows the test points and pads and the nodes they connect to. This schematic should be used with the channel block diagram to determine the exact electrical point the test point is connected to.

7.2. Channel Calibration Using Test Pulse

The RENA-3 chip includes means for the test and calibration of the channels using an external pulse generator. Each channel has a switch connecting the input to the test signal bus (TEST) when the corresponding configuration bit (D[33], ECAL) is set to 1. The switch is coupled through a 75fF capacitor, which provides charge injection into the input amplifier on each ramp of the test pulse voltage in the amount 75fC/Volt. An example of a compensated network used for test pulse generation is shown in Figure 21. Typically the test pulse should have a rectangular waveform with sharp edges as shown in Figure 22. The width of the pulse should be larger than the shaping time to ensure that all charge from a pulse edge is accumulated in the peak detectors. This way the same pulser can be used for calibration of both positive and negative input signals.

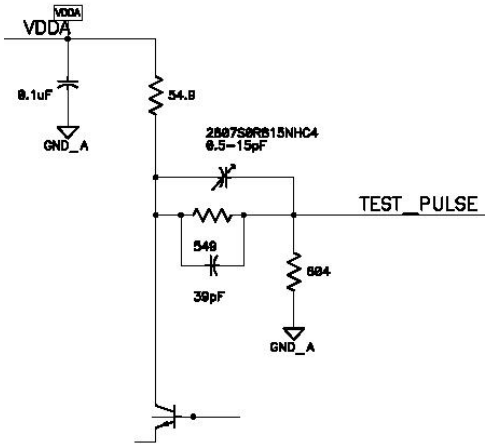

Figure 21: An example of compensated network for test pulse connection.

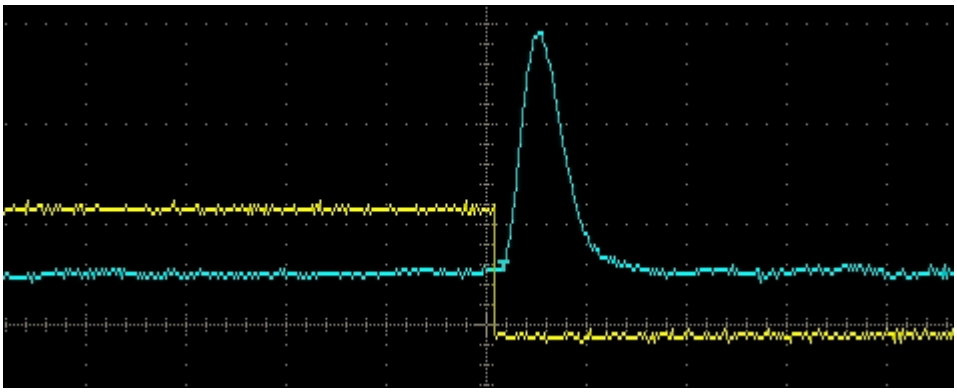

Figure 22: Test pulse (yellow) and RENA-3 output in the FOLLOWER mode (blue).

8. Appendix: RENA-3 in 144-pin CQFP Package

The RENA-3 chip is available in die form or assembled in a 144-pin CQFP package (Kyocera QC-144398-WZ). A photograph of packaged RENA-3 parts is shown in Figure 23. Table III shows the package pin number versus pad name mapping.

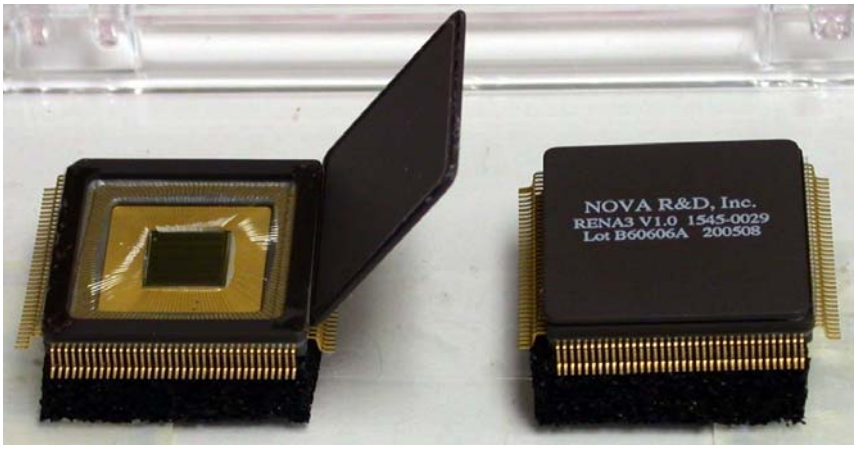

Figure 23: Photographs of RENA-3 in 144-pin CQFP package (Kyocera QC-144398-WZ).

Table III. Mapping of RENA-3 pads to CQFP package pins.

Pin #	Pad Name	Description
1-2		NC
3	VRI	Very Low Noise Power Supply
4	VRI	Very Low Noise Power Supply
5	ISET	Input FET Bias Current
6	FBBIAS	Feedback Circuit Bias Current
7	VDDA1	Low Noise Analog Supply #1
8	VSSA1	Low Noise Analog GND #1
9	VREFLO	Low Level DAC Reference
10	VDDA2	Low Noise Analog Suppply #2
11	VREFHI	High Level Dac Reference
12	VSSA1	Low Noise Analog GND #1
13	T[2]	Test Point
14	VSSA	Analog GND
15		Substrate
16	T[3]	Test Point

Pin #	Pad Name	Description
17	VDDA	Analog Supply
18	T[4]	Test Point
19	VSSA	Analog GND
20	T[5]	Test Point
21	RBIAS	Feedback Circuit Bias Current
22	T[6]	Test Point
23	PBIAS	Amplifier Bias Current
24	T[7]	Test Point
25	VDDA	Analog Supply
26	T[8]	Test Point
27	VSSA	Analog GND
28		Substrate
29	T[9]	Test Point
30	VDDA	Analog Supply
31	T[10]	Test Point
32	DACREF	DAC Reference level
33	EXTRA	Spare Pad
34	AOUTN	Negative Differential Output
35	EXTRA	Spare Pad
36	AOUTP	Positive Differential Output
Corner		
37-42		NC
43	TOUTP	Trigger Output
44	FOUTP	Fast Token Output
45	SOUTP	Slow Token Output
46	TFP	Fast trigger, positive differential Output
47	TFN	Fast trigger, negative differential Output
48	TSP	Slow trigger, positive differential output
49	TSN	Slow trigger, negative differential output
50	OVRFLOW	Counter Overflow Output
51	VSS	Digital GND
52	VDD	Digital Supply
53	CS	Chip Select
54	CSHIFT	Shift one bit into shift register
55	CIN	Data Input
56	ACQUIREN	Data Acquisition Negative differential input
57	ACQUIREP	Data Acqusition Positive differential input

Pin #	Pad Name	Description
58	CLSN	Peak Det. Reset, negative differential input
59	CLSP	Peak Det. Reset, positive differential input
60	CLFP	Clear Fast Latch input
61	TCLK	Token clock
62	READ	Enable Analog Output
63	FHRCLK	Fast Hit register clock
64	SHRCLK	Slow Hit register clock
65	SINP	Slow token Input
66	FINP	Fast Token Input
67	TINP	Token Input
68-72		NC
Corner		
73	VU	Time stamp input #1
74	EXTRA	Spare Pad
75	VV	Time Stamp input #2
76	T[22]	Test Point
77		
78	T[21]	Test Point
79	VDDA	Analog Supply
80	T[20]	Test Pont
81		Substrate
82	VSSA	Analog GND
83	T[19}	Test Point
84	VREFLO	LOW Level DAC reference
85	T[18]	Test Point
86	VREFHI	High Level DAC reference
87	T[17]	Test Point
88	VDDA	Analog Supply
89	T[16]	Test Point
90	VSSA	Analog GND
91	T[15]	Test Point
92	VDDA	Anaolg Supply
93	T[14]	Test Point
94	VSSA	Analog GND
95		Substrate
96	T[13]	Test Point
97	VSSA1	Low Noise Analog GND

Pin #	Pad Name	Description
98	T[12]	Test Point
99	VDDA2	Low Noise Analog Supply #2
100	T[11]	Test Point
101	VSSA1	Low Noise Analog GND
102	VDDA1	Low noise Analog Supply #1
103	VGATE	Gate Feedback Reference
104	TEST	Test Input
105	VRI	Very low noise analog supply
106	VRI	Very low noise analog supply
107-108		NC
Corner		
109	DET0	Detector Input #1
110	DET1	Detector Input #2
111	DET2	Detector Input #3
112	DET3	Detector Input #4
113	DET4	Detector Input #5
114	DET5	Detector Input #6
115	DET6	Detector Input #7
116	DET7	Detector Input #8
117	DET8	Detector Input #9
118	DET9	Detector Input #10
119	DET10	Detector Input #11
120	DET11	Detector Input #12
121	DET12	Detector Input #13
122	DET13	Detector Input #14
123	DET14	Detector Input #15
124	DET15	Detector Input #16
125	DET16	Detector Input #17
126	DET17	Detector Input #18
127	DET18	Detector Input #19
128	DET19	Detector Input #20
129	DET20	Detector Input #21
130	DET21	Detector Input #22
131	DET22	Detector Input #23
132	DET23	Detector Input #24
133	DET24	Detector Input #25
134	DET25	Detector Input #26

Pin #	Pad Name	Description
135	DET26	Detector Input #27
136	DET27	Detector Input #28
137	DET28	Detector input #29
138	DET29	Detector Input #30
139	DET30	Detector Input #31
140	DET31	Detector Input #32
141	DET32	Detector Input #33
142	DET33	Detector Input #34
143	DET34	Detector Input #35
144	DET35	Detector Input #36
Corner		